Power Products Division

HIGH AND LOW SIDE DRIVER

The MPIC2112 is a high voltage, high speed, power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross—conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N—channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

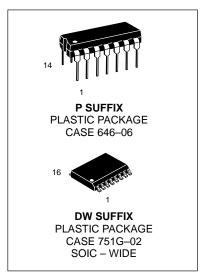
- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout for Both Channels
- Separate Logic Supply
- Operating Supply Range from 5 to 20 V
- Logic and Power Ground Operating Offset Range from -5 to +5 V
- CMOS Schmitt-triggered Inputs with Pull-down
- Cycle by Cycle Edge-triggered Shutdown Logic
- Matched Propagation Delay for Both Channels
- Outputs in Phase with Inputs

PRODUCT SUMMARY

 $\begin{array}{lll} \text{VoFFSET} & 600 \text{ V MAX} \\ \text{I}_{\text{O+}/-} & 200 \text{ mA}/400 \text{ mA} \\ \\ \text{VouT} & 10-20 \text{ V} \\ \\ \text{t}_{\text{on/off}} \text{ (typical)} & 125 \& 105 \text{ ns} \\ \\ \text{Delay Matching} & 30 \text{ ns} \\ \end{array}$

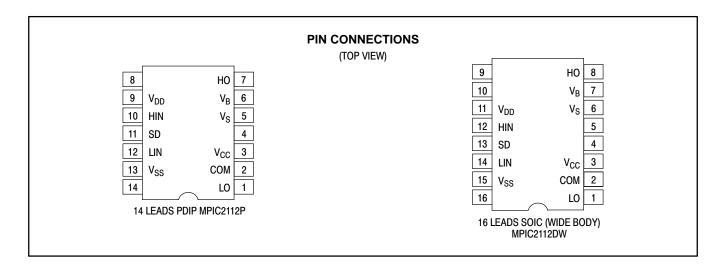
MPIC2112

HIGH AND LOW SIDE DRIVER

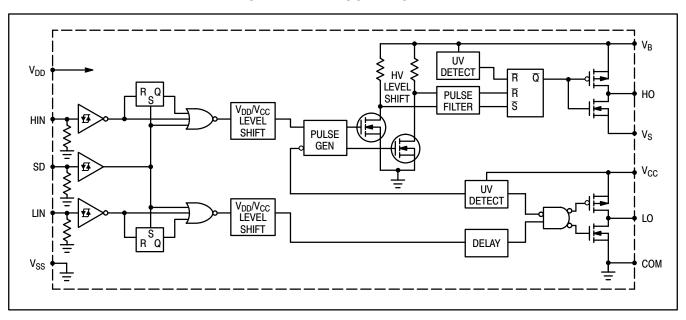


ORDERING INFORMATION

Device	Package
MPIC2112DW	SOIC WIDE
MPIC2112P	PDIP



SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Rating		Symbol	Min	Max	Unit
High Side Floating Absolute Voltage High Side Floating Supply Offset Voltage High Side Floating Output Voltage Low Side Fixed Supply Voltage Low Side Output Voltage Logic Supply Voltage Logic Supply Voffset Voltage Logic Input Voltage (HIN, LIN & SD)		VB VS VHO VCC VLO VDD VSS VIN	-0.3 V _B -25 V _S -0.3 -0.3 -0.3 -0.3 V _{CC} -25 V _{SS} -0.3	625 V _B +0.3 V _B +0.3 25 V _{CC} +0.3 V _{SS} +25 V _{CC} +0.3 V _{DD} +0.3	V _{DC}
Allowable Offset Supply Voltage Transient		dV _S /dt	-	50	V/ns
*Package Power Dissipation @ T _A ≤ +25°C	(14 Lead DIP) (16 SOIC-WIDE)	P _D	_ _	1.6 1.25	Watt
Thermal Resistance, Junction to Ambient	(14 Lead DIP) (16 SOIC-WIDE)	$R_{ heta JA}$	_ _	75 100	°C/W
Operating and Storage Temperature		T _j , T _{stg}	-55	150	°C
Lead Temperature for Soldering Purposes, 10 se	TL	-	260	°C	

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15 V differential.

High Side Floating Supply Absolute Voltage	V _B	V _S +10	V _S +20	V
High Side Floating Supply Offset Voltage	V _S	Note 1	600	
High Side Floating Output Voltage	V _{HO}	Vs	V _B	
Low Side Fixed Supply Voltage	V _{CC}	10	20	
Low Side Output Voltage	V _{LO}	0	V _{CC}	
Logic Supply Voltage	V _{DD}	V _{SS} +5	V _{SS} +20	
Logic Supply Offset Voltage	V _{SS}	-5	5	
Logic Input Voltage (HIN, LIN & SD)	V _{IN}	V _{SS}	V_{DD}	
Ambient Temperature	T _A	-40	125	°C

Note 1: Logic operational for V_S of –5 to +600 V. Logic state held for V_S of –5 V to – V_{BS} .

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

	Characteristic	Symbol	Min	Тур	Max	Unit	
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STATIC ELECTRICAL CHARACTERISTICS – SUPPLY CHARACTERISTICS

 V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15 V and V_{SS} = COM unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The VO and IO parameters are referenced to COM or V_{SS} and are applicable to the respective output leads: HO or LO.

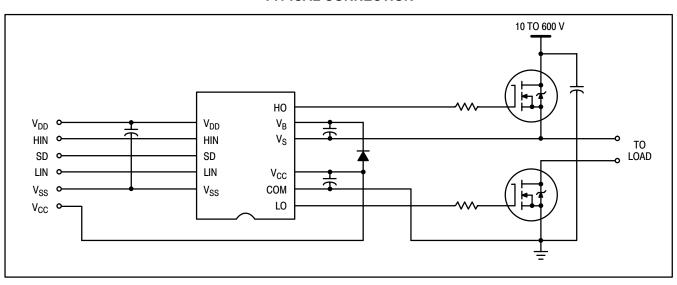
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Logic "1" Input Voltage	V _{IH}	9.5	-	-	V
Logic "0" Input Voltage	V _{IL}	-	-	6.0	
High Level Output Voltage, V _{BIAS} -V _O @ V _{IN} = V _{IH} , I _O = 0 A	V _{OH}	-	-	100	mV
Low Level Output Voltage, V _O @ V _{IN} = V _{IL} , I _O = 0 A	V _{OL}	-	-	100	
Offset Supply Leakage Current @ V _B = V _S = 600 V	I _{LK}	-	-	50	μΑ
Quiescent V _{BS} Supply Current @ V _{IN} = 0 V or V _{DD}	I _{QBS}	-	25	60	
Quiescent V _{CC} Supply Current @ V _{IN} = 0 V or V _{DD}	Iqcc	-	80	180	
Quiescent V _{DD} Supply Current @ V _{IN} = 0 V or V _{DD}	I _{QDD}	-	2.0	5.0	
Logic "1" Input Bias Current @ V _{IN} = 15 V	I _{IN+}	-	20	40	
Logic "0" Input Bias Current @ V _{IN} = 0 V	I _{IN} _	-	-	1.0	
V _{BS} Supply Undervoltage Positive Going Threshold	V _{BSUV+}	7.4	-	9.6	V
V _{BS} Supply Undervoltage Negative Going Threshold	V _{BSUV} -	7.0	-	9.2	
V _{CC} Supply Undervoltage Positive Going Threshold	V _{CCUV+}	7.6	-	9.6	
V _{CC} Supply Undervoltage Negative Going Threshold	V _{CCUV} -	7.2	-	9.2	
Output High Short Circuit Pulsed Current @ $V_{OUT} = 0 \text{ V}$, $V_{IN} = 15 \text{ V}$, PW $\leq 10 \mu s$	I _{O+}	200	250	-	mA
Output Low Short Circuit Pulsed Current @ V_{OUT} = 15 V, V_{IN} = 0 V, PW \leq 10 μs	I _{O-}	420	500	_	

DYNAMIC ELECTRICAL CHARACTERISTICS

 V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15 V and V_{SS} = COM unless otherwise specified. T_A = 25°C.

Turn–On Propagation Delay @ V _S = 0 V	t _{on}	_	125	180	ns
Turn–Off Propagation Delay @ V _S = 600 V	t _{off}	_	105	160	
Shutdown Propagation Delay @ V _S = 600 V	t _{sd}	_	105	160	
Turn–On Rise Time @ C _L = 1000 pF	t _r	_	80	130	
Turn–Off Fall Time @ C _L = 1000 pF		_	40	65	
Delay Matching, HS & LS Turn-On/Off	MT	_	_	30	

TYPICAL CONNECTION



MPIC2112

LEAD DEFINITIONS

Symbol	Lead Description
V_{DD}	Logic Supply
HIN	Logic Input for High Side Gate Driver Output (HO), In Phase
SD	Logic Input for Shutdown
LIN	Logic Input for Low Side Gate Driver Output (LO), In Phase
V _{SS}	Logic Ground
V _B	High Side Floating Supply
НО	High Side Gate Drive Output
V _S	High Side Floating Supply Return
V _{CC}	Low Side Supply
LO	Low Side Gate Drive Output
СОМ	Low Side Return

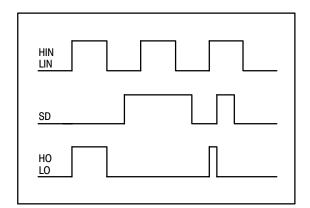


Figure 1. Input / Output Timing Diagram

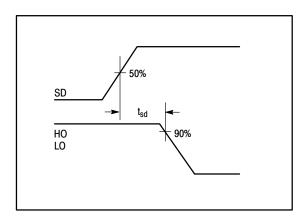


Figure 3. Deadtime Waveform Definitions

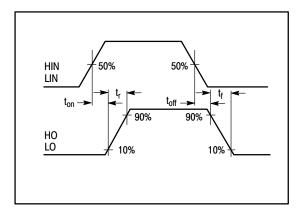


Figure 2. Switching Time Waveform Definitions

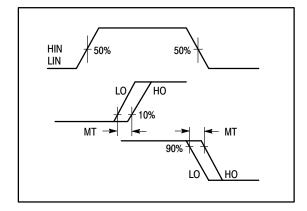
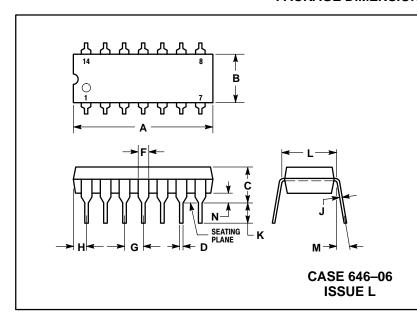


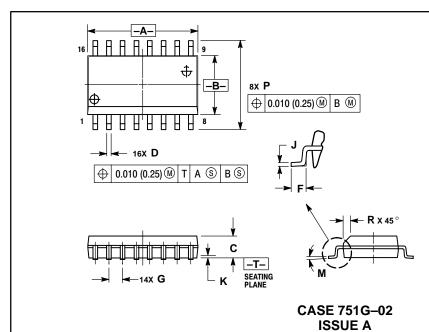
Figure 4. Delay Matching Waveform Definitions

PACKAGE DIMENSIONS



- NOTES:
 1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE
 POSITION AT SEATING PLANE AT MAXIMUM
 MATERIAL CONDITION.
 2. DIMENSION L TO CENTER OF LEADS WHEN
 FORMED PARALLEL.
 3. DIMENSION B DOES NOT INCLUDE MOLD
 FI ASH
- FLASH.
 4. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.715	0.770	18.16	19.56
В	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54	BSC
Н	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300	BSC	7.62	BSC
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1 01



- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- SIDE.

 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	10.15	10.45	0.400	0.411
В	7.40	7.60	0.292	0.299
С	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

MPIC2112

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