

NTD110N02R

Power MOSFET 110 Amps, 24 Volts

N-Channel DPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	24	Vdc
Gate-to-Source Voltage - Continuous	V_{GS}	± 20	Vdc
Thermal Resistance - Junction-to-Case	$R_{\theta JC}$	1.35	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	92.5	W
Drain Current			
- Continuous @ $T_A = 25^\circ\text{C}$, Chip	I_D	110	A
- Continuous @ $T_A = 25^\circ\text{C}$, Limited by Package	I_D	110	A
- Continuous @ $T_A = 25^\circ\text{C}$, Limited by Wires	I_D	32	A
- Single Pulse ($t_p = 10 \mu\text{s}$)	I_D	110	A
Thermal Resistance			
- Junction-to-Ambient (Note 1)	$R_{\theta JA}$	52	$^\circ\text{C/W}$
- Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.4	W
- Drain Current - Continuous @ $T_A = 25^\circ\text{C}$	I_D	17	A
Thermal Resistance			
- Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^\circ\text{C/W}$
- Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.25	W
- Drain Current - Continuous @ $T_A = 25^\circ\text{C}$	I_D	12	A
Operating and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50 \text{ Vdc}$, $V_{GS} = 10 \text{ Vdc}$, $I_L = 15.5 \text{ Apk}$, $L = 1.0 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	120	mJ
Maximum Lead Temperature for Soldering Purposes, $1/8''$ from case for 10 seconds	T_L	260	$^\circ\text{C}$

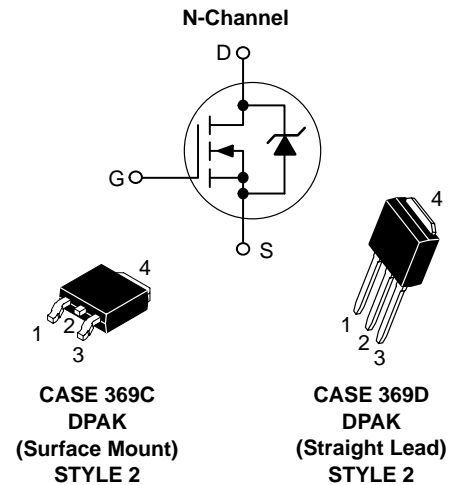
1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. When surface mounted to an FR4 board using 0.5 sq. in. drain pad size.



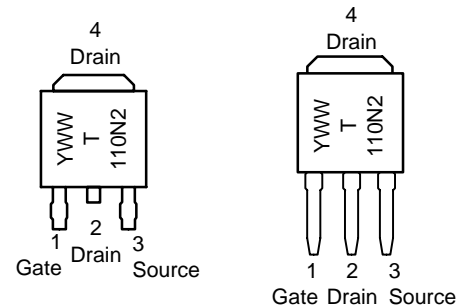
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
24 V	3.7 m Ω @ 4.5 V	110 A



MARKING DIAGRAM & PIN ASSIGNMENTS



Y = Year
WW = Work Week
110N02R = Device Code

ORDERING INFORMATION

Device	Package	Shipping
NTD110N02R	DPAK	75 Units/Rail
NTD110N02RT4	DPAK	2500/Tape & Reel
NTD110N02R-1	DPAK Straight Lead	75 Units/Rail

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Positive Temperature Coefficient	V _{(BR)DSS}	24 -	28 15	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	- -	- -	1.5 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	±100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μAdc) Negative Threshold Temperature Coefficient	V _{GS(th)}	1.0 -	1.5 5.0	2.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 10 Vdc, I _D = 110 Adc) (V _{GS} = 4.5 Vdc, I _D = 55 Adc) (V _{GS} = 10 Vdc, I _D = 20 Adc) (V _{GS} = 4.5 Vdc, I _D = 20 Adc)	R _{DS(on)}	- - - -	3.7 4.9 3.7 4.7	- - 4.6 6.2	mΩ
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 15 Adc) (Note 3)	g _{FS}	-	44	-	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 20 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	-	2710	3440	pF
Output Capacitance		C _{oss}	-	1105	1670	
Transfer Capacitance		C _{rss}	-	227	640	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{GS} = 10 Vdc, V _{DD} = 10 Vdc, I _D = 40 Adc, R _G = 3.0 Ω)	t _{d(on)}	-	11	22	ns
Rise Time		t _r	-	39	80	
Turn-Off Delay Time		t _{d(off)}	-	27	40	
Fall Time		t _f	-	21	40	
Gate Charge	(V _{GS} = 4.5 Vdc, I _D = 40 Adc, V _{DS} = 10 Vdc) (Note 3)	Q _T	-	23.6	28	nC
		Q ₁	-	5.1	-	
		Q ₂	-	11	-	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 20 Adc, V _{GS} = 0 Vdc) (Note 3) (I _S = 55 Adc, V _{GS} = 0 Vdc) (I _S = 20 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	- - -	0.82 0.99 0.65	1.2 - -	Vdc
Reverse Recovery Time	(I _S = 30 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs) (Note 3)	t _{rr}	-	36.5	-	ns
		t _a	-	17.7	-	
		t _b	-	18.8	-	
Reverse Recovery Stored Charge		Q _{rr}	-	0.024	-	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

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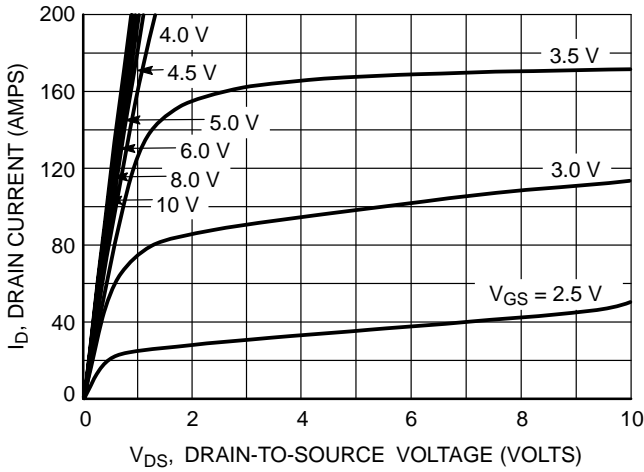


Figure 1. On-Region Characteristics

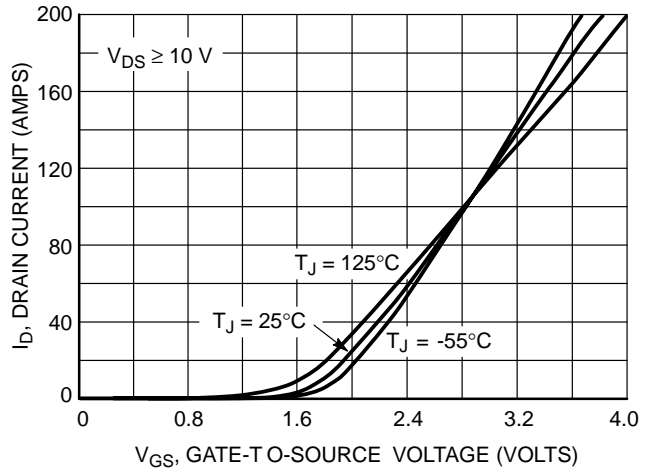


Figure 2. Transfer Characteristics

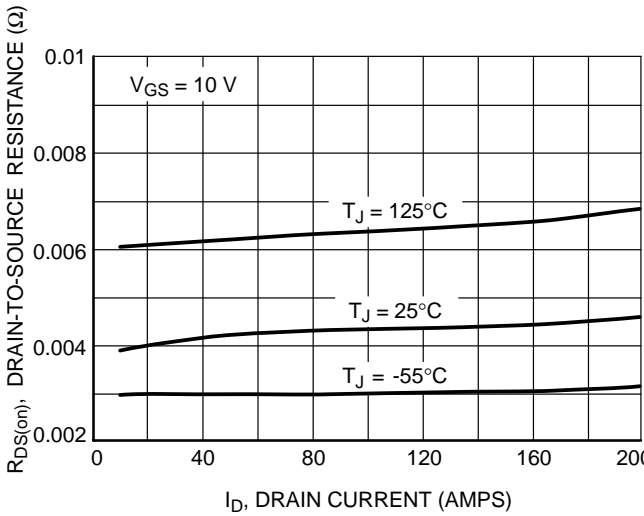


Figure 3. On-Resistance versus Drain Current and Temperature

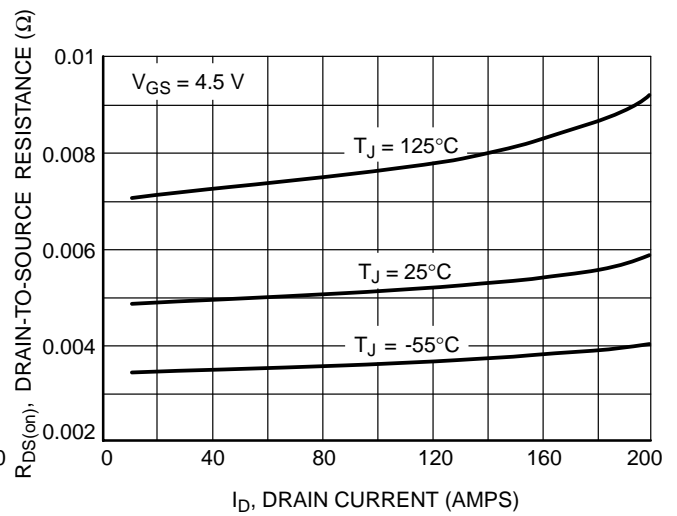


Figure 4. On-Resistance versus Drain Current and Temperature

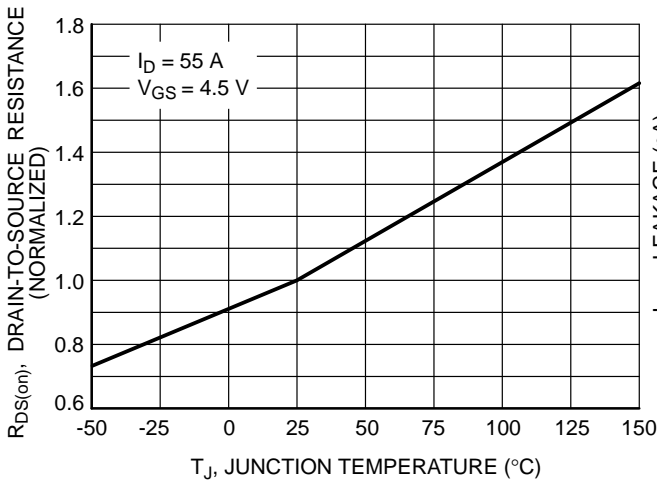


Figure 5. On-Resistance Variation with Temperature

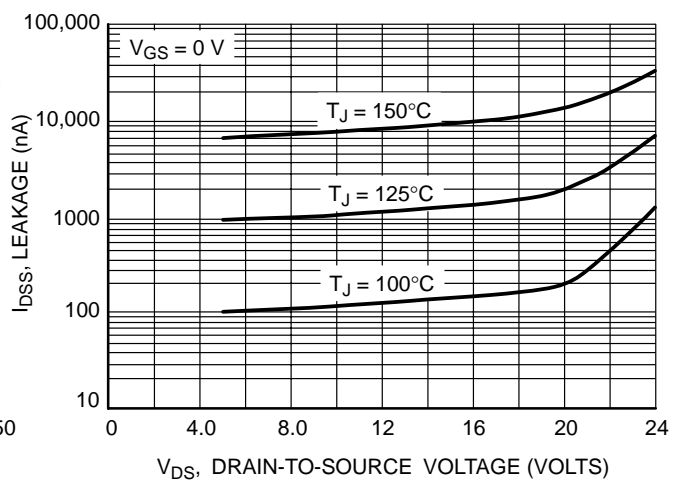


Figure 6. Drain-to-Source Leakage Current versus Voltage

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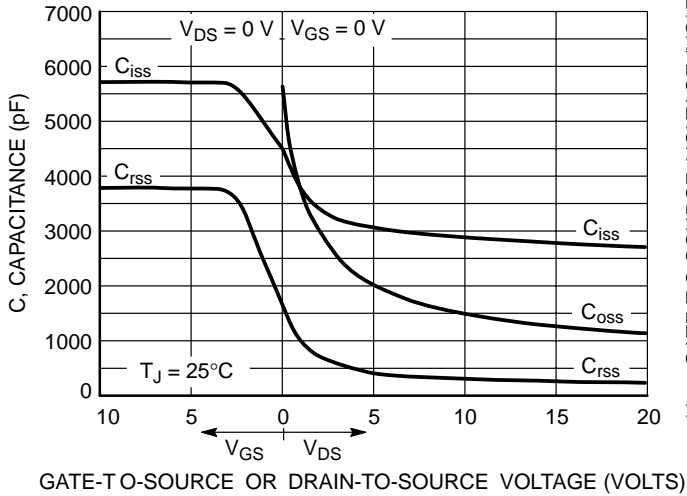


Figure 7. Capacitance Variation

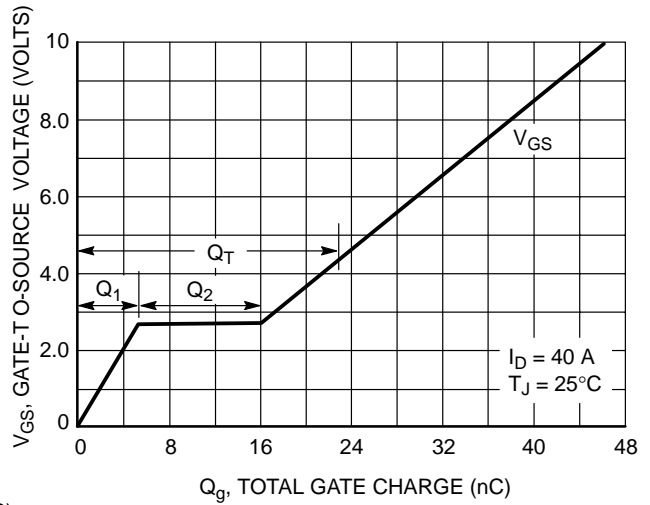


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

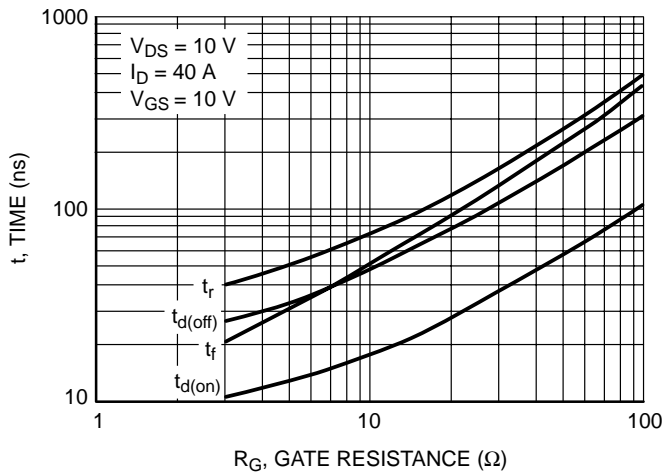


Figure 9. Resistive Switching Time Variation versus Gate Resistance

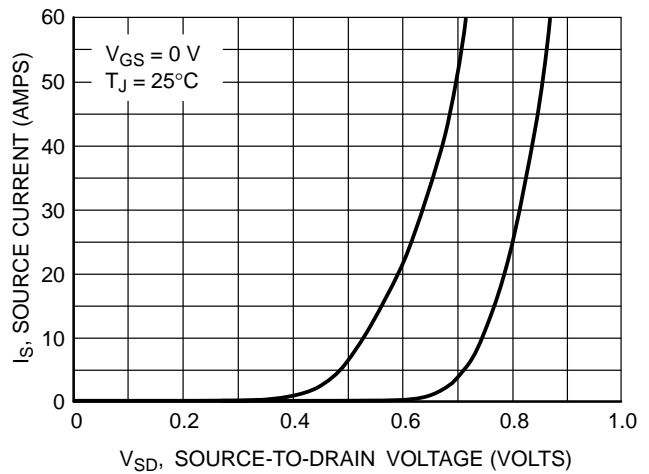


Figure 10. Diode Forward Voltage versus Current

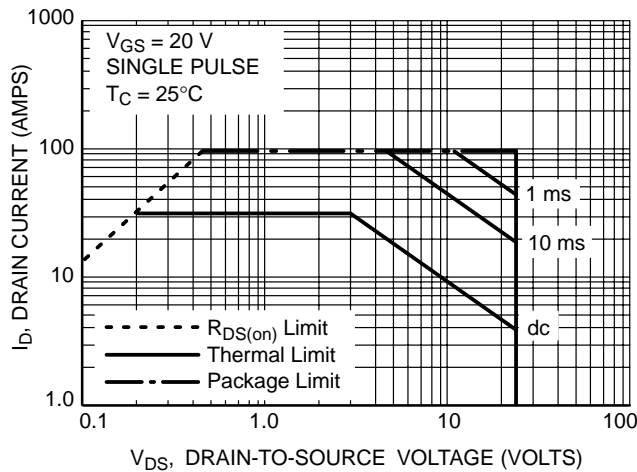


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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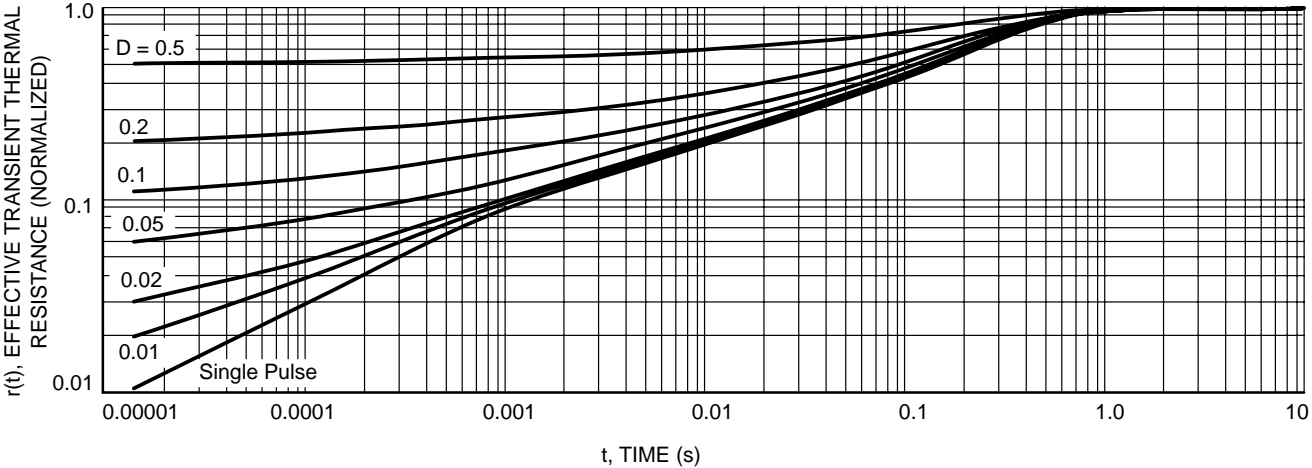


Figure 12. Thermal Response

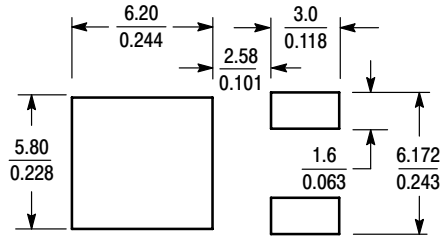
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INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

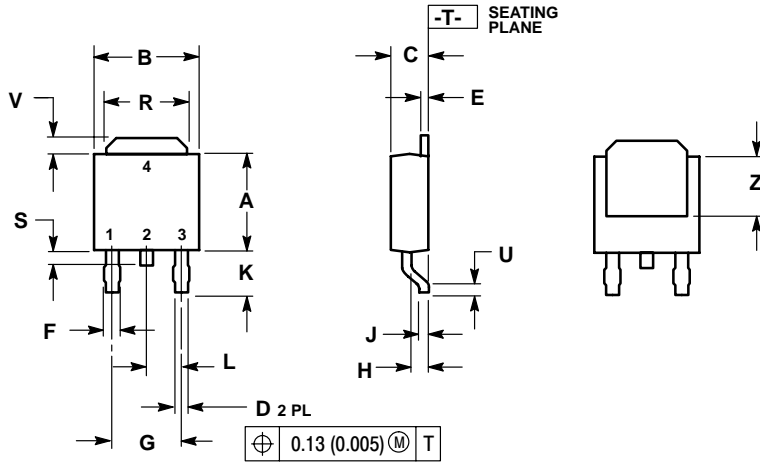


SCALE 3:1 ($\frac{\text{mm}}{\text{inches}}$)

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PACKAGE DIMENSIONS

DPAK
CASE 369C-01
ISSUE O



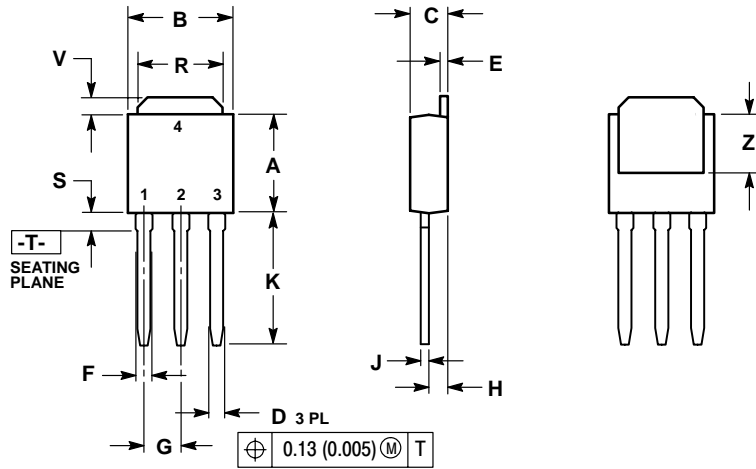
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NTD110N02R

PACKAGE DIMENSIONS

DPAK
CASE 369D-01
ISSUE O




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

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