

NTHD3101F

Power MOSFET and Schottky Diode

–20 V, Fetky, P–Channel, –3.2 A, with 2.2A Schottky Barrier Diode, ChipFET™

Features

- Leadless SMD Package Featuring a MOSFET and Schottky Diode
- 40% Smaller than TSOP–6 Package
- Leadless SMD Package Provides Great Thermal Characteristics
- Independent Pinout to each Device to Ease Circuit Design
- Trench P–Channel for Low On Resistance
- Ultra Low VF Schottky

Applications

- Li–Ion Battery Charging
- High Side DC–DC Conversion Circuits
- High Side Drive for Small Brushless DC Motors
- Power Management in Portable, Battery Powered Products

MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Units
Drain-to-Source Voltage			V _{DSS}	−20	V
Gate-to-Source Voltage			V _{GS}	±8.0	V
Continuous Drain Current (Note 1)	Steady State	T _J = 25°C	I _D	−3.2	A
		T _J = 85°C		−2.3	
	t≤10 s	T _J = 25°C		−4.4	
Power Dissipation (Note 1)	Steady State	T _J = 25°C	P _D	1.1	W
	t≤10 s			2.1	
Pulsed Drain Current	t _p = 10 μs		I _{DM}	−13	A
Operating Junction and Storage Temperature			T _J , T _{STG}	−55 to 150	°C
Source Current (Body Diode)			I _S	−1.1	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

SCHOTTKY DIODE MAXIMUM RATINGS

(T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Units
Peak Repetitive Reverse Voltage	V _{RRM}	20	V
DC Blocking Voltage	V _R	20	V
Average Rectified Forward Current	I _F	2.2	A

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction–to–Ambient – Steady State (Note 1)	R _{θJA}	113	°C/W
Junction–to–Ambient – t ≤ 10 s (Note 1)	R _{θJA}	60	°C/W

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).



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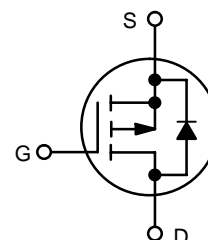
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MOSFET

V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
–20 V	64 mΩ @ –4.5 V	–3.2 A
	85 mΩ @ –2.5 V	

SCHOTTKY DIODE

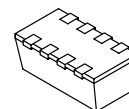
V _R MAX	V _F TYP	I _F MAX
20 V	0.510 V	2.2 A



P–Channel MOSFET

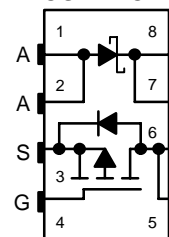


SCHOTTKY DIODE

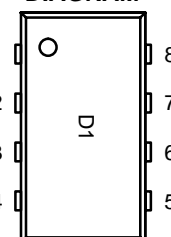


ChipFET
CASE 1206A
STYLE 3

PIN CONNECTIONS



MARKING DIAGRAM



Top View

D1 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTHD3101FT1	ChipFET	3000/Tape & Reel
NTHD3101FT1G	ChipFET (Pb–free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTHD3101F

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			-15		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		-1.0	μA
			$T_J = 125^\circ\text{C}$		-5.0	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8.0\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-0.45		-1.5	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			2.7		mV/ $^\circ\text{C}$
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -3.2\text{ A}$		64	80	m Ω
		$V_{GS} = -2.5\text{ V}, I_D = -2.2\text{ A}$		85	110	
		$V_{GS} = -1.8\text{ V}, I_D = -1.0\text{ A}$		120	170	
Forward Transconductance	g_{FS}	$V_{DS} = -10\text{ V}, I_D = -2.9\text{ A}$		8.0		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -10\text{ V}$		680		pF
Output Capacitance	C_{OSS}			100		
Reverse Transfer Capacitance	C_{RSS}			70		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -3.2\text{ A}$		7.4		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.6		
Gate-to-Source Charge	Q_{GS}			1.4		
Gate-to-Drain Charge	Q_{GD}			2.5		

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -10\text{ V}, I_D = -3.2\text{ A}, R_G = 2.4\text{ }\Omega$		5.8		ns
Rise Time	t_r			11.7		
Turn-Off Delay Time	$t_{d(OFF)}$			16		
Fall Time	t_f			12.4		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -3.2\text{ A}$	$T_J = 25^\circ\text{C}$		-0.8	-1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_S = -1.0\text{ A}, di_S/dt = 100\text{ A}/\mu\text{s}$		13.5			ns
Charge Time	t_a			9.5			
Discharge Time	t_b			4.0			
Reverse Recovery Charge	Q_{RR}			6.5			nC

SCHOTTKY DIODE ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Maximum Instantaneous Forward Voltage	V_F	$I_F = 0.1\text{ A}$		0.425		V
		$I_F = 1.0\text{ A}$		0.510	0.575	
Maximum Instantaneous Reverse Current	I_R	$V_R = 10\text{ V}$			1.0	μA
		$V_R = 20\text{ V}$			5.0	

2. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

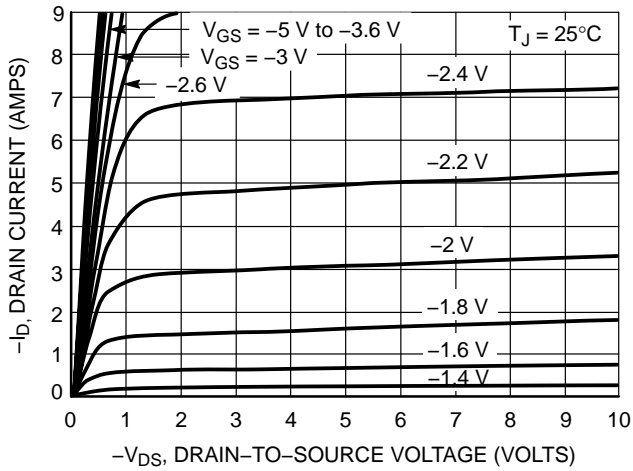


Figure 1. On-Region Characteristics

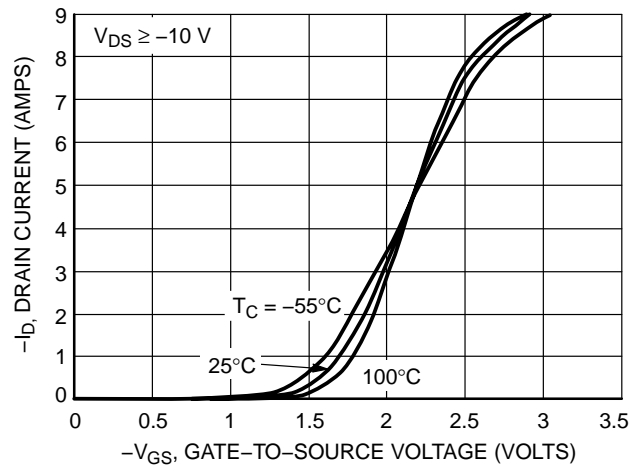


Figure 2. Transfer Characteristics

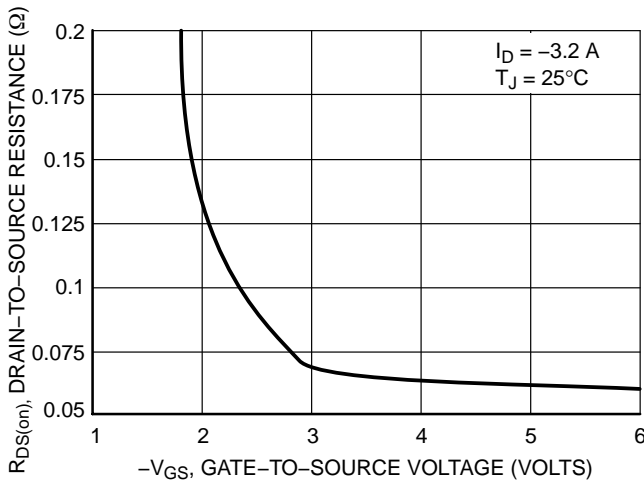


Figure 3. On-Resistance vs. Gate-to-Source Voltage

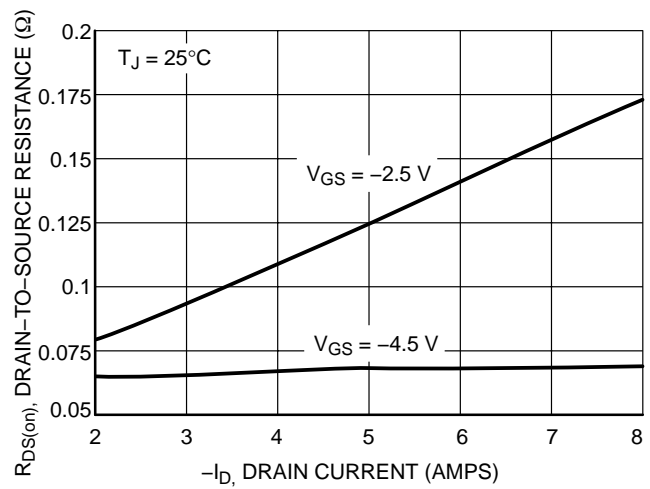


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

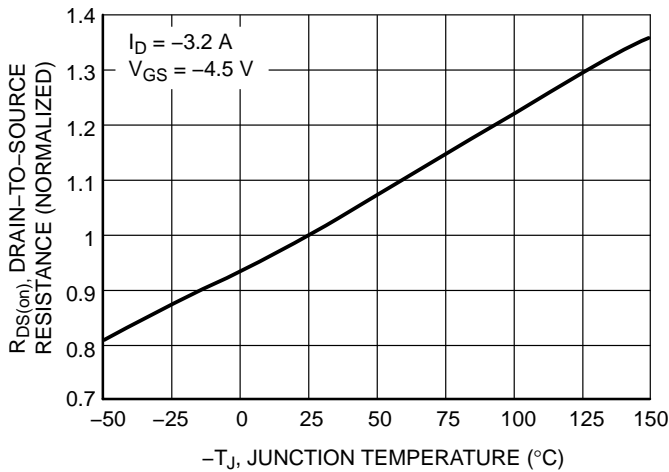


Figure 5. On-Resistance Variation with Temperature

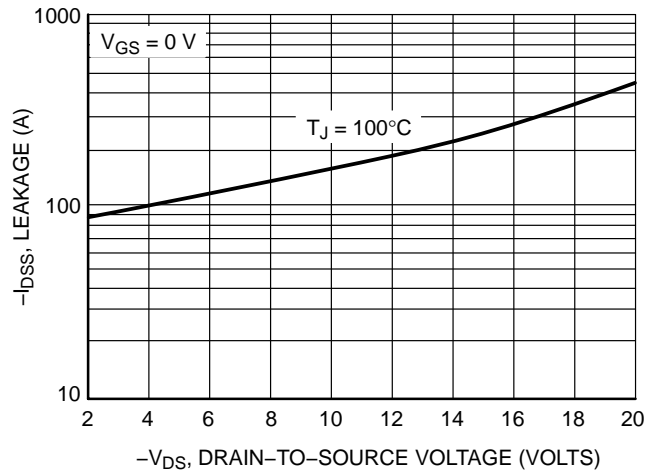
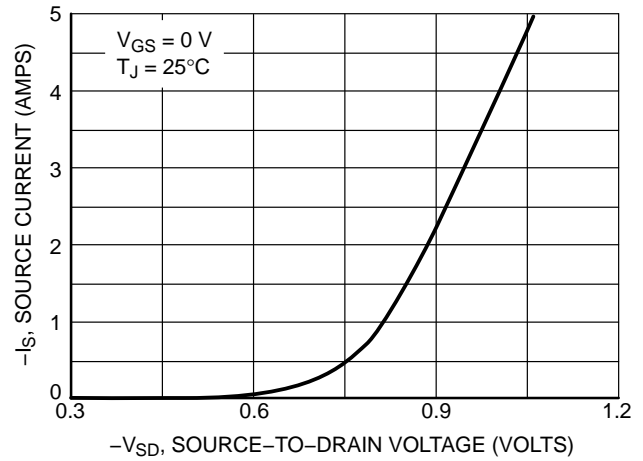
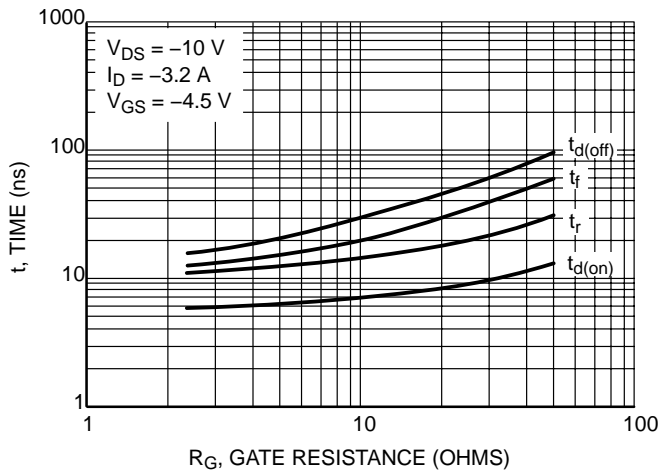
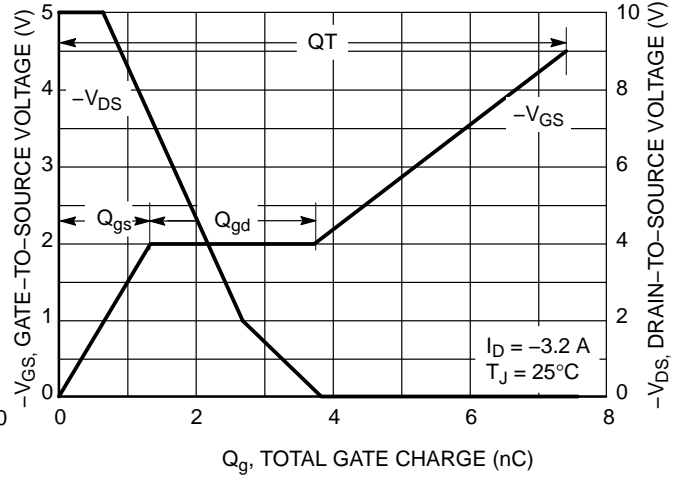
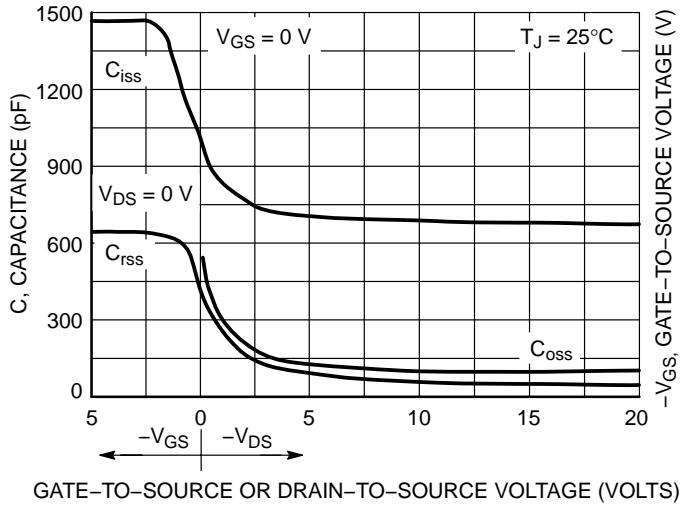


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)



TYPICAL SCHOTTKY PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

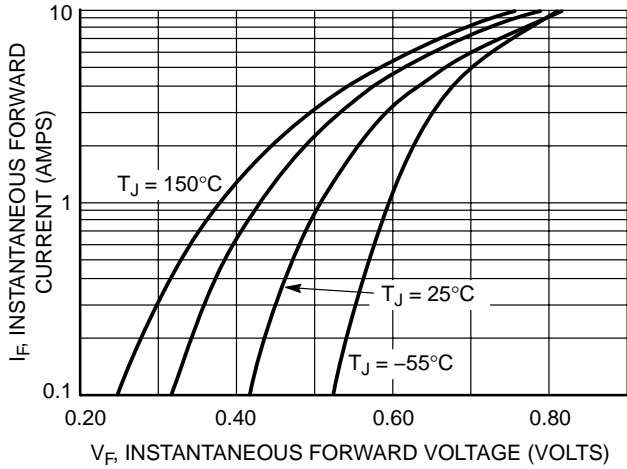


Figure 11. Typical Forward Voltage

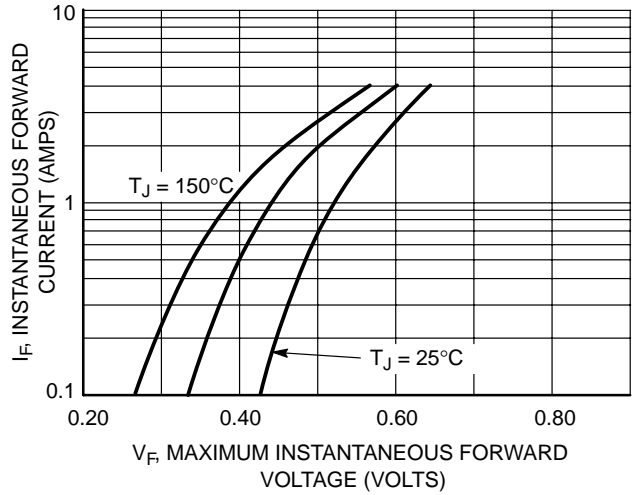


Figure 12. Maximum Forward Voltage

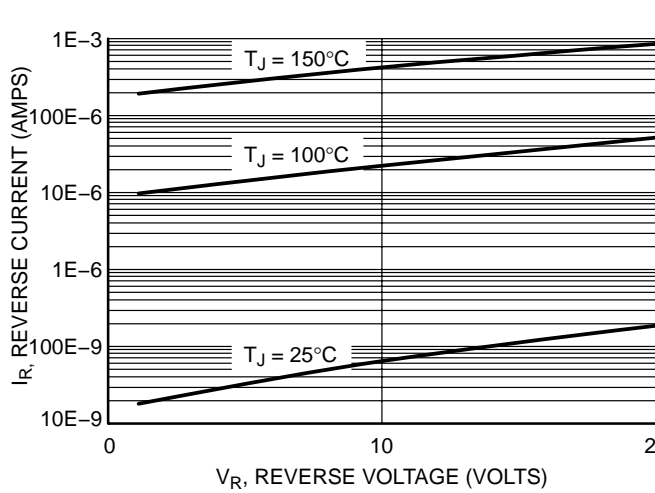


Figure 13. Typical Reverse Current

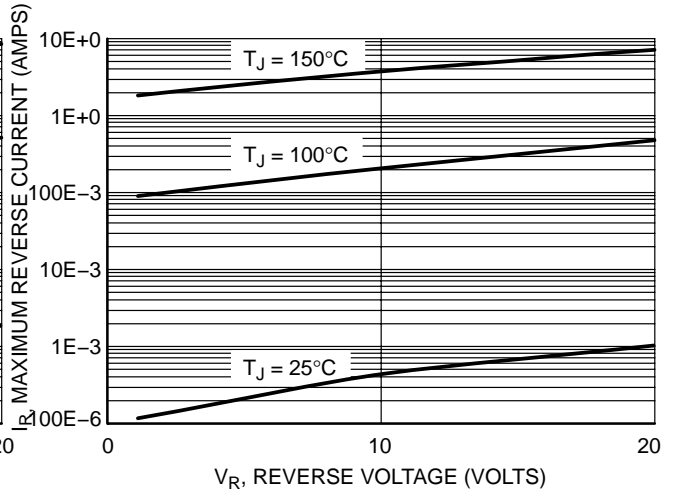


Figure 14. Maximum Reverse Current

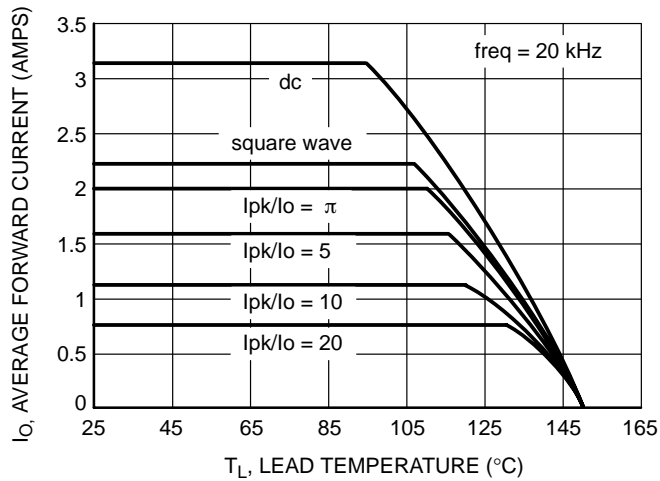


Figure 15. Current Derating

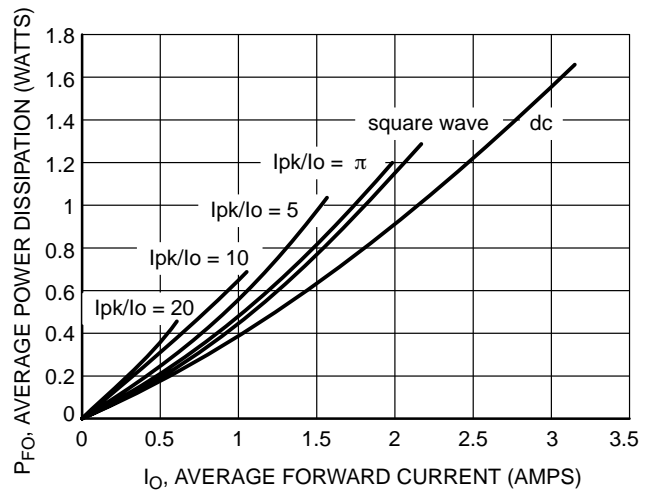


Figure 16. Forward Power Dissipation

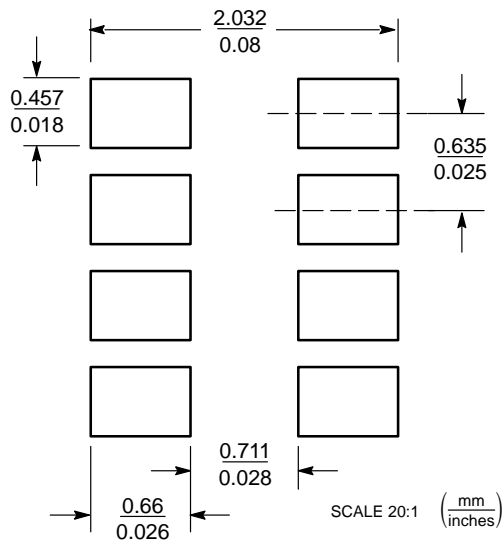


Figure 17. Basic

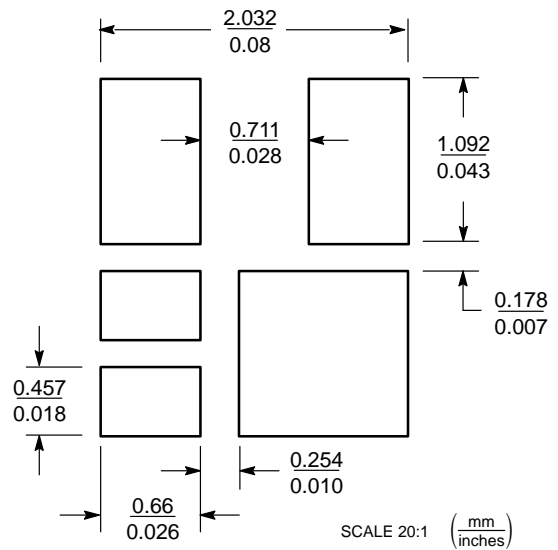


Figure 18. Style 3

BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 17. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

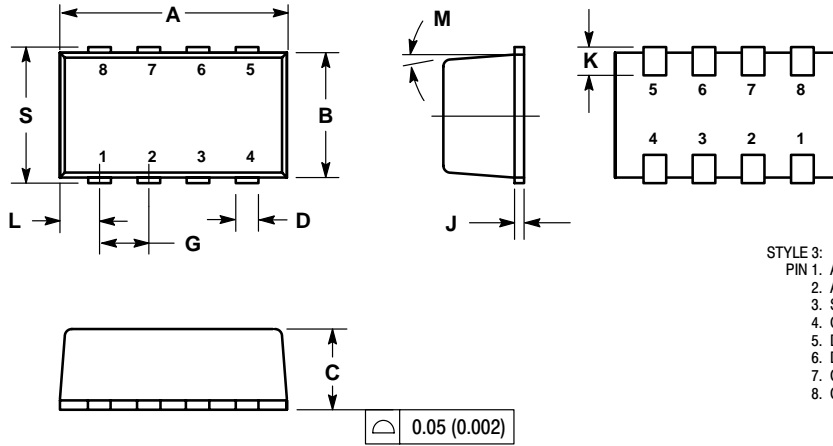
The minimum recommended pad pattern shown in Figure 18 improves the thermal area of the drain connections (pins 5, 6) while remaining within the confines

of the basic footprint. The drain copper area is 0.0019 sq. in. (or 1.22 sq. mm). This will assist the power dissipation path away from the device (through the copper lead-frame) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

NTHD3101F

PACKAGE DIMENSIONS

ChipFET CASE 1206A-03 ISSUE E




STYLE 3:
PIN 1. A
2. A
3. S
4. G
5. D
6. D
7. C
8. C

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5 ° NOM		5 ° NOM	
S	1.80	2.00	0.072	0.080

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