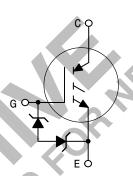
Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

N-Channel Enhancement-Mode Silicon Gate

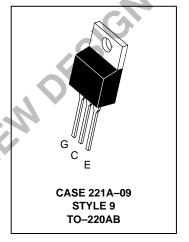
This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage—blocking capability. Its new 600 V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{\text{CE(on)}}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. This new E–series introduces an energy efficient, ESD protected, and short circuit rugged device.

- Industry Standard TO-220 Package
- High Speed: E_{off} = 60 μJ/A typical at 125°C
- High Voltage Short Circuit Capability 10 μs minimum at 125°C, 400 V
- Low On–Voltage 2.0 V typical at 3.0 A, 125°C
- Robust High Voltage Termination
- ESD Protection Gate-Emitter Zener Diodes



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IGBT IN TO-220 4.0 A @ 90°C 6.0 A @ 25°C 600 VOLTS SHORT CIRCUIT RATED LOW ON-VOLTAGE



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V _{CES}	600	Vdc
Collector–Gate Voltage ($R_{GE} = 1.0 \text{ M}\Omega$)	V _{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V _{GE}	±20	Vdc
Collector Current — Continuous @ T _C = 25°C — Continuous @ T _C = 90°C — Repetitive Pulsed Current (1)	I _{C25} I _{C90} I _{CM}	6.0 4.0 8.0	Adc Apk
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	62.5 0.51	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t _{sc}	10	μS
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	R _{θJC} R _{θJA}	2.0 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

⁽¹⁾ Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Characteristic		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V _{GE} = 0 Vdc, I _C = 250 µAdc) Temperature Coefficient (Positive)			600 —	— 870		Vdc mV/°C
Emitter-to-Collector Breakdown	V _{(BR)ECS}	15	_	_	Vdc	
Zero Gate Voltage Collector Current $ (V_{CE} = 600 \text{ Vdc}, V_{GE} = 0 \text{ Vdc}) $ $ (V_{CE} = 600 \text{ Vdc}, V_{GE} = 0 \text{ Vdc}, T_{J} = 125^{\circ}\text{C}) $					10 200	μAdc
Gate-Body Leakage Current (V _G	I _{GES}	_	_	50	μAdc	
ON CHARACTERISTICS (1)						_
Collector-to-Emitter On-State V (V_{GE} = 15 Vdc, I_{C} = 1.5 Adc) (V_{GE} = 15 Vdc, I_{C} = 1.5 Adc, T (V_{GE} = 15 Vdc, I_{C} = 3.0 Adc)	V _{CE(on)}	_ _ _	1.6 1.5 2.0	1.9	Vdc	
Gate Threshold Voltage $(V_{CE} = V_{GE}, I_C = 1.0 \text{ mAdc})$ Threshold Temperature Coefficient (Negative)		V _{GE(th)}	4.0 —	6.0 10	8.0 —	Vdc mV/°C
Forward Transconductance (V _{CE}	9 _{fe}		1.8	_	Mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance		C _{ies}	7	342	_	pF
Output Capacitance	$(V_{CE} = 25 \text{ Vdc}, V_{GE} = 0 \text{ Vdc}, f = 1.0 \text{ MHz})$	C _{oes}		40	_	
Transfer Capacitance		C _{res}	_	3.0	_	
SWITCHING CHARACTERISTICS	5 (1)					
Turn-On Delay Time		t _{d(on)}	_	34	_	ns
Rise Time	$(V_{CC} = 360 \text{ Vdc}, I_C = 3.0 \text{ Adc},$	t _r	_	30	_	
Turn-Off Delay Time	$V_{GE} = 15 \text{ Vdc}, L = 300 \mu\text{H}, \\ R_{G} = 20 \Omega)$	t _{d(off)}	_	36	_	
Fall Time	Energy losses include "tail"	t _f	_	216	_	
Turn-Off Switching Loss		E _{off}	_	0.10	0.15	mJ
Turn-On Delay Time		t _{d(on)}	_	33	_	ns
Rise Time	$(V_{CC} = 360 \text{ Vdc}, I_{C} = 3.0 \text{ Adc},$	t _r	_	32	_	
Turn-Off Delay Time	$V_{GE} = 15 \text{ Vdc}, L = 300 \mu\text{H}, \\ R_{G} = 20 \Omega, T_{J} = 125^{\circ}\text{C})$	t _{d(off)}	_	56	_	
Fall Time	Energy losses include "tail"	t _f	_	340	_	1
Turn-Off Switching Loss		E _{off}	_	0.165	_	mJ
Gate Charge		Q _T	_	18.1	_	nC
	$(V_{CC} = 360 \text{ Vdc}, I_{C} = 3.0 \text{ Adc}, V_{GE} = 15 \text{ Vdc})$	Q ₁	_	3.8	_	1
	vGE = 13 vuc)	Q ₂	_	7.8	_	
NTERNAL PACKAGE INDUCTAR	ICE					
Internal Emitter Inductance (Measured from the emitter lead 0.25" from package to emitter bond pad)		LE	_	7.5	_	nH

⁽Measured from the emitter lead 0.25" from package (1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

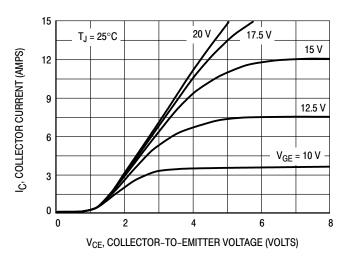


Figure 1. Output Characteristics

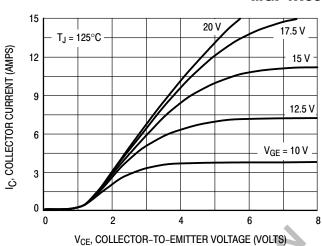


Figure 2. Output Characteristics

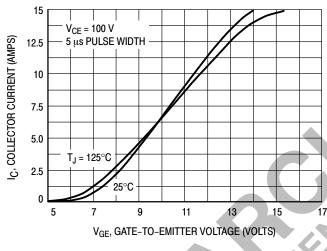


Figure 3. Transfer Characteristics

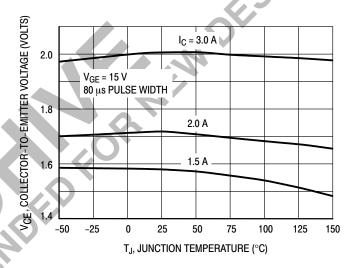


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

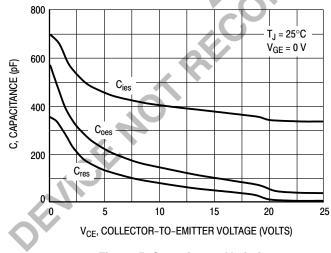


Figure 5. Capacitance Variation

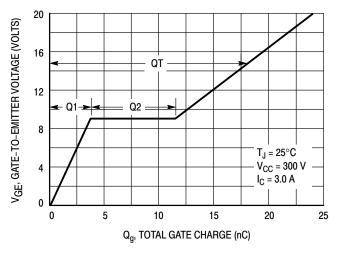


Figure 6. Gate-To-Emitter Voltage versus
Total Charge

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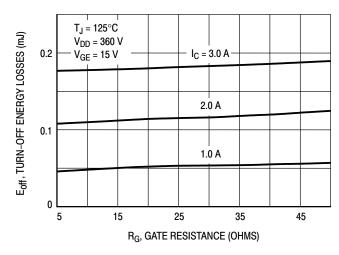


Figure 7. Turn-Off Losses versus **Gate Resistance**

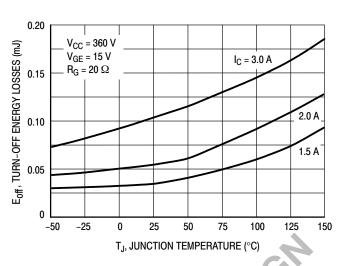
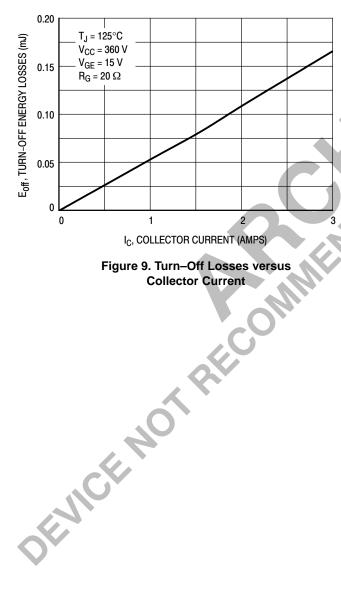


Figure 8. Turn-Off Losses versus **Junction Temperature**



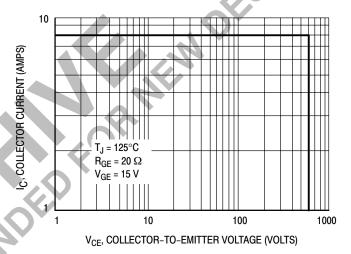
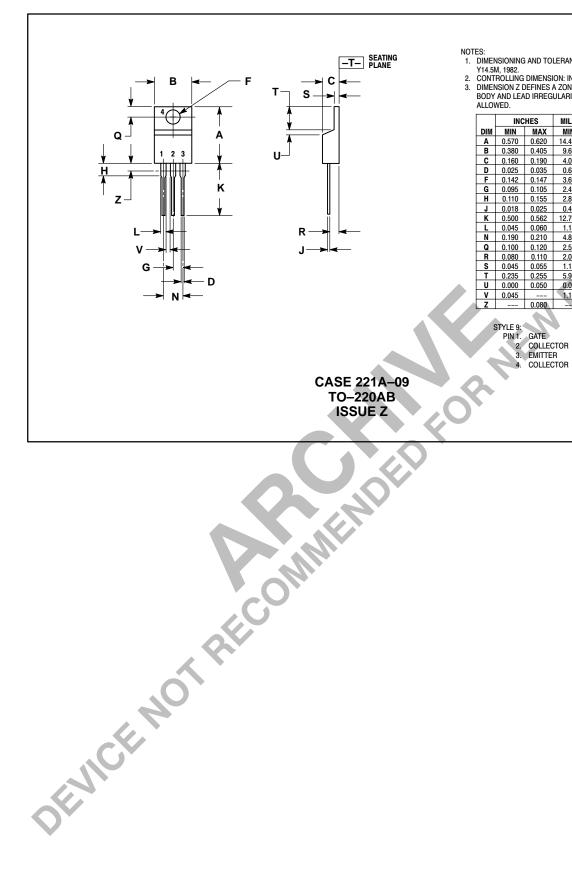


Figure 10. Reverse Biased Safe **Operating Area**

PACKAGE DIMENSIONS



- DIMENSIONING AND TOLERANCING PER ANSI
- DIMENSIONING AND TOLERANCING PER ANS Y14.5M, 1982. CONTROLLING DIMENSION: INCH. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INC	HES	MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
Н	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
Г	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
Т	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

TO-220AB



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