NTMD4102PR2

Product Preview **Trench Power MOSFET** -20 V, P-Channel, SO-8 Dual

This P-Channel device was designed using ON Semiconductor's leading edge trench technology for low $R_{DS(on)}$ performance in the SO-8 dual package for high power and current handling capability. The low $R_{DS(on)}$ performance is particularly suited for game systems, notebook and desktop computers, and printers.

Features & Benefits

- Leading -20 V Trench for Low R_{DS(on)}
- SO-8 Package Provides Excellent Thermal Performance
- Surface Mount SO-8 Package Saves Board Space
- Pb Free Package for Green Manufacturing

Applications

- Load/Power Management
- Battery Switching for Multi Cell Li-Ion
- Buck-Boost Synchronous Rectification

MAXIMUM RATINGS ($T_A = 25^{\circ}C$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|-----------------------------------|---------------|------|
| Drain-to-Source Voltage | V _{DSS} | -20 | V |
| Gate-to-Source Voltage | V _{GS} | ±20 | V |
| Drain Current - Continuous @ T _A = 25°C (Note 1) - Pulsed Drain Current (t = 10 μs) | I _D I _{DM} | -6.5 -30 | A |
| Steady State Power Dissipation @ T _A = 25°C (Note 1) | P _D | 1.1 | W |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | -55 to 150 | °C |
| Continuous Source Current (Body Diode) | ۱ _S | -0.9 | А |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds) | TL | 260 | °C |

THERMAL RESISTANCE RATINGS

| Thermal Resistance | | | °C/W |
|---|------------------|-----|------|
| - Junction- to- Ambient - Steady State (Note 1) | $R_{\theta JA}$ | TBD | |
| Junction-to-Ambient - t ≤ 10 s (Note 1) | $R_{\theta J A}$ | TBD | |
| - Junction-to-Lead - Steady State (Note 2) | R_{\thetaJL} | TBD | |

1. Surface-mounted on FR4 board using 1" sq pad size (Cu area = 1.127 in sq [1 oz] including traces)

 Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = TBD in sq)

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 $\begin{array}{l} V_{BR(DSS)} = -20 \ VOLTS \\ R_{DS(on)} \ (max) = 19 \ m\Omega \ @ \ -10 \ V \\ I_{D(max)} \ ^{(Note \ 1)} = -8.5 \ A \\ R_{DS(on)} \ (max) = 30 \ m\Omega \ @ \ -4.5 \ V \\ I_{D(max)} \ ^{(Note \ 1)} = -6.5 \ A \end{array}$





ORDERING INFORMATION

| Device | Package | Shipping |
|-------------|---------|------------------|
| NTMD4102PR2 | SO-8 | 2500/Tape & Reel |

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ELECTRICAL CHARACTERISTICS (T_A = 25° C unless otherwise noted)

| Characteristic | | | Min | Тур | Max | Unit |
|--|--|---------------------|------|------------|----------|------|
| OFF CHARACTERISTICS | | | | - | - | |
| Drain-to-Source Breakdown Voltage (Note 3) $(V_{GS} = 0 \text{ V}, I_D = 250 \ \mu\text{A})$ | | | -20 | - | - | V |
| Zero Gate Voltage Drain Current (Note 3) ($V_{GS} = 0 V$, $V_{DS} = -16 V$) | | | - | - | -1.0 | μΑ |
| Gate-to-Source Leakage Current $(V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V})$ | | I _{GSS} | - | - | ±100 | nA |
| ON CHARACTERISTICS | | | | | | |
| Gate Threshold Voltage (Note 3) $(V_{GS} = V_{DS}, I_D = -250 \ \mu A)$ | | V _{GS(th)} | -1.0 | - | - | V |
| Drain-to-Source On-Resistance (V_{GS} = -10 V, I_D = -8.5 A) (V_{GS} = -4.5 V, I_D = -6.5 A) | | | | TBD TBD | 19 30 | mΩ |
| Forward Transconductance ($V_{DS} = $ | -10 V, I _D = -8.4 A) | 9 FS | - | TBD | - | S |
| CHARGES, CAPACITANCES & GAT | E RESISTANCE | | | | | |
| Input Capacitance | | C _{iss} | - | TBD | - | pF |
| Output Capacitance | (V _{GS} = 0 V, f = 1 MHz, V _{DS} = -10 V) | C _{oss} | - | TBD | - | |
| Reverse Transfer Capacitance | | C _{rss} | - | TBD | - | |
| Total Gate Charge | $(V_{GS} = -4.5 V, V_{DS} = -10 V, I_{D} = -8.4 A)$ | Q _{G(tot)} | - | TBD | TBD | nC |
| Threshold Gate Charge | $(V_{GS} = -4.5 V, V_{DS} = -10 V, I_{D} = -8.4 A)$ | Q _{G(th)} | - | TBD | TBD | nC |
| Gate-to-Source Gate Charge | $(V_{DS} = -10 \text{ V}, I_D = -8.4 \text{ A})$ | Q _{GS} | - | TBD | - | nC |
| Gate-to-Drain "Miller" Charge | $(V_{DS} = -10 \text{ V}, I_D = -8.4 \text{ A})$ | Q _{GD} | - | TBD | - | nC |
| Output Charge | $(V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V})$ | Q _{OSS} | - | TBD | - | nC |
| Gate Resistance | | R _G | - | TBD | - | Ω |
| SWITCHING CHARACTERISTICS | lote 4) | 1 | | | | I |
| Turn-On Delay Time | | t _{d(on)} | - | TBD | - | ns |
| Rise Time | (V _{GS} = -4.5 V, V _{DS} = -10 V, | t _r | - | TBD | - | |
| Turn-Of f Delay Time | $I_{\rm D} = -1.0 \text{ A}, \text{ R}_{\rm G} = 6.0 \Omega$ | t _{d(off)} | - | TBD | - | |
| Fall Time | | t _f | - | TBD | - | |
| DRAIN-SOURCE DIODE CHARACT | ERISTICS | | | | | |
| Forward Diode Voltage | $(V_{GS} = 0 V, I_{SD} = -1.7 A)$ | V _{SD} | - | TBD | TBD | V |
| Reverse Recovery Time | | t _{rr} | - | TBD | TBD | ns |
| Charge Time | $(V_{GS} = 0 V, V_{DS} = -10 V,$ | | - | TBD | - | ns |
| Discharge Time | | t _b | - | TBD | - | ns |
| Reverse Recovery Charge | | Q _{rr} | - | TBD | - | nC |

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS

SOIC-8 NB CASE 751-07 **ISSUE AA**



NOTES:

- NOTES:
 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| | MILLIN | IETERS | INC | HES | |
|-----|----------|--------|-----------|-------|--|
| DIM | MIN | MAX | MIN | MAX | |
| Α | 4.80 | 5.00 | 0.189 | 0.197 | |
| В | 3.80 | 4.00 | 0.150 | 0.157 | |
| С | 1.35 | 1.75 | 0.053 | 0.069 | |
| D | 0.33 | 0.51 | 0.013 | 0.020 | |
| G | 1.27 BSC | | 0.050 BSC | | |
| Н | 0.10 | 0.25 | 0.004 | 0.010 | |
| J | 0.19 | 0.25 | 0.007 | 0.010 | |
| Κ | 0.40 | 1.27 | 0.016 | 0.050 | |
| М | 0 ° | 8 ° | 0 ° | 8 ° | |
| Ν | 0.25 | 0.50 | 0.010 | 0.020 | |
| S | 5.80 | 6 20 | 0 228 | 0 244 | |

STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN

2. 3. 4. 5. 6. 7. 8.

DRAIN

drain Drain

DRAIN

NTMD4102PR2

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JAPAN: ON Semiconductor, Japan Customer Focus Center 2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051 Phone: 81-3-5773-3850

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