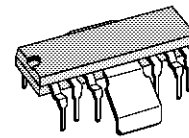


LOW-NOISE TV VERTICAL DEFLECTION SYSTEM

- COMPLETE VERTICAL DEFLECTION SYSTEM
- LOW NOISE
- SUITABLE FOR HIGH DEFINITION MONITORS

DESCRIPTION

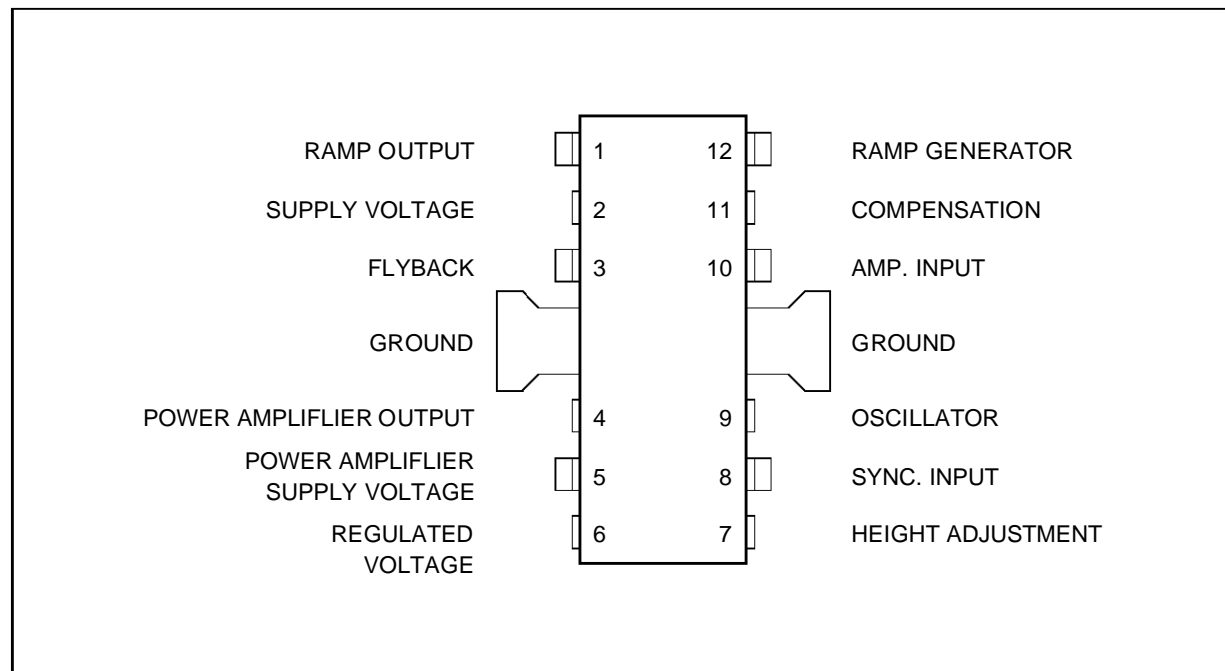
The TDA1170N is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It is intended for use in black and white and colour TV receivers. Low-noise makes this device particularly suitable for use in monitors. The functions incorporated are : synchronization circuit, oscillator and ramp generator, high power gain amplifier, flyback generator, voltage regulator.



FINDIP12
(Plastic Package)

ORDER CODE : TDA1170N

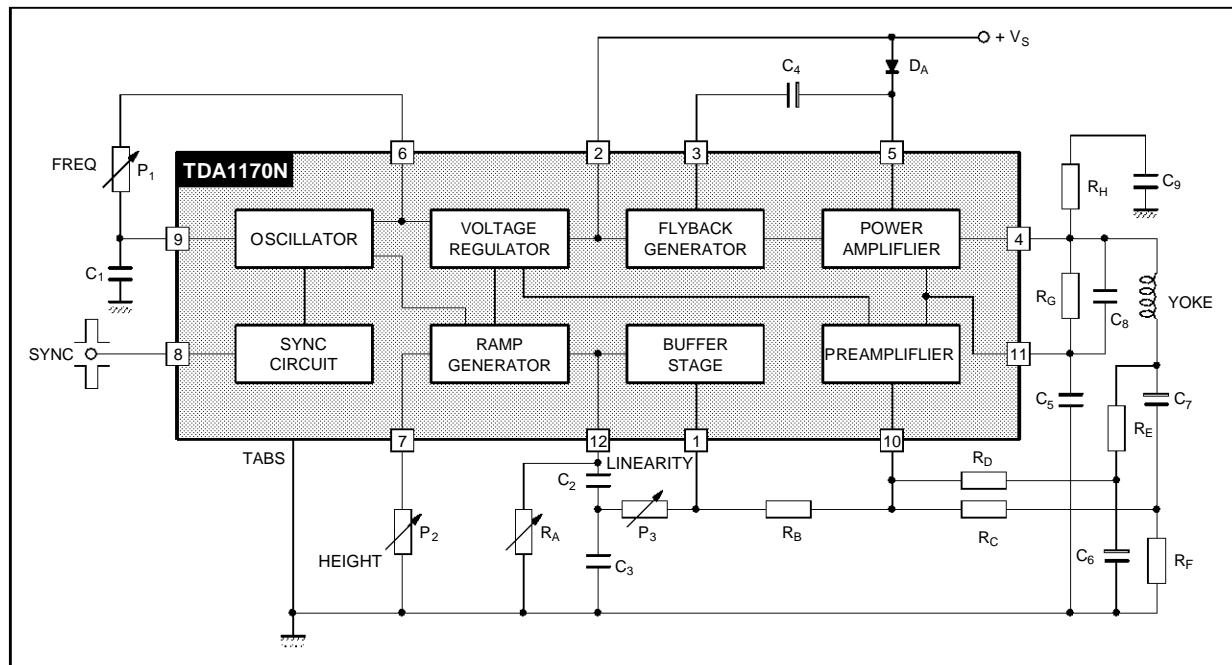
PIN CONNECTIONS



1170N-01.EPS

TDA1170N

BLOCK DIAGRAM



1170N-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 2	35	V
V_4, V_5	Flyback Peak Voltage	60	V
V_{10}	Power Amplifier Input Voltage	+ 10 - 0.5	V
I_o	Output Peak Current (non repetitive) at $t = 2\text{msec}$	2	A
I_o	Output Peak Current at $f = 50\text{Hz}$ $t \leq 10\mu\text{sec}$	2.5	A
I_o	Output Peak Current at $f = 50\text{Hz}$ $t > 10\mu\text{sec}$	1.5	A
I_3	Pin 3 DC Current at $V_4 < V_2$	100	mA
I_3	Pin 3 Peak to Peak Flyback Current for $f = 50\text{Hz}$, $t_{fly} \leq 1.5\text{msec}$	1.8	A
I_8	Pin 8 Current	± 20	mA
P_{tot}	Power Dissipation : at $T_{ab} = 90^\circ\text{C}$ at $T_{amb} = 80^\circ\text{C}$ (free air)	5 1	W
T_{stg}, T_j	Storage and Junction Temperature	- 40, +150	$^\circ\text{C}$

1170N-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j-tab}$	Thermal Resistance Junction-tab	Max	$^\circ\text{C/W}$
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max	$^\circ\text{C/W}^*$

* Obtained with tabs soldered to printed circuit with minimized copper area.

1170N-02.TBL

ELECTRICAL CHARACTERISTICS(Refer to the test circuits, $V_S = 35\text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$, unless otherwise specified)**DC CHARACTERISTICS**

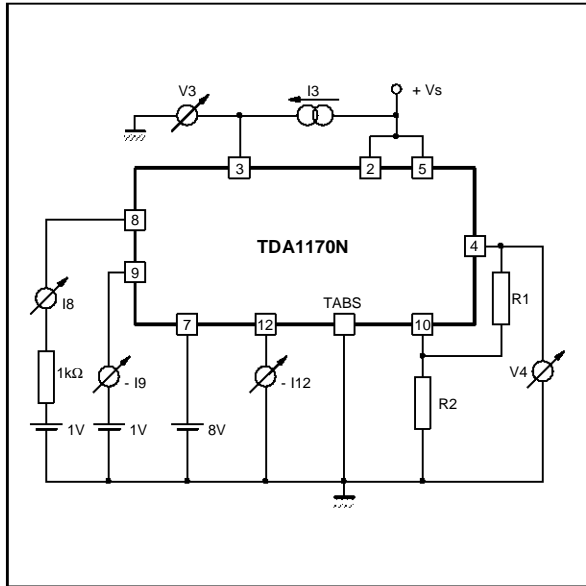
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_3 = 0$		7	14	mA	1b
I_5	Pin 5 Quiescent Current	$I_4 = 0$		8	17	mA	1b
$-I_9$	Oscillator Bias Current	$V_9 = 1\text{V}$		0.1	1	μA	1a
$-I_{10}$	Amplifier Input Bias Current	$V_{10} = 1\text{V}$		1	10	μA	1b
$-I_{12}$	Ramp Generator Bias Current	$V_{12} = 0$		0.02	0.3	μA	1a
$-I_{12}$	Ramp Generator Current	$I_7 = 20\mu\text{A}$, $V_{12} = 0$	18.5	20	21.5	μA	1b
$\frac{\Delta I_{12}}{I_{12}}$	Ramp Generator Non-linearity	$\Delta V_{12} = 0$ to 12V , $I_7 = 20\mu\text{A}$		0.2	1	%	1b
V_S	Supply Voltage Range		10		35	V	
V_1	Pin 1 Saturation Voltage to Ground	$I_1 = 1\text{mA}$		1	1.4	V	
V_3	Pin 3 Saturation Voltage to Ground	$I_3 = 10\text{mA}$		300	450	mV	1a
V_4	Quiescent output Voltage	$V_S = 10\text{V}$ $R_1 = 1\text{k}\Omega$, $R_2 = 1\text{k}\Omega$	4.1	4.4	4.75	V	1a
		$V_S = 35\text{V}$ $R_1 = 3\text{k}\Omega$, $R_2 = 1\text{k}\Omega$	8.3	8.8	9.45	V	1a
V_{4L}	Output Saturation Voltage to Ground	$-I_4 = 0.1\text{A}$		0.9	1.2	V	1c
		$-I_4 = 0.8\text{A}$		1.9	2.3	V	1c
V_{4H}	Output Saturation Voltage to Supply	$I_4 = 0.1\text{A}$		1.4	2.1	V	1d
		$I_4 = 0.8\text{A}$		2.8	3.2	V	1d
V_6	Regulated Voltage at Pin 6		6.1	6.5	6.9	V	1b
V_7	Regulated Voltage at Pin 7	$I_7 = 20\mu\text{A}$	6.2	6.6	7	V	1b
$\frac{ \Delta V_6 }{\Delta V_S}, \frac{\Delta V_7}{\Delta V_S}$	Regulated Voltage Drift with Supply Voltage	$\Delta V_S = 10$ to 35V		1		mV/V	1b
V_{10}	Amplifier Input Reference Voltage		2.07	2.2	2.3	V	
R8	Pin 8 Input Resistance	$V_8 \leq 0.4\text{V}$	1			$\text{M}\Omega$	1a

1170N-03.TBL

TDA1170N

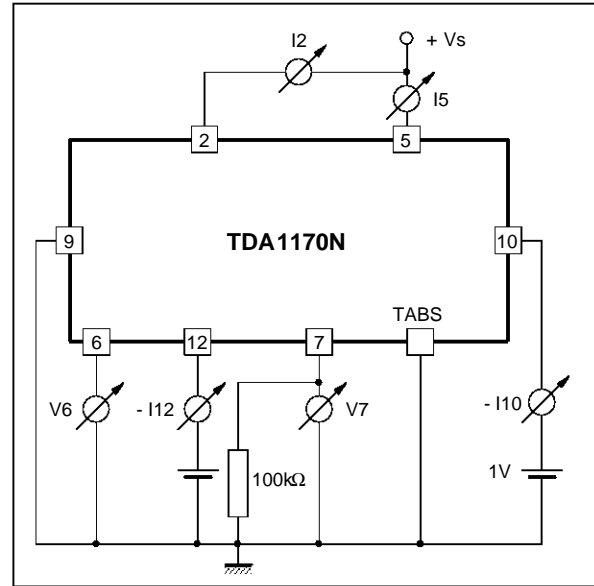
Figure 1 : DC Test Circuits

Figure 1a



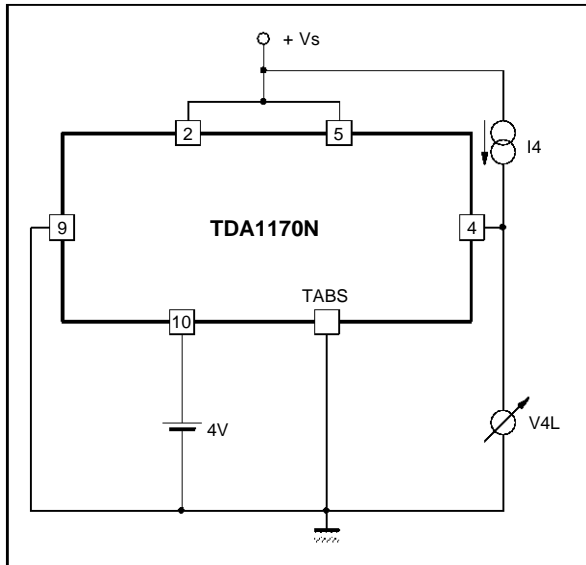
1170N-03.EPS

Figure 1b



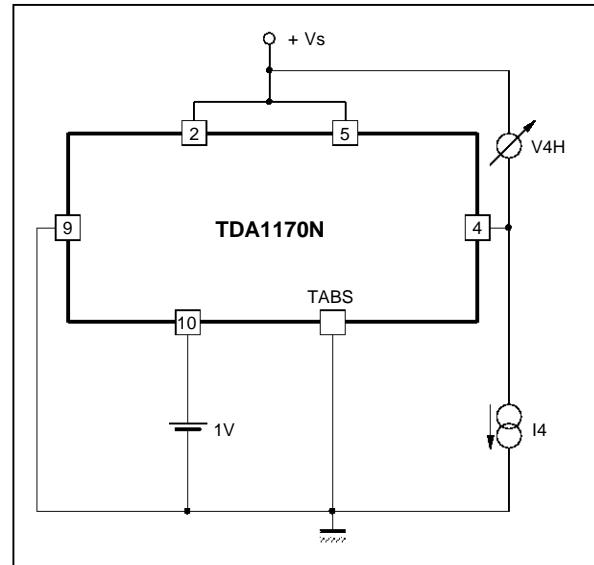
1170N-04.EPS

Figure 1c



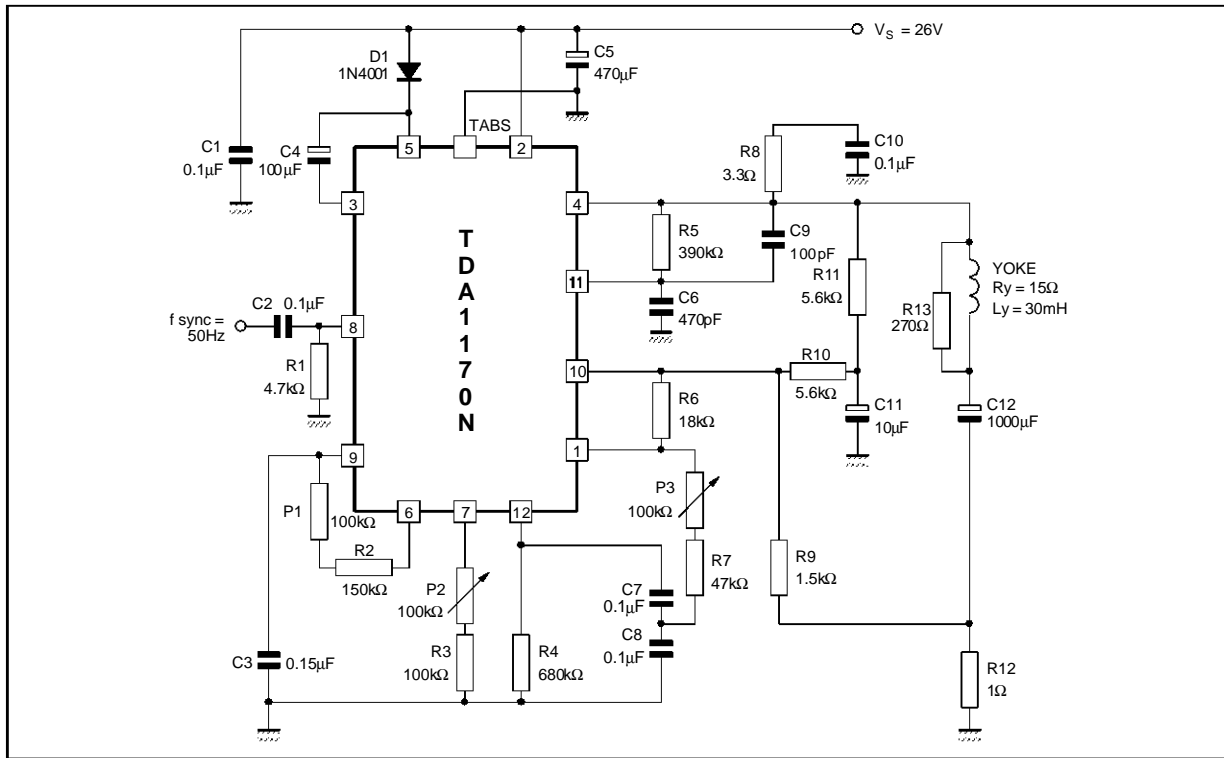
1170N-05.EPS

Figure 1d



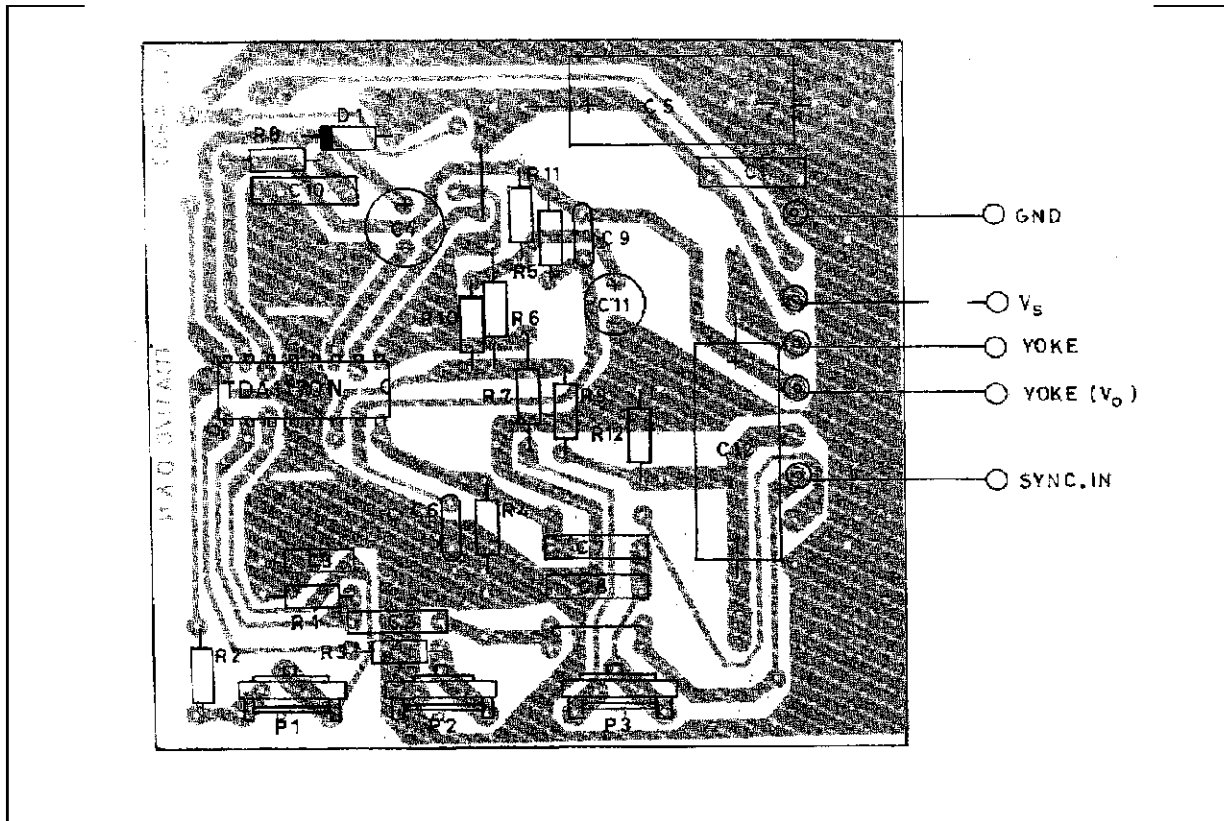
1170N-06.EPS

Figure 3 : Typical Application Circuit for Small Screen 90° TVC Set ($R_Y = 15\Omega$, $L_Y = 30\text{mH}$, $I_Y = 0.82\text{ App}$)



1170N-08.EPS

Figure 4 : P.C. Board and Components Layout of the Circuit of fig. 3 (1:1 scale)



1170N-09.TIF

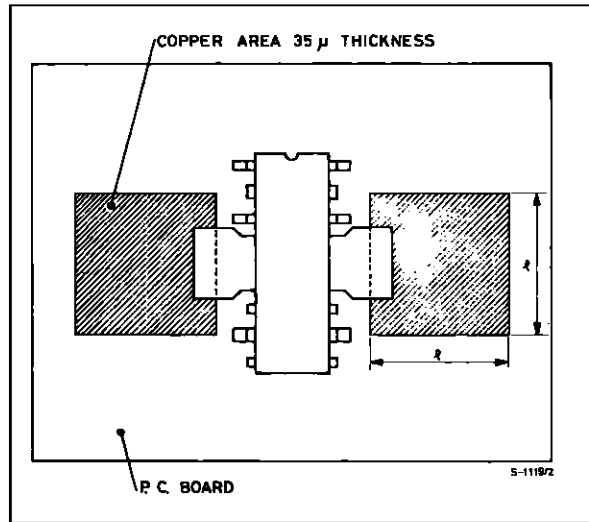
MOUNTING INSTRUCTION

During soldering the tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

The junction to ambient thermal resistance can be

Figure 5 : Example of P.C. Board Copper Area Used as Heatsink

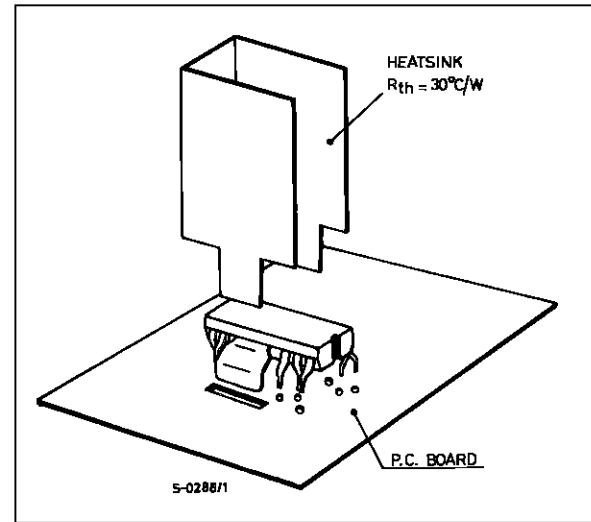


1170N-10.EPS

reduced by soldering the tabs to a suitable copper area of the printed circuit board (fig. 5) or to an external heatsink (fig. 6).

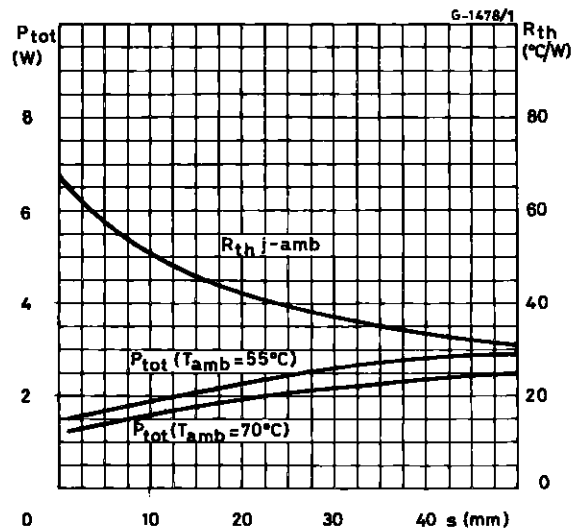
The diagram of fig. 7 shows the maximum dissippable power P_{tot} and the $R_{th\ j-amb}$ as a function of the side "e" of two equal square copper areas having a thickness of 35 μ (1.4 mil).

Figure 6 : Example of External heatsink



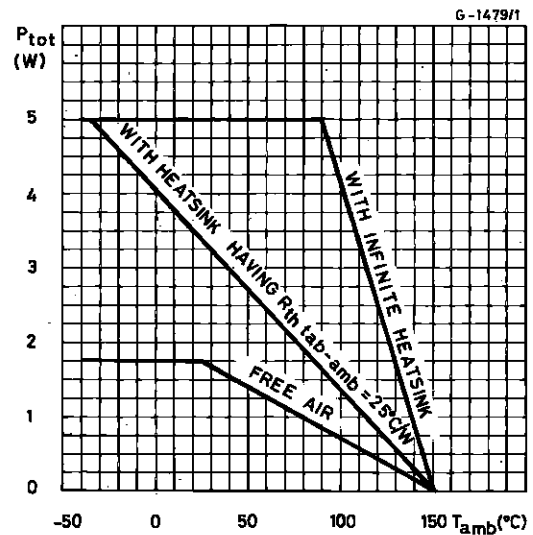
1170N-11.EPS

Figure 7 : Maximum Power Dissipation and Junction-Ambient Thermal Resistance versus "e"



1170N-12.EPS

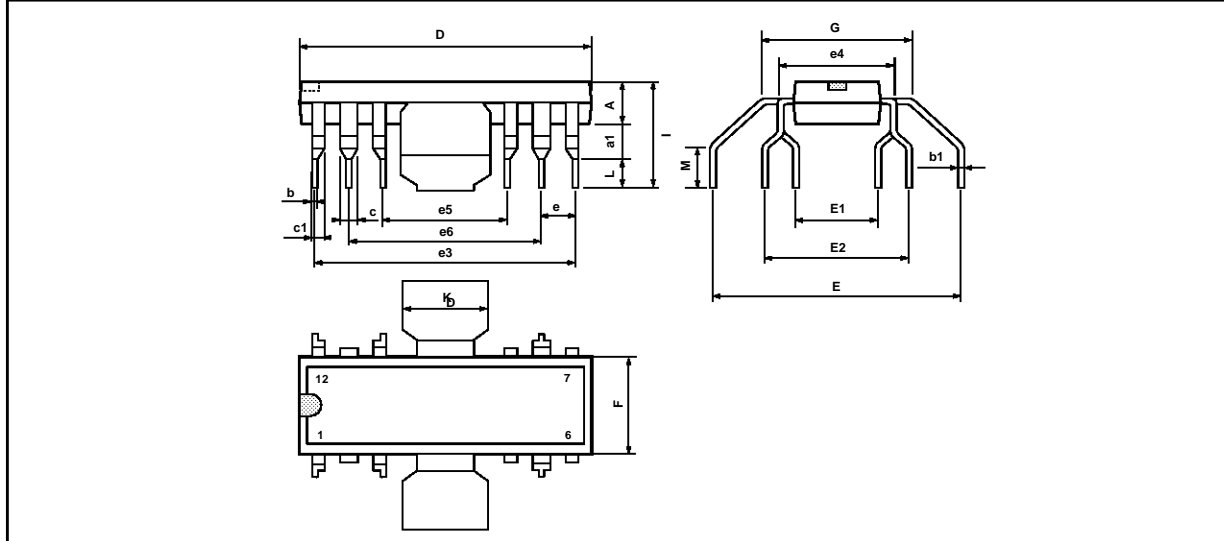
Figure 8 : Maximum Allowable Power Dissipation versus Ambient Temperature



1170N-13.EPS

TDA1170N

PACKAGE MECHANICAL DATA : 12 PINS - PLASTIC FINDIP



PM-FDIP/EP5

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.8		4.05	0.150		0.159
a1	1.5		1.75	0.059		0.069
b	0.55		0.6	0.022		0.024
b1	0.3		0.35	0.012		0.014
c		1.32			0.052	
c1		0.94			0.037	
D	19.2		19.9	0.756		0.783
E	16.8	17.2	17.6	0.661	0.677	0.693
E1	4.86		5.56	0.191		0.219
E2	10.11		10.81	0.398		0.426
e	2.29	2.54	2.79	0.090	0.100	0.110
e3	17.43	17.78	18.13	0.686	0.700	0.714
e4		7.62			0.300	
e5	7.27	7.62	7.97	0.286	0.300	0.314
e6	12.35	12.7	13.05	0.486	0.500	0.514
F	6.3		7.1	0.248		0.280
G		9.8			0.386	
I	7.8		8.6	0.307		0.339
K	6.1		6.5	0.240		0.256
L	2.5		2.9	0.098		0.114
M	2.5		3.1	0.098		

FINDIP, TBL

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