

TEA2164

SWITCH MODE POWER SUPPLY PRIMARY CIRCUIT

- POSITIVE AND NEGATIVE OUTPUT CURRENT UP TO 1.2A AND 1.7A
- A TWO LEVEL COLLECTOR CURRENT LIMI-TATION
- COMPLETE TURN OFF AFTER LONG DURA-TION OVERLOADS
- UNDER AND OVER VOLTAGE LOCK-OUT
- SOFT START BY PROGRESSIVE CURRENT LIMITATION
- DOUBLE PULSE SUPPRESSION
- BURST MODE OPERATION UNDER STAND-BY CONDITIONS

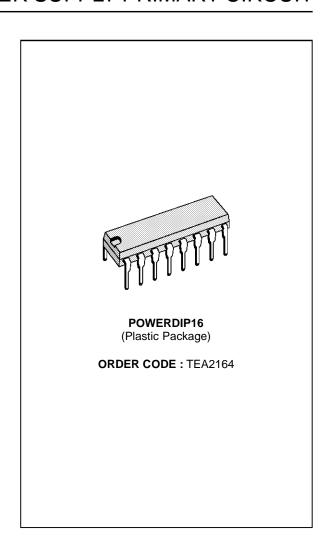
DESCRIPTION

In a master slave architecture, the TEA2164 control IC achieves the slave function. Primarily designed for TV receivers and monitors applications, this circuit provides an easy synchronization and smart solution for low power stand by operation.

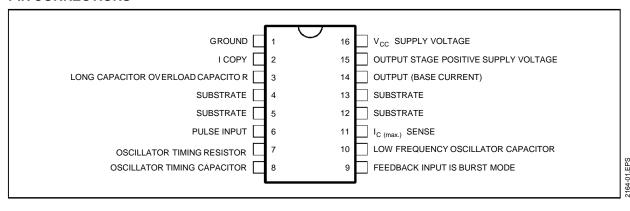
Located at the primary side the TEA2164 Control IC ensures:

- the power supply start-up
- the power supply control under stand-by conditions
- the process of the regulation signals sent by the master circuit located at the secondary side
- direct base drive of the bipolar switching transistor
- the protection of the transistor and the power supply under abnormal conditions.

For more details, refer to application note AN409.



PIN CONNECTIONS



December 1992 1/15

BLOCK DIAGRAM

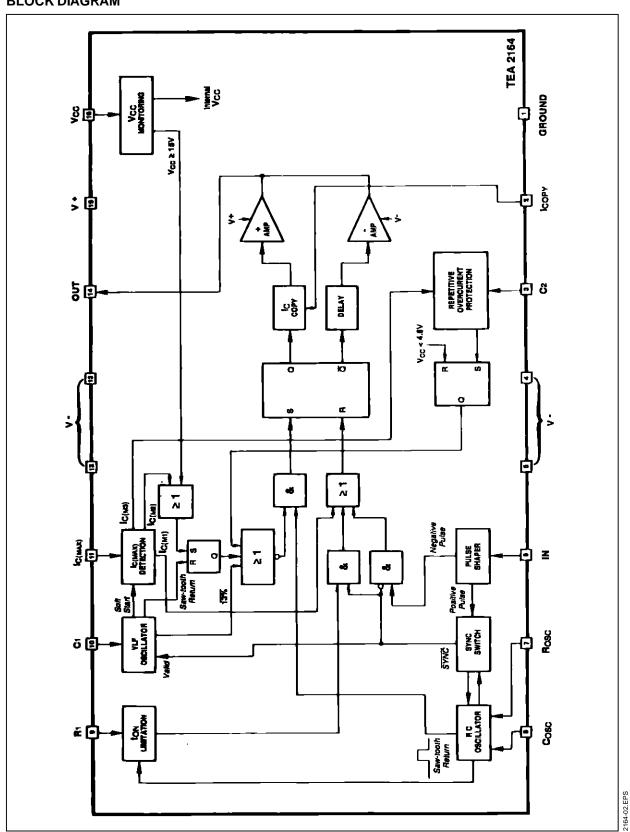
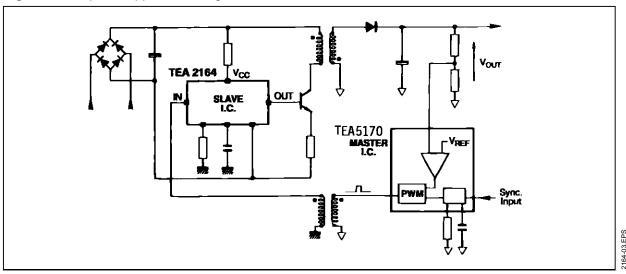


Figure 1: Simplified Application Diagram



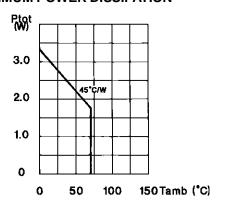
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Positive Power Supply V16-V1	18	V
V+	Positive Power Supply of the Output Stage V15-V1	18	٧
V–	Negative Power Supply V4, 5, 12, 13-V1	-5	V
V _{CC} - V- V+ - V-	Total Power Supply V16-V4, 5, 12, 13 or V15-V4, 5, 12, 13	20	V
I _{out+}	Positive Output Current	1.5	Α
I _{out}	Negative Output Current	2	Α
Tj	Operating Junction Temperature	150	°C
T _{stag}	Storage Temperature Range	- 40, + 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th(j-c)}	Junction Case Thermal Resistance	11	°C/W

MAXIMUM POWER DISSIPATION

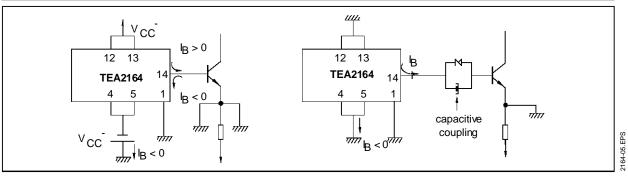


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RECOMMANDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Тур.	Max.	Unit
V _{CC}	Positive Power Supply		10	14	V
V_	Negative Power Supply (absolute value) (note 1)	0		5	V
V _{CC} – V–	Total Power Supply			18	V
I _{out+}	Positive Output Current			1.2	Α
I _{out} _	Negative Output Current			1.7	Α
Fsw	Switching Frequency			50	khz
Ro	Oscillator Resistor Range	30		150	kΩ
Co	Oscillator Capacitor Range	470		2700	pF
C1	Starting Oscillator Capacitor Range	0.1		4.7	μF
C2	Repetitive Overload Protection Capacitor	1		22	μF
V _{in}	Input Pulses Amplitude (peak) (derivated pulses - time constant = 1 μs)	0.5		1	V
Toper	Operating Ambiant Temperature	- 20		70	°C



ELECTRICAL OPERATING CHARACTERISTICS

 $T_{amb} = 25^{\circ}C$, $V_{CC} = 10V$, $V_{CC-} = 0V$, potentials referenced to ground (Pin 1) (unless otherwise specified)

Symbol	Parameter	Тур.	Max.	Unit		
OWER SUPPLY	′					
V _{CC} (start)	Starting Voltage (V _{CC} increasing)	8	9	9.6	V	
V _{CC} (stop)	Stopping Voltage (V _{CC} decreasing)	5	6.2	7.4	V	
ΔV_{CC}	Hysteresis (V _{CC} start – V _{CC} stop)	2	2.8	3.5	٧	
V _{ccmax}	Overvoltage Lock-out	14.8	15.5	16.2	V	
Iccstart	Starting Positive Supply Current	0.5	0.8	1.5	mΑ	
CURRENT LIMIT	ATION AND PROTECTION (pin 11)					
VCM1	Pulse by Pulse Current Limitation Threshold	720	840	970	mV	
VCM2	Current Monitoring 2nd Threshold	1200 13		1500	mV	
ΔVCM	$\Delta VCM = VCM2 - VCM1 $	300	300 500 70		mV	
REPETITIVE OVI	ERCURRENT PROTECTION	•	•			
VCM3	Repetitive Overcurrent Threshold (pin 11)	700	900	1100	mV	
VCM3-VCM1	(VCM3-VCM1)	- 20	50	130	mV	
VC2	Lock-out Voltage on Pin 3	2.4	3	3.6	V	
I3 disch	Capacitor C2 Discharge Current (synchronized mode)	10	10 20 30		μΑ	
I3 ch.	Capacitor C2 Charge Current 50 80 110					
SCILLATOR, M	IAX DUTY CYCLE, SYNCHRONIZATION		<u> </u>	<u> </u>		
To	Oscillator Initial Accuracy RT = 50 K, CT = 1 nF	19.3	21	22.7	μs	
T _{on(max)}	Maximum Duty Cycle (T _{syn} = 1.05 T _o)	60	70	85	%	

ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Тур.	Max.	Unit		
OSCILLATOR, MAX DUTY CYCLE, SYNCHRONIZATION (continued)							
$\frac{T_{syn}}{T_{O}}$	Synchronization Window	1.0		1.5			
OUTPUT STAGE							
l ₁₄ /l ₂	I _c Copy Current Gain		1000				
I _{BON}	Base Current Starting Pulse		300		mA		
VERY LOW FREC	QUENCY OSCILLATOR						
	Burst Duty Cycle		13		%		

I. FIELD OF APPLICATION

The TEA2164 control circuit has been designed primarily for discontinuous mode flyback built with a master-slave architecture, whatever the field of application.

But due to its capability to synchronize the transistor switching-off with an external signal (line flyback) and due to an adapted burst-mode operation for a low power stand-by operation, the TEA2164 offers a smart solution for monitors and TV sets applications.

Power supply main features:

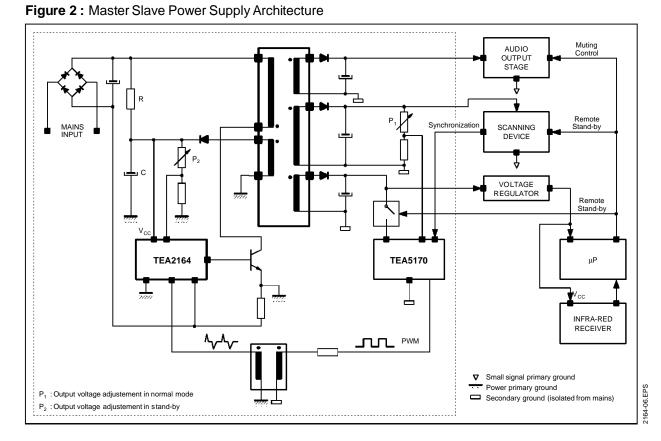
- maximum output power 140W (transistor forced gain : 3.5)

- stand-by mode output power (1W \leq Psb \leq 6W; efficiency > 50%)
- operating frequency up to 50kHz
- power-switch : bipolar transistor

Adapted master-circuit:

 $\begin{array}{ccc} \text{Monitor application} & \rightarrow & \text{TEA5170} \\ \text{Standard TV application} & \rightarrow & \text{TEA2028B} \\ & & \text{TEA2029C} \\ & & \text{TEA2128} \\ & & \text{TEA5170} \\ \\ \text{Digital TV application} & \rightarrow & \text{TEA5170} \\ \end{array}$

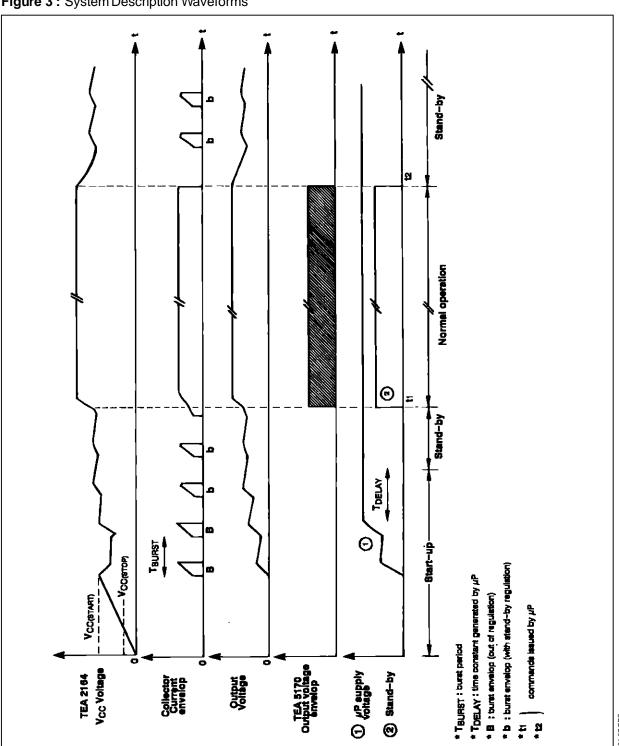
(TEA2028B, TEA2029C and TEA2128 are deflection processors with built-in PWM generator).



II. GENERAL DESCRIPTION

In a master slave architecture, the TEA2164 Control IC, located at the primary side of an off line power supply achieves the slave function; whereas the master circuit is located at the secondary side. The link between both circuits is realized by a small pulse transformer (Figure 3).

Figure 3: System Description Waveforms



In the operation of the master-slave architecture, four majors cases must be considered:

- normal operating
- stand-by mode
- power supply start-up
- abnormal conditions: off load, short circuit, ...

II.1. Normal Operating (master slave mode)

In this configuration, the master circuit generates a pulse width modulated signal issued from the monitoring of the output voltage which needs the best accuracy (in TV applications: the horizontal deflection stage supply voltage). The master circuit power supply can be supplied by another output.

The PWM signal are sent towards the primary side through small differentiating transformer. For the TEA2164 positive pulses are transistor switching-on commands; and negative pulses are transistor switching-off commands (Figure 4). In this configuration, only by synchronizing the master oscillator, the switching transistor may be synchronized with an external signal.

II.2. Stand-by Mode

In this configuration the master circuit no longer

Figure 4: Master Slave Mode Waveforms

sends PWM signals, the structure is not synchronized; and the TEA2164 operates in burst mode. The average power consumption at the secondary side may be very low $1W \le P \le 6W$ (as it is consumed in TV set during stand by).

By action on the maximum duty cycle control, a primary loop maintains a semi-regulation of the output voltages. Voltage on feed-back is applied on Pin 9.

Burst period is externally programmed by capacitor C1.

II.3. Power Supply Start-up

After the mains have been switched-on, the V_{CC} storage capacitor of the TEA2164 is charged through a high value resistor connected to the rectified high voltage. When Vcc reaches V_{CC} start threshold (9V typ), the TEA2164 starts operating in burst mode. Since available output power is low in burst mode the output power consumption must remain low before complete setting-up of output voltage. In TV application it can be achieved by maintaining the TV in stand-by mode during start-up (Figure 6).

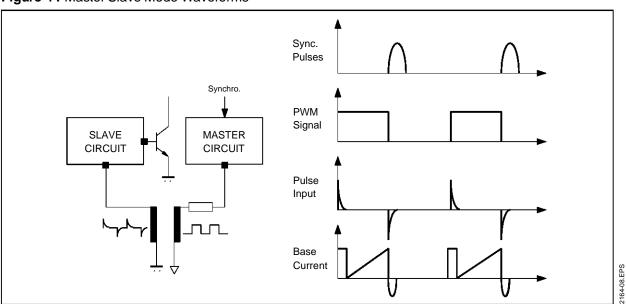


Figure 5: Burst Mode Waveforms

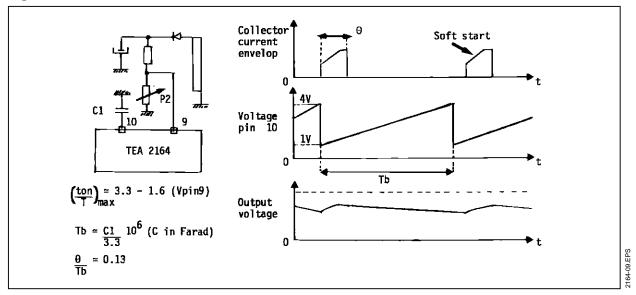
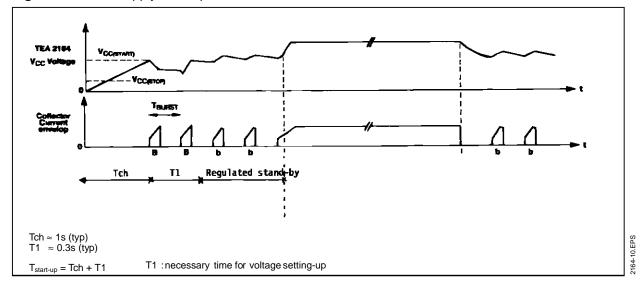


Figure 6: Power Supply Start-up



d) Abnormal conditions : safety functions

Overvoltage Protection

When V_{CC} exceeds V_{CC} max, an internal flip-flop stops output conduction signals. The circuit will start again after the capacitor C1 discharge; it means: after loss of synchronization or after V_{CC} stop crossing (Figure 7).

In flyback converters, this function protects the power supply against output voltage runaway.

Under Voltage Lock-out

The TEA2164 control circuit stops operating when Vcc goes under Vcc stop.

Power Limitation, Current Protection, Long Duration Overload Protection

- Output power limitation: by a pulse by pulse collector current limitation the TEA2164 limits the maximum output power. V_{CM1} is the corresponding voltage threshold, its detection is memorized up to the next period.
- Current protection (transistor protection)
 Under particular conditions a hard overload or short circuit may induce a flux runaway in spite of the current limitation (V_{CM1}).

The TEA2164 control circuit features a second current protection, V_{CM2}. When this threshold is reached an internal flip-flop memorizes it and

output conduction signals are inhibited. The circuit will send base drives again after capacitor C1 discharge (Figure 7).

- Long duration overload protection : (Figure 8) An overload is detected when the sense-voltage on Pin 11 reaches V_{CM3} before a negative pulse has been applied to Pin 6. In this case the capacitor C2 (connected to Pin 3) is charged with I_3 ch up to the end of the period and discharged with I_3 disch until a next V_{CM3} detector. By this way in case of long duration overload, the capacitor

keeps charging at each period and its voltage encreases gradually. When the voltage on Pin 3 exceeds V_{C2} , the TEA2164 control circuit stops sending base drives and memorizes this event. No restart is allowed as long as $V_{pin\ 3}$ is higher than V_{C2} and V_{CC} higher than 4.8V.

* Remark:

- The harder is the overload the faster is the protection
- The capacitor keeps charging between two burst after V_{CM2} detection.

Figure 7: Overvoltages Lock-out

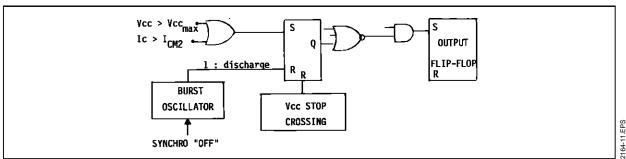


Figure 8: Long Duration Overload Monitoring Circuit

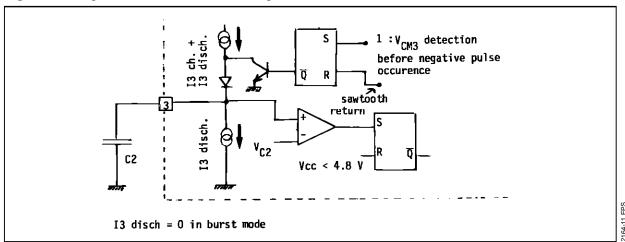


Figure 9: Long Duration Overload Detection

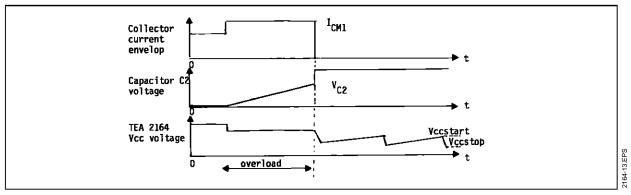
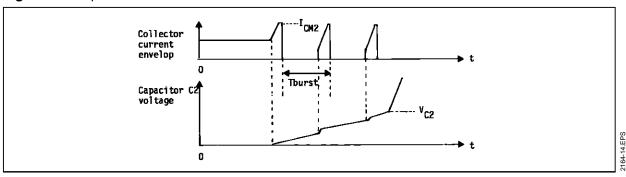


Figure 10: Repetitive Over-current Protection



III. SWITCHING OSCILLATOR AND SYNCHRONIZATION

III.1. Switching oscillator

When the TEA2164 control circuit operates in burst mode, the switching frequency is fixed by the free frequency oscillator. The period is determined by two external components Co and Ro.

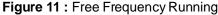
III.2. Synchronization

When the master-circuit starts to send pulses both

oscillators are not synchonuous. In order to avoid any erratic conduction of the power transistor, the first synchronization pulse will arrive simultanously with the sawtooth return of the TEA2164 oscillator.

To get synchronization the free frequency must be higher than the synchronization frequency.

$$T_O < T_{sync.} < 1.50 T_O$$



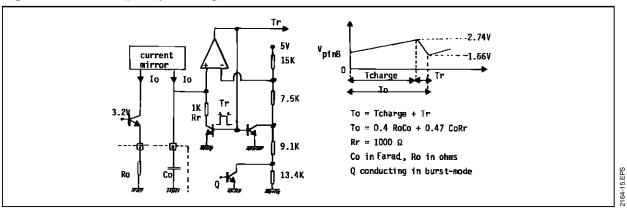
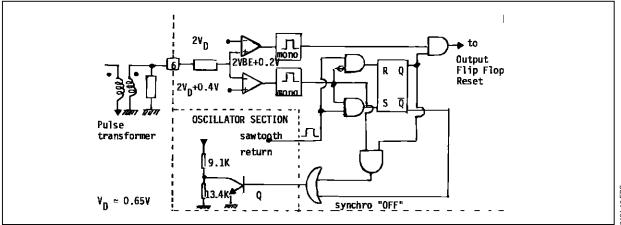
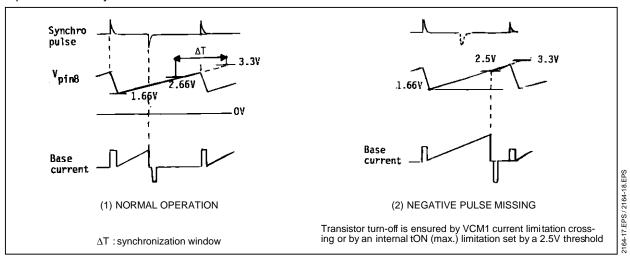


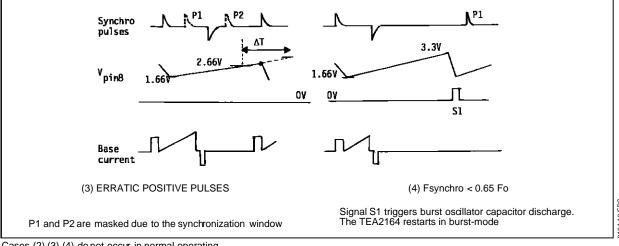
Figure 12: Synchronization Pulse Shaper and Synchronization



Operation after synchronization



Operation after synchronization



Cases (2) (3) (4) do not occur in normal operating.

IV - MAXIMUM DUTY CYCLE LIMITATION

Burst mode: The maximum duty cycle is controlled by the voltage on Pin 9 (Figure 13).

Synchronized mode: Normally the maximum duty cycle is set by the master circuit. Oowever the maximum conducting time will never exceed the value given by the comparison of the oscillator wave-form with the 2.5V internal threshold.

V - OUTPUT STAGE

TEA2164 output stage has been designed to drive switching bipolar transistor.

- Each base drive begins with a positive pulse IBON

that realizes an efficient transistor turn-on.

- After the starting pulse I_{BON}, the base current is proportional to the collector current. The current gain is easily fixed by a resistor R (Figure 14).
- A fast and safe transistor turn-off is realized by a fast positive base current cut-off and by applying a negative base drive which draws stored carriers. A typical 0.7s delay prevents from cross-conduction of positive and negative output stages.

Remark: In order to reduce power dissipation on the positive output stage with the low gain transistors, for high base currents the positive output stage operates in saturated mode (Figure 15). This can be achieved by using a resistor between V_{CC} and V+.

Figure 13: Maximum Duty Cycle Limitation

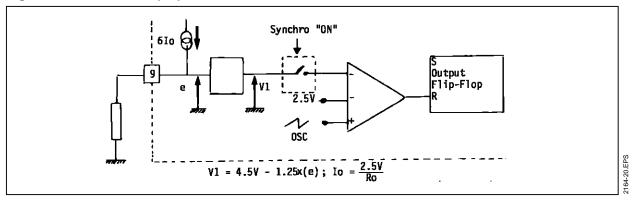
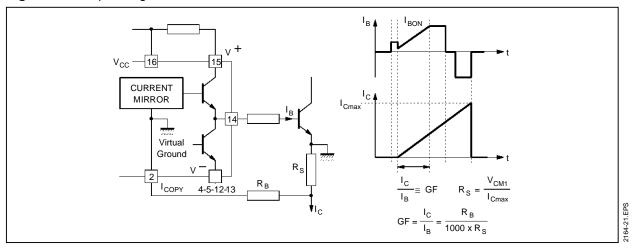


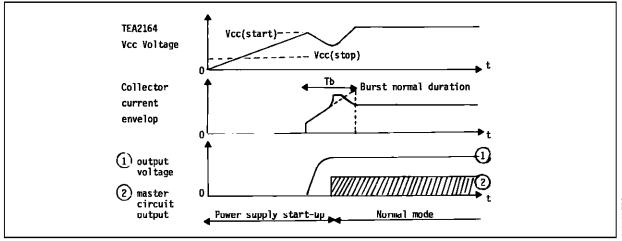
Figure 14: Output Stage Architecture and Base Drive



VI - MONITOR APPLICATIONS

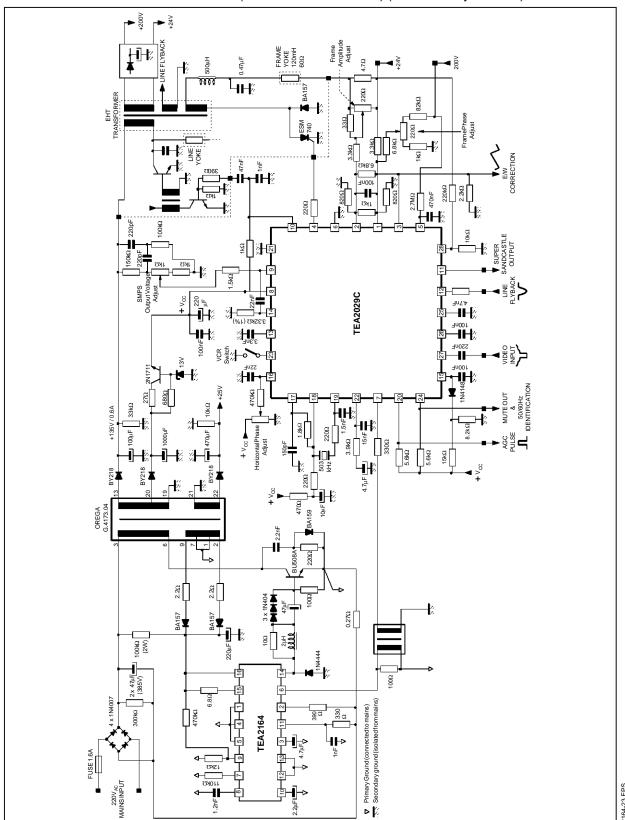
In most of monitor applications, the power supply must start-up under full load conditions and the stand-by mode is no longer useful. The energy of the starting burst must be high enough to ensure start-up, then the capacitor C1 must be higher in these applications than on TV application (typ.: $1\mu F$).

Figure 15: Power Supply Start-up and Normal Operation

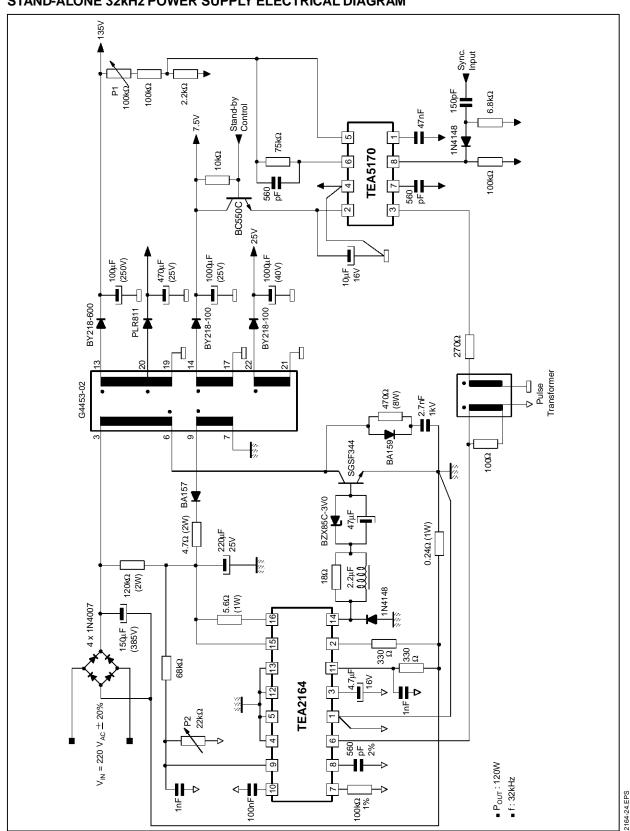


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COMPLETE APPLICATION DIAGRAM (SMPS + DEFLECTION) (with stand-by function)

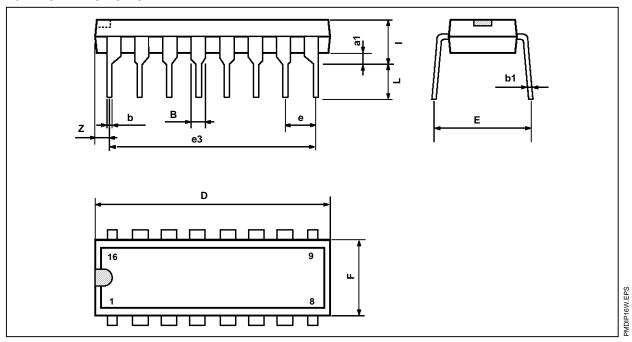


STAND-ALONE 32kHz POWER SUPPLY ELECTRICAL DIAGRAM



PACKAGE MECHANICAL DATA

16 PINS - PLASTIC POWERDIP



Dimensions		Millimeters			Inches	
Difficusions	Min.	Тур.	Max.	Min.	Тур.	Max.
a1	0.51			0.020		
В	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			20			0.787
Е		8.8			0.346	
е		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

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