

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4531B

MSI

13-input parity checker/generator

Product specification
File under Integrated Circuits, IC04

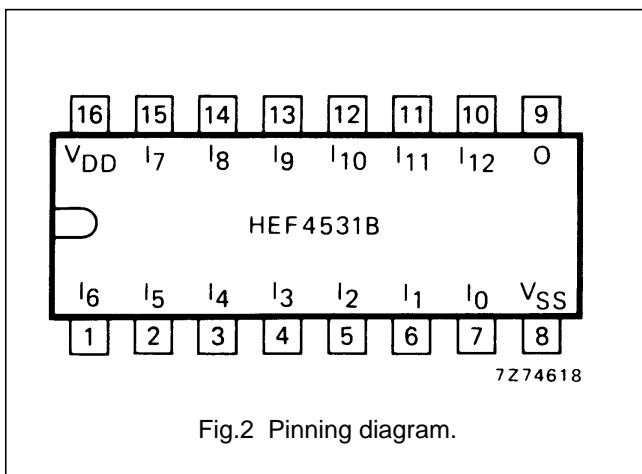
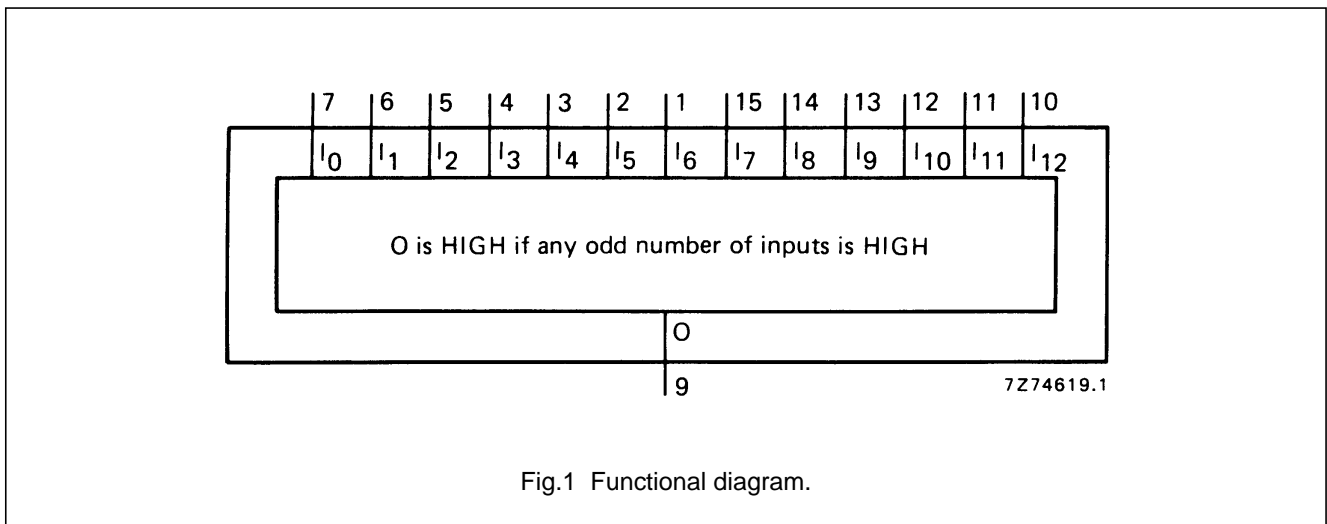
January 1995

13-input parity checker/generator

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DESCRIPTION

The HEF4531B is a parity checker/generator with 13 parity inputs (I_0 to I_{12}) and a parity output (O). When the number of parity inputs that are HIGH is even, the output is LOW. When the number of parity inputs that are HIGH is odd, the output is HIGH. For words of 12 bits or less, the output can be used to generate either odd or even parity by appropriate termination of the unused parity input(s). For words of 14 or more bits, the devices can be cascaded by connecting the output of one device to any parity input of another device. When cascading devices, it is recommended that the output of one device be connected to the I_{12} input of the other device since there is less delay to the output from the I_{12} input than from any other input (I_0 to I_{11}).



- HEF4531BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4531BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4531BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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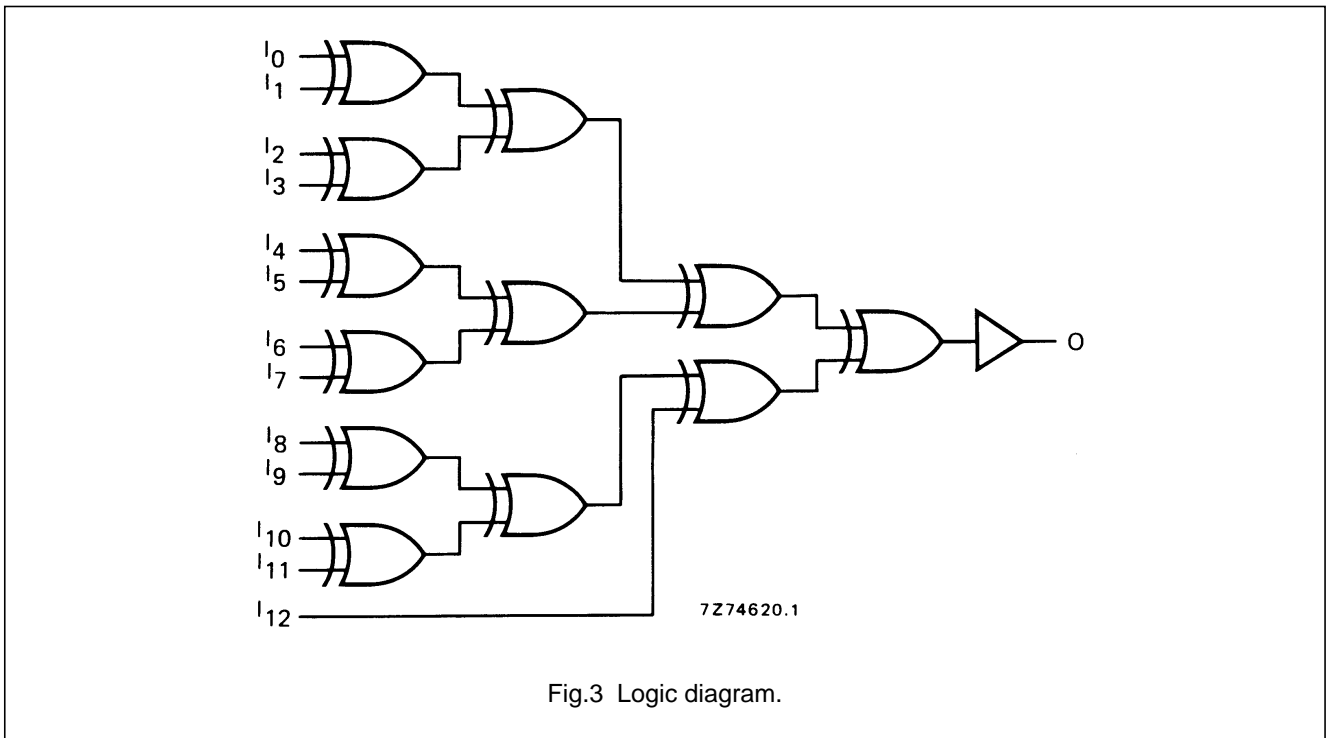


Fig.3 Logic diagram.

FUNCTION TABLE

INPUTS													OUTPUT
I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	I ₈	I ₉	I ₁₀	I ₁₁	I ₁₂	O
L	L	L	L	L	L	L	L	L	L	L	L	L	L
any odd number of inputs HIGH													H
any even number of inputs HIGH													L
H	H	H	H	H	H	H	H	H	H	H	H	H	H

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	425 f _i + ∑ (f _o C _L) × V _{DD} ² 2 400 f _i + ∑ (f _o C _L) × V _{DD} ² 7 700 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)

13-input parity checker/generator

HEF4531B
MSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA	
Propagation delays	I_0 to $I_{11} \rightarrow O$ HIGH to LOW	t_{PHL}	145	290	ns	$118\text{ ns} + (0,55\text{ ns/pF}) C_L$	
			60	120	ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$	
			45	90	ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	t_{PLH}	135	270	ns	$108\text{ ns} + (0,55\text{ ns/pF}) C_L$	
			55	110	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$	
			45	90	ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	$I_{12} \rightarrow 0$	HIGH to LOW	t_{PHL}	105	210	ns	$78\text{ ns} + (0,55\text{ ns/pF}) C_L$
				45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$
				35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
		LOW to HIGH	t_{PLH}	85	170	ns	$58\text{ ns} + (0,55\text{ ns/pF}) C_L$
				35	70	ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$
				25	50	ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times	HIGH to LOW	t_{THL}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
	LOW to HIGH	t_{TLH}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	