INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT7080 16-bit even/odd parity generator/checker

Product specification
File under Integrated Circuits, IC06

December 1990





74HC/HCT7080

FEATURES

- · Word-length easily expanded by cascading
- Generates either even or odd parity for 16-data bits
- · Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT7080 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7080 are 16-bit parity generators or checkers commonly used to detect errors in high-speed data transmission or data retrieval systems.

The even and odd parity output is available for generating or checking even/odd parity up to 16-bits.

The even/odd parity output (E/\overline{O}) is HIGH when an even number of data inputs $(I_0 \text{ to } I_{15})$ are HIGH and the cascade/even-odd-changing input (\overline{X}) is HIGH.

Expansion to larger word sizes is accomplished by connecting the even/odd parity output (E/\overline{O}) to the cascade/even-odd-changing input (\overline{X}) of the final stage.

QUICK REFERENCE DATA

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

SYMBOL	PARAMETER	CONDITIONS	TYF	TYPICAL		
	PARAMETER	CONDITIONS	НС	нст	UNIT	
t _{PHL} / t _{PLH}	propagation delay	C _L = 15 pF; V _{CC} = 5 V				
	I_n to E/ \overline{O}		29	32	ns	
	\overline{X} to E/ \overline{O}		12	15	ns	
C _I	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	24	25	pF	

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

f_i = input frequency in MHz

f_o = output frequency in MHz

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = GND$ to V_{CC} For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

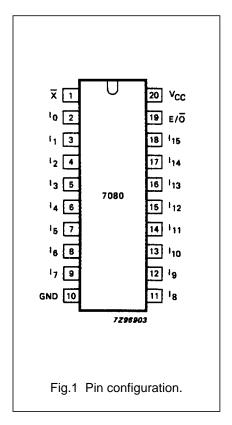
ORDERING INFORMATION

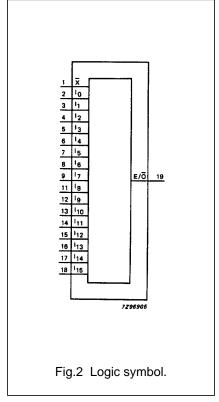
See "74HC/HCT/HCU/HCMOS Logic Package Information".

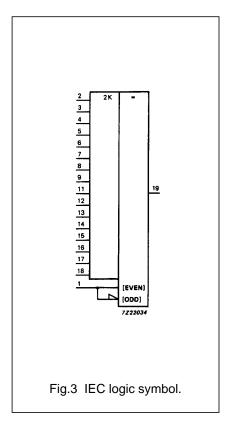
74HC/HCT7080

PIN DESCRIPTION

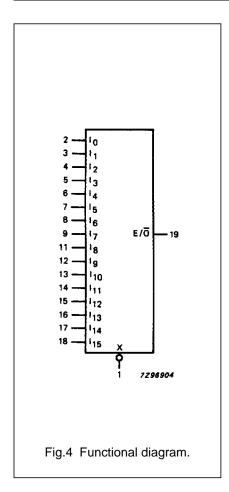
PIN NO.	SYMBOL	NAME AND FUNCTION
1	X	cascade/even-odd-changing input
2, 3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 17, 18	I ₀ to I ₁₅	data inputs
10	GND	ground (0 V)
19	E/O	even/odd parity output
20	V _{CC}	positive supply voltage







74HC/HCT7080



FUNCTION TABLE

INP	UTS	OUTPUTS
In	$\overline{\mathbf{x}}$	E/O
Σ = E	H _	H
∑ ≠ E	H L	L H

7296995 Fig.5 Logic diagram.

Notes

H = HIGH voltage level
 L = LOW voltage level
 E = even

Philips Semiconductors Product specification

16-bit even/odd parity generator/checker

74HC/HCT7080

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	PARAMETER	T _{amb} (°C)							LINIT	TEST CONDITIONS	
SYMBOL		74HC									
SYMBOL		+25		-40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		(',	
t _{PHL} / t _{PLH}	propagation delay I_n to E/\overline{O}		91 33 26	280 56 48		350 70 60		420 84 71	ns	2.0 4.5 6.0	Fig.7
t _{PHL} / t _{PLH}	propagation delay X to E/O		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

Philips Semiconductors Product specification

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74HC/HCT7080

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I _n	1.0
\overline{X}	1.0

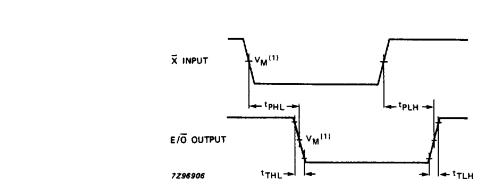
AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \ V; \ t_r = t_f = 6 \ ns; \ C_L = 50 \ pF$

SYMBOL	T _{amb} (°C)								TEST CONDITIONS		
	PARAMETER	74HCT						UNIT			
		+25		−40 to +85		-40 to +125		CIVIT	V _{CC} (V)	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		(1)	
t _{PHL} / t _{PLH}	propagation delay I _n to E/O		37	63		79		95	ns	4.5	Fig.7
t _{PHL} / t _{PLH}	propagation delay X to E/O		18	32		40		48	ns	4.5	Fig.6
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

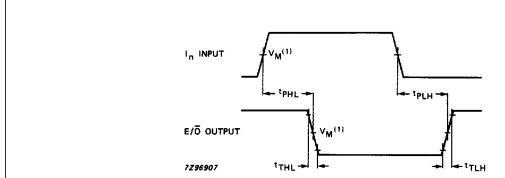
74HC/HCT7080

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the cascade/even-odd-changing input (\overline{X}) to the even/odd parity output (E/\overline{O}) propagation delays and the output transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the data inputs (I_n) to the even/odd parity output (E/\overline{O}) propagation delays and the output transition times.

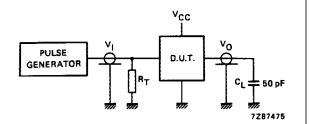
74HC/HCT7080

TEST CIRCUIT AND WAVEFORMS

C_L = load capacitance including jig and probe capacitance

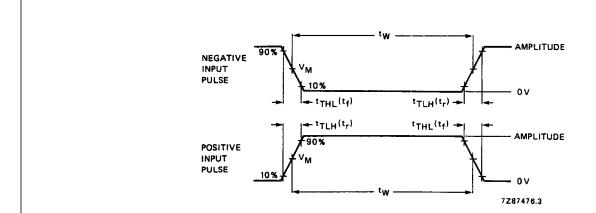
(see AC CHARACTERISTICS for values).

 R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.



FAMILY	AMPLITUDE	V _M	t _r ; t _f				
PAWILI			f _{max} ; PULSE WIDTH	OTHER			
74HC	V _{CC}	50%	< 2 ns	6 ns			
74HCT	3.0 V	1.3 V	< 2 ns	6 ns			

Fig.8 Test circuit for measuring AC performance.



C_L = load capacitance including jig and probe capacitance

(see AC CHARACTERISTICS for values).

 $R_T = {\rm termination\ resistance\ should\ be\ equal\ to\ the\ output\ impedance\ } Z_O$ of the pulse generator.

FAMILY	AMPLITUDE	V _M	t _r ; t _f				
FAMILI			f _{max} ; PULSE WIDTH	OTHER			
74HC	V _{CC}	50%	< 2 ns	6 ns			
74HCT	3.0 V	1.3 V	< 2 ns	6 ns			

Fig.9 Input pulse definitions.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".