

# 2SK2788

## Silicon N Channel MOS FET High Speed Power Switching

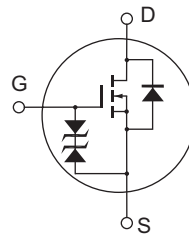
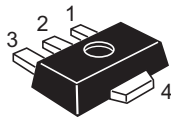
REJ03G1033-0200  
(Previous: ADE-208-538)  
Rev.2.00  
Sep.07,2005

### Features

- Low on-resistance  
 $R_{DS(on)} = 0.12 \Omega$  typ ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 1 \text{ A}$ )
- Low drive current
- High speed switching
- 4 V gate drive devices.

### Outline

RENESAS Package code: PLZZ0004CA-A  
(Package name: UPAK<sup>®</sup>)



1. Gate
2. Drain
3. Source
4. Drain

Note: Marking is "VY"

\*UPAK is a trademark of Renesas Technology Corp.

## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	60	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	2	A
Drain peak current	$I_{D(pulse)}^{*1}$	4	A
Body to drain diode reverse drain current	$I_{DR}$	2	A
Channel dissipation	$P_{ch}^{*2}$	1	W
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1 \%$ 

2. When using the alumina ceramic board (12.5 x 20 x 0.7 mm)

## Electrical Characteristics

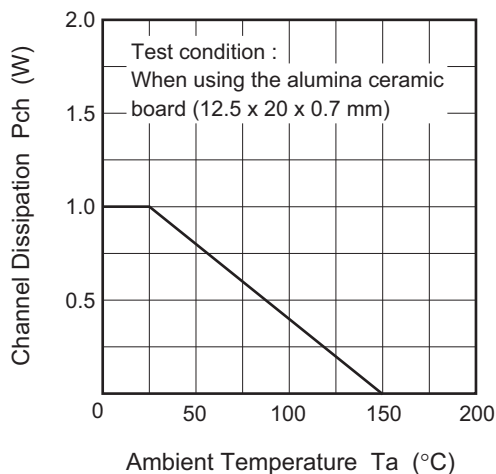
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \mu A$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu A$	$V_{DS} = 60 \text{ V}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu A$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$I_D = 1 \text{ mA}$ , $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.16	$\Omega$	$I_D = 1 \text{ A}$ , $V_{GS} = 10 \text{ V}^{*3}$
	$R_{DS(on)}$	—	0.16	0.25	$\Omega$	$I_D = 1 \text{ A}$ , $V_{GS} = 4 \text{ V}^{*3}$
Forward transfer admittance	$ y_{fs} $	1.6	2.8	—	S	$I_D = 1 \text{ A}$ , $V_{DS} = 10 \text{ V}^{*3}$
Input capacitance	$C_{iss}$	—	180	—	pF	$V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1 \text{ MHz}$
Output capacitance	$C_{oss}$	—	90	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	30	—	pF	
Turn-on delay time	$t_{d(on)}$	—	9	—	ns	$V_{GS} = 10 \text{ V}$ , $I_D = 1 \text{ A}$ , $R_L = 30 \Omega$
Rise time	$t_r$	—	15	—	ns	
Turn-off delay time	$t_{d(off)}$	—	40	—	ns	
Fall time	$t_f$	—	35	—	ns	
Body to drain diode forward voltage	$V_{DF}$	—	0.9	—	V	$I_D = 2 \text{ A}$ , $V_{GS} = 0$
Body to drain diode reverse recovery time	$t_{rr}$	—	35	—	ns	$I_F = 2 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu s$

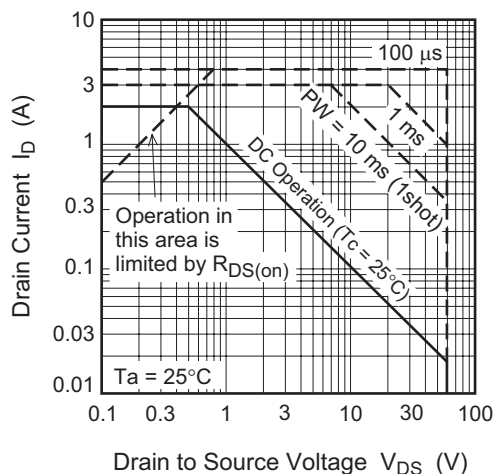
Notes: 3. Pulse test

## Main Characteristics

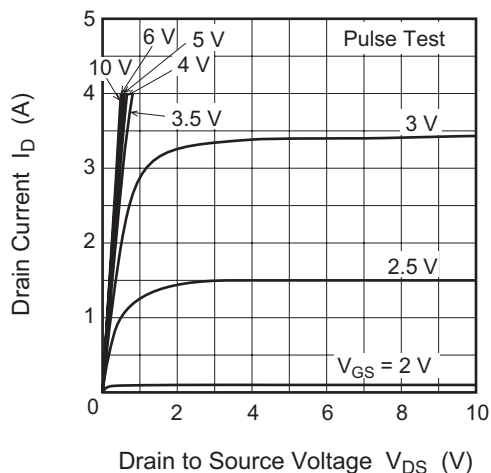
Power vs. Temperature Derating



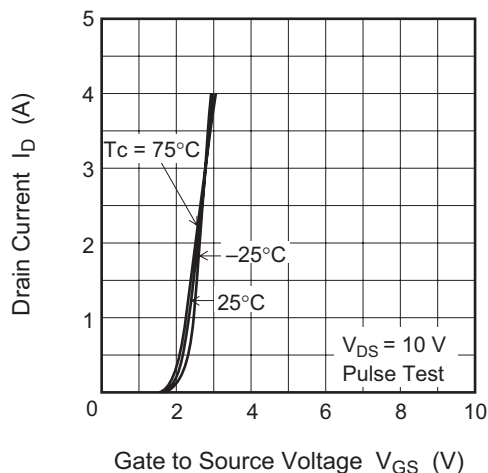
Maximum Safe Operation Area



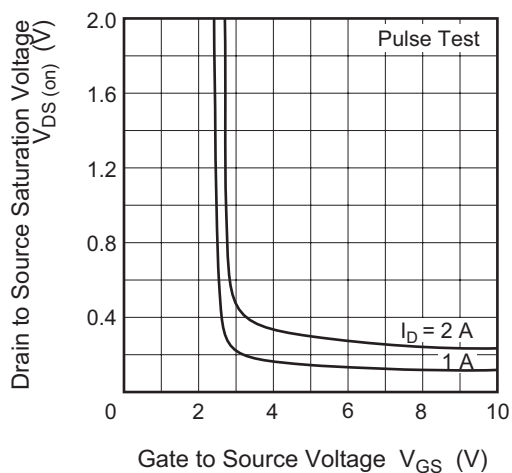
Typical Output Characteristics



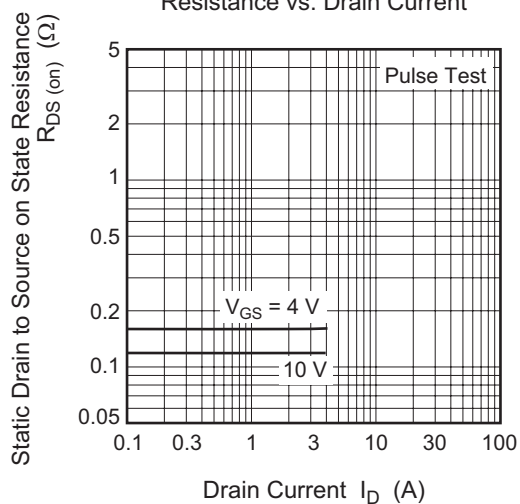
Typical Transfer Characteristics



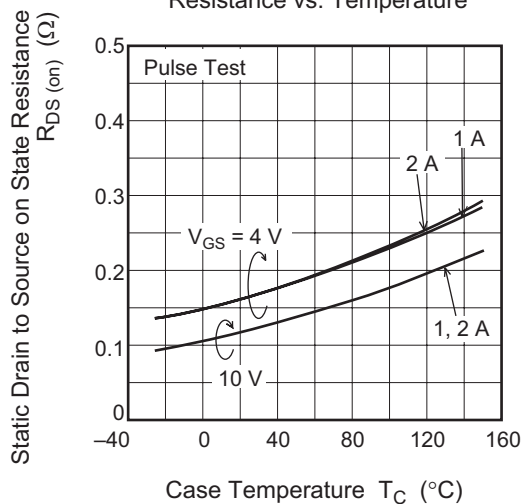
Drain to Source Saturation Voltage vs. Gate to Source Voltage



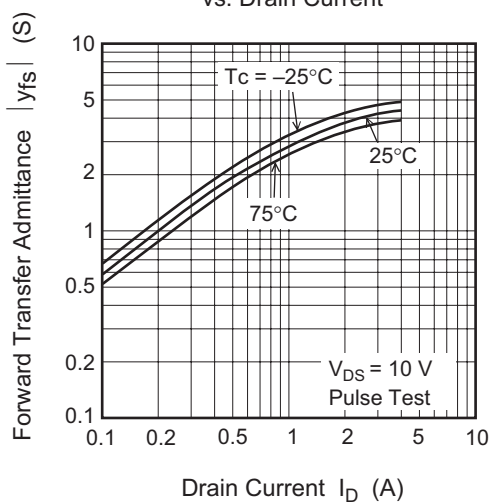
Static Drain to Source on State Resistance vs. Drain Current



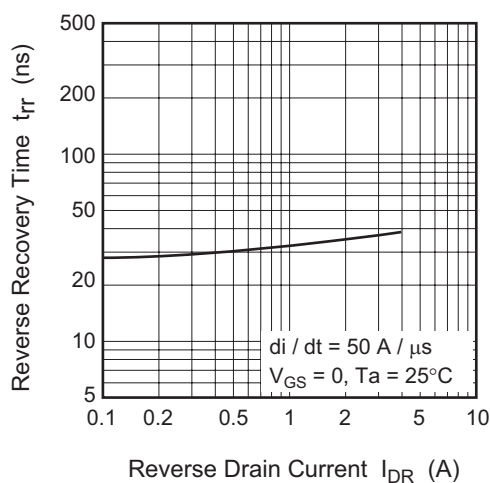
Static Drain to Source on State Resistance vs. Temperature



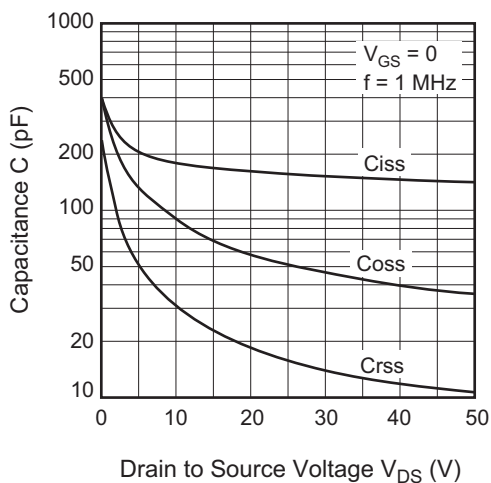
Forward Transfer Admittance vs. Drain Current



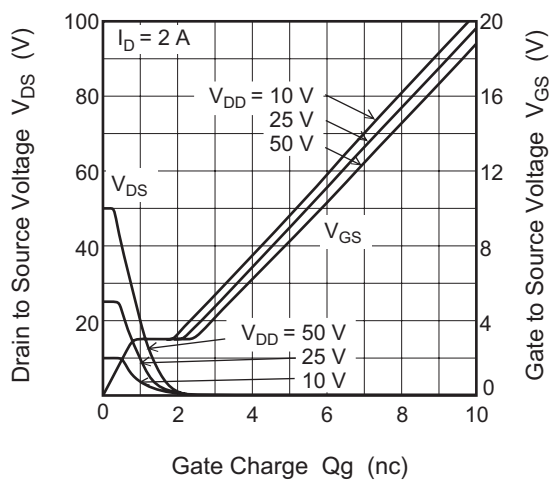
Body to Drain Diode Reverse Recovery Time



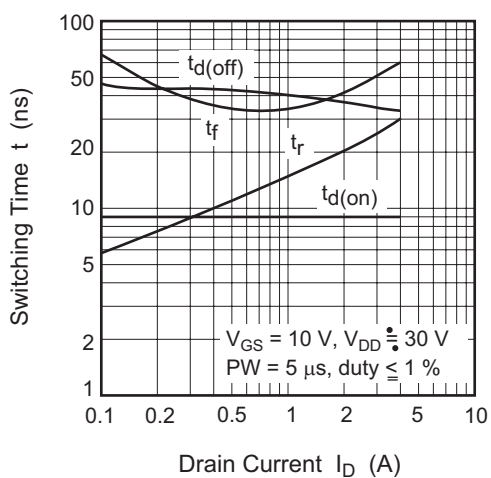
Typical Capacitance vs. Drain to Source Voltage

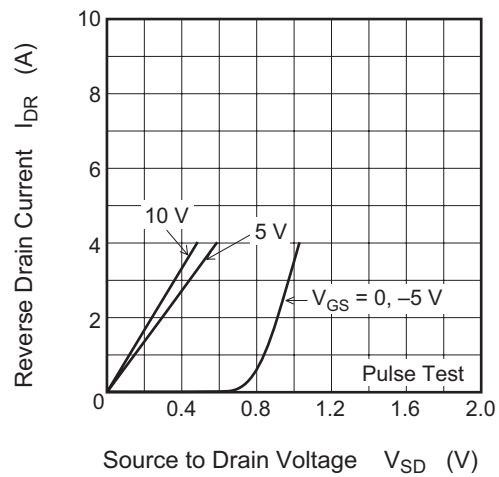


Dynamic Input Characteristics

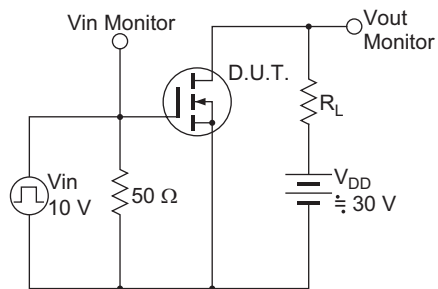


Switching Characteristics

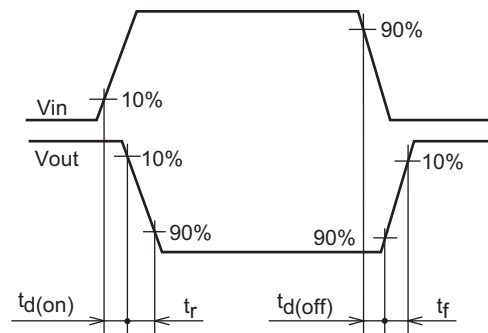


Reverse Drain Current vs.  
Source to Drain Voltage

Switching Time Test Circuit



Waveform



## Package Dimensions

JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
SC-62	PLZZ0004CA-A	UPAK / UPAKV	0.050g

Unit: mm

The drawing shows three views of the package:
 

- Top View:** Overall width is  $4.5 \pm 0.1$  mm. The central circular feature has a diameter of  $\phi 1$  mm. The distance from the center to the top edge is  $1.8 \text{ Max}$  mm. The distance from the center to the bottom edge is  $2.5 \pm 0.1$  mm. The distance from the center to the left edge is  $0.53 \text{ Max}$  mm. The distance from the center to the right edge is  $0.48 \text{ Max}$  mm. The distance between the two mounting holes is  $3.0$  mm. The distance from the center to the bottom edge of the mounting holes is  $0.8 \text{ Min}$  mm.
- Side View:** The height of the package is  $1.5 \pm 0.1$  mm. The distance from the top edge to the bottom edge of the mounting holes is  $0.44 \text{ Max}$  mm.
- End View:** The width of the package is  $1.5$  mm. The distance from the top edge to the bottom edge of the mounting holes is  $0.44 \text{ Max}$  mm. The distance from the top edge to the bottom edge of the mounting holes is  $0.44 \text{ Max}$  mm. The distance from the top edge to the bottom edge of the mounting holes is  $0.44 \text{ Max}$  mm.

## Ordering Information

Part Name	Quantity	Shipping Container
2SK2788VYTL-E	1000 pcs	Taping
2SK2788VYTR-E	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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