

H5N2501LD, H5N2501LS, H5N2501LM

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G1250-0200

Rev.2.00

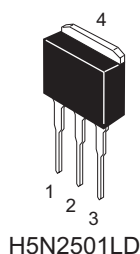
Jul.21,2005

Features

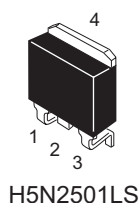
- Low on-resistance
- Low leakage current
- High speed switching

Outline

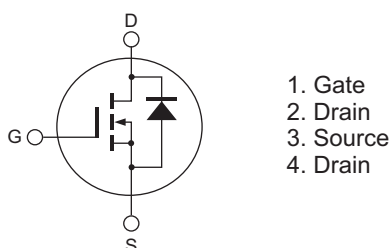
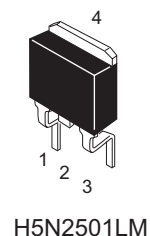
RENESAS Package code: PRSS0004AE-A
(Package name LPAK(L))



RENESAS Package code: PRSS0004AE-B
(Package name LPAK(S)-(1))



RENESAS Package code: PRSS0004AE-C
(Package name LPAK(S)-(2))



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source voltage	V_{DSS}	250	V
Gate to Source voltage	V_{GSS}	± 30	V
Drain current	I_D	18	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	72	A
Body-Drain diode reverse Drain current	I_{DR}	18	A
Avalanche current	I_{AP} ^{Note3}	18	A
Channel dissipation	P_{ch} ^{Note2}	75	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. Value at $T_c = 25^\circ C$

3. $STch = 25^\circ C$, $T_{ch} \leq 150^\circ C$

Electrical Characteristics

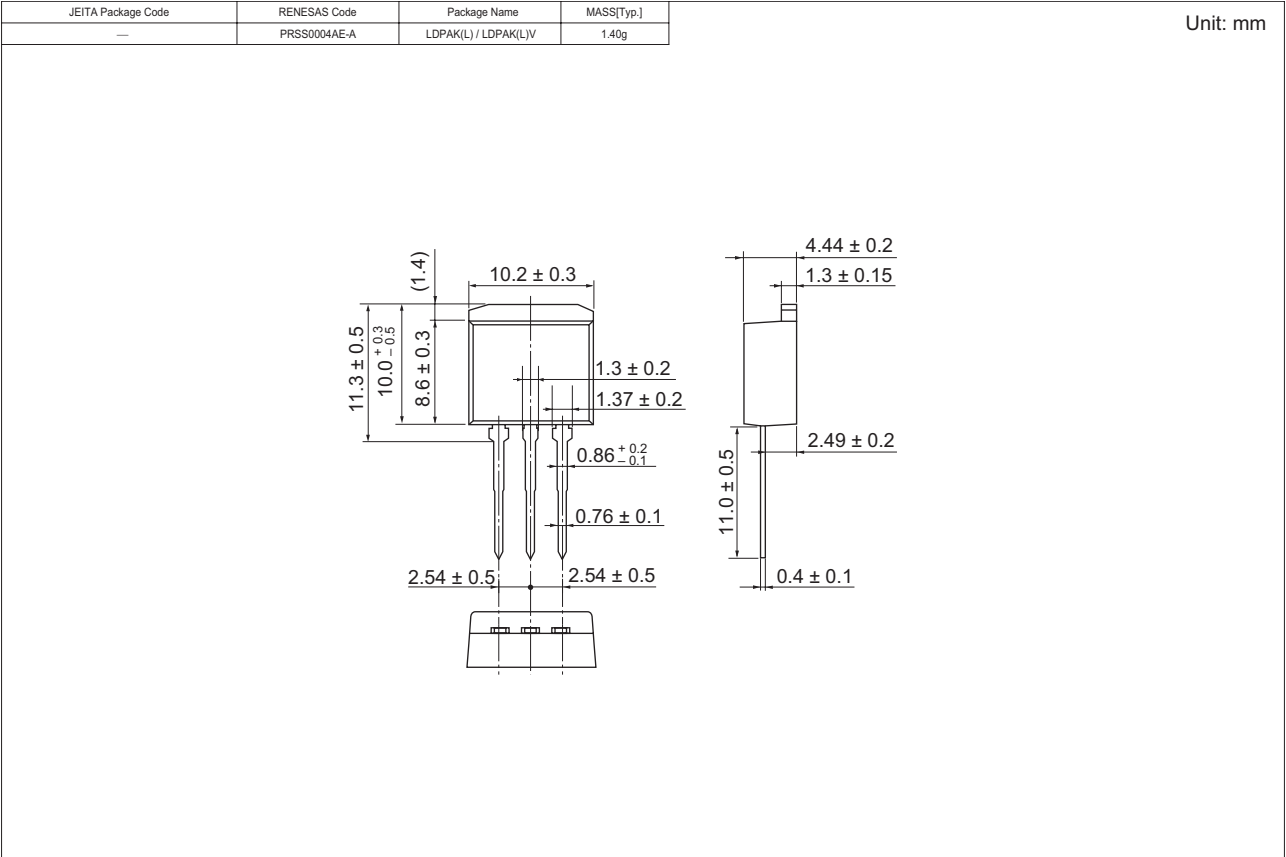
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to Source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Zero Gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 250 \text{ V}$, $V_{GS} = 0$
Gate to Source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Gate to Source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	8	14	—	S	$I_D = 9 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Static Drain to Source on state resistance	$R_{DS(on)}$	—	0.14	0.18	Ω	$I_D = 9 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1350	—	pF	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	170	—	pF	
Reverse transfer capacitance	C_{rss}	—	50	—	pF	
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	$I_D = 9 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 13.9 \Omega$ $R_g = 10 \Omega$
Rise time	t_r	—	65	—	ns	
Turn-off delay time	$t_{d(off)}$	—	95	—	ns	
Fall time	t_f	—	18	—	ns	
Total Gate charge	Q_g	—	45	—	nC	$V_{DD} = 200 \text{ V}$ $V_{GS} = 10 \text{ V}$ $I_D = 18 \text{ A}$
Gate to Source charge	Q_{gs}	—	8	—	nC	
Gate to Drain charge	Q_{gd}	—	22	—	nC	
Body-Drain diode forward voltage	V_{DF}	—	0.9	1.4	V	$I_F = 18 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-Drain diode reverse recovery time	t_{rr}	—	160	—	ns	$I_F = 18 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$
Body-Drain diode reverse recovery charge	Q_{rr}	—	1.0	—	μC	

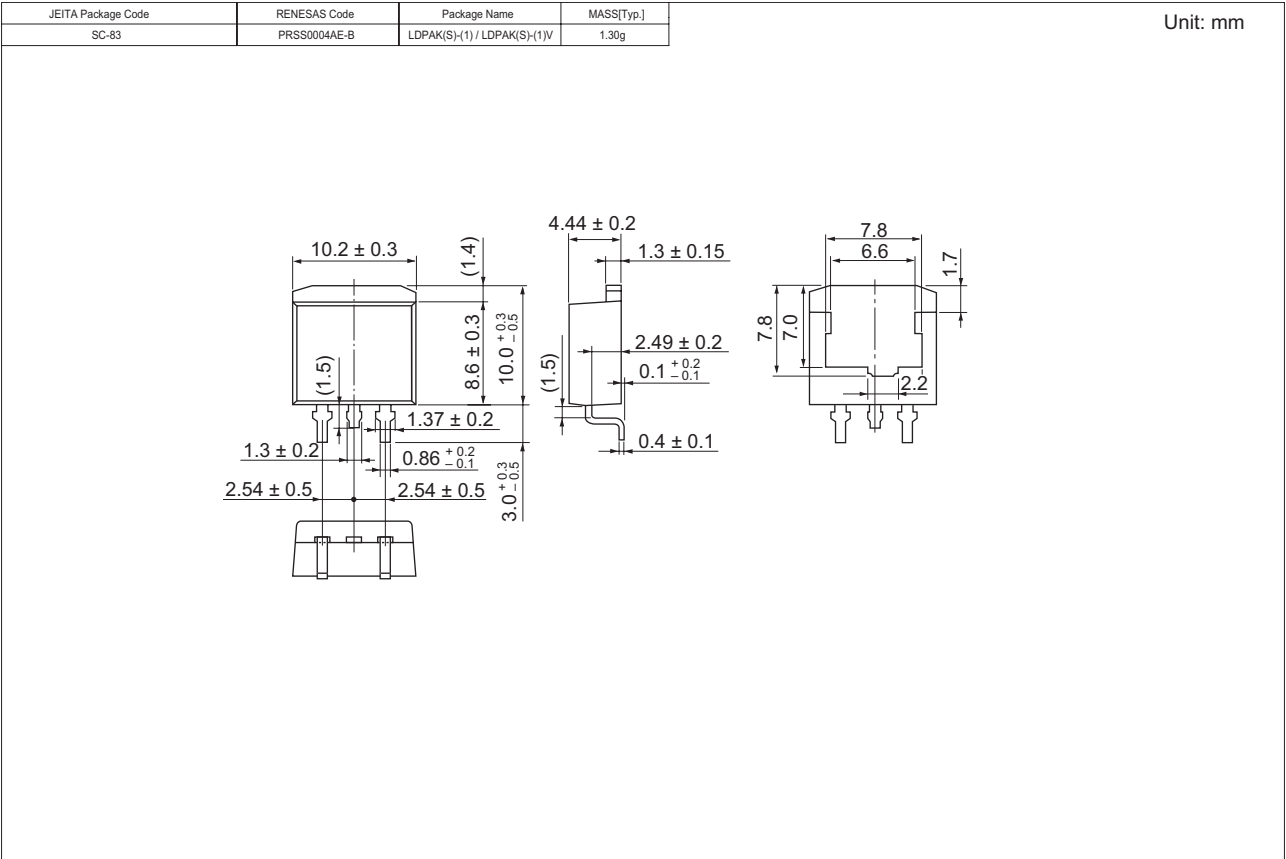
Notes: 4. Pulse test

Package Dimensions

• H5N2501LD



• H5N2501LS



• H5N2501LM

JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]	Unit: mm
—	PRSS0004AE-C	LDBAK(S)-(2) / LDBAK(S)-(2)V	1.35g	

The drawing shows the mechanical specifications of the H5N2501LM package. The top view shows a rectangular package with a width of 10.2 ± 0.3 mm and a length of 10.0 ± 0.3 mm. The side view shows a height of 4.44 ± 0.2 mm. The bottom view shows the lead dimensions: a lead width of 1.3 ± 0.2 mm, a lead pitch of 2.54 ± 0.5 mm, and a lead thickness of 0.4 ± 0.1 mm. Other dimensions include a lead length of 1.37 ± 0.2 mm, a lead angle of 0.86 ± 0.1 mm, and a lead spacing of 0.1 ± 0.1 mm. The package is labeled with (1.5) and (2.3) in parentheses.

Ordering Information

Part Name	Quantity	Shipping Container
H5N2501LSTL-E	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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