HA13173H

Multiple Voltage Regulator for Car Audio

REJ03F0226-0100
Rev.1.00
Jan 16, 2007

Description

The HA13173H is a multiple voltage regulator for car audio system. This IC has 5.0 V output for a microcontroller, 3.3 V output for a Digital Signal Processor, 8.0 V output for CD driver, 8.4 V output for audio control, 8.4 V output for illuminations, and high side switch output for external output.

The HA13173H also has FREG that is possible to control external PNP transistor. It is adjustable output voltage by changing an external resistor.

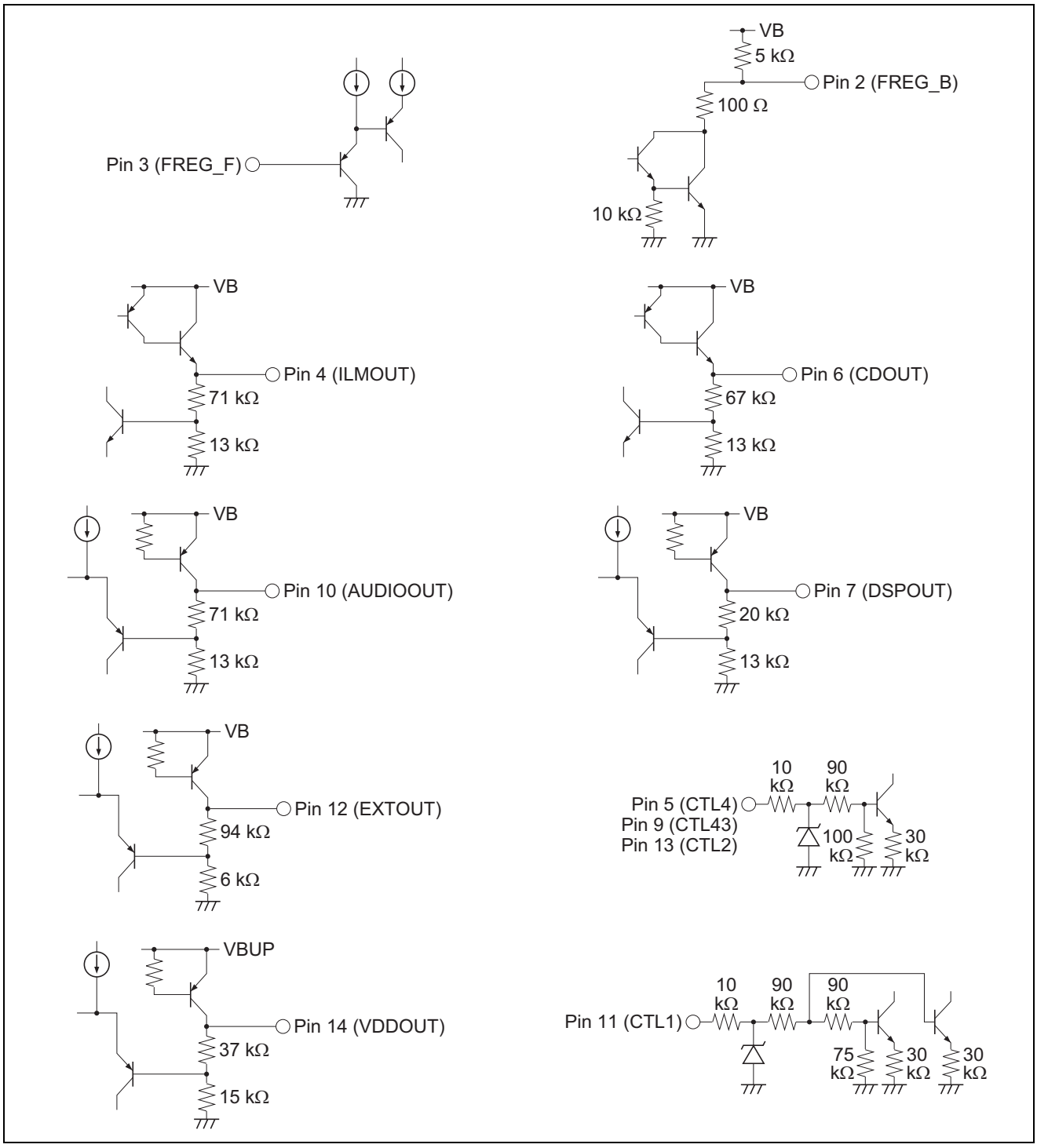
Functions

- Standby current is 100 μA max.
- The Vdd output for microcontroller has backup function, by independent power supply line.
- Low saturation output (PNP output) used for audio output.
- Output current limit circuit to avoid device destruction caused by shorted output, etc.
- High surge input protector against VB and VBUP.
- Built in a thermal shutdown circuit to prevent against the thermal destruction.
- The package is PRSS0015DA-C (SP-15TGV).

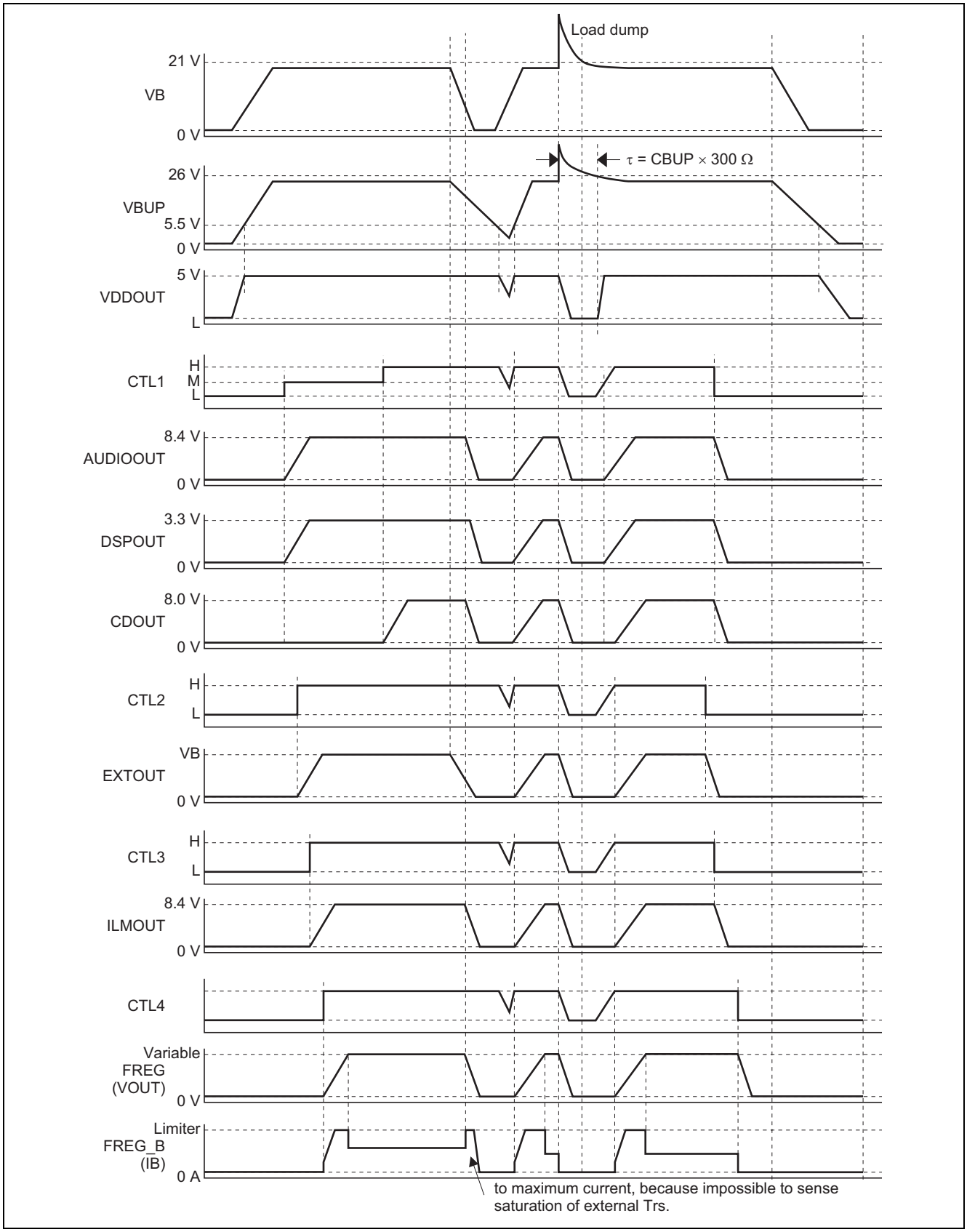
Pin Description

Pin No.	Pin Name	Specification	Protection			
			Normal	TSD ON	VB = 24 V	VB = 50 V
1	GND	Ground	—	—	—	—
2	FREG_B	External transistor bias operation	On/Off	On/Off	Off	Off
3	FREG_F	FREG feed back terminal	On/Off	On/Off	Off	Off
4	ILM OUT	8.4 V output for ILM/500 mA max	On/Off	Off	Off	Off
5	CTL4	FREG control terminal	—	—	—	—
6	CD OUT	8.0 V output for CD/1.3 A max	On/Off	Off	Off	Off
7	DSP OUT	3.3 V output for DSP/250 mA max	On/Off	Off	Off	Off
8	VB	Battery	—	—	—	—
9	CTL3	ILM control terminal	—	—	—	—
10	AUDIO OUT	8.4 V output for AUDIO/500 mA max	On/Off	Off	Off	Off
11	CTL1	DSP, CD, AUDIO control terminal	—	—	—	—
12	EXT OUT	High side output/600 mA max	On/Off	Off	Off	Off
13	CTL2	EXT control terminal	—	—	—	—
14	VDD OUT	5.0 V output for microcontroller	On	On	On	Off
15	VBUP	Back up	—	—	—	—

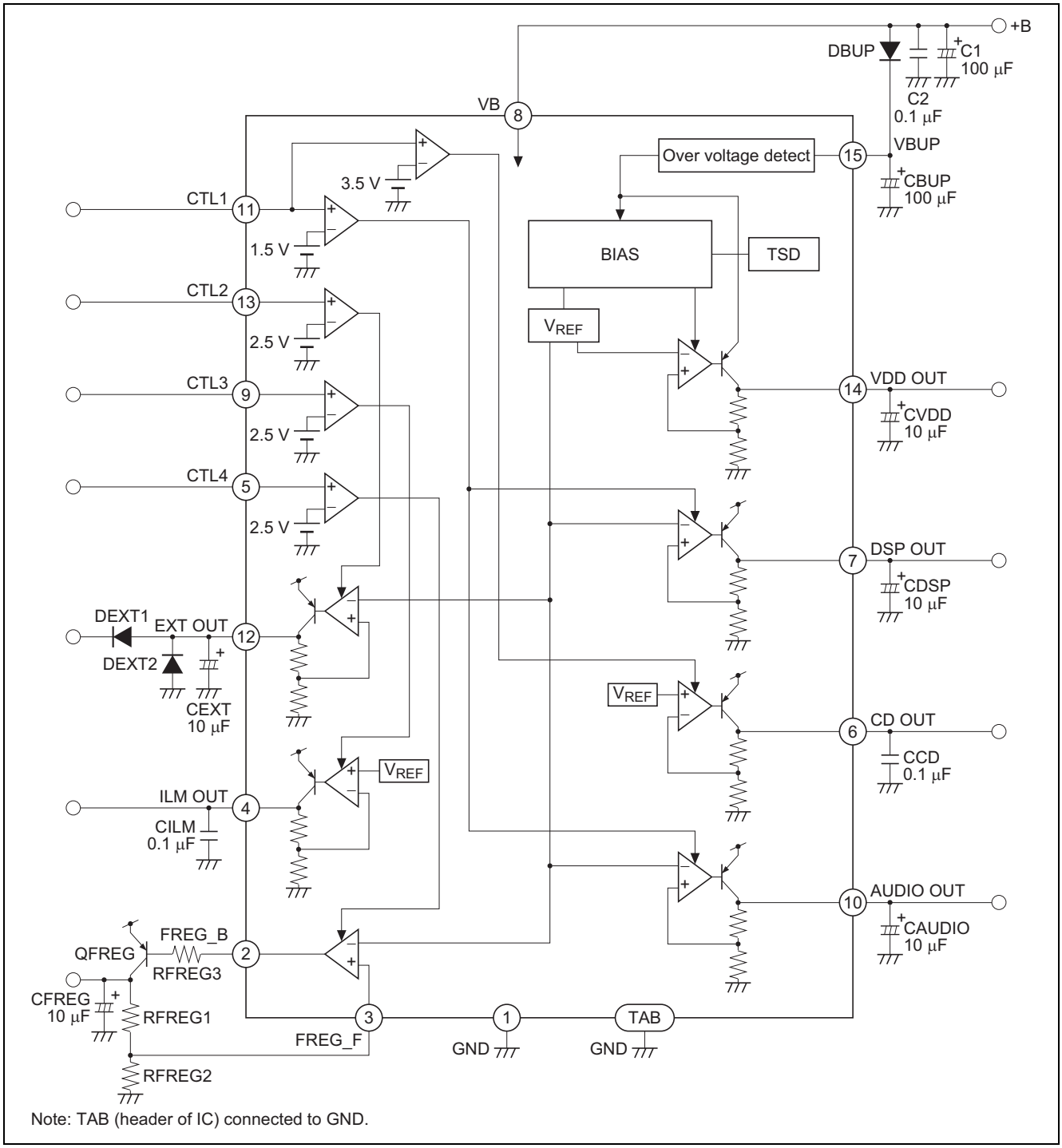
Equivalent Circuit



Timing Chart



Block Diagram



Note: TAB (header of IC) connected to GND.

External Parts Lineup

Parts No.	Function	Range of Recommended	Operation with Different Value from the Range of Recommended Value	
			More than the Range	Less than the Range
C1	Bypass capacitor	Upper 100 μF	—	Unstable Lower ripple rejection ratio
C2	To prevent oscillation	0.1 μF	Stability improve	Unstable
CBUP	B backup capacitor	0.1 to 1000 μF	Backup time becomes long	Unstable
CCD CILM	To prevent oscillation	0.1 to 1000 μF	Unconfirmed	Unstable
CVDD CDSP CAUDIO CFREG CEXT	To prevent oscillation	0.1 to 470 μF	Unconfirmed	Unstable
DBUP		IF ≥ 200 mA	Be careful of the maximum rating	
DEXT1 DEXT2	Protection against mistake in joining. Terminal protection for short circuit to +B when VCC terminal is open and for short circuit to GND when GND terminal is open. We recommend Schottky barrier diodes.	IF ≥ 1 A	—	Be careful of the maximum rating. The ability to protect terminal lower. And there is some possibility of destruction.
RFREG1 RFREG2	Output voltage = (1 + RFREG1/RFREG2) × 1.26 V	100 to 10 kΩ	Unstable	Loss of current increases
GFREG3	Resistance for limiting base current of PNP transistor	Choose resistance by a required output current value and hFE of PNP transistor		
QFREG	Output PNP transistor for FREG (We recommend Renesas 2SB857.)	hFE = 50 to 200	Choose resistance by a required output current value and hFE of PNP transistor	
			Unstable	Lower output current capability

Notes: 1. We recommend Polyester film capacitor. To improve stability, take notes of the below precautions.
(1) Use capacitor that is temperature independent.
(2) Use capacitor that is bias voltage independent.
(3) In order to bypass high frequency noise efficiently, mount the capacitor as close as possible to the VCC and GND of IC to eliminate PCB pattern inductance.

2. For using of the lower limit of recommended value, take notes of the below precautions.
(1) Use capacitor that is temperature independent.
(2) Use capacitor that is bias voltage independent.
(3) To eliminate PCB pattern inductance mount the capacitor as close as possible to the output pin and GND of IC.

3. To improve stability, take notes of the below precautions.
(1) Use capacitor that is temperature independent.
(2) Use capacitor that is bias voltage independent.
(3) ESR needs to be less than 10 Ω in all the temperature ranges to be used.
(4) To eliminate PCB pattern inductance mount the capacitor as close as possible to the output pin and GND of IC.

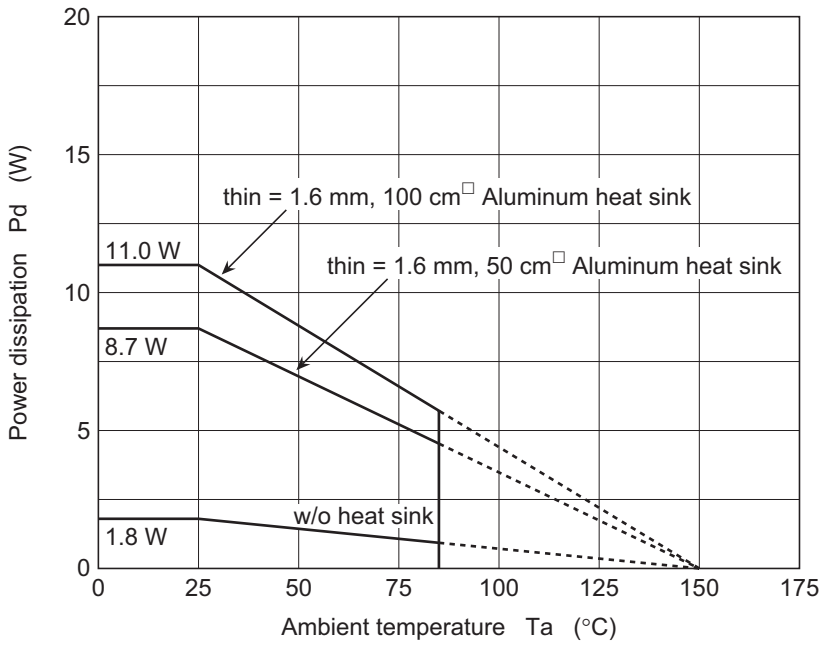
Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating	Unit	Note
Operating power supply voltage 1	Vcc1	19	V	
Operating power supply voltage 2	Vcc2	24	V	1
Peak voltage	Vcc(PEAK)	50	V	2
Power dissipation	Pd	36	W	3
Junction temperature	Tj	150	°C	
Operating temperature	Topr	–40 to +85	°C	
Storage temperature	Tstg	–55 to +125	°C	

Notes: Recommended power supply voltage range 10 to 16 V.

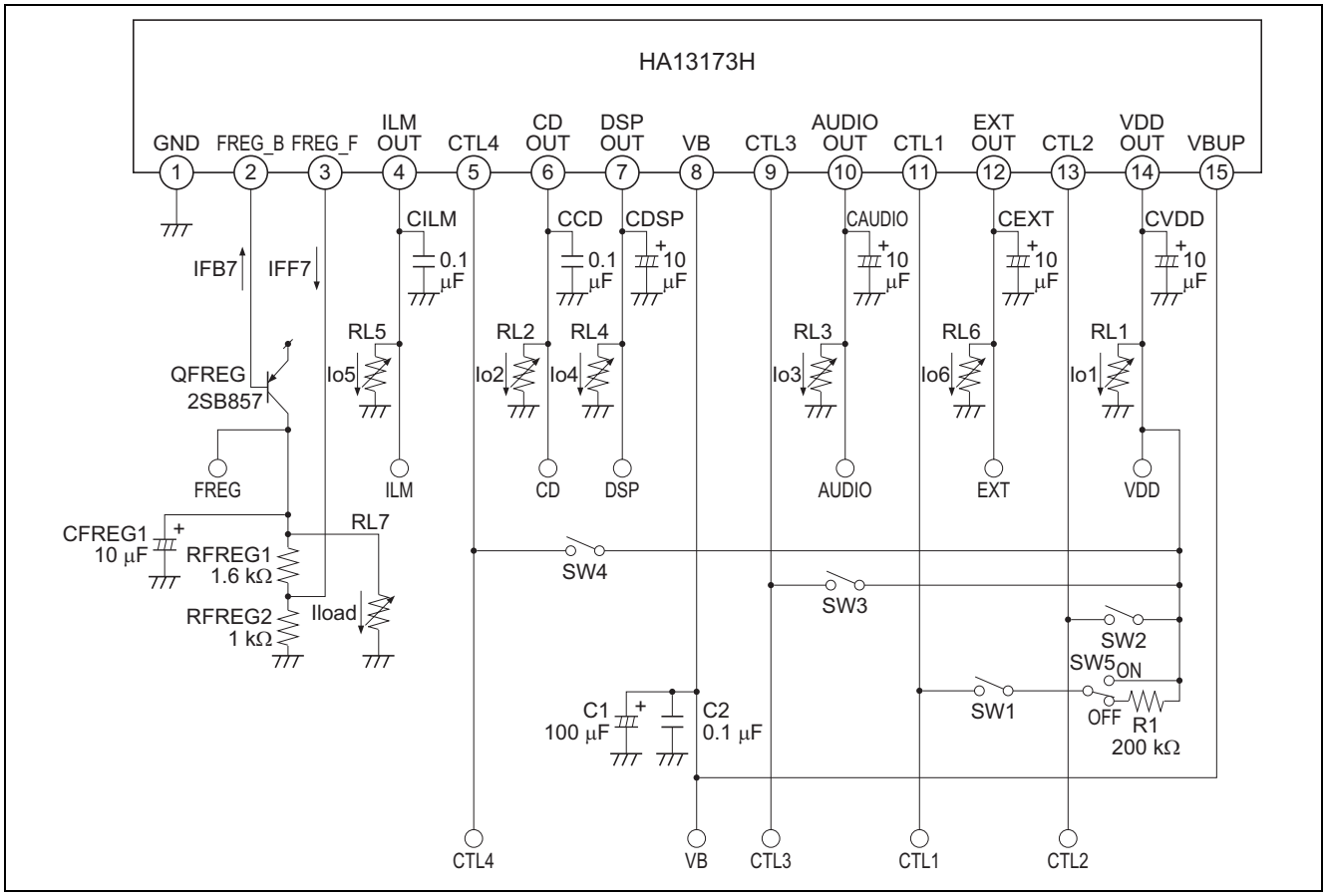
1. Applied time is less than 60 s.
2. Surge pulse as input.
3. Ta = 25°C. : Permissible power dissipation when using a heat sink of infinite area. Refer to the derating curves below.



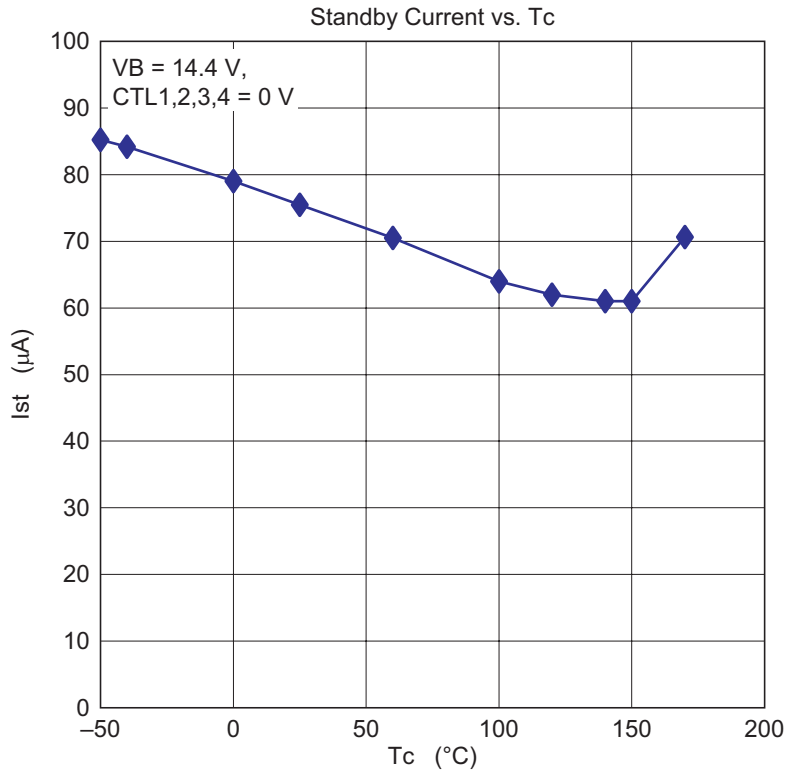
Electrical Characteristics

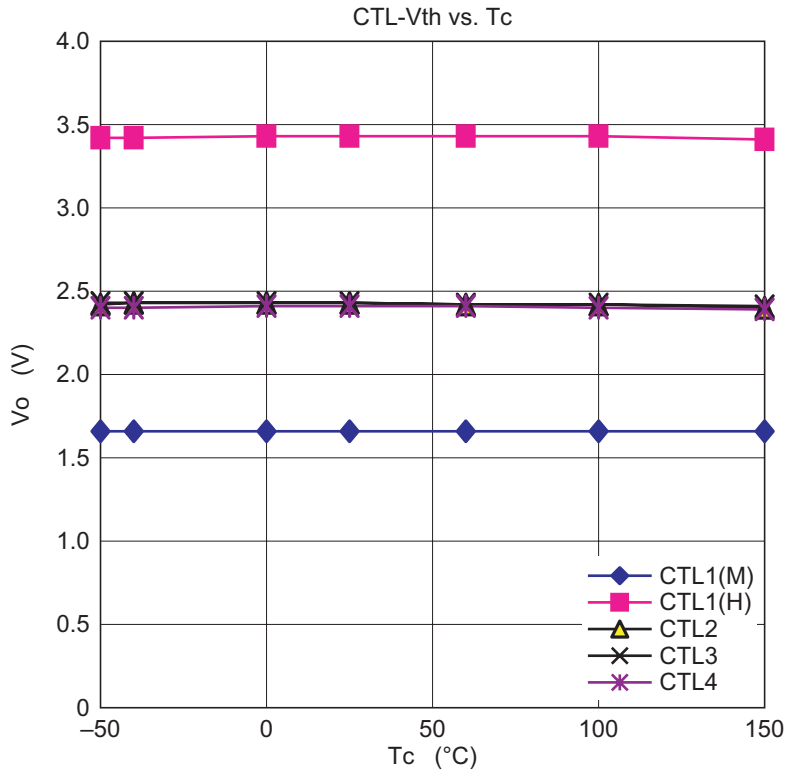
Item		Symbol	Min	Typ	Max	Unit	Test Condition
Standby current		IST	—	65	100	μA	CTL1, 2, 3, 4 = 0 V
CTL1 L level (DSP, AUDIO, CD OFF)		VC1L	0.0	—	1.0	V	
CTL1 M level (DSP, AUDIO ON, CD OFF)		VC1M	2.0	—	3.0	V	
CTL1 H level (DSP, AUDIO, CD ON)		VC1H	4.0	—	6.0	V	
CTL2 L level (EXT OFF)		VC2L	0.0	—	2.0	V	
CTL2 H level (EXT ON)		VC2H	3.0	—	6.0	V	
CTL3 L level (ILM OFF)		VC3L	0.0	—	2.0	V	
CTL3 H level (ILM ON)		VC3H	3.0	—	6.0	V	
CTL4 L level (FREG OFF)		VC4L	0.0	—	2.0	V	
CTL4 H level (FREG ON)		VC4H	3.0	—	6.0	V	
VDD OUT	Output voltage	Vo1	4.75	5.00	5.25	V	Io1 = 160 mA
	Voltage regulation	ΔVo11	—	10	50	mV	Vcc = 10 to 16 V, Io1 = 160 mA
	Load regulation	ΔVo12	—	50	100	mV	Io1 = 0 to 160 mA
	Minimum I/O voltage differential	ΔVo13	—	0.4	0.9	V	Io1 = 160 mA
	Output current capacity	Io1	200	400	—	mA	Vo1 ≥ 4.75 V
	Ripple rejection ratio	SVR1	45	55	—	dB	f = 100 Hz, Io1 = 160 mA
CD OUT	Output voltage	Vo2	7.6	8.0	8.4	V	Io2 = 1.0 A
	Voltage regulation	ΔVo21	—	40	100	mV	Vcc = 10 to 16V, Io2 = 1.0 A
	Load regulation	ΔVo22	—	70	150	mV	Io2 = 10m to 1.0 A
	Minimum I/O voltage differential	ΔVo23	—	1.0	1.5	V	Io2 = 1.0 A
	Output current capacity	Io2	1.3	2.0	—	mA	Vo2 ≥ 7.6 V
	Ripple rejection ratio	SVR2	40	50	—	dB	f = 100 Hz, Io2 = 1.0 A
AUDIO OUT	Output voltage	Vo3	8.1	8.4	8.7	V	Io3 = 400 mA
	Voltage regulation	ΔVo31	—	30	90	mV	Vcc = 10 to 16 V, Io3 = 400 mA
	Load regulation	ΔVo32	—	100	200	mV	Io3 = 10 to 400 mA
	Minimum I/O voltage differential	ΔVo33	—	0.4	0.9	V	Io3 = 400 mA
	Output current capacity	Io3	500	850	—	mA	Vo3 ≥ 8.1 V
	Ripple rejection ratio	SVR3	45	50	—	dB	f = 100 Hz, Io3 = 400 mA
DSP OUT	Output voltage	Vo4	3.1	3.3	3.5	V	Io4 = 200 mA
	Voltage regulation	ΔVo41	—	40	100	mV	Vcc = 10 to 16 V, Io4 = 200 mA
	Load regulation	ΔVo42	—	50	100	mV	Io4 = 0 to 200 mA
	Output current capacity	Io4	250	500	—	mA	Vo4 ≥ 3.1 V
	Ripple rejection ratio	SVR4	45	55	—	dB	f = 100 Hz, Io4 = 200 mA
ILM OUT	Output voltage	Vo5	8.0	8.4	8.8	V	Io5 = 400 mA
	Voltage regulation	ΔVo51	—	40	100	mV	Vcc = 10 to 16 V, Io5 = 400 mA
	Load regulation	ΔVo52	—	70	150	mV	Io5 = 10 to 400 mA
	Minimum I/O voltage differential	ΔVo53	—	1.0	1.3	V	Io5 = 400 mA
	Output current capacity	Io5	500	900	—	mA	Vo5 ≥ 8.0 V
	Ripple rejection ratio	SVR5	40	50	—	dB	f = 100 Hz, Io5 = 400 mA
EXT OUT	Minimum I/O voltage differential	ΔVo61	—	0.6	1.0	V	Vcc = 10 to 16 V, Io6 = 480 mA
	Output current capacity	Io6	600	900	—	mA	Vo61 ≤ 1.0 V
FREG OUT	FREG_F Output voltage	VFF7	1.20	1.26	1.32	V	Iload (external PNP) = 400 mA
	FREG_F Voltage regulation	ΔVFF71	—	10	25	mV	Vcc = 10 to 16 V, Iload = 400 mA
	FREG_F Load regulation	ΔVFF72	—	10	25	mV	Iload = 10 to 400 mA
	FREG_B Output current capacity	IFB7	35	50	80	mA	VFF ≥ 1.20 V
	FREG_F input bias current	IFF7	—	50	300	nA	

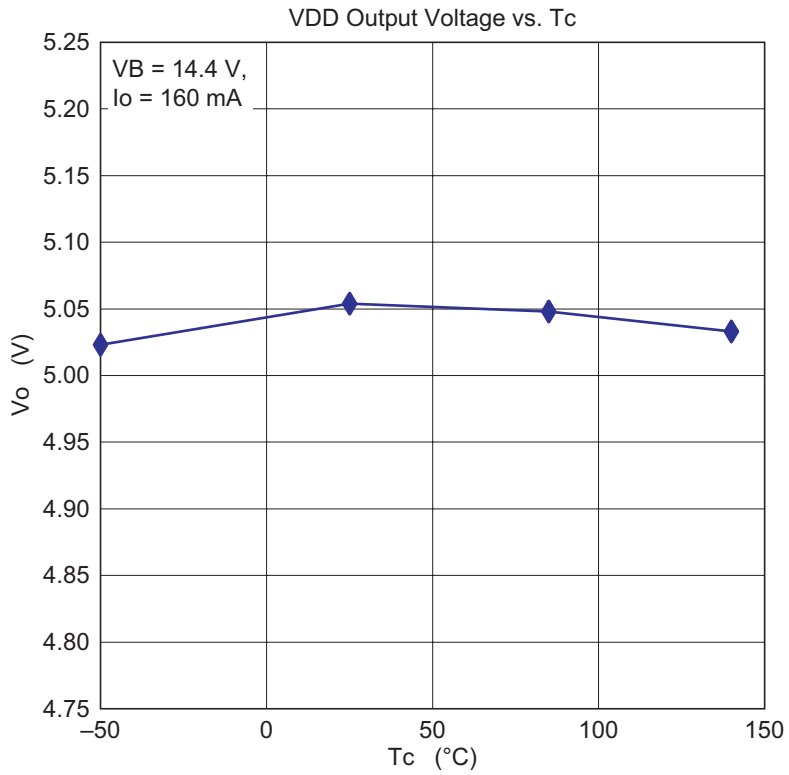
Evaluation Circuit

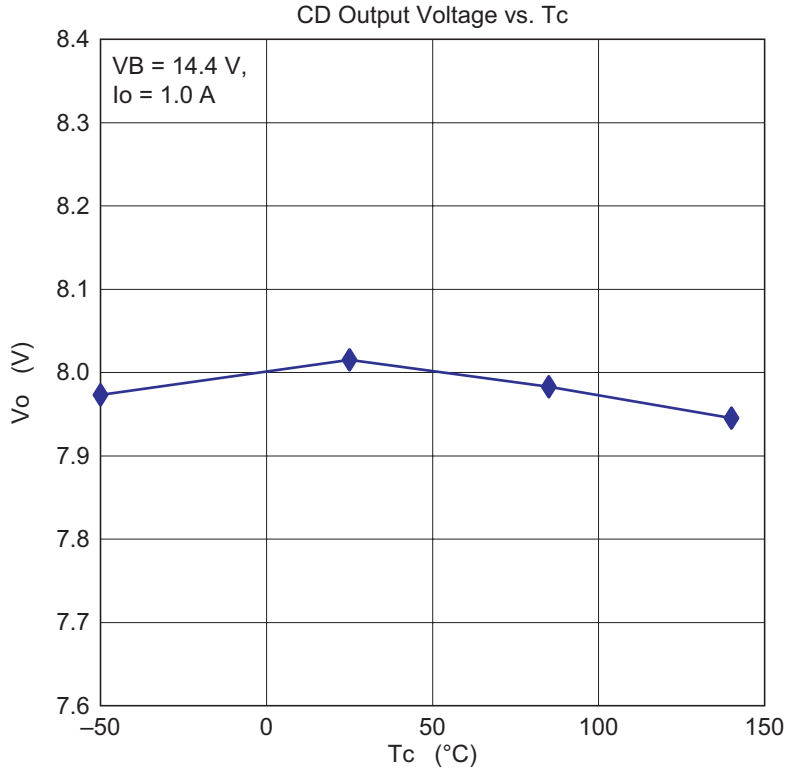


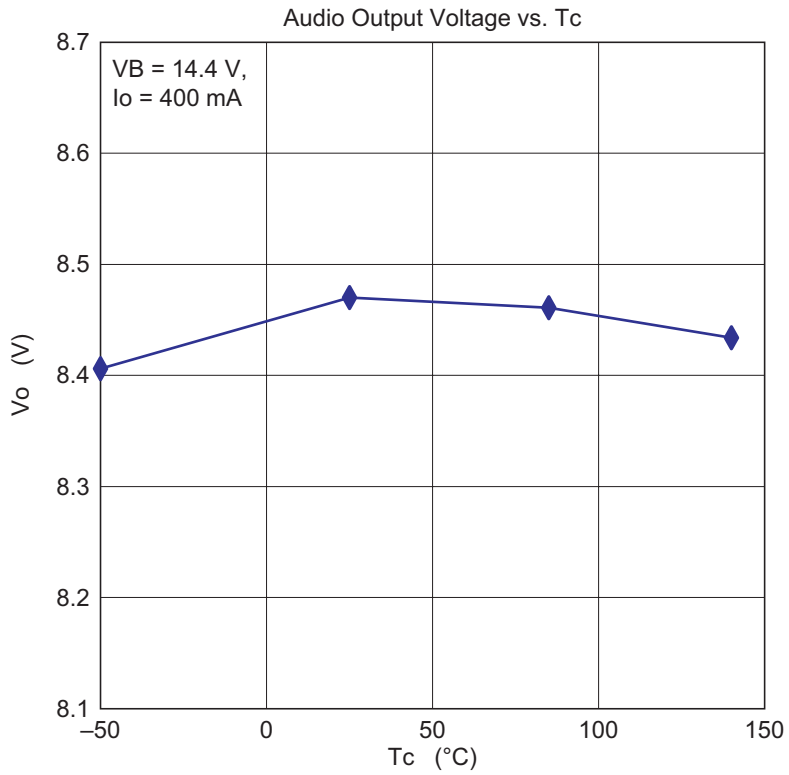
Main Characteristics

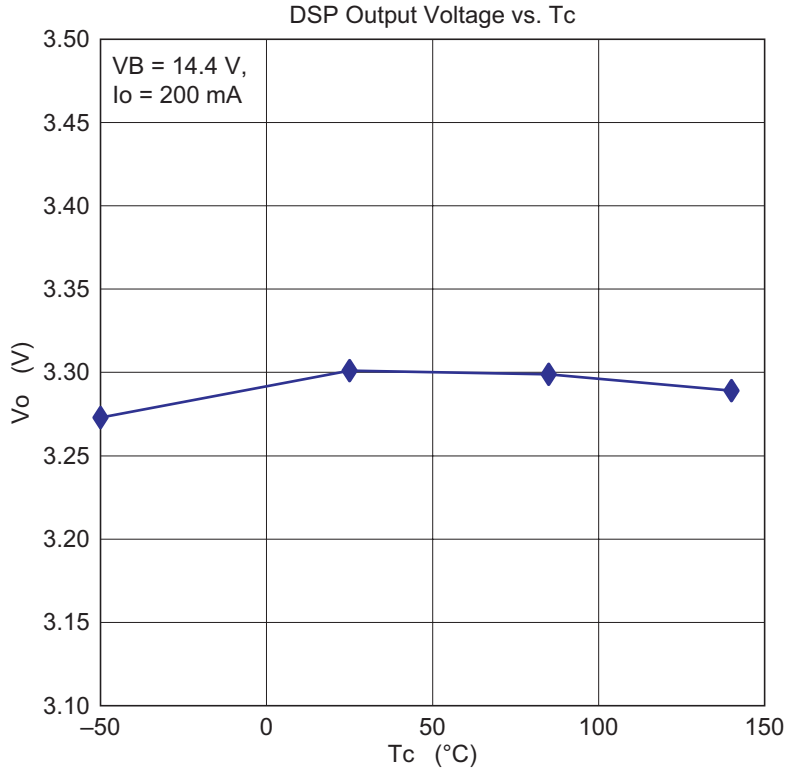


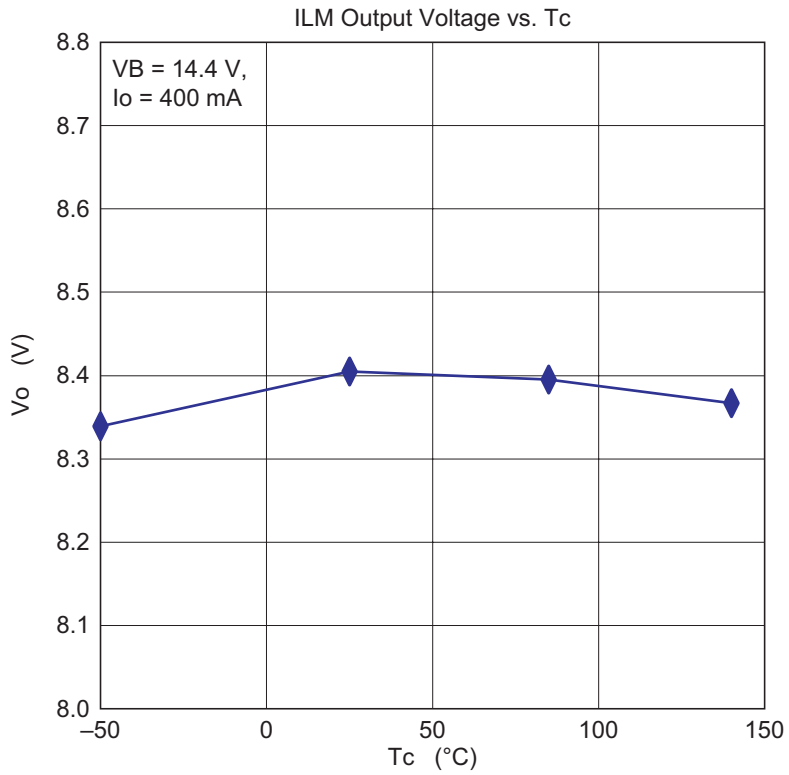


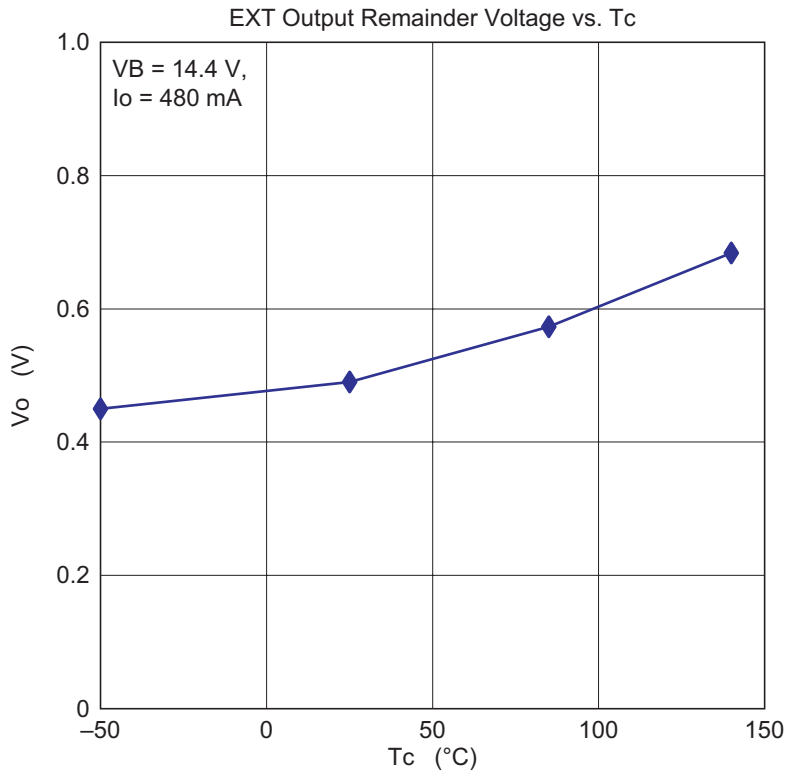

VDD Output Voltage vs. Tc
VB = 14.4 V,
Io = 160 mA
5.25
5.20
5.15
5.10
5.05
5.00
4.95
4.90
4.85
4.80
4.75
Vo (V)
–50
0
50
100
150
Tc (°C)

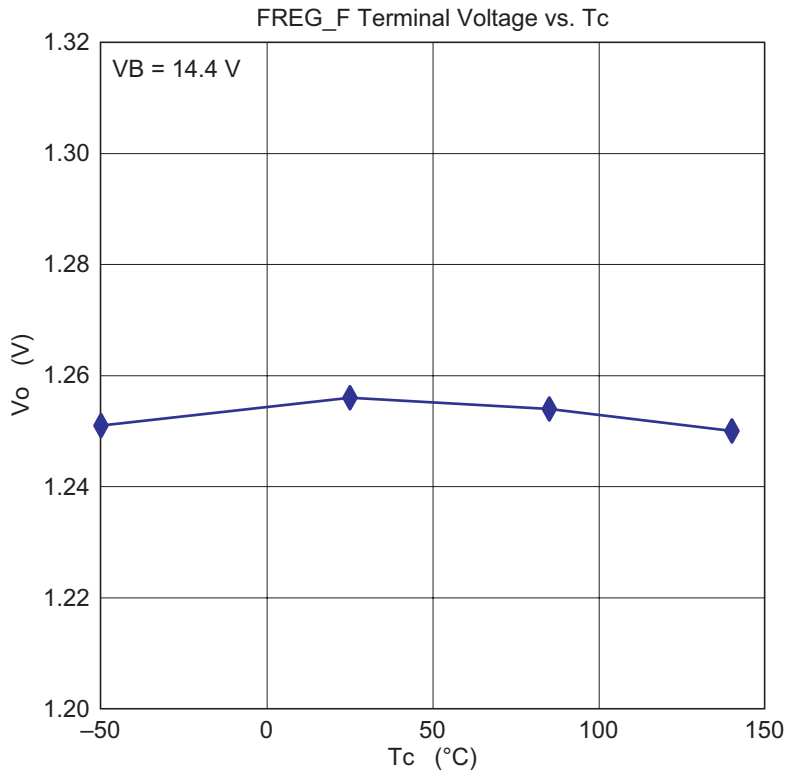

CD Output Voltage vs. Tc
VB = 14.4 V,
Io = 1.0 A
8.4
8.3
8.2
8.1
8.0
7.9
7.8
7.7
7.6
Vo (V)
–50
0
50
100
150
Tc (°C)

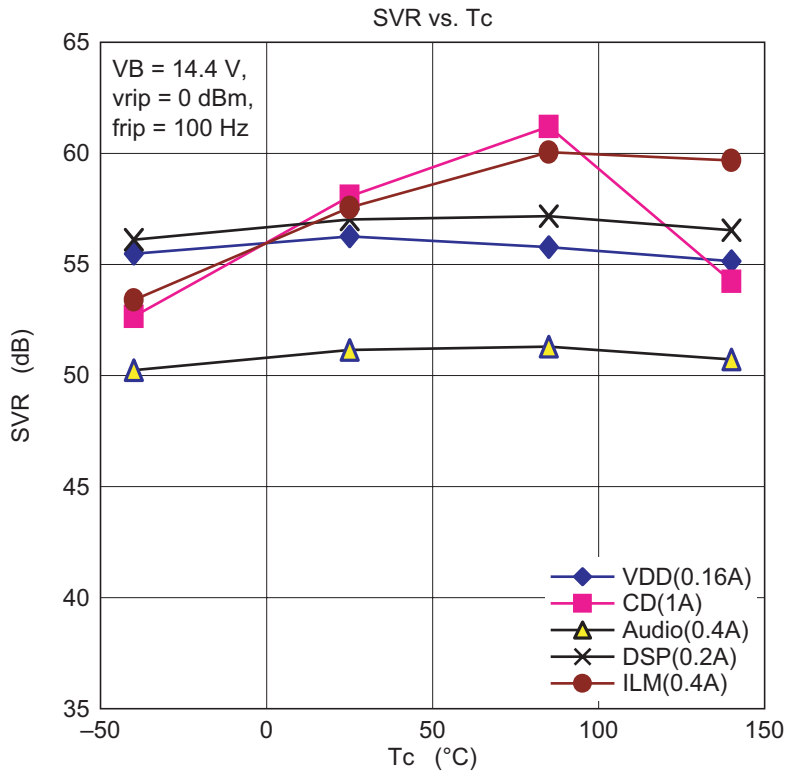

Audio Output Voltage vs. Tc
VB = 14.4 V,
Io = 400 mA
8.7
8.6
8.5
8.4
8.3
8.2
8.1
Vo (V)
–50
0
50
100
150
Tc (°C)

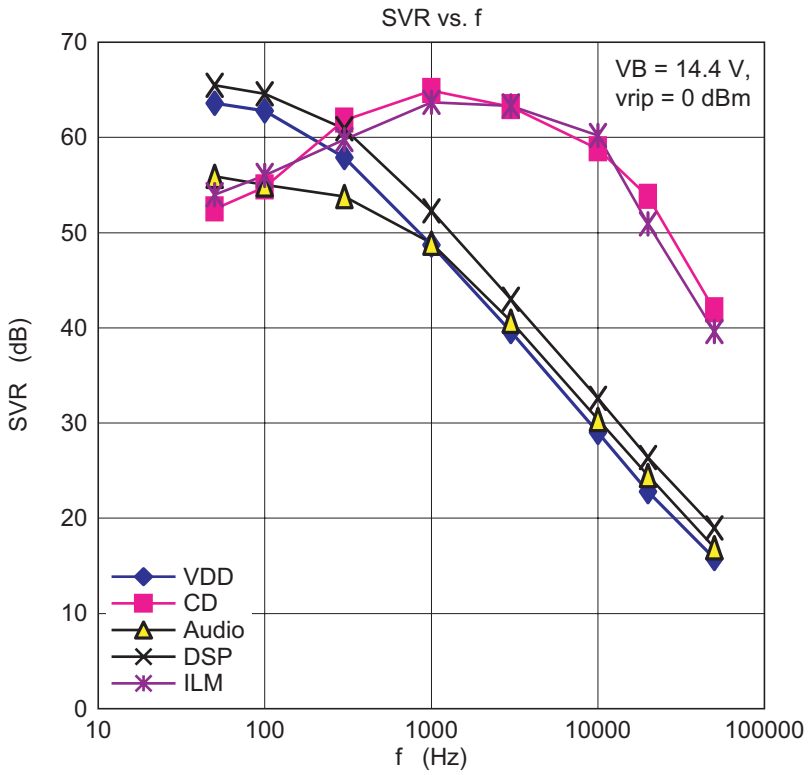

DSP Output Voltage vs. Tc
VB = 14.4 V,
Io = 200 mA
3.50
3.45
3.40
3.35
3.30
3.25
3.20
3.15
3.10
Vo (V)
–50
0
50
100
150
Tc (°C)

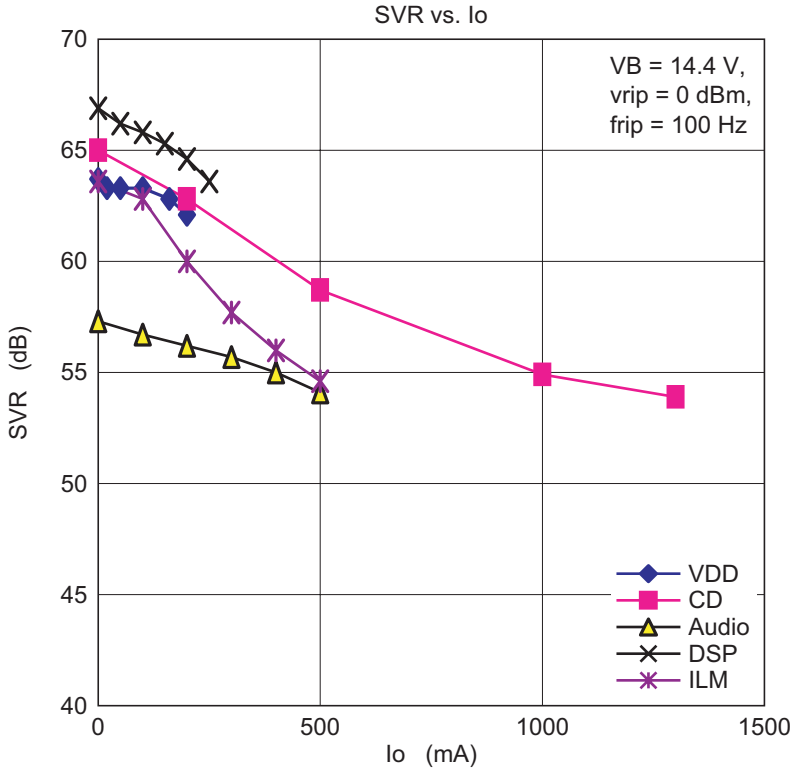

ILM Output Voltage vs. Tc
VB = 14.4 V,
Io = 400 mA
8.8
8.7
8.6
8.5
8.4
8.3
8.2
8.1
8.0
Vo (V)
–50
0
50
100
150
Tc (°C)

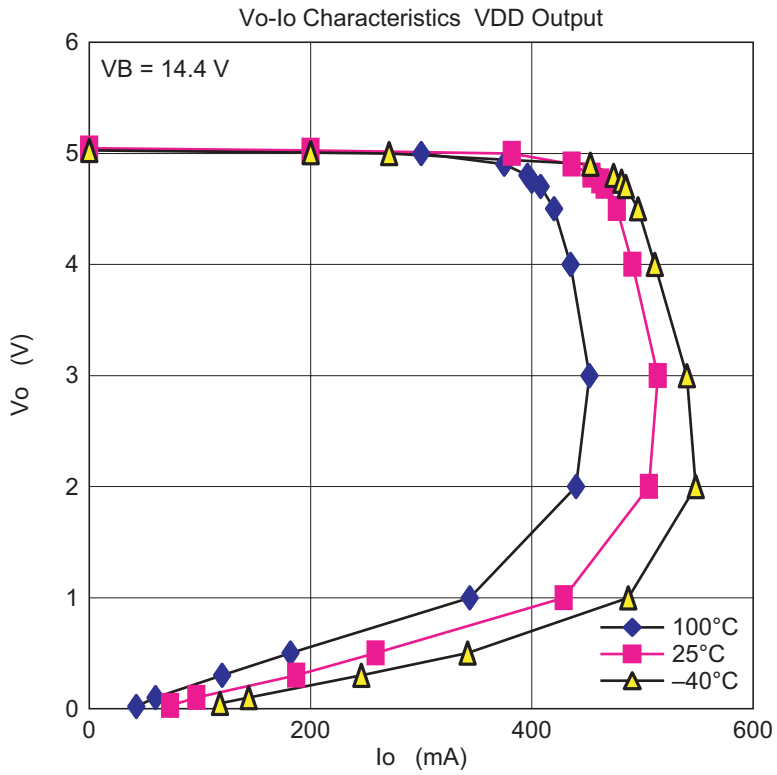

EXT Output Remainder Voltage vs. Tc
VB = 14.4 V,
Io = 480 mA
1.0
0.8
0.6
0.4
0.2
0
Vo (V)
–50
0
50
100
150
Tc (°C)

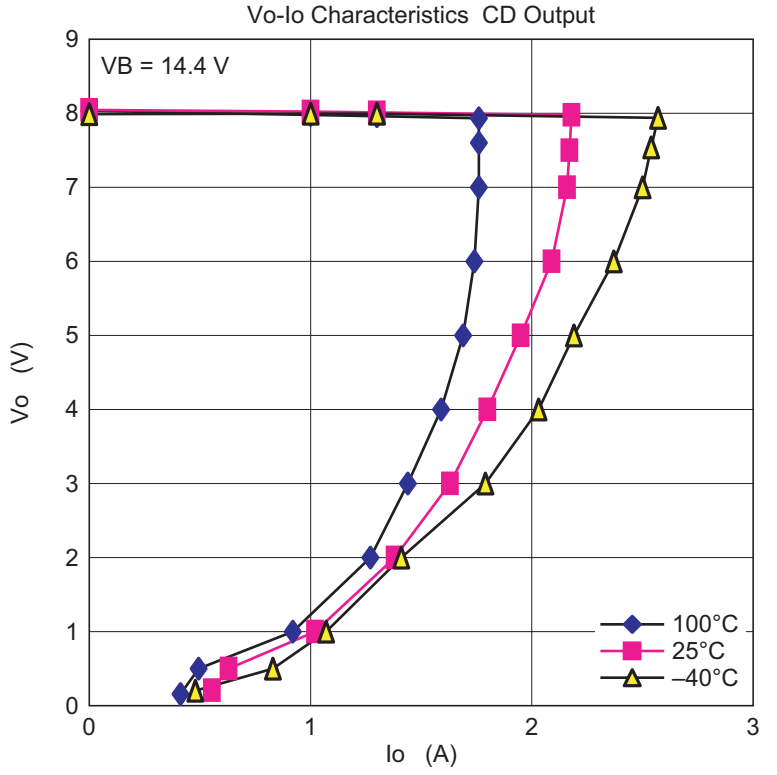

FREG_F Terminal Voltage vs. Tc
VB = 14.4 V
1.32
1.30
1.28
1.26
1.24
1.22
1.20
Vo (V)
–50
0
50
100
150
Tc (°C)

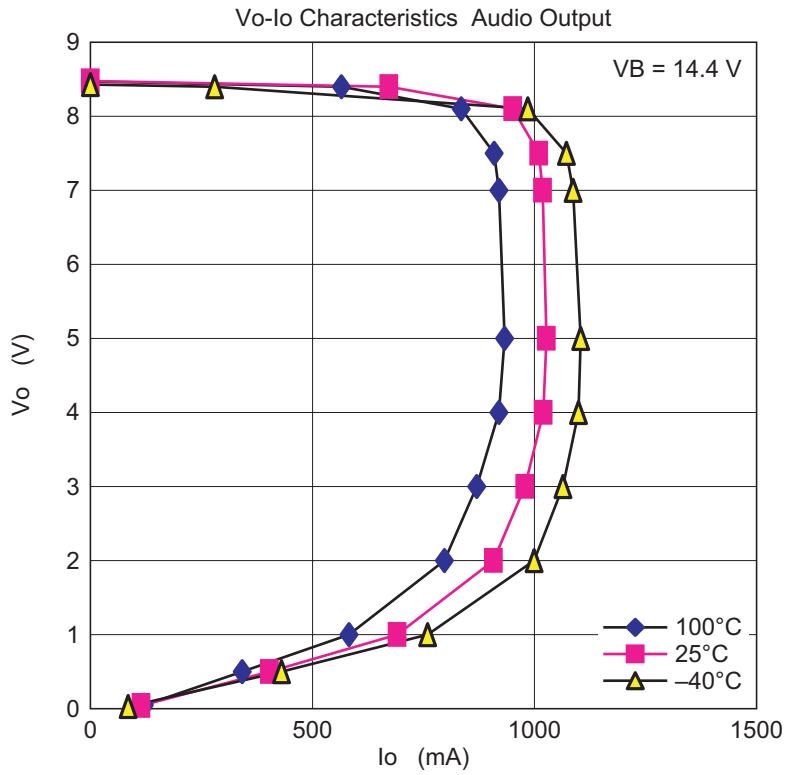

SVR vs. Tc
VB = 14.4 V,
vrip = 0 dBm,
frip = 100 Hz
65
60
55
50
45
40
35
SVR (dB)
–50
0
50
100
150
Tc (°C)
VDD(0.16A)
CD(1A)
Audio(0.4A)
DSP(0.2A)
ILM(0.4A)

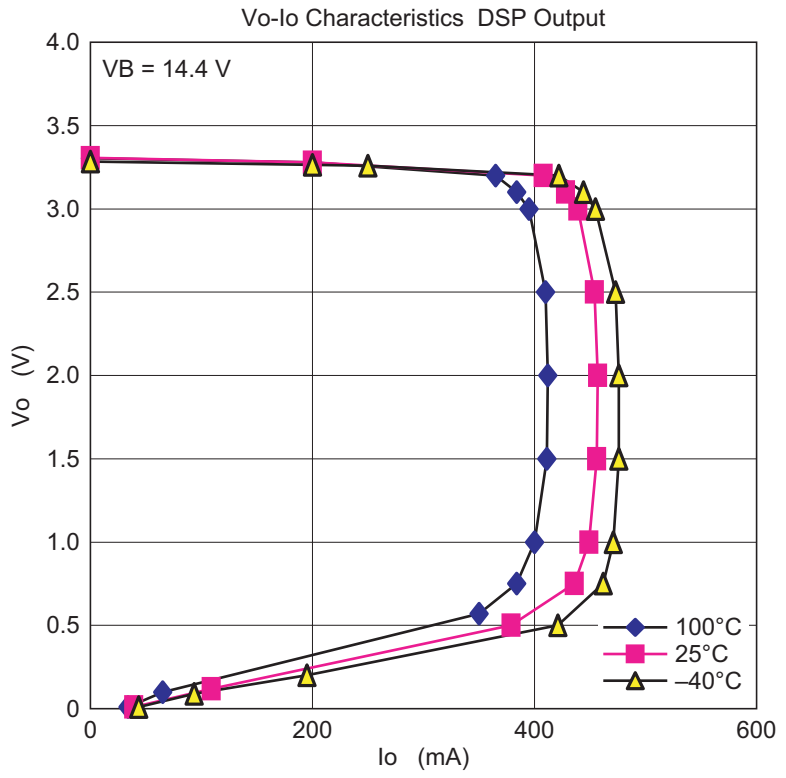

SVR vs. f
VB = 14.4 V,
vrip = 0 dBm
SVR (dB)
f (Hz)
VDD
CD
Audio
DSP
ILM
70
60
50
40
30
20
10
0
10
100
1000
10000
100000

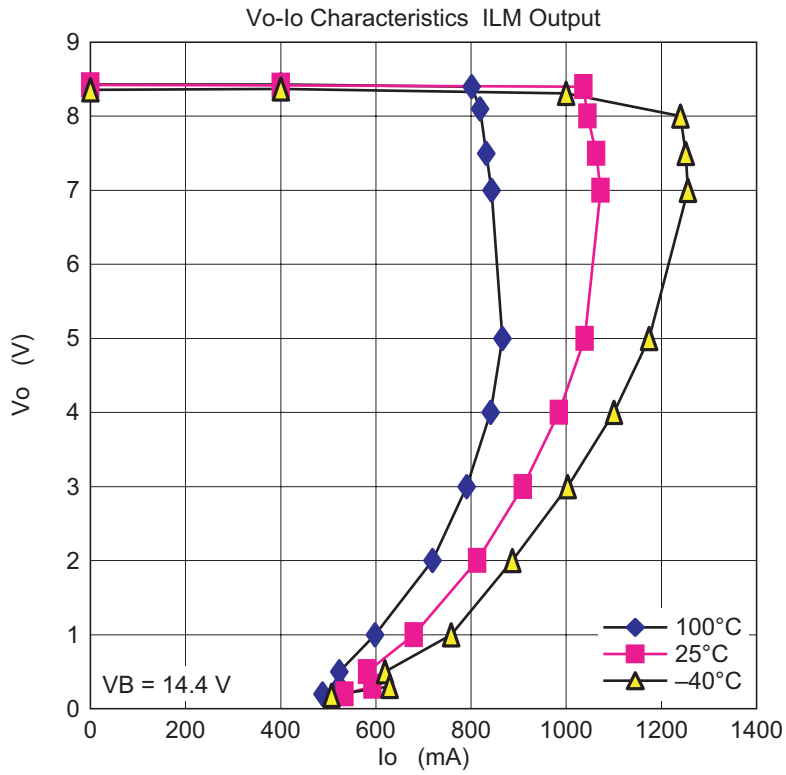

SVR vs. Io
VB = 14.4 V,
vrip = 0 dBm,
frip = 100 Hz
SVR (dB)
Io (mA)
VDD
CD
Audio
DSP
ILM
70
65
60
55
50
45
40
0
500
1000
1500

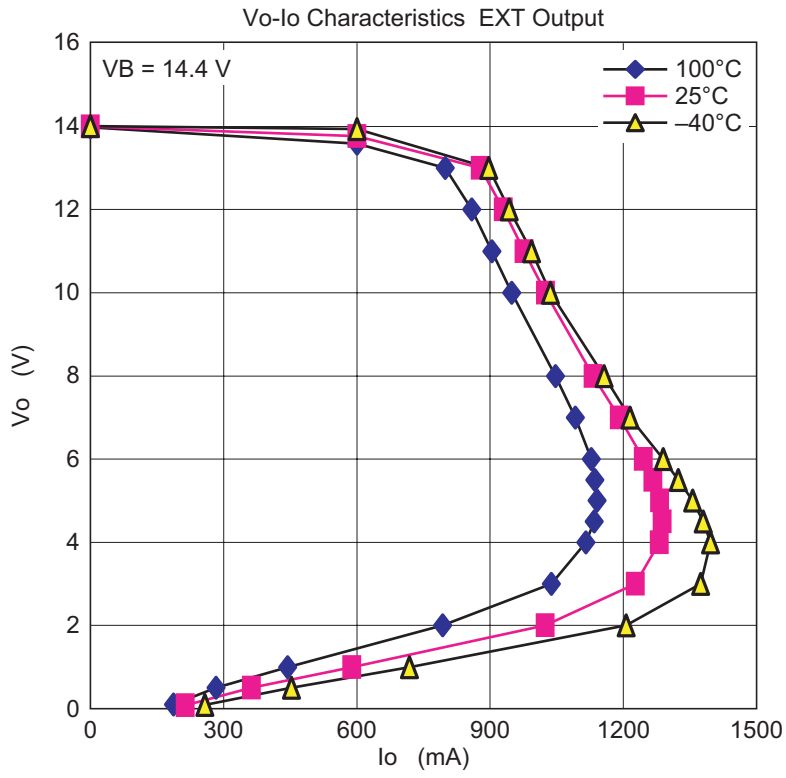

Vo-Io Characteristics VDD Output
VB = 14.4 V
Vo (V)
Io (mA)
0
1
2
3
4
5
6
0
200
400
600
100°C
25°C
–40°C

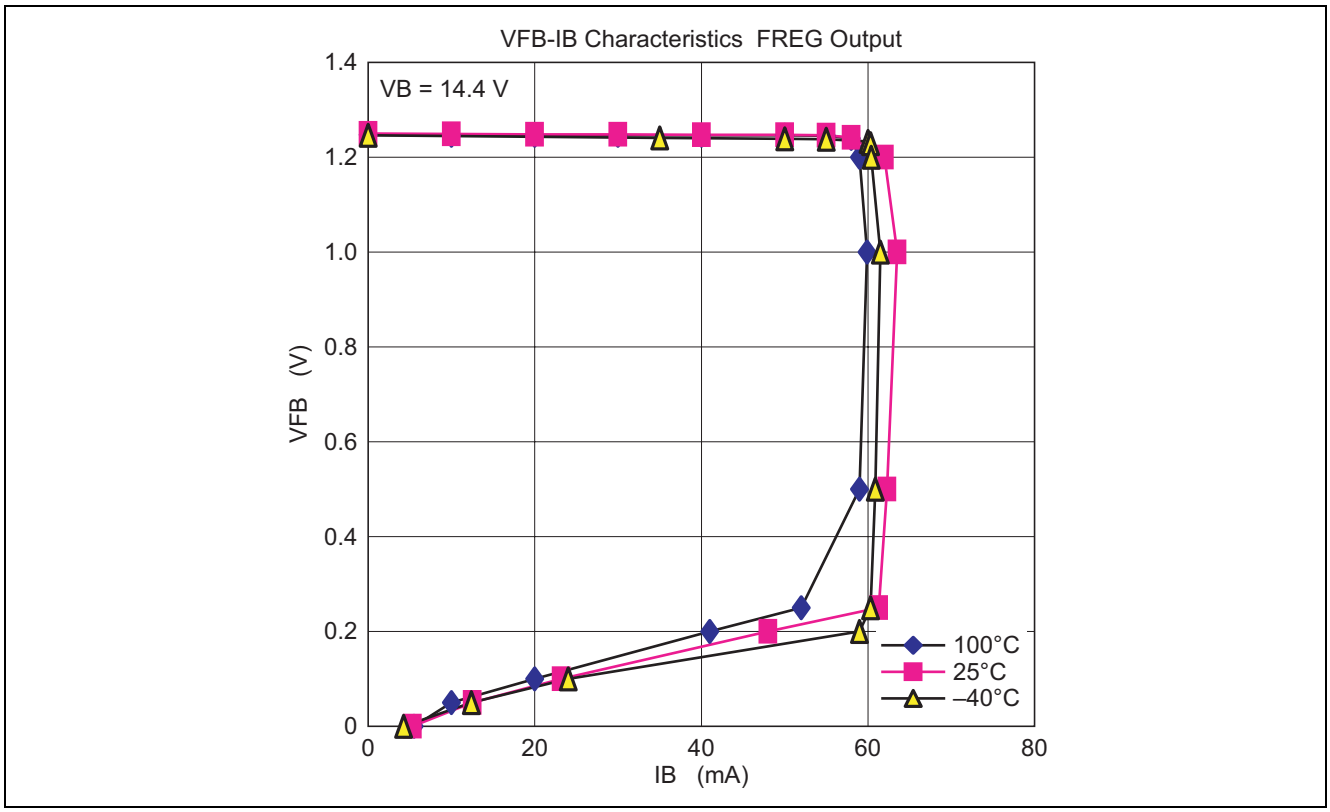

Vo-Io Characteristics CD Output
VB = 14.4 V
Vo (V)
Io (A)
0
1
2
3
4
5
6
7
8
9
0
1
2
3
100°C
25°C
–40°C


Vo-Io Characteristics Audio Output
VB = 14.4 V
Vo (V)
Io (mA)
0
1
2
3
4
5
6
7
8
9
0
500
1000
1500
100°C
25°C
–40°C


Vo-Io Characteristics DSP Output
VB = 14.4 V
Vo (V)
Io (mA)
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
0
200
400
600
100°C
25°C
–40°C


Vo-Io Characteristics ILM Output
Vo (V)
Io (mA)
VB = 14.4 V
100°C
25°C
–40°C
0
1
2
3
4
5
6
7
8
9
0
200
400
600
800
1000
1200
1400


Vo-Io Characteristics EXT Output
Vo (V)
Io (mA)
VB = 14.4 V
100°C
25°C
–40°C
0
2
4
6
8
10
12
14
16
0
300
600
900
1200
1500

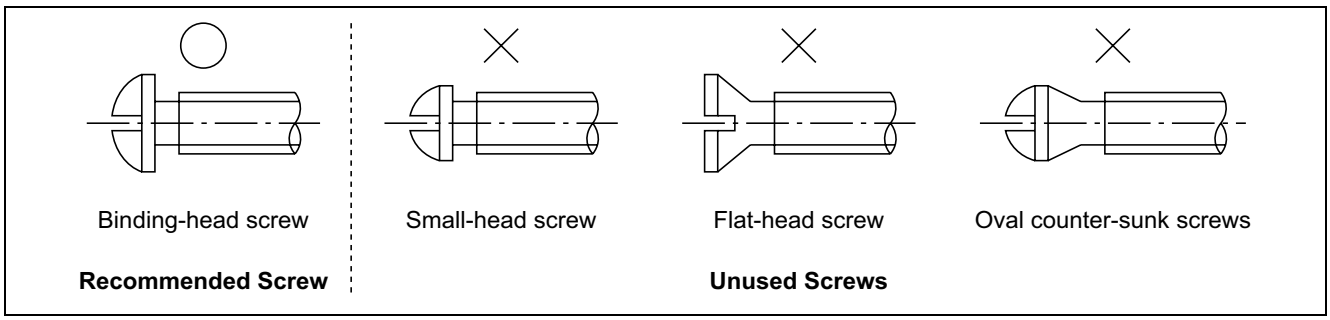

VFB-IB Characteristics FREG Output
VB = 14.4 V
VFB (V)
IB (mA)
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
0
20
40
60
80
100°C
25°C
–40°C

Handling Cautions (SP-15TGV Package)

Mounting

1. For mounting the package on the heat sink, 4 to 8 kg·cm of screwing-torque is recommended; excessive torque will cause device deformation, resulting in pellet-crack, connector-lead-wire-breaking, etc., and too less torque will increase the heat resistance.

2. The use of screws needs the following cautions.
   1) Use the standardized binding-head screws.
   2) Ova counter-sunk screws, subjecting the IC to intense stress, must not be used.
   3) To the use of tapping screws the cautions for binding torque strength must be applied.
   4) Use a tapping screw diameter smaller than an IC mounting-hole.



3. In IC binding, metal-fittings striking on the plastic of the IC may cause characteristics-deterioration or package-crack.

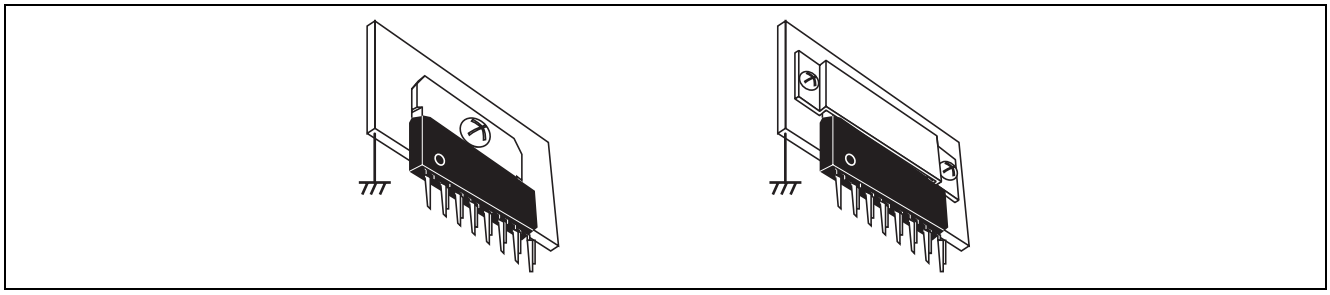
4. Poor flatness of heat sink sometimes prevents effective heat-sinking or subjects the IC surface to intense stress, causing characteristics-deterioration or package-crack.
   1) 0.1 mm max. of heat-sink flatness error for the contact area (14.3 mm × 19.66 mm) will be tolerated.
   2) Contact-surface ruggedness should be finished in ∇∇ grade.
   3) For aluminum, copper, or iron plates, check them for no burr and mold them for screw-holes.
   4) Cutting chips between the IC header and the heat sink will cause heat-sinking deterioration.
   5) The heat-sink hole diameter should not exceed 4.0 mm.

5. As silicone grease, the Shin-Etsu Chemical Industry G746 is recommended. Coarse or an excessive amount of grease may cause intensive stress to the IC, when binding.

6. Do not Screw the IC on the heat sink after soldering the lead wires on the printed circuit board (PCB). If the IC is screwed after the lead wires are soldered on the PCB then characteristics of the IC may deteriorate in the cause of large strain concentrate to the lead wires because of dimension-difference of the PCB and the heat sink.

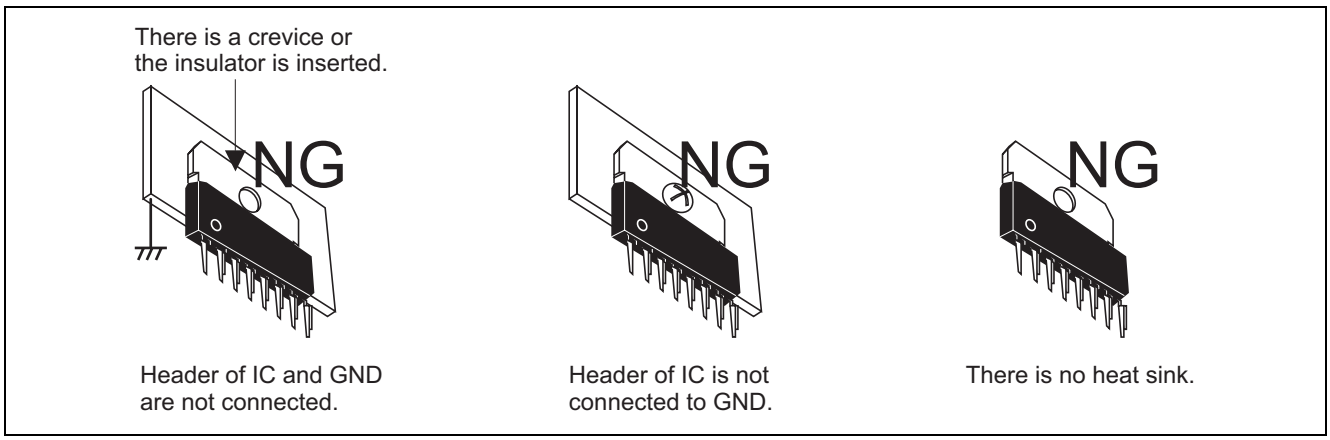
7. Do not solder of lead wires to the header of the IC on direct. If you solder direct then the IC life characteristics will deteriorate remarkably with bad-influence on the die.
   For the method and conditions of lead-wire forming, users are requested to contact the vendor.

8. Header of IC (TAB) have to connect to GND.
   For mounting the header of IC on the heat sink with the screw, heat sink have to connect to GND. When header of IC mount with heat sink with holding parishes conductive material, holding parts have to connect to GND. At this time, the holding parts mount with heat sink with the screw, or it must connect to header of IC. If users have question or request, please contact the vendor.



Example of Recommendation about the Method of Connecting Header of IC to GND

Bad example



9. Soldering should be done within the soldering heat test standard of the IC, specifying that the lead wires, up to 1 to 1.5 mm off the IC body, are kept in solder at 260°C for 10 seconds (2 or less times) and at 350°C for 3 seconds. Therefore give careful consideration in order to do not exceed the condition. In a soldering iron is used, use a soldering iron grounded and do not leak at the tip.

Characteristics

1. When there may be the mode which VB, VBUP or GND, and each output reverse with a normal potential state in application, it recommends attaching a diode for IC protection. When outputting the terminal of IC to the direct set exterior, a diode is required in order to protect IC from incorrect contact on a battery and a GND line. Especially EXTOUT is required.

2. In the parts shown in external part lineup, the value of a capacitor is the minimum value required in order to secure the oscillation stability of IC. Please use the capacitor independent of temperature and bias. Moreover, please use the capacitor whose ESR is 10 Ω or less in the operating temperature range.

Protections

1. Overvoltage protection circuit
   The overvoltage protection circuit (surge protector) turns off all outputs without Vdd, when VB voltage is more than about 21 V.
   And the overvoltage protection circuit (surge protector) turns off Vdd output with other all outputs, when VB voltage is more than about 26 V.
   The VB ≥ 18 V condition, the stand by current increases.

2. Overcurrent protection circuit
   FREG_B (pin 2), ILM OUT (pin 4), CD OUT (pin 6), DSP OUT (pin 7), AUDIO OUT (pin 10), EXT OUT (pin 12), VDD OUT (pin 14) output circuits are built-in overcurrent protection circuit, based on the respective output current.

3. Thermal protection circuit
   A built-in thermal protection circuit (TSD: Thermal Shut Down) prevents thermal damage to the IC.
   All outputs except VDD (pin 14) and FREG (pin 2, 3) are switched off when the circuit operates, revert to the original state when the temperature drops to a certain level.

4. FREG operation
   FREG function needs external PNP transistor, feedback resistor, stability capacitor. If the external transistor become saturation level, the base current depend on IC specification, that is FREG_B (pin 2) maximum current specification.

5. We recommend to mount a bypass diode in your application if there is a mode where potential difference between each output and VB (pin 8), VBUP (pin 15) or GND (pin 1) is reversed from the normal state.

6. **Header of IC (TAB) have to connect to GND.**
   For mounting the header of IC on the heat sink with the screw, heat sink have to connect to GND. When header of IC mount with heat sink with holding parts (use conductive material), holding parts have to connect to GND.
   At this time, the holding parts mount with heat sink with the screw, or it must connect to header of IC.
   If users have question or request, please contact the vendor.

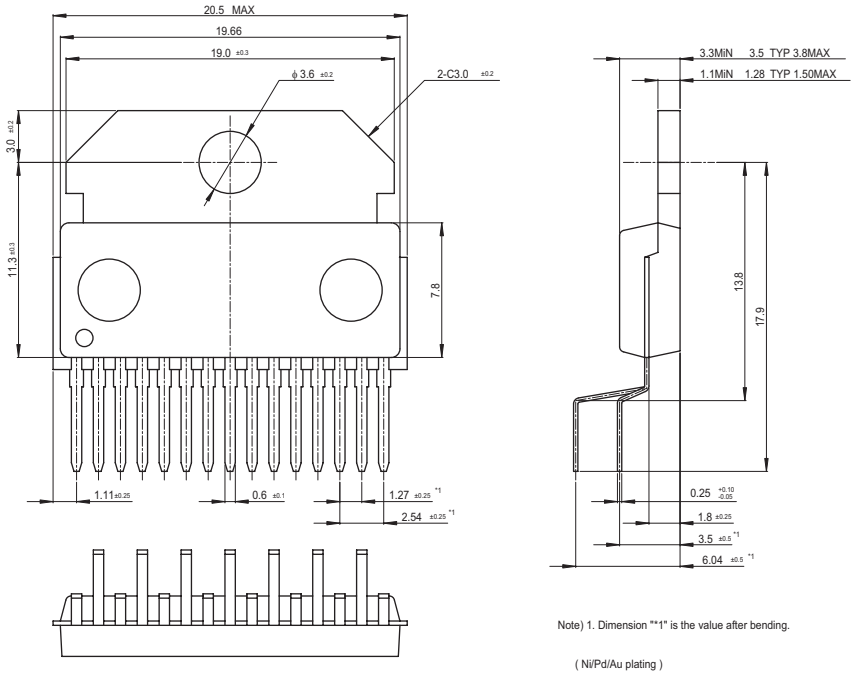
7. Soldering should be done within the soldering heat test standard of the IC, specifying that the lead wires, up to 1 to 1.5 mm off the IC body, are kept in solder at 260°C for 10 s and at 350°C for 3 s. Therefore give careful consideration in order to do not exceed the condition. In a soldering iron is used, use a soldering iron grounded and do not leak at the tip.

8. To keep stability regulation
   The stability capacitor should be no temperature dependability and no bias voltage dependability.
   ESR level should be bellow 10 W all temperature range.

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HSIP15-14.3x19.66-1.27	PRSS0015DA-C	SP-15TGV	3.0g

Unit : mm



Note) 1. Dimension "*1" is the value after bending.

(Ni/Pd/Au plating)

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Colophon .7.0