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R1LV0416D Series

4M SRAM (256-kword × 16-bit)

Description

The R1LV0416D is a 4-Mbit static RAM organized 256-kword × 16-bit, fabricated by Renesas's high-performance 0.15µm CMOS and TFT technologies. R1LV0416D Series has realized higher density, higher performance and low power consumption. The R1LV0416D Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. The R1LV0416D Series is packaged in a 44-pin thin small outline mount device, or a 48-ball fine pitch ball grid array.
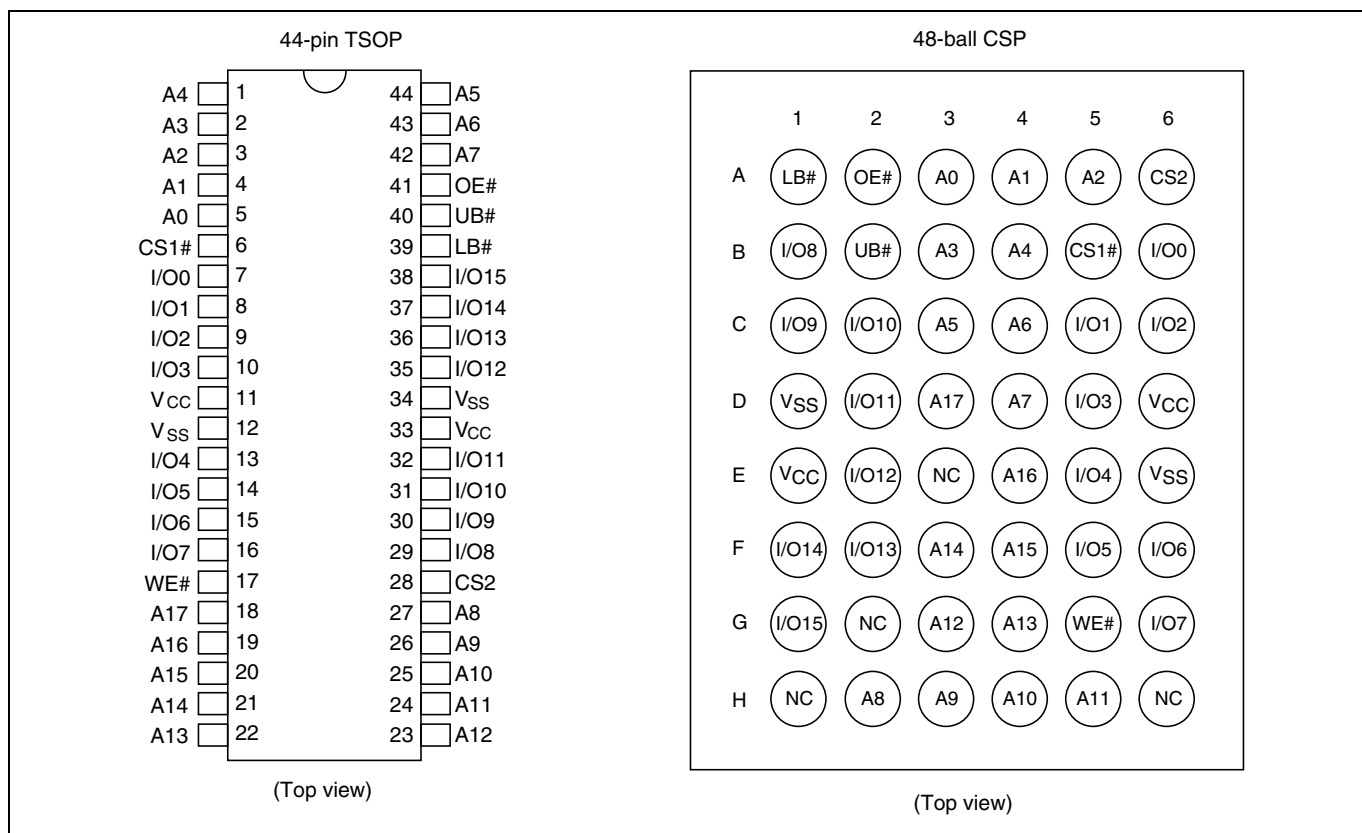
Features

- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 55/70 ns (max)
- Power dissipation:
  — Standby: 3 µW (typ) (V_{cc} = 3.0 V)
- Equal access and cycle times
- Common data input and output.
  — Three state output
- Battery backup operation.
  — 2 chip selection for battery backup
- Temperature Range: -40 to +85°C

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Ordering Information

Type No.	Access time	Package
R1LV0416DSB-5SI	55 ns	400-mil 44-pin plastic TSOP II
R1LV0416DSB-7LI	70 ns	PTSB0044GA-A (44P3W-H)
R1LV0416DBG-5SI	55 ns	48-ball CSP with 0.75 mm ball pitch
R1LV0416DBG-7LI	70 ns	PTBG0048HB-A (48FHH)

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Pin Arrangement

44-pin TSOP

A4	1		44	A5
A3	2		43	A6
A2	3		42	A7
A1	4		41	OE#
A0	5		40	UB#
CS1#	6		39	LB#
I/O0	7		38	I/O15
I/O1	8		37	I/O14
I/O2	9		36	I/O13
I/O3	10		35	I/O12
V_{CC}	11		34	V_{SS}
V_{SS}	12		33	V_{CC}
I/O4	13		32	I/O11
I/O5	14		31	I/O10
I/O6	15		30	I/O9
I/O7	16		29	I/O8
WE#	17		28	CS2
A17	18		27	A8
A16	19		26	A9
A15	20		25	A10
A14	21		24	A11
A13	22		23	A12

(Top view)

48-ball CSP

	1	2	3	4	5	6
A	LB#	OE#	A0	A1	A2	CS2
B	I/O8	UB#	A3	A4	CS1#	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	V_{SS}	I/O11	A17	A7	I/O3	V_{CC}
E	V_{CC}	I/O12	NC	A16	I/O4	V_{SS}
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	NC	A12	A13	WE#	I/O7
H	NC	A8	A9	A10	A11	NC

(Top view)

Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
CS1# ($\overline{CS1}$)	Chip select 1
CS2	Chip select 2
OE# ($\overline{OE}$)	Output enable
WE# ($\overline{WE}$)	Write enable
LB# ($\overline{LB}$)	Lower byte select
UB# ($\overline{UB}$)	Upper byte select
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram

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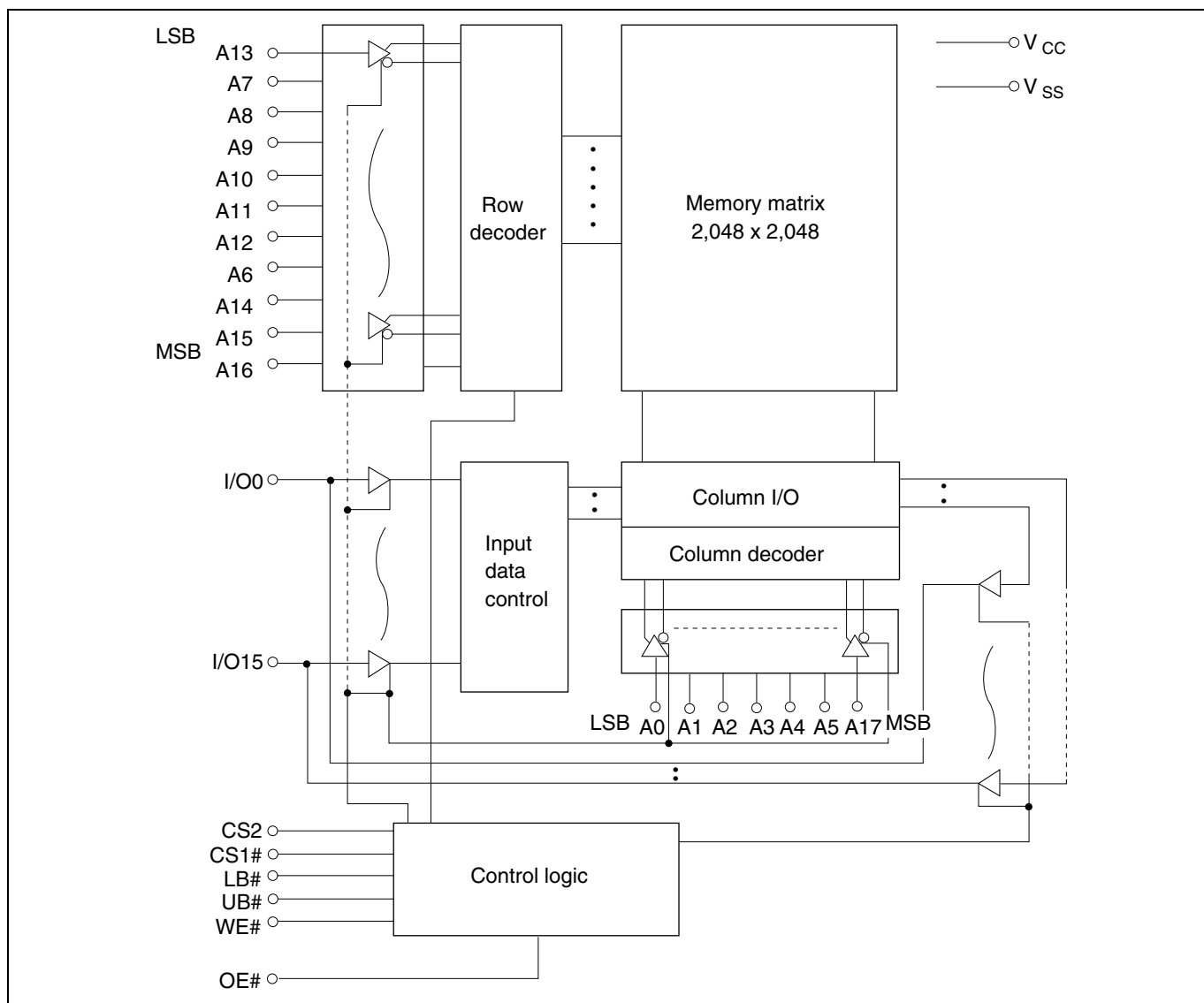
Operation Table

CS1#	CS2	WE#	OE#	UB#	LB#	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	×	High-Z	High-Z	Standby
×	L	×	×	×	×	High-Z	High-Z	Standby
×	×	×	×	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	×	L	L	Din	Din	Write
L	H	L	×	H	L	Din	High-Z	Lower byte write
L	H	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	H	×	×	High-Z	High-Z	Output disable

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{ss}	V_{cc}	−0.5 to +4.6	V
Terminal voltage on any pin relative to V_{ss}	V_T	−0.5*[1] to V_{cc} + 0.3*[2]	V
Power dissipation	P_T	0.7	W
Operating temperature1	Topr	−40 to +85	°C
Storage temperature range	Tstg	−65 to +150	°C
Storage temperature range under bias	Tbias	−40 to +85	°C

Notes: 1. V_T min: −3.0 V for pulse half-width ≤ 30 ns.
      2. Maximum voltage is +4.6 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{cc}	2.7	3.0	3.6	V	
	V_{ss}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	V_{cc} + 0.3	V	
Input low voltage	V_{IL}	−0.3	—	0.6	V	1
Ambient temperature range	Ta	−40	—	+85	°C	

Note: 1. V_{IL} min: −3.0 V for pulse half-width ≤ 30 ns.

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DC Characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current			$|I_{LI}|$	—	—	1	μA	Vin = V_{SS} to V_{CC}
Output leakage current			$|I_{LO}|$	—	—	1	μA	CS1# = V_{IH} or CS2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL} or LB# = UB# = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating current			I_{CC}	—	—	20	mA	CS1# = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Average operating current			I_{CC1}	—	—	25	mA	Min. cycle, duty = 100%, $I_{I/O}$ = 0 mA, CS1# = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}
			I_{CC2}	—	—	5	mA	Cycle time = 1 μs, duty = 100%, $I_{I/O}$ = 0 mA, CS1# ≤ 0.2 V, CS2 ≥ V_{CC} − 0.2 V V_{IH} ≥ V_{CC} − 0.2 V, V_{IL} ≤ 0.2 V
Standby current			I_{SB}	—	0.1*[1]	0.3	mA	CS2 = V_{IL}
Standby current	−5SI	to +85°C	I_{SB1}	—	—	10	μA	Vin ≥ 0 V
		to +70°C	I_{SB1}	—	—	8	μA	(1) 0 V ≤ CS2 ≤ 0.2 V or
		to +40°C	I_{SB1}	—	—	3	μA	(2) CS1# ≥ V_{CC} − 0.2 V,
		to +25°C	I_{SB1}	—	1*[1]	2.5	μA	CS2 ≥ V_{CC} − 0.2 V or
	−7LI	to +85°C	I_{SB1}	—	—	20	μA	(3) LB# = UB# ≥ V_{CC} − 0.2 V,
		to +70°C	I_{SB1}	—	—	16	μA	CS2 ≥ V_{CC} − 0.2 V,
		to +40°C	I_{SB1}	—	—	10	μA	CS1# ≤ 0.2 V
		to +25°C	I_{SB1}	—	1*[1]	10	μA	Average values
Output high voltage			V_{OH}	2.4	—	—	V	I_{OH} = −1 mA
			V_{OH2}	V_{CC} − 0.2	—	—	V	I_{OH} = −100 μA
Output low voltage			V_{OL}	—	—	0.4	V	I_{OL} = 2 mA
			V_{OL2}	—	—	0.2	V	I_{OL} = 100 μA

Note: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.

Capacitance

(Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	—	8	pF	Vin = 0 V	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics

(Ta = -40 to +85°C, V_{CC} = 2.7 V to 3.6 V)

Test Conditions

Input pulse levels: V_{IL} = 0.4 V, V_{IH} = 2.4 V

- Input rise and fall time: 5 ns
- Input/output timing reference levels: 1.4 V
- Output load: See figures (Including scope and jig)

Output load
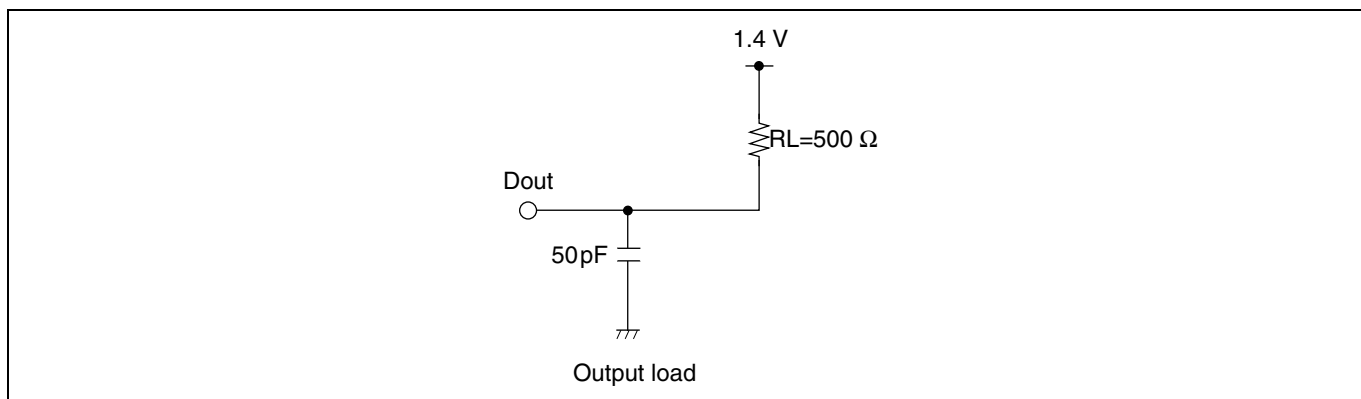
Read Cycle

Parameter	Symbol	R1LV0416D				Unit	Notes
		-5SI		-7LI			
		Min	Max	Min	Max		
Read cycle time	t_{RC}	55	—	70	—	ns	
Address access time	t_{AA}	—	55	—	70	ns	
Chip select access time	t_{ACS1}	—	55	—	70	ns	
	t_{ACS2}	—	55	—	70	ns	
Output enable to output valid	t_{OE}	—	35	—	40	ns	
Output hold from address change	t_{OH}	10	—	10	—	ns	
LB#, UB# access time	t_{BA}	—	55	—	70	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	10	—	ns	2, 3
	t_{CLZ2}	10	—	10	—	ns	2, 3
LB#, UB# disable to low-Z	t_{BLZ}	5	—	5	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	0	25	ns	1, 2, 3
	t_{CHZ2}	0	20	0	25	ns	1, 2, 3
LB#, UB# disable to high-Z	t_{BHZ}	0	20	0	25	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1, 2, 3

Write Cycle

Parameter	Symbol	R1LV0416D -5SI Min	-5SI Max	-7LI Min	-7LI Max	Unit	Notes
Write cycle time	t_{WC}	55	—	70	—	ns	
Address valid to end of write	t_{AW}	50	—	60	—	ns	
Chip selection to end of write	t_{CW}	50	—	60	—	ns	5
Write pulse width	t_{WP}	40	—	50	—	ns	4
LB#, UB# valid to end of write	t_{BW}	50	—	55	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	6
Write recovery time	t_{WR}	0	—	0	—	ns	7
Data to write time overlap	t_{DW}	25	—	30	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1, 2, 3
Write to output in high-Z	t_{WHZ}	0	20	0	25	ns	1, 2

Notes: 1. t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.

5. t_{CW} is measured from the later of CS1# going low or CS2 going high to the end of write.

6. t_{AS} is measured from the address valid to the beginning of write.

7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

Timing Waveform

Read Timing Waveform (WE# = V_{IH})
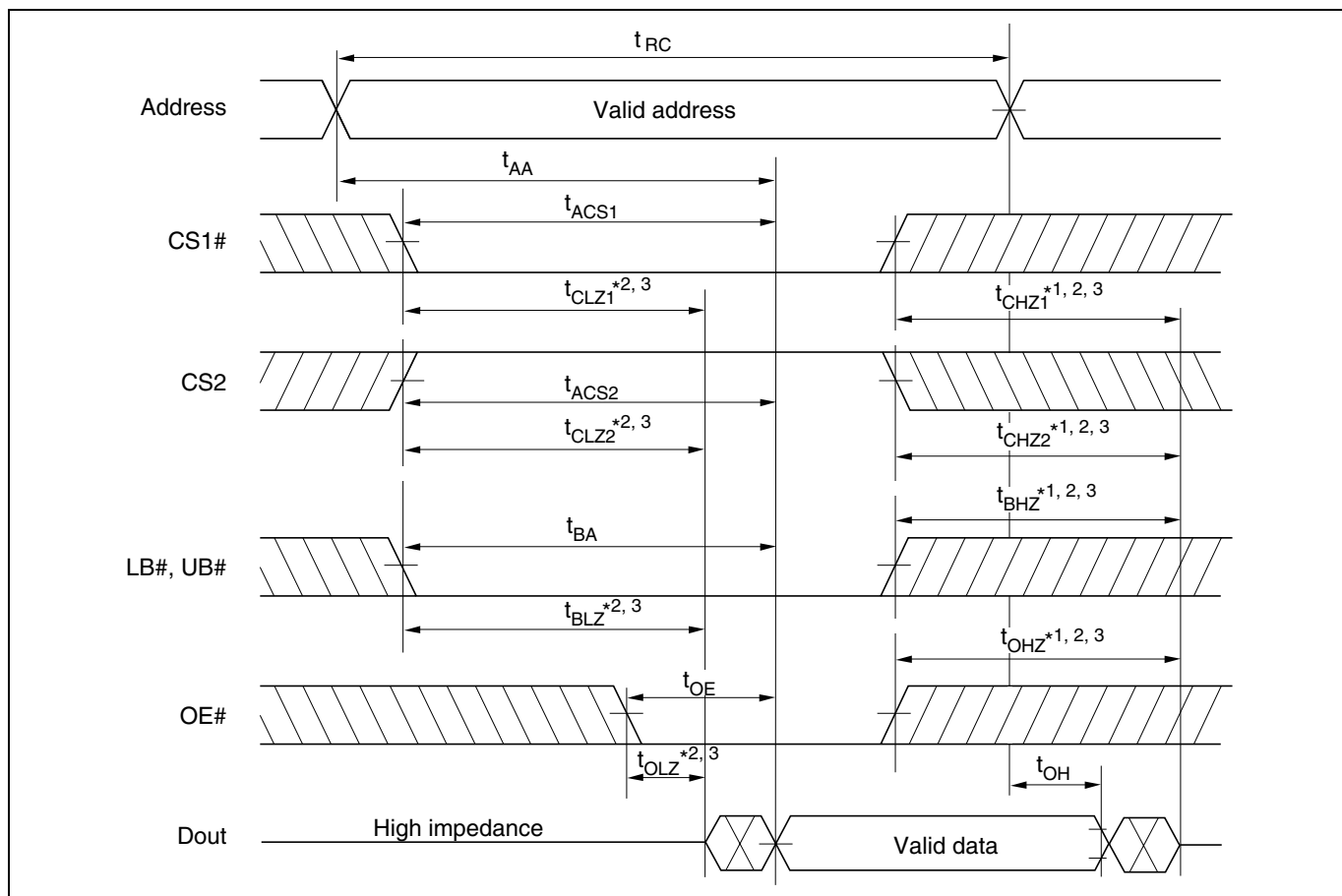
Write Timing Waveform (1) (WE# Clock)
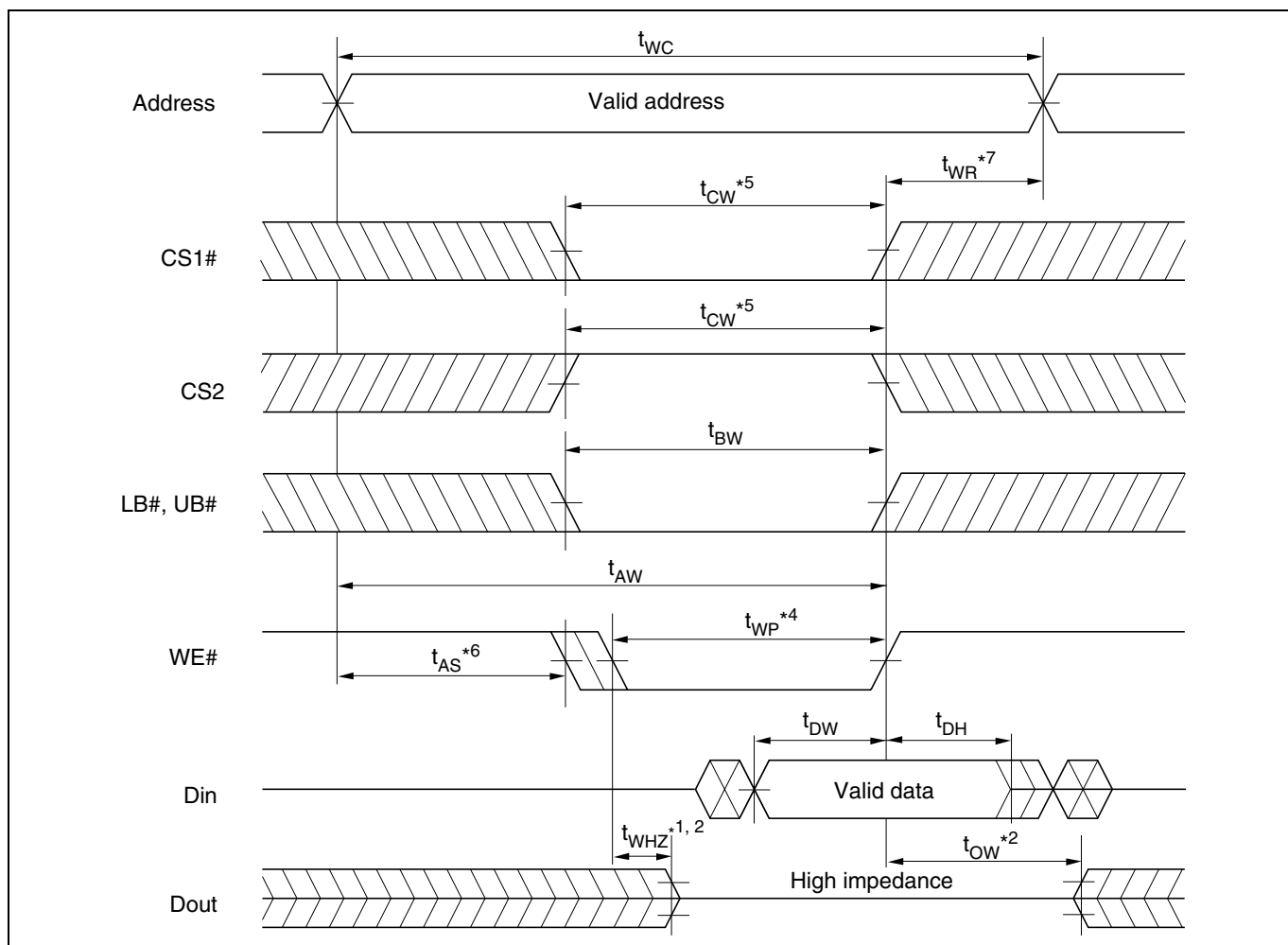
Write Timing Waveform (2) (CS# Clock, OE# = V$_{IH}$)
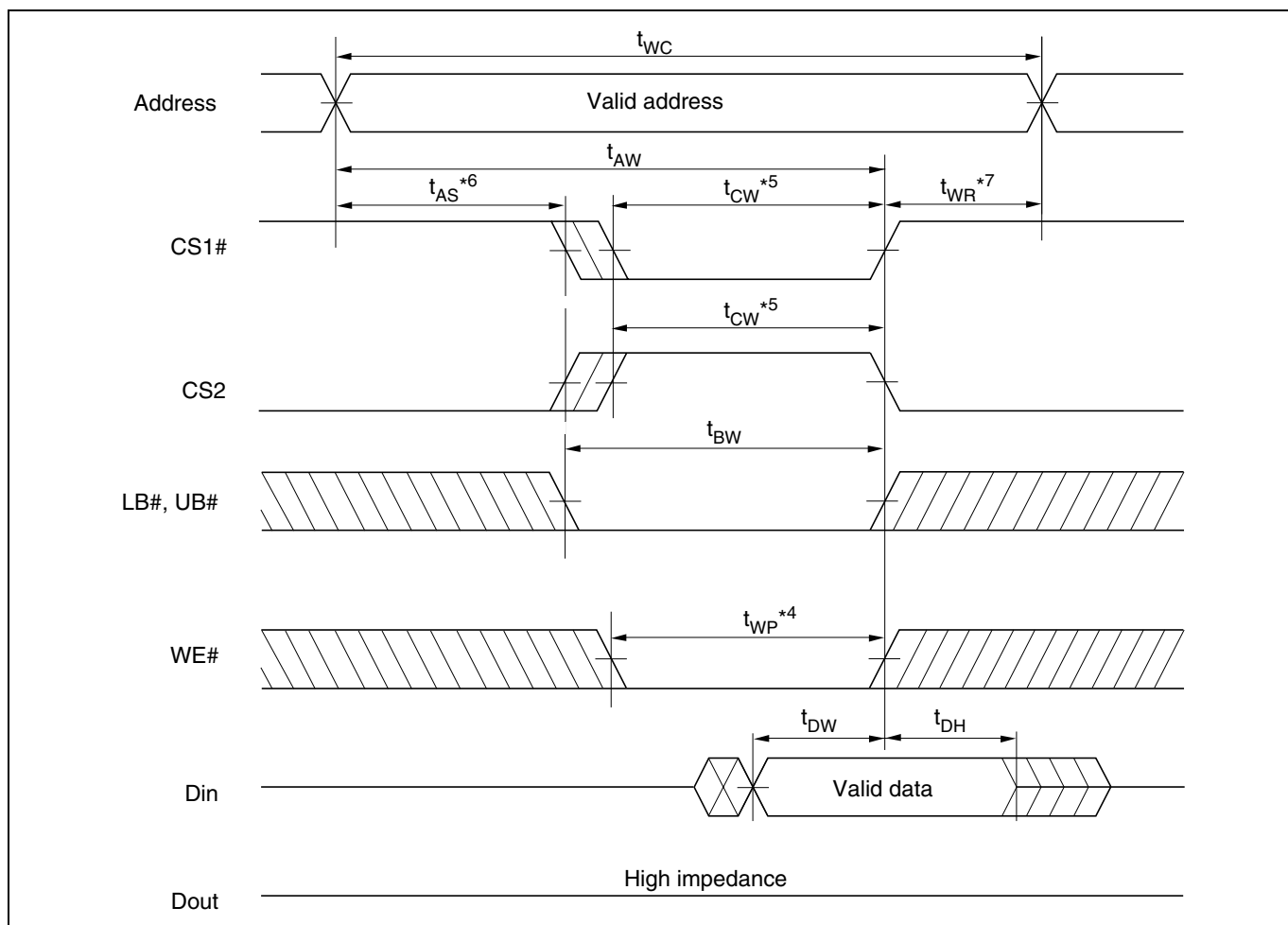
Write Timing Waveform (3) (LB#, UB# Clock, OE# = V$_{IH}$)
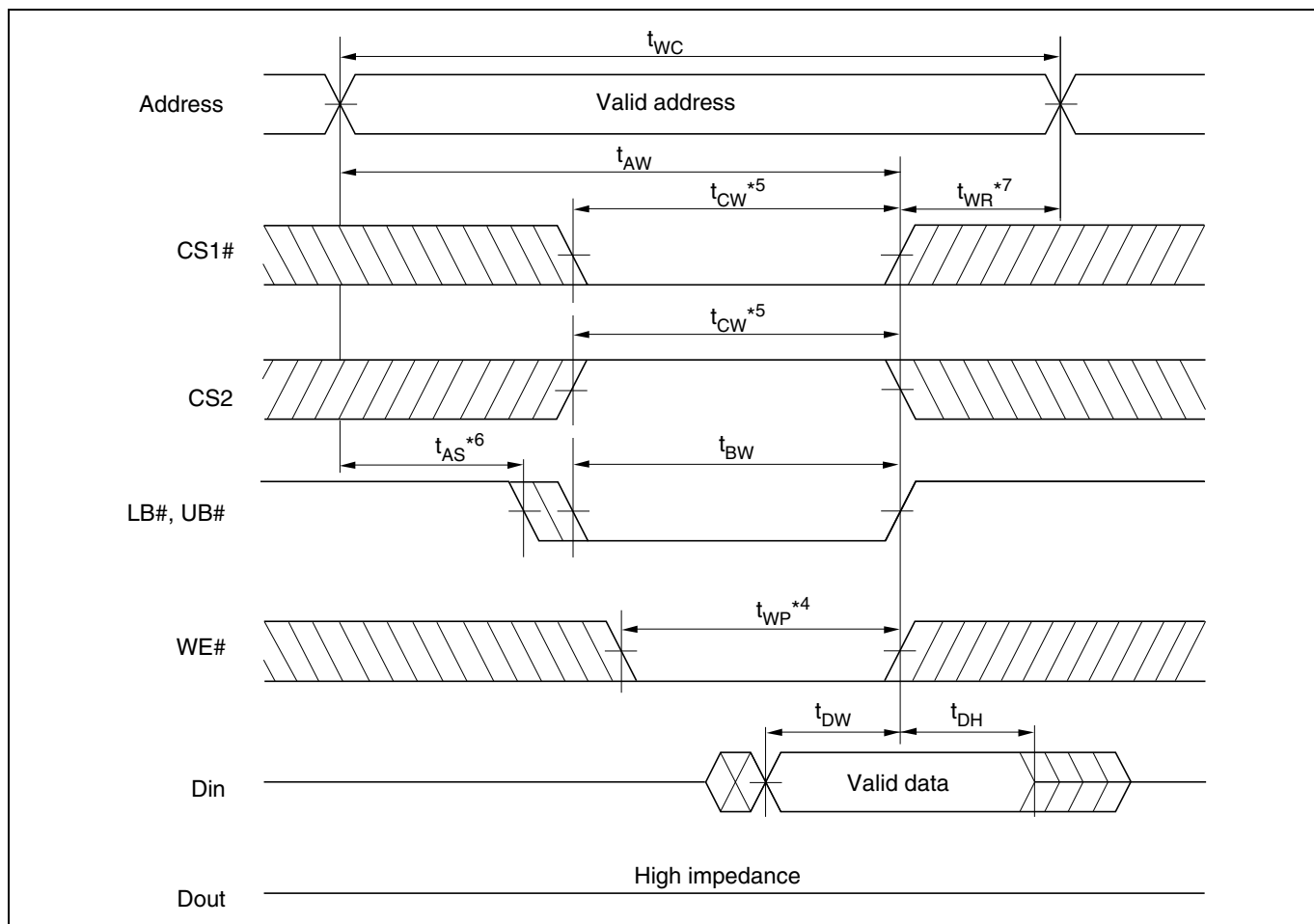
Low V$_{CC}$ Data Retention Characteristics

(Ta = -40 to +85°C)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
V$_{CC}$ for data retention			V$_{DR}$	2.0	—	—	V	Vin ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V$_{CC}$ – 0.2 V, 　　CS1# ≥ V$_{CC}$ – 0.2 V or (3) LB# = UB# ≥ V$_{CC}$ – 0.2 V, 　　CS2 ≥ V$_{CC}$ – 0.2 V, 　　CS1# ≤ 0.2 V
Data retention current	–5SI	to +85°C	I$_{CCDR}$	—	—	10	µA	V$_{CC}$ = 3.0 V, Vin ≥ 0V (1)　0 V ≤ CS2 ≤ 0.2 V or (2)　CS2 ≥ V$_{CC}$ – 0.2 V, 　　　CS1# ≥ V$_{CC}$ – 0.2 V or (3)　LB# = UB# ≥ V$_{CC}$ – 0.2 V, 　　　CS2 ≥ V$_{CC}$ – 0.2 V, 　　　CS1# ≤ 0.2 V Average values
		to +70°C	I$_{CCDR}$	—	—	8	µA	
		to +40°C	I$_{CCDR}$	—	—	3	µA	
		to +25°C	I$_{CCDR}$	—	1[*1]	2.5	µA	
	–7LI	to +85°C	I$_{CCDR}$	—	—	20	µA	
		to +70°C	I$_{CCDR}$	—	—	16	µA	
		to +40°C	I$_{CCDR}$	—	—	10	µA	
		to +25°C	I$_{CCDR}$	—	1[*1]	10	µA	
Chip deselect to data retention time			t$_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time			t$_{R}$	5	—	—	ms	

Note:　1.　Typical values are at V$_{CC}$ = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.

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Low V$_{CC}$ Data Retention Timing Waveform (1) (CS1# Controlled)
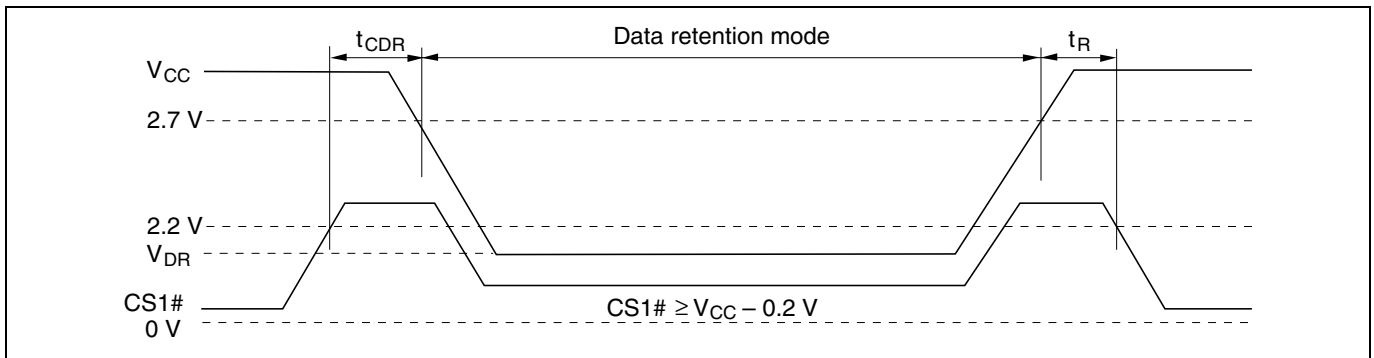
Low V$_{CC}$ Data Retention Timing Waveform (2) (CS2 Controlled)
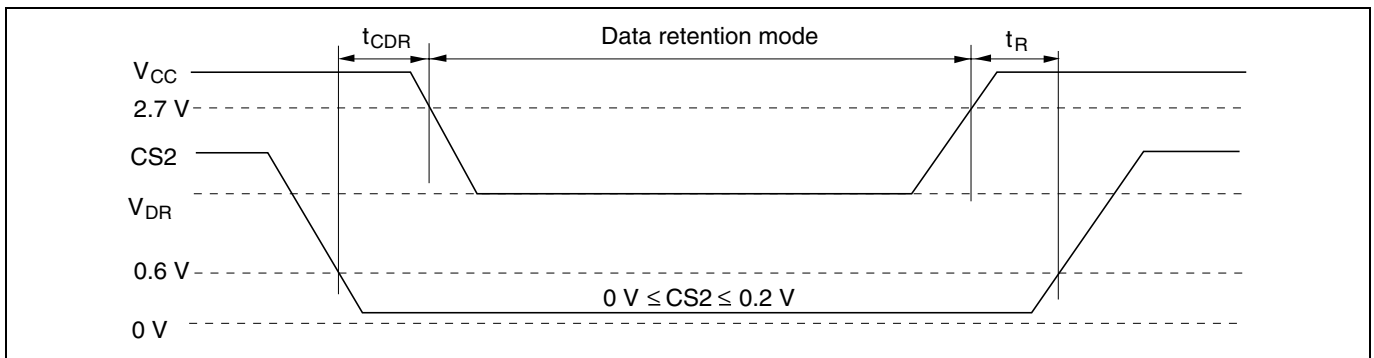
Low V$_{CC}$ Data Retention Timing Waveform (3) (LB#, UB# Controlled)
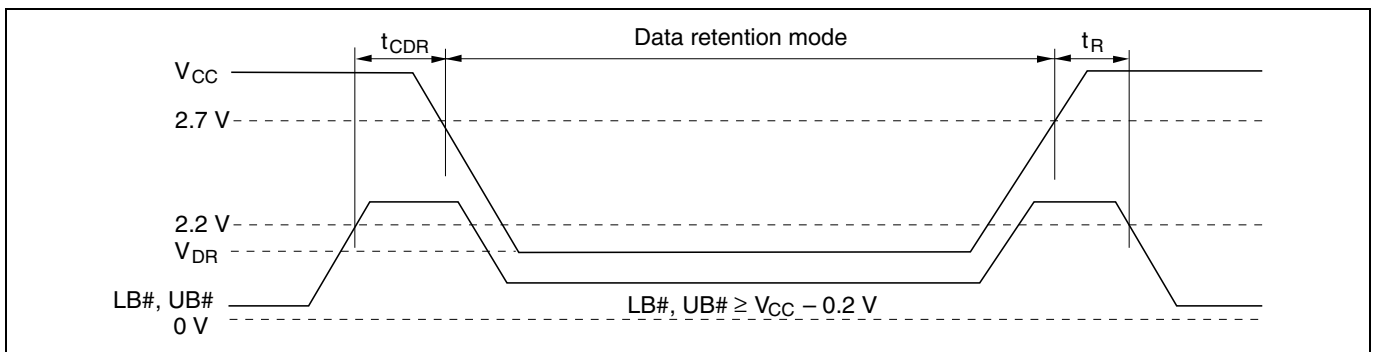
Rev.	Date	Contents of Modification	
		Page	**Description**
0.01	Dec. 25, 2006	—	Initial issue
1.00	May. 24, 2007	2	Ordering Information
			R1LV0416DSB-5S% to R1LV0416DSB-5SI
			R1LV0416DSB-7L% to R1LV0416DSB-7LI
			R1LV0416DBG-5S% to R1LV0416DBG-5SI
			R1LV0416DBG-7L% to R1LV0416DBG-7LI
		3	Pin Arrangement
			A6 to A13, A13 to A6
		4	Change of Block Diagram
		5	Absolute Maximum Ratings: Deletion of R ver. specification
		5	DC Operating Conditions: Deletion of R ver. specification
		6	DC Characteristics
			I_{SB1} (-5SI) (to +25°C) max: 3 µA to 2.5 µA
		7	AC Characteristics: Change of Test Conditions
		14	Low V_{CC} Data Retention Characteristics
			I_{CCDR} (-5SI) (to +25°C) max: 3 µA to 2.5 µA
			Deletion of note 2

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