To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HD74LS273 ●Octal D-type Positive-edge-triggered Flip-Flops (with Clear)

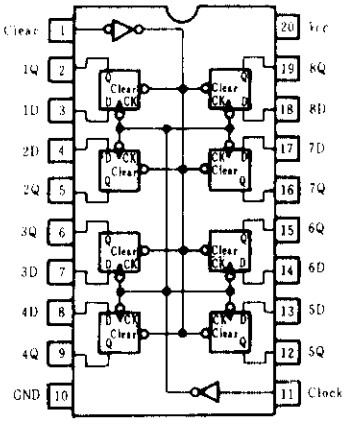
The HD74LS273, positive-edge-triggered flip-flops utilize LS TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse.

Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse.

When the clock input is at either the high or low level, the D input signal has no effect at the output.

■PIN ARRANGEMENT



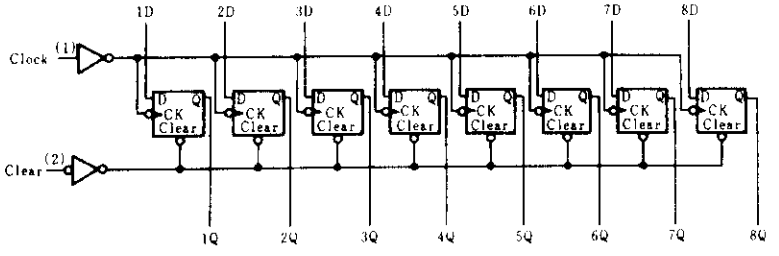
(Top View)

■FUNCTION TABLE

Inputs			Output
Clear	Clock	D	Q
L	×	×	L
H	↑	H	H
H	↑	L	L
H	L	×	Q_0

Notes; H = high level, L = low level,
X = irrelevant
↑ = transition from low to high level
Q_0 = level of Q before the indicated steady-state input conditions were established.

■BLOCK DIAGRAM



■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	−400	μA
		I_{OL}	—	—	8	mA
Clock frequency		f_{clock}	0	—	30	MHz
Clock and clear pulse width		t_W	20	—	—	ns
Setup time	Data	t_{su}	20 ↑	—	—	ns
	Clear inactive-state		25 ↑	—	—	
Data hold time		t_h	5 ↑	—	—	ns

Note) ↑ : The arrow indicates the rising edge of clock pulse.

■ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	—		V
	V_{IL}			—	—	0.8	V
Output voltage	V_{OH}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=−400μA		2.7	—		V
	V_{OL}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V	I_{OL}=8mA	—	—	0.5	V
			I_{OL}=4mA	—	—	0.4	
Input current	I_I	V_{CC}=5.25V, V_I=7V		—	—	0.1	mA
	I_{IH}	V_{CC}=5.25V, V_I=2.7V		—	—	20	μA
	I_{IL}	V_{CC}=5.25V, V_I=0.4V		—	—	−0.4	mA
Short-circuit output current	I_{OS}	V_{CC}=5.25V		−20	—	−100	mA
Supply current	I_{CC}**	V_{CC}=5.25V		—	17	27	mA
Input clamp voltage	V_{IK}	V_{CC}=4.75V, I_{IN}=−18mA		—	—	−1.5	V

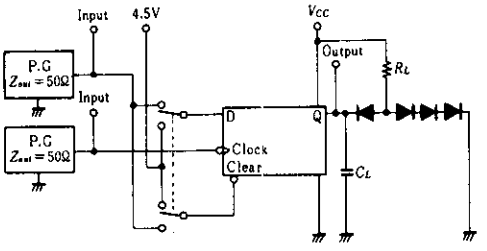
* V_{CC}=5V, Ta=25°C

** : With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C)

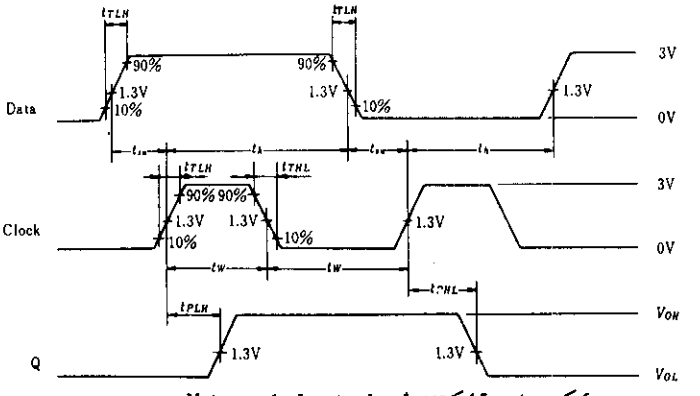
Item	Symbol	Inputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}	Clock	C_L=15pF, R_L=2kΩ	30	—	—	MHz
Propagation Delay Time	t_{PHL}	Clear		—	18	27	ns
	t_{PLH}	Clock		—	17	27	
	t_{PHL}			—	18	27	

■TESTING METHOD



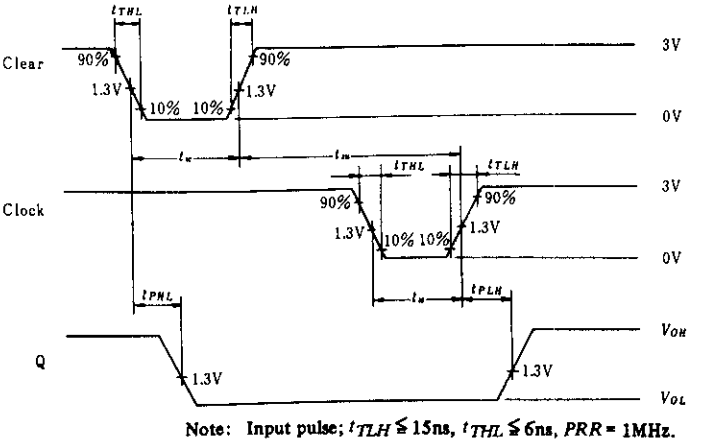
Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

Waveform-1



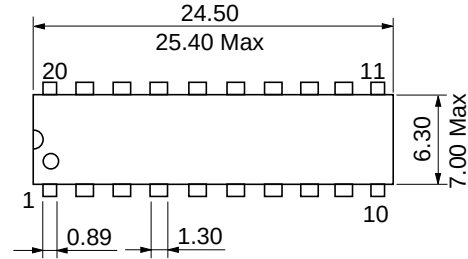
Notes: 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{TLH} \leqq 6$ns
Clock input; PRR = 1MHz, duty cycle 50%
Data input; PRR = 500kHz, duty cycle 50%

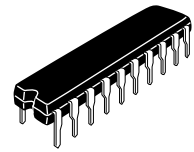
Waveform-2



Note: Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, PRR = 1MHz.

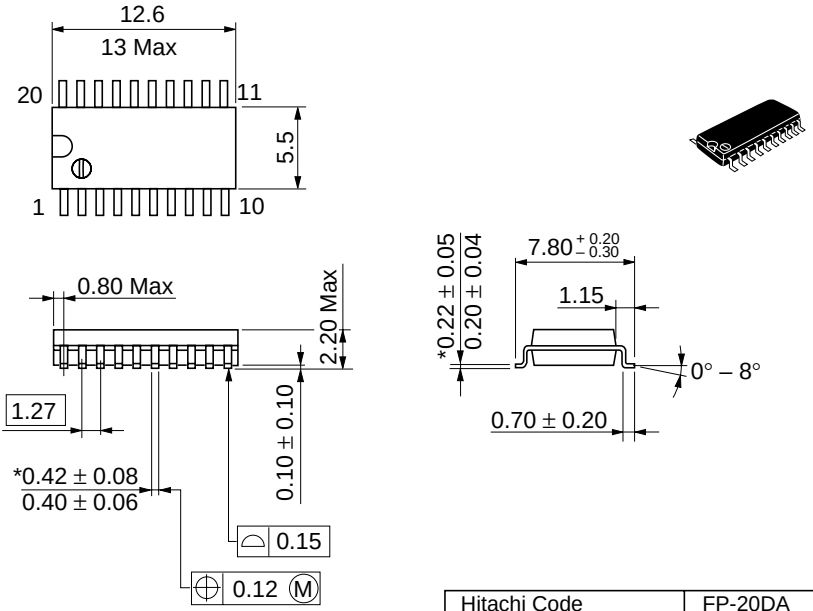
Unit: mm





Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g

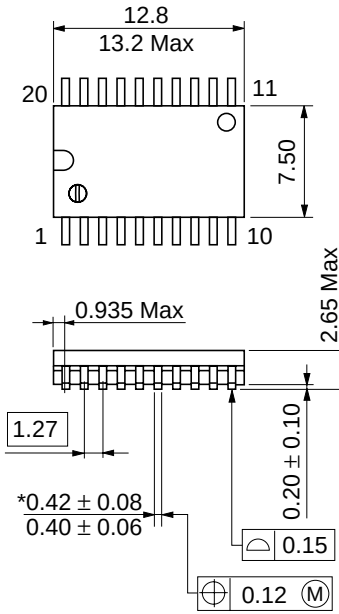
Unit: mm

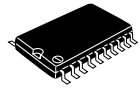


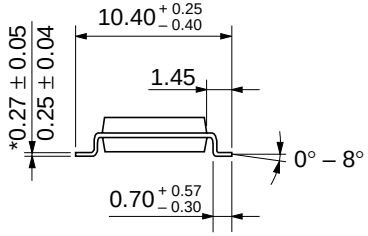
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

Unit: mm







*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

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