38C5 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0028-0110Z
Rev.1.10
Jun 14, 2004

DESCRIPTION

The 38C5 group is the 8-bit microcomputer based on the 740 family core technology.
The 38C5 group has an LCD drive control circuit, an A/D converter, and a serial I/O as additional functions.
The various microcomputers in the 38C5 group include variations of internal memory type, memory size, and packaging. For details, refer to the section on part numbering.

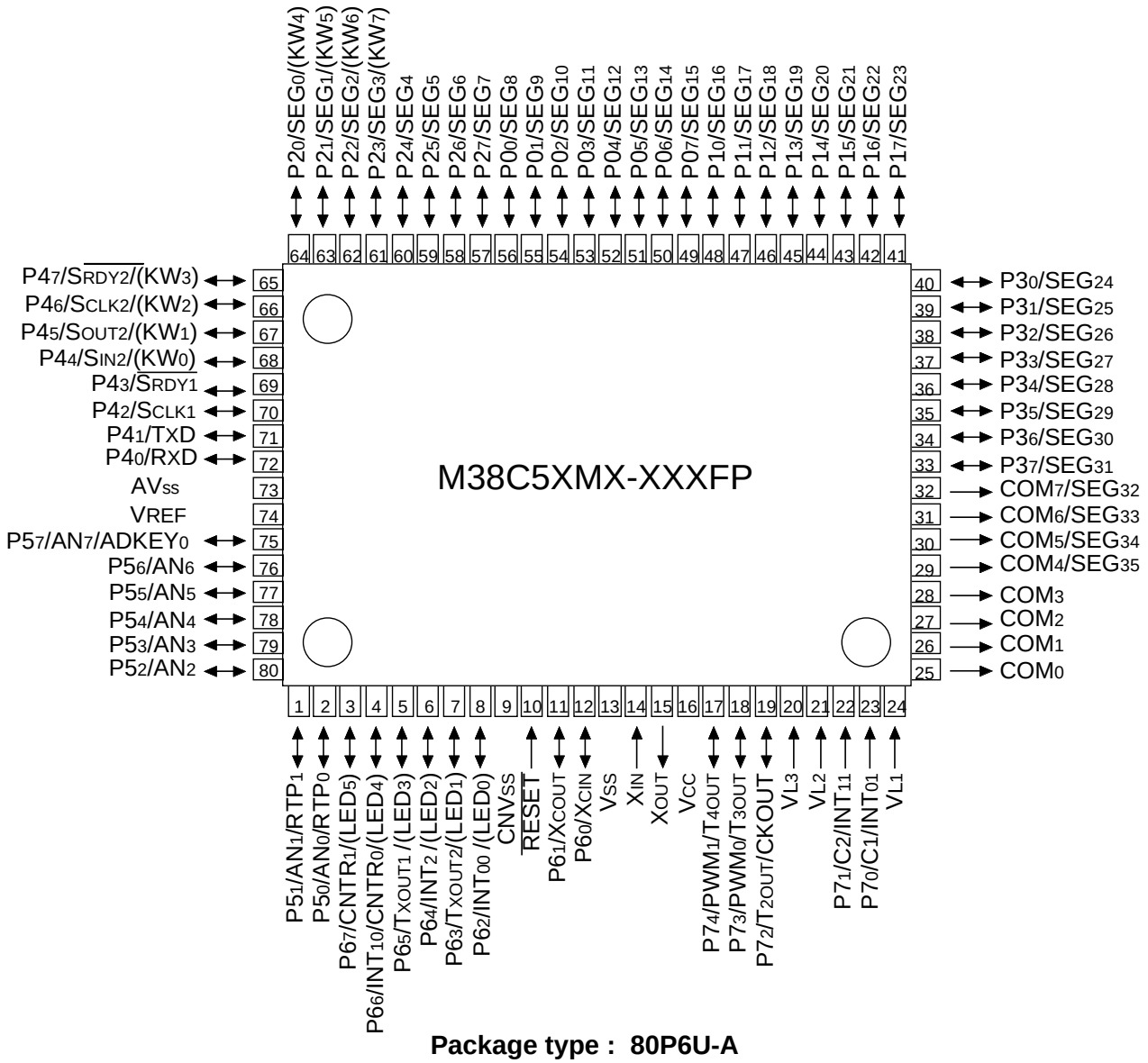
FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.32 µs
  (at 12.5 MHz oscillation frequency)
- Memory size
  ROM ..... 32 K to 60 K bytes
  RAM ..... 1536 to 2048 bytes
- Programmable input/output ports ..... 59 (common to SEG: 36)
- Interrupts ..... 17 sources, 16 vectors
  (Key input interrupt included)
- Timers ..... 8-bit × 4, 16-bit × 2
- Serial I/O1 ..... 8-bit × 1 (UART or Clock-synchronized)
- Serial I/O2 ..... 8-bit × 1 (Clock-synchronized)
- PWM ..... 10-bit × 2, 16-bit × 1 (common to IGBT output)
- A/D converter ..... 10-bit × 8 channels
  (A/D converter can be operated in low-speed mode.)
- Watchdog timer ..... 8-bit × 1
- LED direct drive port 6
  (average current: 15 mA, peak current: 30 mA, total current: 90 mA)
- LCD drive control circuit
  Bias 1/2, 1/3
  Duty ..... Static, 1/2, 1/3, 1/4, 1/8
  Common output 4/8
  Segment output 32/36
- Main clock generating circuit 1
  (connect to external ceramic resonator or on-chip oscillator)
- Sub-clock generating circuit 1
  (connect to external quartz-crystal oscillator)
- Power source voltage
  In high-speed mode (f(X_{IN}) = 12.5 MHz) ..... 4.5 to 5.5 V
  In high-speed mode (f(X_{IN}) = 8.0 MHz) ..... 4.0 to 5.5 V
  In middle-speedmode (f(X_{IN}) = 6.0 MHz) ..... 1.8 to 5.5 V
  In low-speed mode ..... 1.8 to 5.5 V
- Power dissipation (Mask ROM version)
  • In high-speed mode ..... Typ. 32 mW
  (V_{CC} = 5 V, f(X_{IN}) = 12.5 MHz, Ta = 25°C)
  • In low-speed mode ..... Typ. 18 µW
  (V_{CC} = 2.5 V, f(X_{IN}) = stop, f(X_{CIN}) = 32 kHz, Ta = 25°C)
- Operating temperature range ..... – 20 to 85°C

APPLICATION

Household products, Consumer electronics, etc.

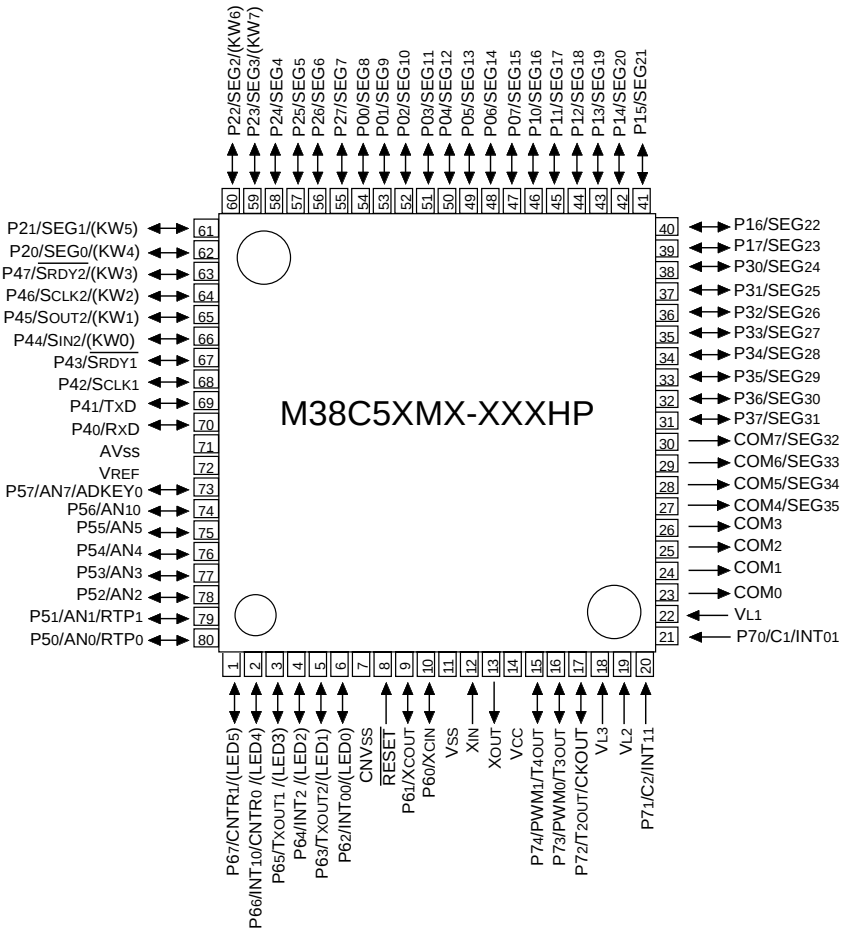
PIN CONFIGURATION (TOP VIEW)



Package type : 80P6U-A

Fig. 1 M38C5XMX-XXXFP pin configuration

PIN CONFIGURATION (TOP VIEW)



Package type : 80P6Q-A

Fig. 2 M38C5XMX-XXXHP pin configuration

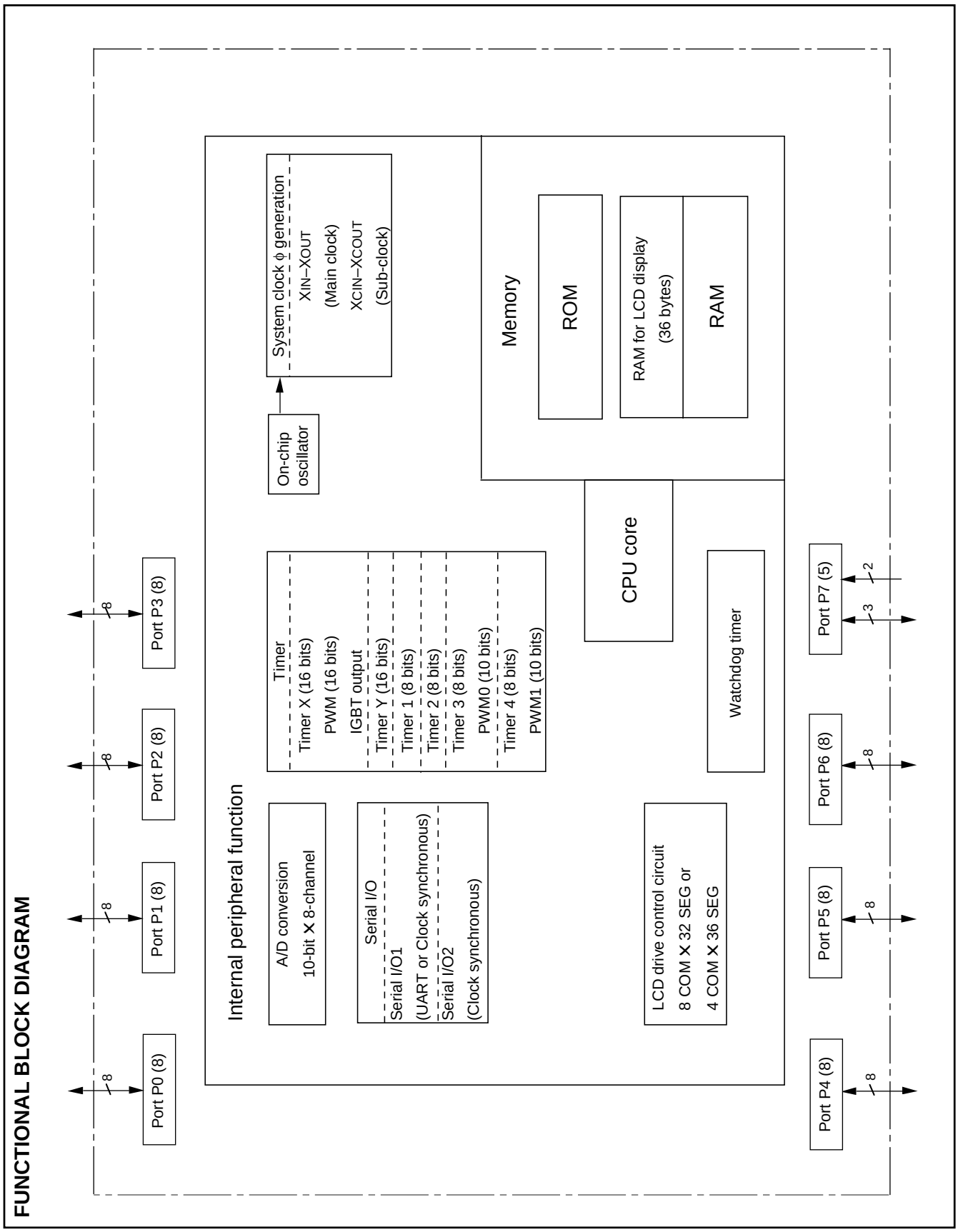


Fig. 3 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description (1)

Pin	Name	Function	Function except a port function
V_{CC}, V_{SS}	Power source	• Apply power source voltage to V_{CC}, and 0 V to V_{SS}.	
$\overline{RESET}$	Reset input	• Reset input pin for active "L."	
X_{IN}	Clock input	• Input and output pins for the main clock generating circuit. • Connect a ceramic resonator or a quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. When an external clock is used, connect the clock source to X_{IN}, and leave X_{OUT} pin open. • Feedback resistor is built in between X_{IN} pin and X_{OUT} pin.	
X_{OUT}	Clock output		
V_{L1}, V_{L2}, V_{L3}	LCD power source	• Input 0 ≤ V_{L1} ≤ V_{L2} ≤ V_{L3} ≤ V_{CC} voltage. • Input 0 – V_{L3} voltage to LCD.	
COM_0 – COM_3	Common output	• LCD common output pins. • COM_2 and COM_3 are not used at 1/2 duty ratio. • COM_3 is not used at 1/3 duty ratio.	
COM_4/SEG_{35} – COM_7/SEG_{32}	Common output Segment output	• LCD common/segment output pins.	
$P0_0/SEG_8$ – $P0_7/SEG_{15}$	I/O port P0	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled in a bit unit.	
$P1_0/SEG_{16}$ – $P1_7/SEG_{23}$	I/O port P1	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each 4-bit pin to be programmed as either input or output. • Pull-up control is enabled in 4-bit unit.	
$P2_0/SEG_0/(KW_4)$– $P2_3/SEG_3/(KW_7)$	I/O port P2	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled in a bit unit.	• Key input interrupt input pins
$P2_4/SEG_4$ – $P2_7/SEG_7$			
$P3_0/SEG_{24}$ – $P3_7/SEG_{31}$	I/O port P3	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each 4-bit pin to be programmed as either input or output. • Pull-up control is enabled in a bit unit.	
$P4_0/RxD$ $P4_1/TxD$ $P4_2/SCLK_1$ $P4_3/\overline{SRDY_1}$	I/O port P4	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each 4-bit pin to be programmed as either input or output. • Pull-up control is enabled in a bit unit.	• Serial I/O1 function pins
$P4_4/SIN_2/(KW_0)$, $P4_5/SOUT_2/(KW_1)$, $P4_6/SCLK_2/(KW_2)$, $P4_7/\overline{SRDY_2}/(KW_3)$,			• Serial I/O2 function pins • Key input interrupt input pins

PIN DESCRIPTION

Table 2 Pin description (2)

Pin	Name	Function	Function except a port function	
P5$_0$/AN$_0$/RTP$_0$, P5$_1$/AN$_1$/RTP$_1$	I/O port P5	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled in a bit unit.	• AD converter input pins	• Real time port function pins
P5$_2$/AN$_2$ – P5$_6$/AN$_6$				
P5$_7$/AN$_7$/ADKEY$_0$				• ADKEY input pin
P6$_0$/XCIN, P6$_1$/XCOUT	I/O port P6	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled in a bit unit. • P6$_2$ to P6$_7$ (6 bits) are enabled to output large current for LED drive.	• Sub clock generating I/O pins (oscillator connected)	
P6$_2$/INT$_{00}$/(LED$_0$),			• External interrupt pin	
P6$_3$/TXOUT2/(LED$_1$),			• Timer X output pin	
P6$_4$/INT$_2$/(LED$_2$)			• External interrupt pin	
P6$_5$/TXOUT1/(LED$_3$)			• Timer X output pin	
P6$_6$/INT$_{10}$/CNTR$_0$/(LED$_4$), P6$_7$/CNTR$_1$/(LED$_5$)			• Timer X, Timer Y output pins	• External interrupt pins
P7$_0$/C$_1$/INT$_{01}$, P7$_1$/C$_2$/INT$_{11}$	Input port P7	• 2-bit input port. • CMOS input level.	• External interrupt pins	• External capacitor connect pins for a voltage multiplier of LCD.
P7$_2$/T$_{2OUT}$/CKOUT	I/O port P7	• 3-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Clock output pin	• Timer 2 output pin
P7$_3$/PWM$_0$/T$_{3OUT}$, P7$_4$/PWM$_1$/T$_{4OUT}$			• PWM output pins	• Timer 3 output pin • Timer 4 output pin
CNVSS	CNVSS	• Connect to VSS.		
VREF	Analog reference voltage	• Reference voltage input pin for A/D converter.		
AVSS	Analog power source	• GND input pin for A/D converter. Connect to VSS.		

PART NUMBERING

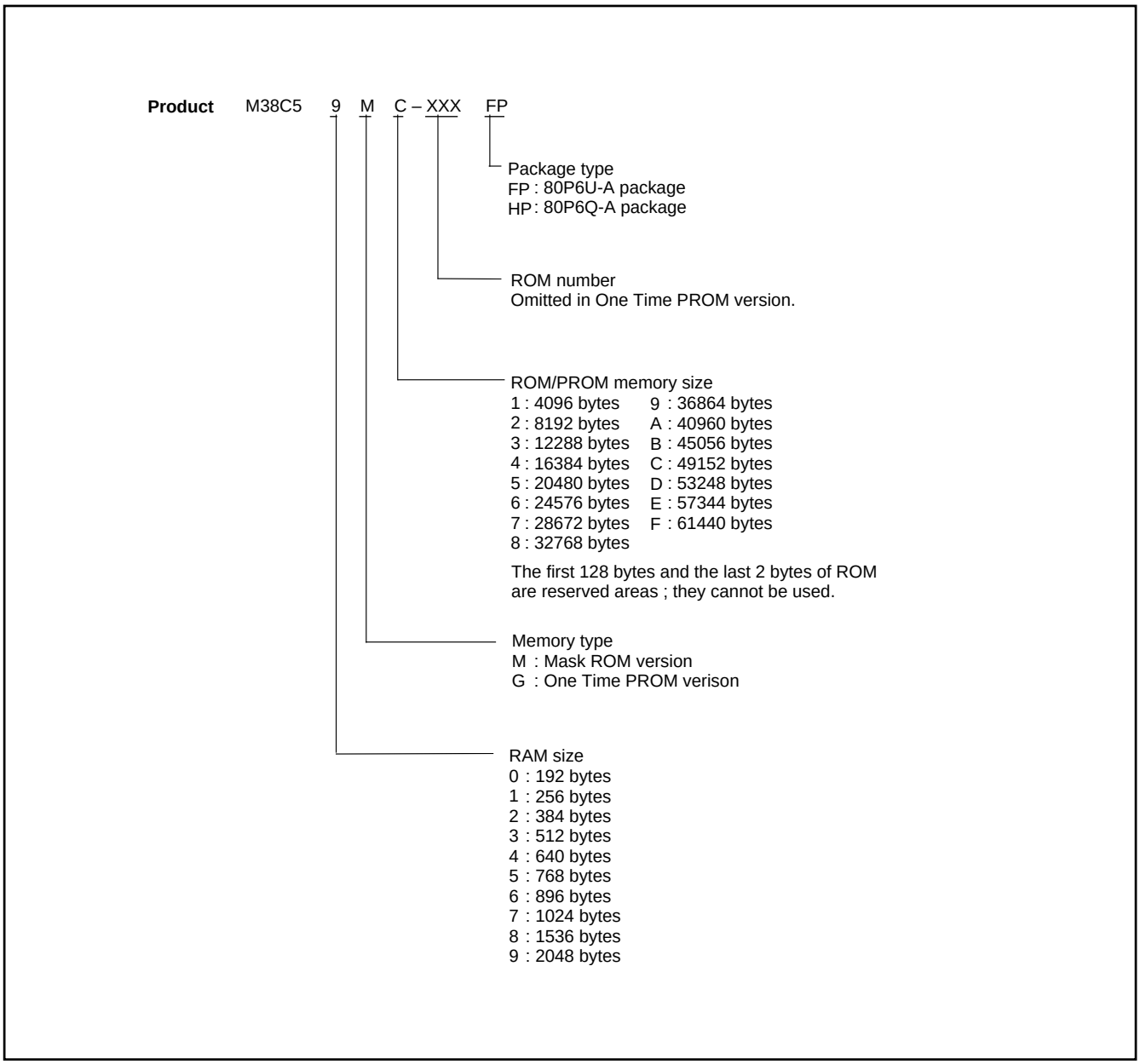


Fig. 4 Part numbering

GROUP EXPANSION

Renesas plans to expand the 38C5 group as follows.

Memory Type

Support for mask ROM, One Time PROM versions

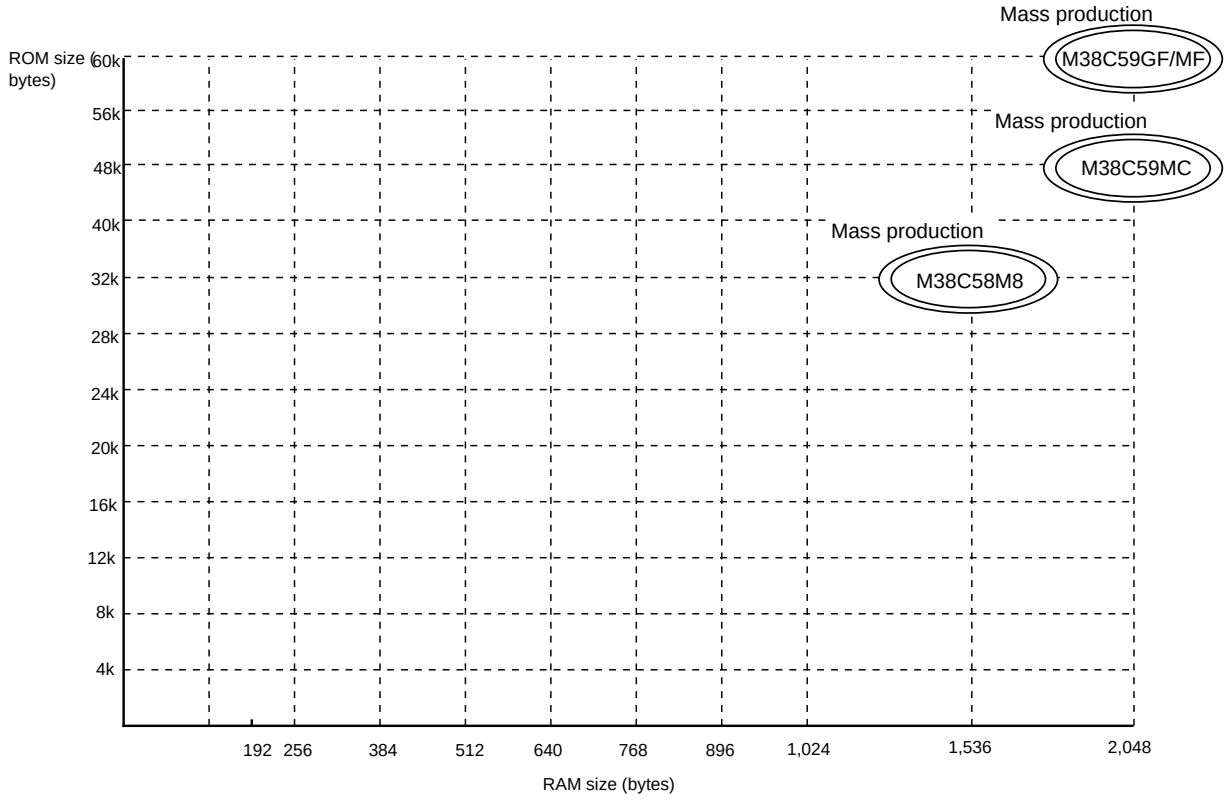
Memory Size

ROM size ..... 32 K to 60 K bytes
One Time PROM size ..... 60 K bytes
RAM size ..... 640 to 2048 bytes

Packages

80P6Q-A ..... 0.5 mm-pitch plastic molded QFP
80P6U-A ..... 0.8 mm-pitch plastic molded QFP

Memory Expansion Plan



Products under development or planning : the development schedule and specification may be revised without notice.

Fig. 5 Memory expansion plan

Currently supported products are listed below.

Table 3 Support products As of June. 2004

Part number	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38C58M8-XXXFP	32768 (32638)	1536	80P6U-A	Mask ROM version
M38C58M8-XXXHP			80P6Q-A	Mask ROM version
M38C59MC-XXXFP	49152 (49022)	2048	80P6U-A	Mask ROM version
M38C59MC-XXXHP			80P6Q-A	Mask ROM version
M38C59MF-XXXFP	61440 (61310)	2048	80P6U-A	Mask ROM version
M38C59MF-XXXHP			80P6Q-A	Mask ROM version
M38C59GFFP	61440 (61310)	2048	80P6U-A	One Time PROM version
M38C59GFHP			80P6Q-A	One Time PROM version

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The 38C5 group uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

The central processing unit (CPU) has six registers. Figure 6 shows the 740 Family CPU register structure.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as arithmetic data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 7.

Table 4 shows the push and pop instructions of accumulator or processor status register.

Store registers other than those described in Figure 7 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

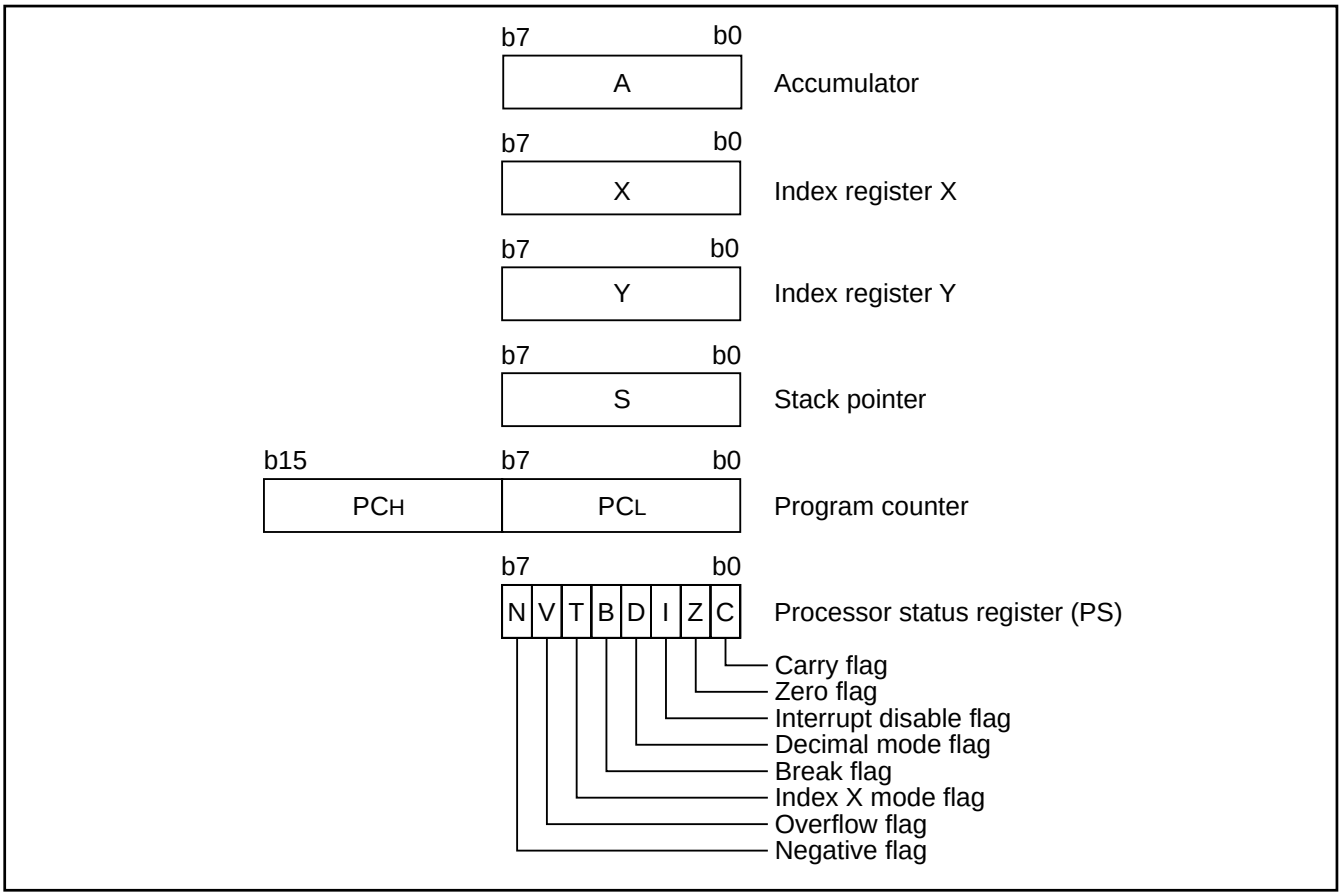


Fig. 6 740 Family CPU register structure

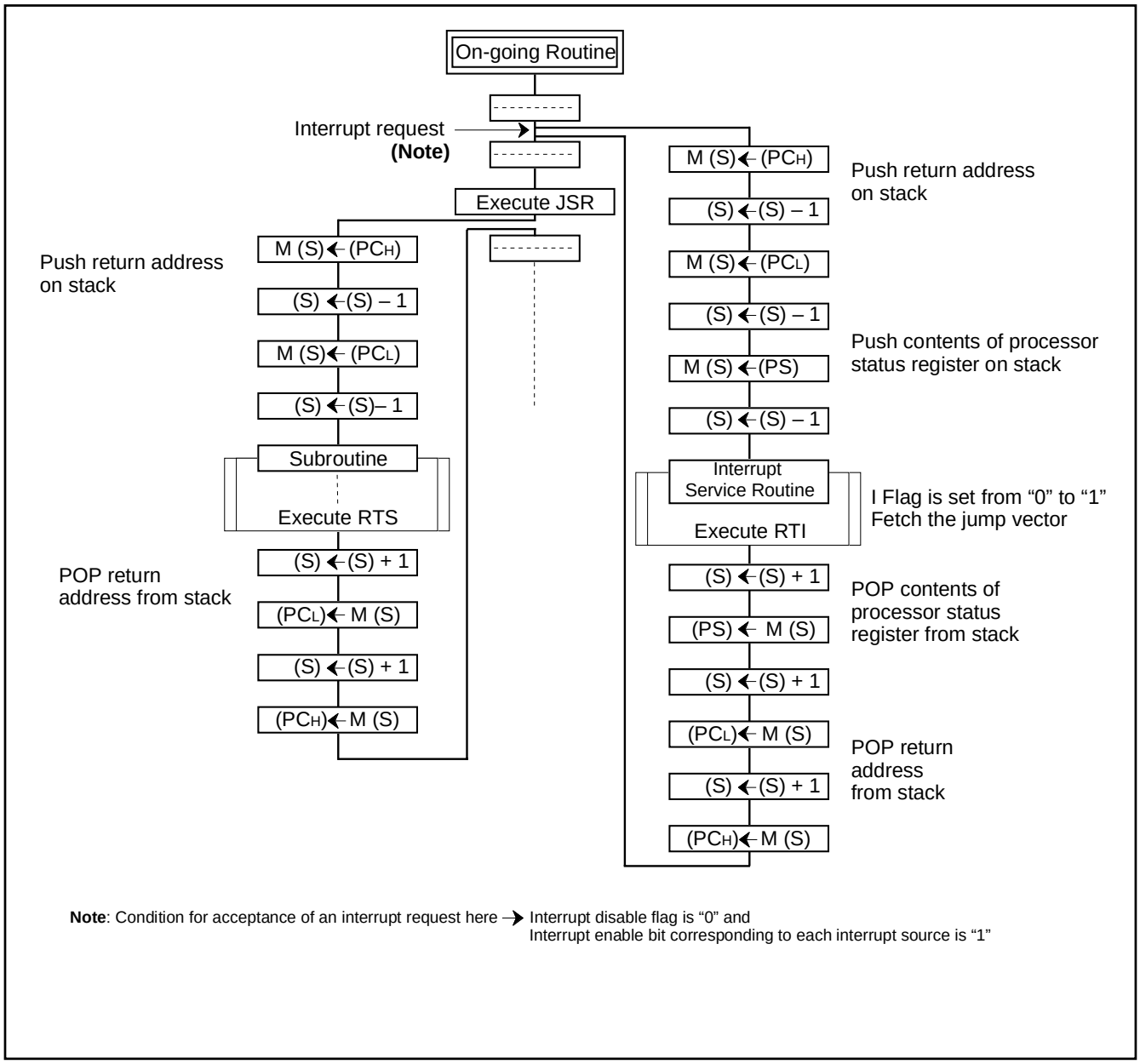


Fig. 7 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor Status Register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

- Bit 0: Carry flag (C)
  The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.
- Bit 1: Zero flag (Z)
  The Z flag is set to “1” if the result of an immediate arithmetic operation or a data transfer is “0”, and set to “0” if the result is anything other than “0”.
- Bit 2: Interrupt disable flag (I)
  The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
  Interrupts are disabled when the I flag is “1”.
- Bit 3: Decimal mode flag (D)
  The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”.
  Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.
- Bit 4: Break flag (B)
  The B flag is used to indicate that the current interrupt was generated by the BRK instruction. When the BRK instruction is generated, the B flag is set to “1” automatically. When the other interrupts are generated, the B flag is set to “0”, and the processor status register is pushed onto the stack.
- Bit 5: Index X mode flag (T)
  When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.
- Bit 6: Overflow flag (V)
  The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.
- Bit 7: Negative flag (N)
  The N flag is set to “1” if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit and the control bit for the internal system clock etc.

The CPU mode register is allocated at address 003B16.

After system is released from reset, the on-chip oscillator mode is selected, and the XIN–XOUT oscillation and the XCIN–XCOUT oscillation are stopped.

When the low-, middle- or high-speed mode is used after the XIN–XOUT oscillation and the XCIN–XCOUT oscillation are enabled, wait in the on-chip oscillator mode etc. until oscillation stabilizes, and then, switch the operation mode.

When the middle- and high-speed mode are not used (XIN–XOUT oscillation and external clock input are not performed), connect XIN to VCC through a resistor.

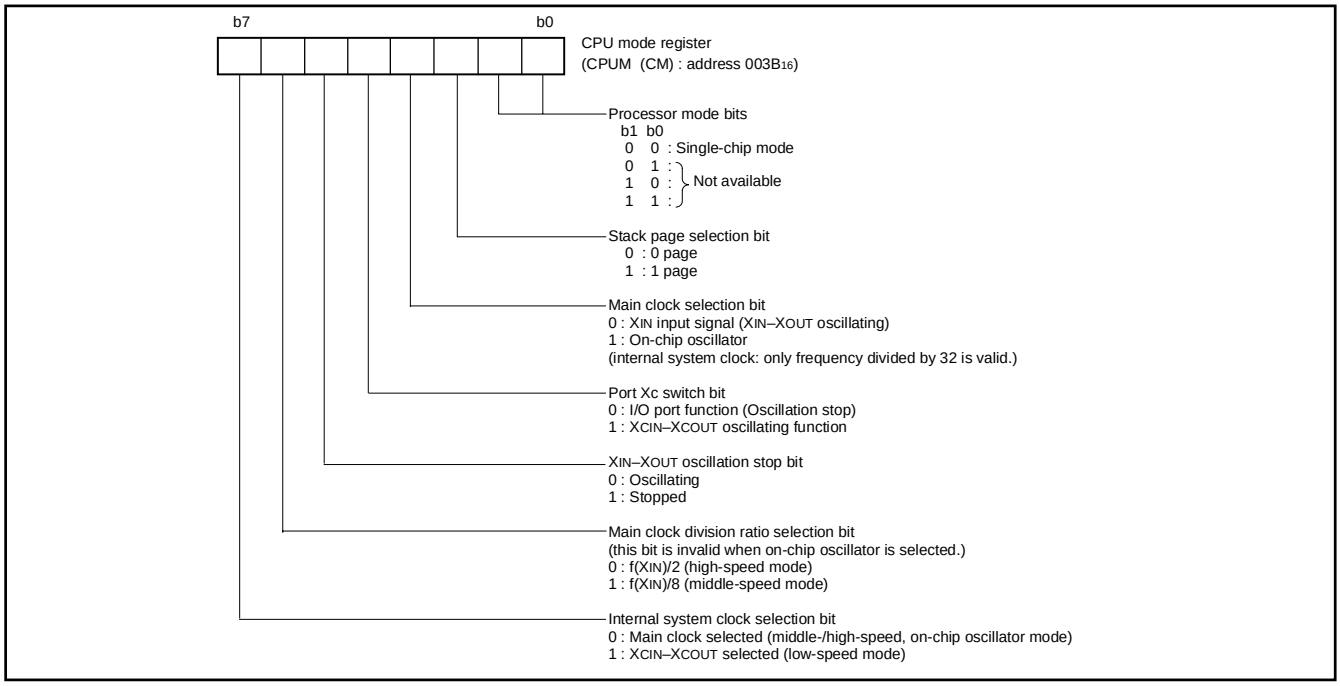


Fig. 8 Structure of CPU mode register

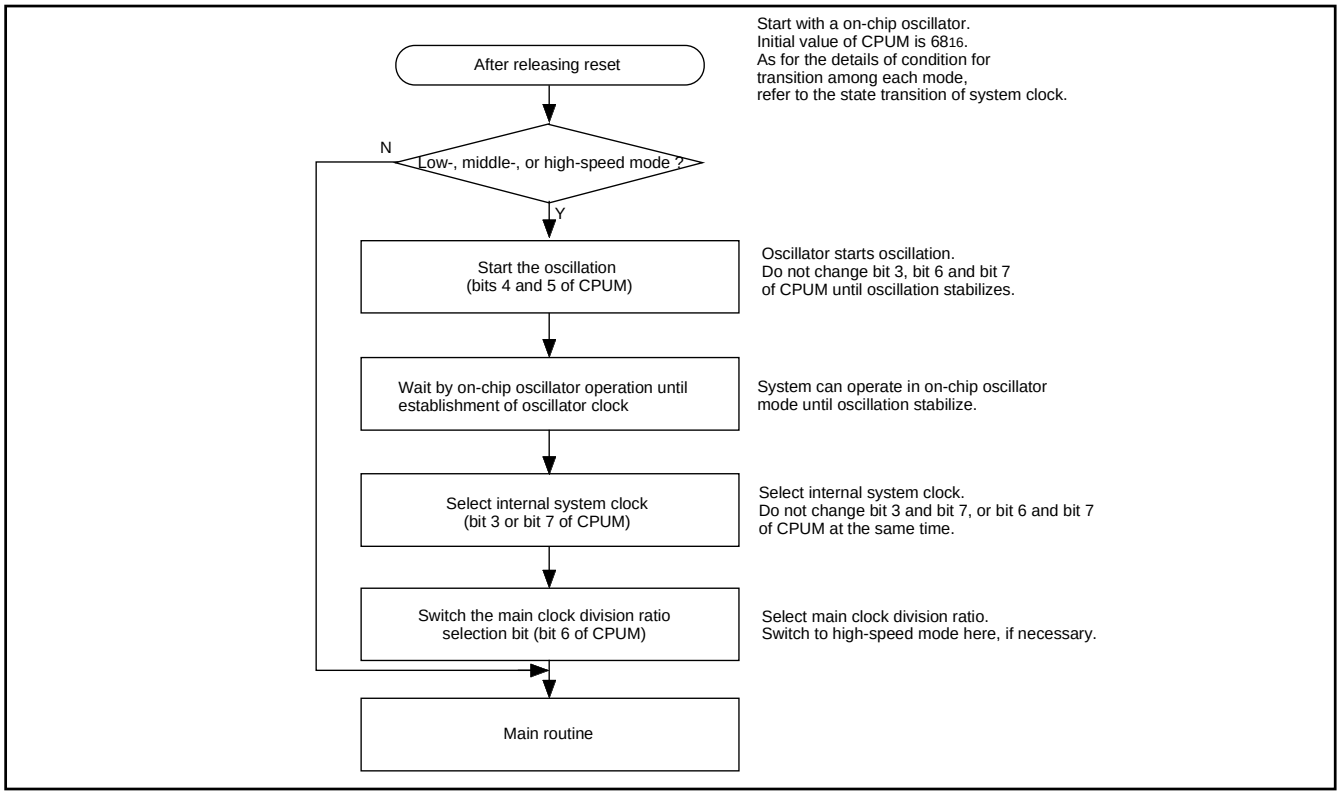


Fig. 9 Switch procedure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address XXXX$_{16}$
192	00FF$_{16}$
256	013F$_{16}$
384	01BF$_{16}$
512	023F$_{16}$
640	02BF$_{16}$
768	033F$_{16}$
896	03BF$_{16}$
1024	043F$_{16}$
1536	063F$_{16}$
2048	083F$_{16}$

ROM area

ROM size (bytes)	Address YYYY$_{16}$	Address ZZZZ$_{16}$
4096	F000$_{16}$	F080$_{16}$
8192	E000$_{16}$	E080$_{16}$
12288	D000$_{16}$	D080$_{16}$
16384	C000$_{16}$	C080$_{16}$
20480	B000$_{16}$	B080$_{16}$
24576	A000$_{16}$	A080$_{16}$
28672	9000$_{16}$	9080$_{16}$
32768	8000$_{16}$	8080$_{16}$
36864	7000$_{16}$	7080$_{16}$
40960	6000$_{16}$	6080$_{16}$
45056	5000$_{16}$	5080$_{16}$
49152	4000$_{16}$	4080$_{16}$
53248	3000$_{16}$	3080$_{16}$
57344	2000$_{16}$	2080$_{16}$
61440	1000$_{16}$	1080$_{16}$

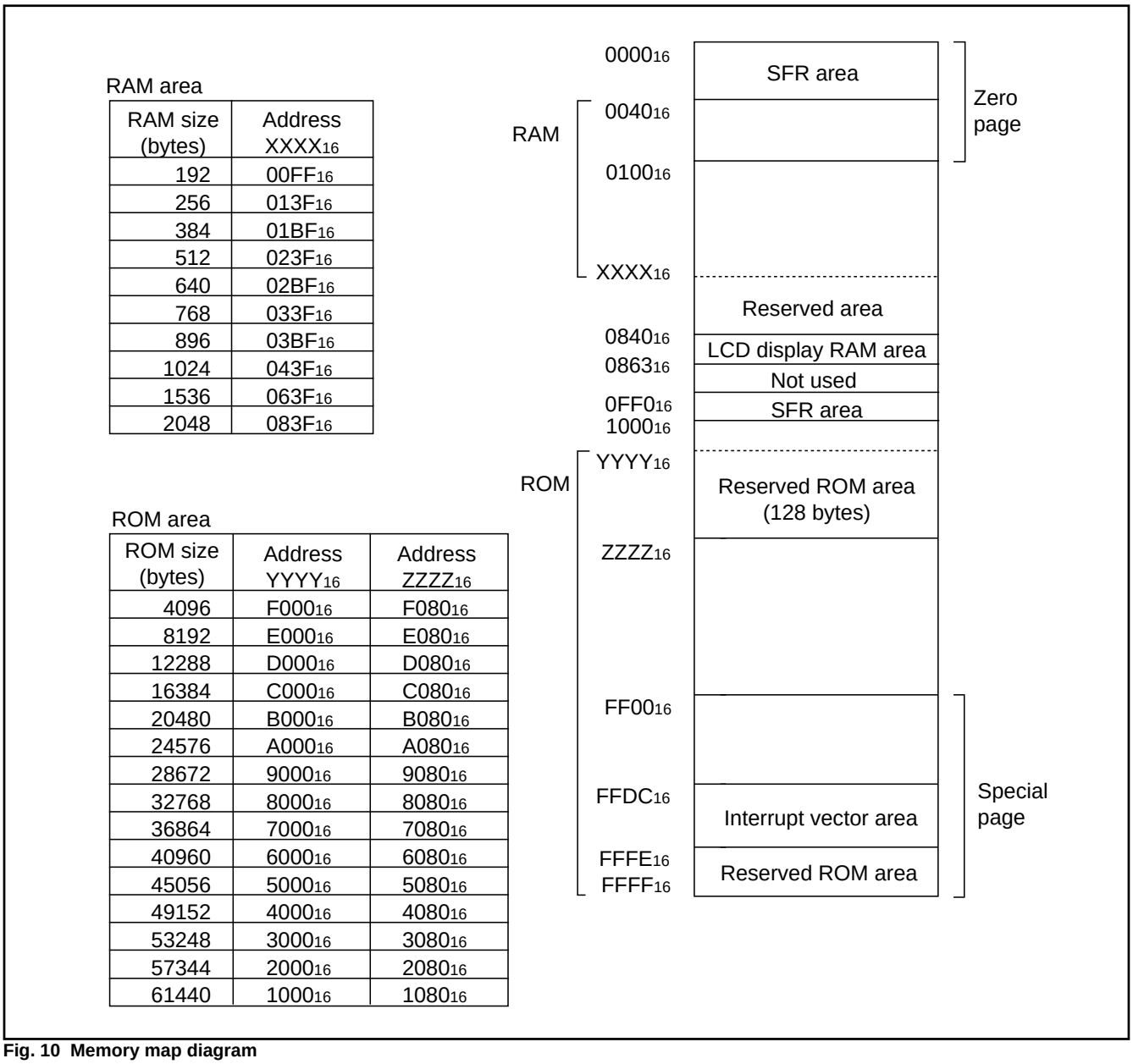


Fig. 10 Memory map diagram

0000₁₆	Port P0 (P0)
0001₁₆	Port P0 direction register (P0D)
0002₁₆	Port P1 (P1)
0003₁₆	Port P1 direction register (P1D)
0004₁₆	Port P2 (P2)
0005₁₆	Port P2 direction register (P2D)
0006₁₆	Port P3 (P3)
0007₁₆	Port P3 direction register (P3D)
0008₁₆	Port P4 (P4)
0009₁₆	Port P4 direction register (P4D)
000A₁₆	Port P5 (P5)
000B₁₆	Port P5 direction register (P5D)
000C₁₆	Port P6 (P6)
000D₁₆	Port P6 direction register (P6D)
000E₁₆	Port P7 (P7)
000F₁₆	Port P7 direction register (P7D)
0010₁₆	
0011₁₆	
0012₁₆	RRF register (RRFR)
0013₁₆	LCD mode register 1 (LM1)
0014₁₆	LCD mode register 2 (LM2)
0015₁₆	A/D control register (ADCON)
0016₁₆	A/D conversion register (low-order) (ADL)
0017₁₆	A/D conversion register (high-order) (ADH)
0018₁₆	Transmit/receive buffer register 1 (TB1/RB1)
0019₁₆	Serial I/O1 status register (SIO1STS)
001A₁₆	Serial I/O1 control register (SIO1CON)
001B₁₆	UART control register (UARTCON)
001C₁₆	Baudrate generator (BRG)
001D₁₆	Serial I/O2 control register (SIO2CON)
001E₁₆	Reserved area (access disabled)
001F₁₆	Serial I/O2 register (SIO2)

0020₁₆	Timer 1 (T1)
0021₁₆	Timer 2 (T2)
0022₁₆	Timer 3 (T3)
0023₁₆	Timer 4 (T4)
0024₁₆	PWM01 register (PWM01)
0025₁₆	Timer 12 mode register (T12M)
0026₁₆	Timer 34 mode register (T34M)
0027₁₆	Timer 1234 mode register (T1234M)
0028₁₆	Timer 1234 frequency division selection register (PRE1234)
0029₁₆	Watchdog timer control register (WDTCON)
002A₁₆	Timer X (low-order) (TXL)
002B₁₆	Timer X (high-order) (TXH)
002C₁₆	Timer X (extension) (TXEX)
002D₁₆	Timer X mode register (TXM)
002E₁₆	Timer X control register 1 (TXCON1)
002F₁₆	Timer X control register 2 (TXCON2)
0030₁₆	Compare register 1 (low-order) (COMP1L)
0031₁₆	Compare register 1 (high-order) (COMP1H)
0032₁₆	Compare register 2 (low-order) (COMP2L)
0033₁₆	Compare register 2 (high-order) (COMP2H)
0034₁₆	Compare register 3 (low-order) (COMP3L)
0035₁₆	Compare register 3 (high-order) (COMP3H)
0036₁₆	Timer Y (low-order) (TYL)
0037₁₆	Timer Y (high-order) (TYH)
0038₁₆	Timer Y mode register (TYM)
0039₁₆	Timer Y control register (TYCON)
003A₁₆	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1 (IREQ1)
003D₁₆	Interrupt request register 2 (IREQ2)
003E₁₆	Interrupt control register 1 (ICON1)
003F₁₆	Interrupt control register 2 (ICON2)

0FF0₁₆	PULL register 1 (PULL1)
0FF1₁₆	PULL register 2 (PULL2)
0FF2₁₆	PULL register 3 (PULL3)
0FF3₁₆	Clock output control register (CKOUT)
0FF4₁₆	Segment output disable register 0 (SEG0)
0FF5₁₆	Segment output disable register 1 (SEG1)
0FF6₁₆	Segment output disable register 2 (SEG2)
0FF7₁₆	Key input control register (KIC)

0FF8₁₆	
0FF9₁₆	
0FFA₁₆	
0FFB₁₆	
0FFC₁₆	
0FFD₁₆	
0FFE₁₆	
0FFF₁₆	

Fig. 11 Memory map of special function register (SFR)

I/O PORTS
Direction Registers (Ports P0–P6, P7$_2$–P7$_4$)

The I/O ports P0–P6, P7$_2$–P7$_4$ have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

When "0" is written to the bit of the direction register, the corresponding pin becomes an input pin. As for ports P0–P3, when "1" is written to the bit of the direction register and the segment output disable register, the corresponding pin becomes an output pin. As for ports P4–P6, P7$_2$–P7$_4$, when "1" is written to the bit of the direction register, the corresponding pin becomes an output pin.

If data is read from a pin set to output, the value of the port latch is read, not the value of the pin itself. However, when RTP$_1$, RTP$_0$, TXOUT$_1$, TXOUT$_2$, T4OUT, T3OUT and T2OUT/CKOUT output are selected, the output value is read, not the value of the port latch. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Ports P7$_0$, P7$_1$

These are input ports which are shared with the voltage multiplier. When these are read out at using the voltage multiplier, the contents are "1".

Pull-up Control

Each individual bit of ports P0–P3 can be pulled up with a program by setting direction registers and segment output disable registers 0 to 2 (addresses 0FF4$_{16}$ to 0FF6$_{16}$).

The pin is pulled up by setting "0" to the direction register and "1" to the segment output disable register.

By setting the PULL registers (addresses 0FF0$_{16}$ to 0FE2$_{16}$), ports P4–P7 can control pull-up with a program.

However, the contents of PULL register do not affect ports programmed as the output ports.

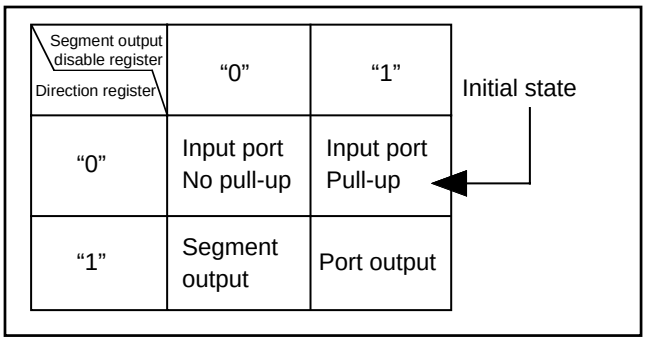
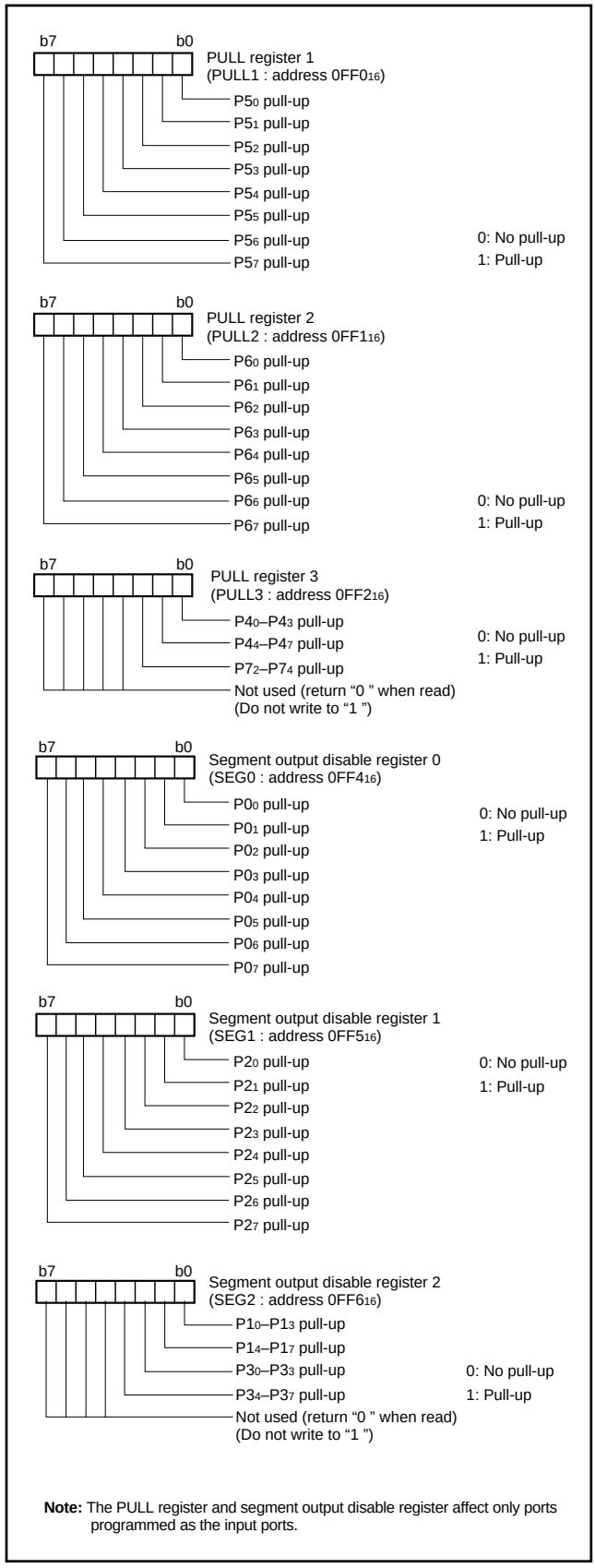


Fig. 12 Structure of ports P0 to P3



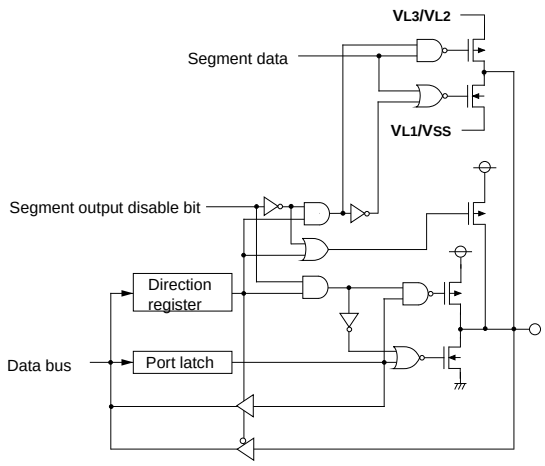
Note: The PULL register and segment output disable register affect only ports programmed as the input ports.

Fig. 13 Structure of PULL register and segment output disable register

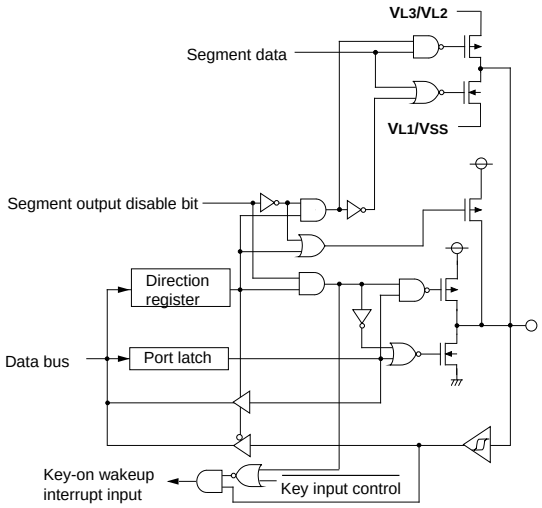
Table 6 List of I/O port function

Pin	Name	Input/Output	I/O format	Non-port function		Related SFRs	Ref. No.
P0$_0$/SEG$_8$ – P0$_7$/SEG$_{15}$	Port P0	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	LCD segment output		Segment output disable register 0	(1)
P1$_0$/SEG$_{16}$ – P1$_7$/SEG$_{23}$	Port P1	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output			Segment output disable register 2	
P2$_0$/SEG$_0$/(KW$_4$)– P2$_3$/SEG$_3$/(KW$_7$)	Port P2	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output		Key input (key-on wakeup) interrupt input	Segment output disable register 1 Key input control register	(2)
P2$_4$/SEG$_4$ – P2$_7$/SEG$_7$						Segment output disable register 1	(1)
P3$_0$/SEG$_{24}$ – P3$_7$/SEG$_{31}$	Port P3	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output			Segment output disable register 2	
P4$_0$/RxD	Port P4	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O1 function I/O		PULL register 3	(3)
P4$_1$/TxD						Serial I/O1 control register	(4)
P4$_2$/SCLK1						Serial I/O1 status register	(5)
P4$_3$/$\overline{\text{SRDY1}}$						UART control register	(6)
P4$_4$/SIN$_2$/(KW$_0$), P4$_5$/SOUT$_2$/(KW$_1$), P4$_6$/SCLK$_2$/(KW$_2$), P4$_7$/$\overline{\text{SRDY2}}$/(KW$_3$)				Serial I/O2 function I/O	Key input (key-on wakeup) interrupt input	PULL register 3 Serial I/O2 control register Serial I/O2 register Key input control register	(7) (8) (9) (10)
P5$_0$/AN$_0$/RTP$_0$, P5$_1$/AN$_1$/RTP$_1$	Port P5	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	A/D conversion input	Real time port function output	PULL register 1 A/D control register Timer Y mode register	(11)
P5$_2$/AN$_2$ – P5$_6$/AN$_6$						PULL register 1 A/D control register	(12)
P5$_7$/AN$_7$/ADKEY$_0$					ADKEY input		(13)
P6$_0$/XCIN, P6$_1$/XCOUT	Port P6	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Sub-clock oscillation circuit		PULL register 2 CPU mode register	(14) (15)
P6$_2$/INT$_{00}$/(LED$_0$)				External interrupt input		PULL register 2 Interrupt edge selection register	(16)
P6$_3$/TXOUT$_2$/ (LED$_1$)				Timer X output 2		PULL register 2 Timer X mode register Timer X control registers 1, 2	(18)
P6$_4$/INT$_2$/(LED$_2$)				External interrupt input		PULL register 2 Interrupt edge selection register	(17)
P6$_5$/TXOUT$_1$/ (LED$_3$)				Timer X output 1		PULL register 2 Timer X mode register Timer X control register 1	(18)
P6$_6$/INT$_{10}$/ CNTR$_0$/(LED$_4$),				Timer X function input External interrupt input		PULL register 2 Interrupt edge selection register Timer X mode register Timer X control registers 1, 2	(19)
P6$_7$/CNTR$_1$/ (LED$_5$)				Timer Y function input		PULL register 2 Timer Y mode register	(17)
P7$_0$/C$_1$/INT$_{01}$, P7$_1$/C$_2$/INT$_{11}$	Port P7	Input	CMOS compatible input level	External interrupt input LCD voltage multiplier input		Interrupt edge selection register LCD mode registers 1, 2	(20)
P7$_2$/T$_{2OUT}$/CKOUT P7$_3$/PWM$_0$/T$_{3OUT}$, P7$_4$/PWM$_1$/T$_{4OUT}$		Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Timer 2 output Timer 3 output Timer 4 output	Clock output PWM output	PULL register 3 Timer 1234 mode register Timer 1234 frequency division register	(21)
COM$_0$–COM$_3$	Common	Output	LCD common output	LCD common output		LCD mode registers 1, 2	(22)
COM$_4$/SEG$_{35}$– COM$_7$/SEG$_{32}$	Common/ Segment		LCD common/segment output		LCD segment output		(23)

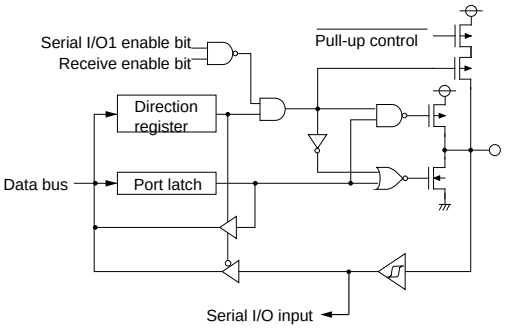
(1)Ports P0,P1,P24–P27,P3



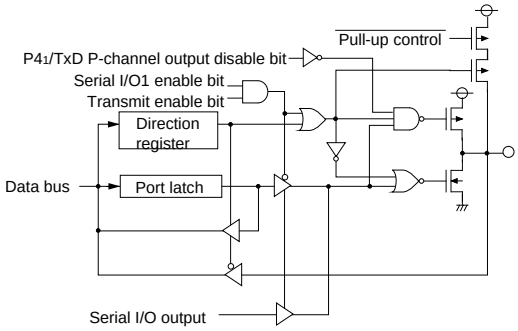
(2)Ports P20–P23



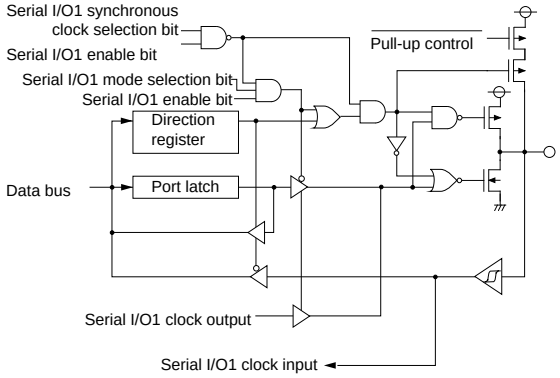
(3)Port P40



(4)Port P41



(5)Port P42



(6)Port P43

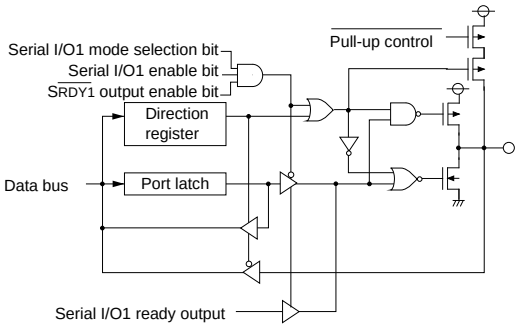


Fig. 14 Port block diagram (1)

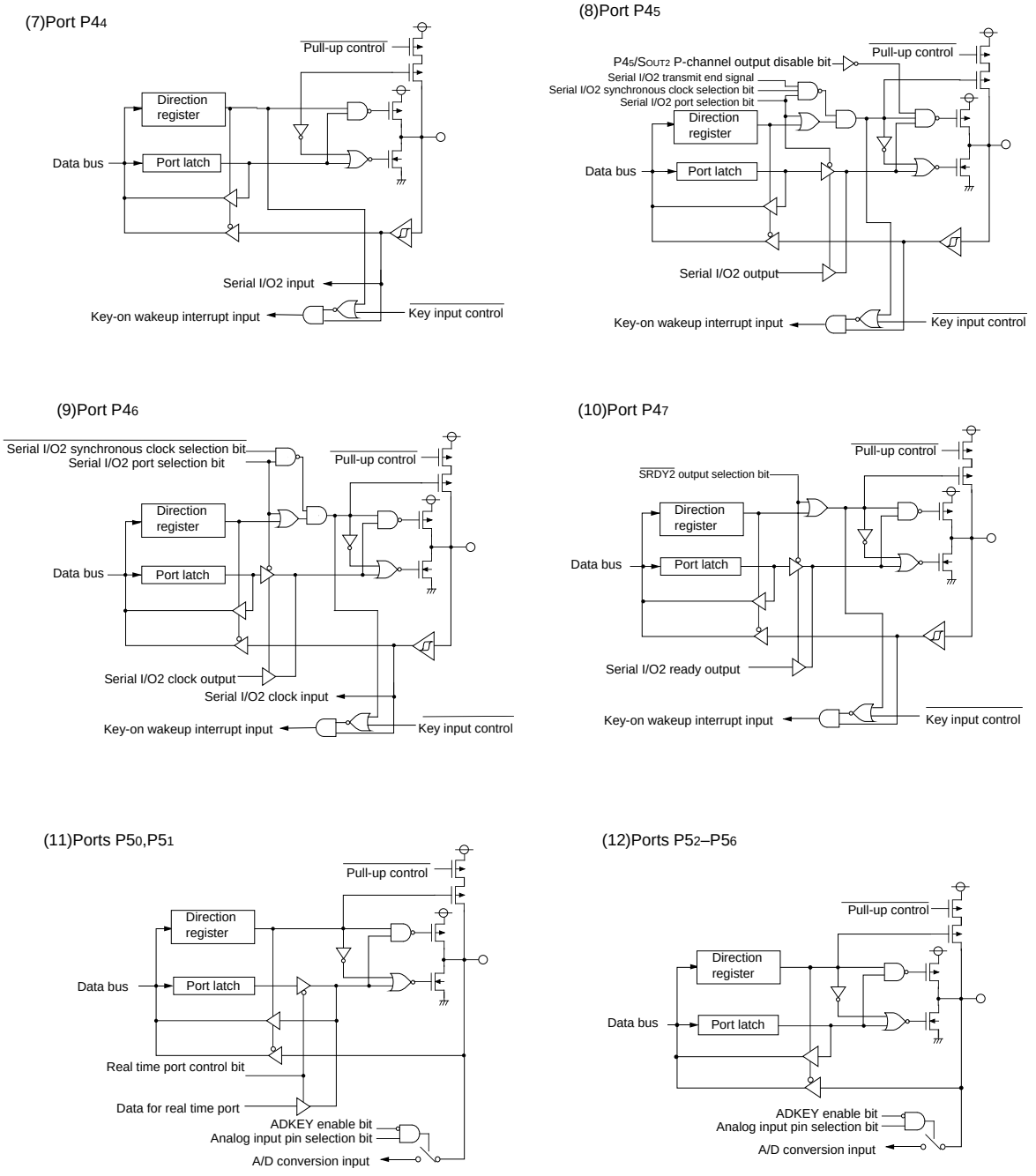
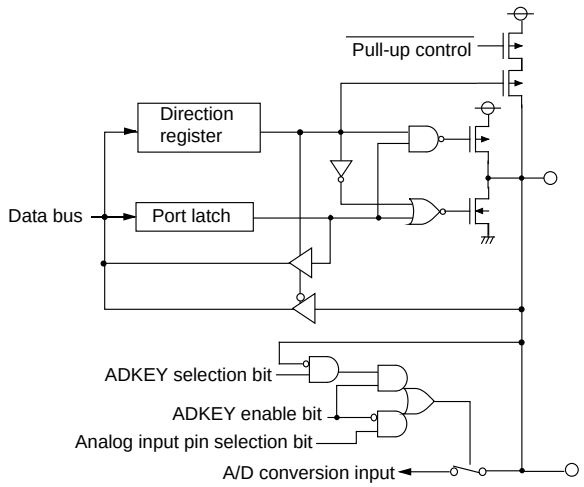
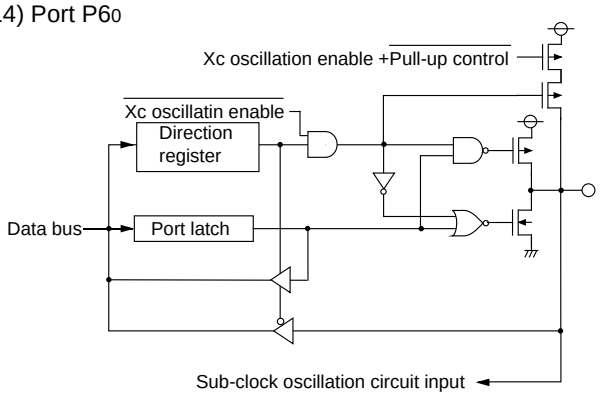


Fig. 15 Port block diagram (2)

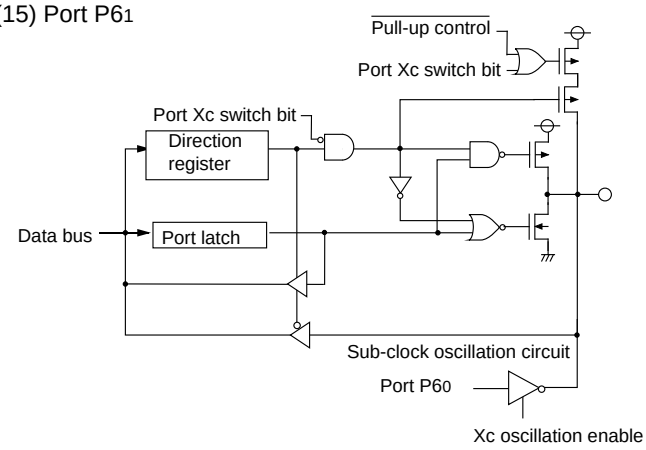
(13) Port P5$_7$



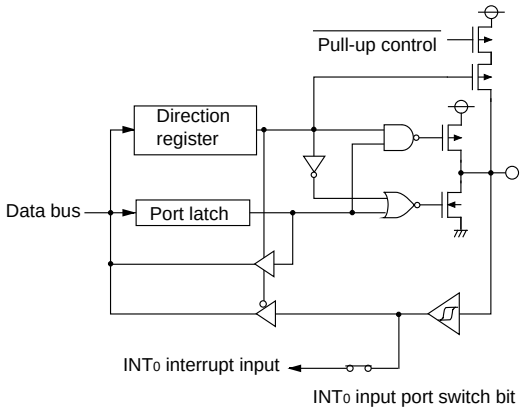
(14) Port P6$_0$



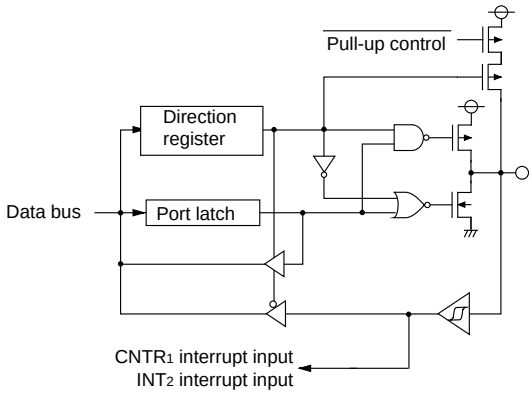
(15) Port P6$_1$



(16) Port P6$_2$



(17) Ports P6$_4$,P6$_7$



(18) Ports P6$_3$,P6$_5$

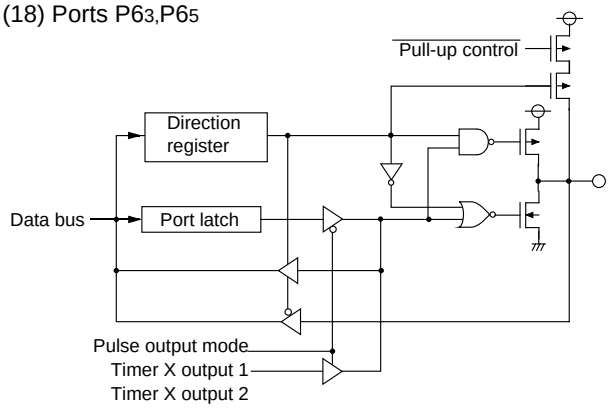
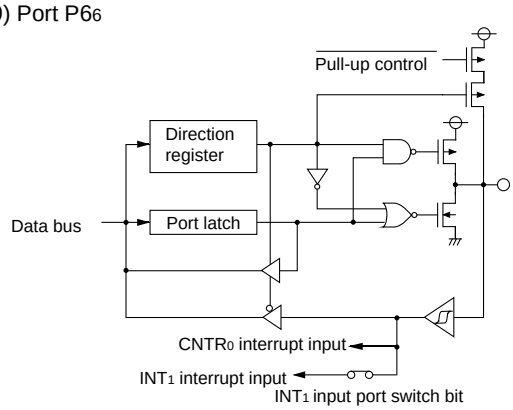
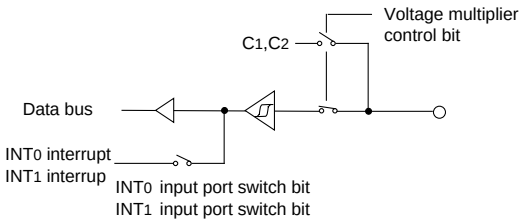


Fig. 16 Port block diagram (3)

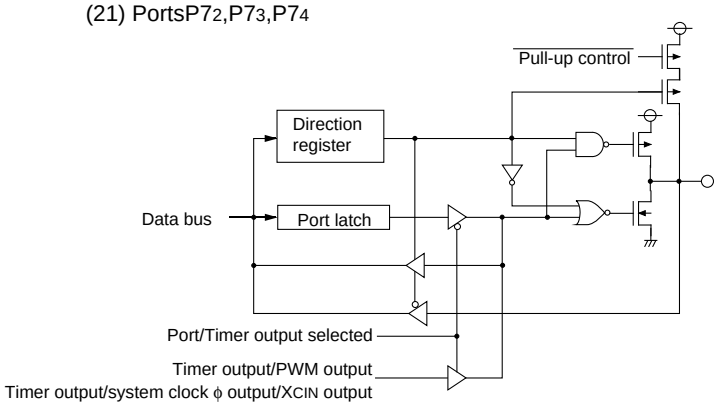
(19) Port $P6_6$



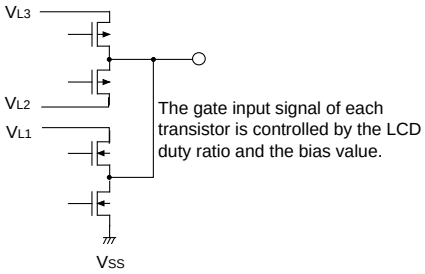
(20) Ports $P7_0$, $P7_1$



(21) Ports$P7_2$,$P7_3$,$P7_4$



(22) COM_0 to COM_3



(23) COM_4/SEG_{35} to COM_7/SEG_{32}

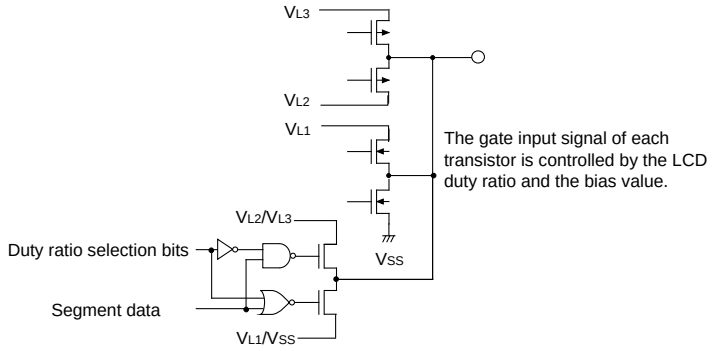


Fig. 17 Port block diagram (4)

Termination of unused pins

• Termination of common pins

I/O ports: Select an input port or an output port and follow each processing method.

Output ports: Open.

Input ports: If the input level become unstable, through current flow to an input circuit, and the power supply current may increase.

Especially, when expecting low consumption current (at STP or WIT instruction execution etc.), pull-up or pull-down input ports to prevent through current (built-in resistor can be used).

We recommend processing unused pins through a resistor which can secure $I_{OH(avg)}$ or $I_{OL(avg)}$.

Because, when an I/O port or a pin which have an output function is selected as an input port, it may operate as an output port by incorrect operation etc.

Table 7 Termination of unused pins

Pin	Termination 1 (recommend)	Termination 2	Termination 3
P0$_0$/SEG$_8$–P0$_7$/SEG$_{15}$	I/O port	When selecting SEG output, open.	–
P1$_0$/SEG$_{16}$–P1$_7$/SEG$_{23}$			
P2$_0$/SEG$_0$–P2$_7$/SEG$_7$			
P3$_0$/SEG$_{24}$–P3$_7$/SEG$_{31}$			
P4$_0$/RxD		When selecting RxD function, perform termination of input port.	–
P4$_1$/TxD		When selecting TxD function, perform termination of input port.	–
P4$_2$/SCLK1		When selecting external clock input, perform termination of output port.	When selecting internal clock output, perform termination of output port.
P4$_3$/$\overline{\text{SRDY1}}$		When selecting $\overline{\text{SRDY1}}$ function, perform termination of output port.	–
P4$_4$/SIN2		When selecting SIN2 function, perform termination of input port.	–
P4$_5$/SOUT2		When selecting SOUT2 function, perform termination of output port.	–
P4$_6$/SCLK2		When selecting external clock input, perform termination of output port.	When selecting internal clock output, perform termination of output port.
P4$_7$/$\overline{\text{SRDY2}}$		When selecting $\overline{\text{SRDY2}}$ function, perform termination of output port.	–
P5$_0$/AN$_0$/RTP$_0$ P5$_1$/AN$_1$/RTP$_1$		When selecting AN function, these pins can be opened. (A/D conversion result cannot be guaranteed.)	When selecting RTP function, perform termination of output port.
P5$_2$/AN$_2$–P5$_6$/AN$_6$			–
P5$_7$/AN$_7$/ADKEY			When selecting ADKEY function, pull-up this pin through a resistor.
P6$_0$/XCIN P6$_1$/XCOUT		Do not select XCIN-XCOUT oscillation function by program.	–
P6$_2$/INT$_{00}$		When selecting INT function, perform termination of input port.	–
P6$_3$/TXOUT2		When selecting TXOUT function, perform termination of output port.	–
P6$_4$/INT$_2$		When selecting INT function, perform termination of input port.	–
P6$_5$/TXOUT1		When selecting TXOUT function, perform termination of output port.	–
P6$_6$/INT$_{10}$/CNTR$_0$		When selecting CNTR input function or INT function, perform termination of input port.	–
P6$_7$/CNTR$_1$		When selecting CNTR input function, perform termination of input port.	–
P7$_0$/C$_1$/INT$_{01}$ P7$_1$/C$_2$/INT$_{11}$	Input port	When selecting INT function, perform termination of input port.	Do not select the C pin (voltage multiplir).
P7$_2$/T2OUT/CKOUT	I/O port	When selecting T2OUT function or CKOUT function, perform termination of output port.	–
P7$_3$/PWM$_0$/T3OUT P7$_4$/PWM$_1$/T4OUT		When selecting PWM, T3OUT, or T4OUT function, perform termination of output port.	–
VL3	Connect to Vcc	–	–
VL2	VL3 ≤ VL2 ≤ VL1	–	–
VL1	Connect to Vss	–	–
COM$_0$–COM$_3$	Open	–	–
COM$_4$/SEG$_{35}$–COM$_7$/SEG$_{32}$	Open	–	–
VREF	Connect to Vcc	–	–

INTERRUPTS

Interrupts occur by seventeen sources: six external, ten internal, and one software.

Interrupt Control

Each interrupt except the BRK instruction interrupt have both an interrupt request bit and an interrupt enable bit, and is controlled by the interrupt disable flag. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”.

Interrupt enable bits can be set or cleared by program. Interrupt request bits can be cleared by program, but cannot be set by software. The BRK instruction interrupt and reset cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt and reset. If several interrupt requests occur at the same time, the interrupt with highest priority is accepted first.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set to “1” and the corresponding interrupt request bit is set to “0”.
3. The interrupt jump destination address is read from the vector table into the program counter.

■ Notes on Interrupts

When setting the followings, the interrupt request bit may be set to “1”.

•When switching external interrupt active edge
Related register: Interrupt edge selection register (address $3A_{16}$)
Timer X control register (address $2E_{16}$)
Timer Y mode register (address 38_{16})

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
Related register: Interrupt edge selection register (address $3A_{16}$)

When not requiring the interrupt occurrence synchronous with these setting, take the following sequence.

①Set the corresponding interrupt enable bit to “0” (disabled).
②Set the interrupt edge selection bit (polarity switch bit) or the interrupt source selection bit.
③Set the corresponding interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the corresponding interrupt enable bit to “1” (enabled).

Table 7 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses **(Note 1)**		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset **(Note 2)**	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0 (INT_{00} or INT_{01}) (**Note 3**)	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1 (INT_{10} or INT_{11}) (**Note 3**)	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
INT_2	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_2 input	Valid when INT_2 interrupt is selected External interrupt (active edge selectable)
Key input (key-on wakeup)	5	$FFF5_{16}$	$FFF4_{16}$	At falling of ports $P2_0$–$P2_3$, $P4_4$–$P4_7$ input logical level AND	Valid when key input interrupt is selected External interrupt (falling valid)
Timer X	6	$FFF3_{16}$	$FFF2_{16}$	At timer X underflow	
Timer 1	7	$FFF1_{16}$	$FFF0_{16}$	At timer 1 underflow	
Timer 2	8	$FFEF_{16}$	$FFEE_{16}$	At timer 2 underflow	
Timer 3	9	$FFED_{16}$	$FFEC_{16}$	At timer 3 underflow	
Timer 4	10	$FFEB_{16}$	$FFEA_{16}$	At timer 4 underflow	
Serial I/O1 receive	11	$FFE9_{16}$	$FFE8_{16}$	At completion of serial I/O1 data receive	Valid only when serial I/O1 is selected
Serial I/O1 transmit	12	$FFE7_{16}$	$FFE6_{16}$	At completion of serial I/O1 transmit shift or transmit buffer is empty	Valid only when serial I/O1 is selected
Serial I/O2	13	$FFE5_{16}$	$FFE4_{16}$	At completion of serial I/O2 data transmit/receive	
$CNTR_0$	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
Timer Y	15	$FFE1_{16}$	$FFE0_{16}$	At timer Y underflow	
$CNTR_1$				At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
A/D conversion	16	$FFDF_{16}$	$FFDE_{16}$	At completion of A/D conversion	
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.
3: INT_0 (INT_{00} or INT_{01}), INT_1 (INT_{10} or INT_{11}) input pins are selected by the interrupt edge selection register (INTEDGE).

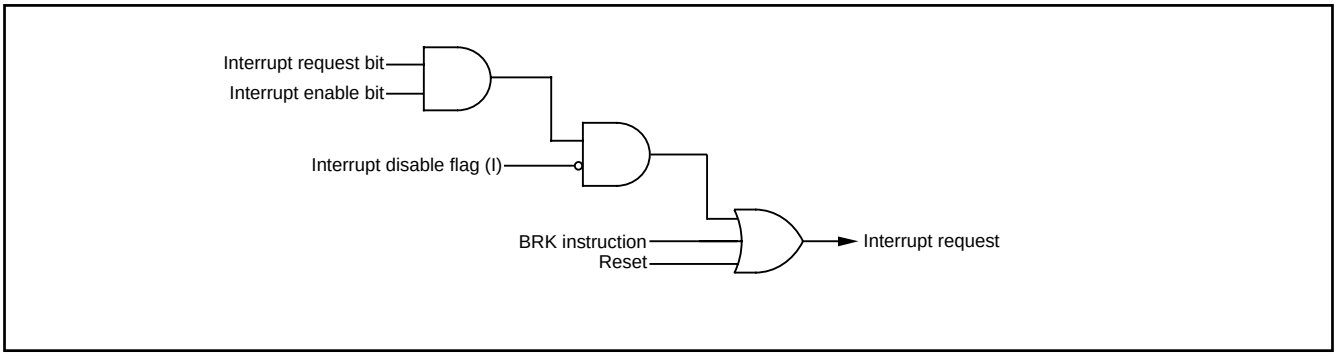


Fig. 18 Interrupt control

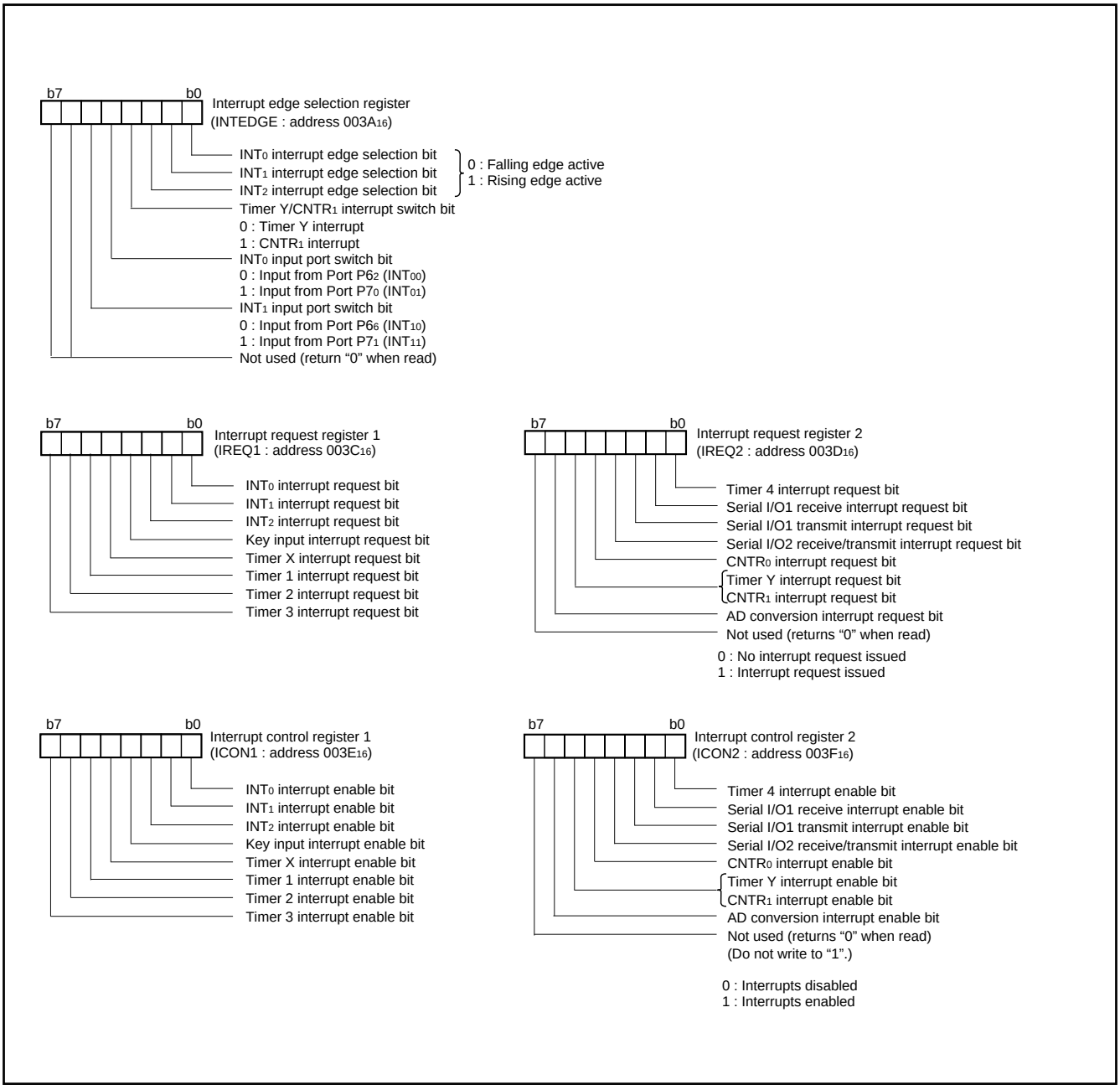


Fig. 19 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake-Up)

A key input interrupt request is generated by detecting the falling edge from any pin of ports P20–P23, P44–P47 that have been set to input mode. In other words, it is generated when AND of input level goes from “1” to “0”. An example of using a key input interrupt is shown in Figure 20, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P44–P47.

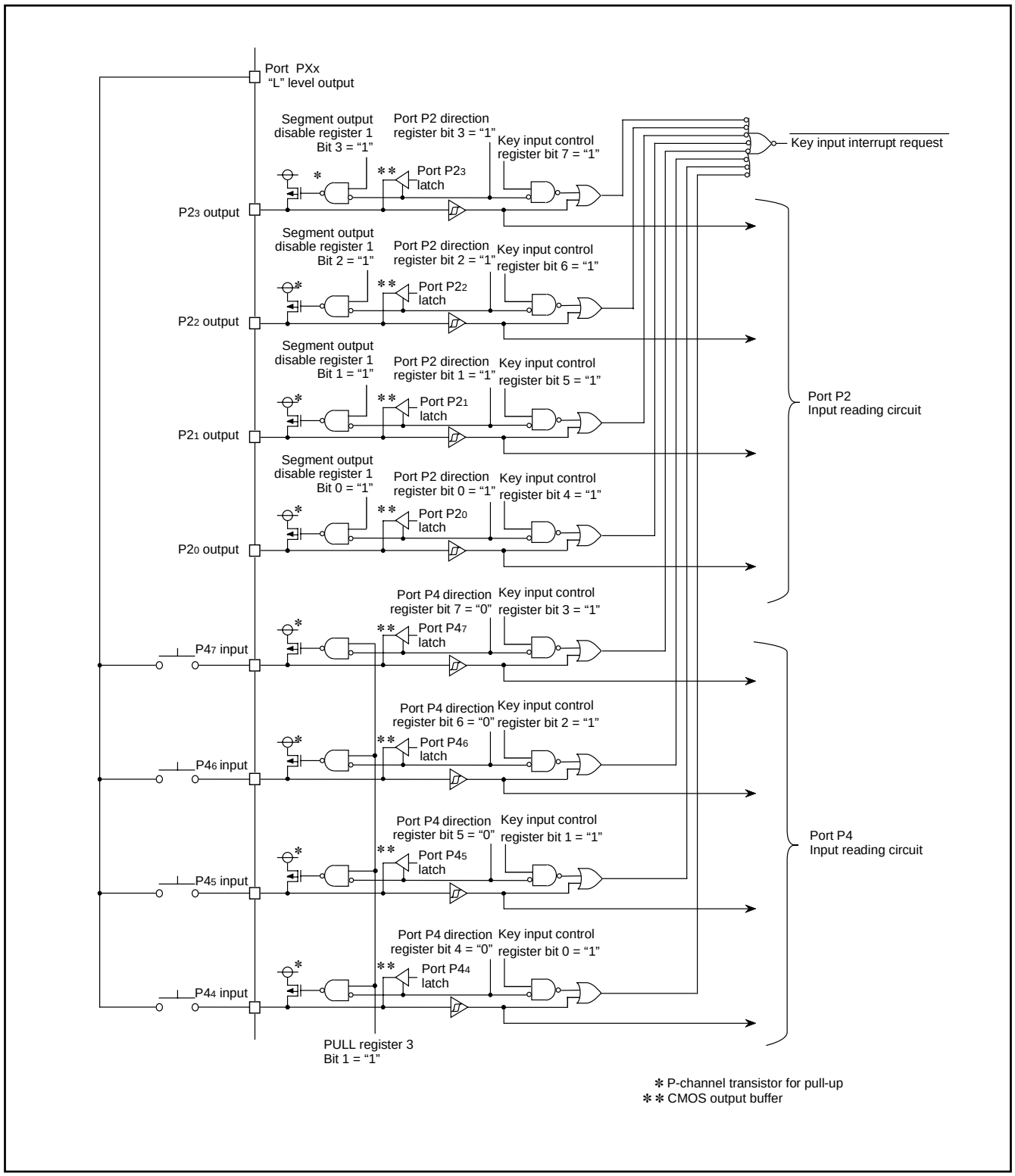


Fig. 20 Connection example when using key input interrupt

A key input interrupt is controlled by the key input control register and port direction registers. When the key input interrupt is enabled, set “1” to the key input control register. A key input of any pin of ports $P2_0$–$P2_3$, $P4_4$–$P4_7$ that have been set to input mode is accepted.

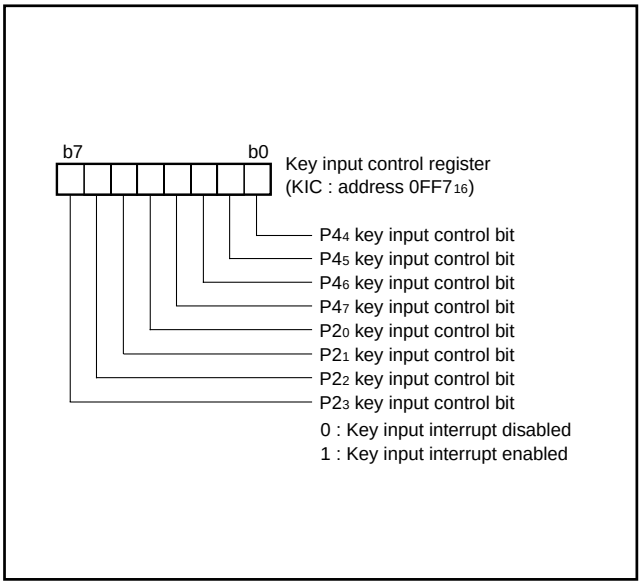


Fig. 21 Structure of key input control register

TIMERS
8-Bit Timer

The 38C5 group has four built-in 8-bit timers : Timer 1, Timer 2, Timer 3, and Timer 4.

Each timer has the 8-bit timer latch. All timers are down-counters. When the timer reaches "00_{16}", the contents of the timer latch is reloaded into the timer with the next count pulse. In this mode, the interrupt request bit corresponding to that timer is set to "1".
The count can be stopped by setting the stop bit of each timer to "1".

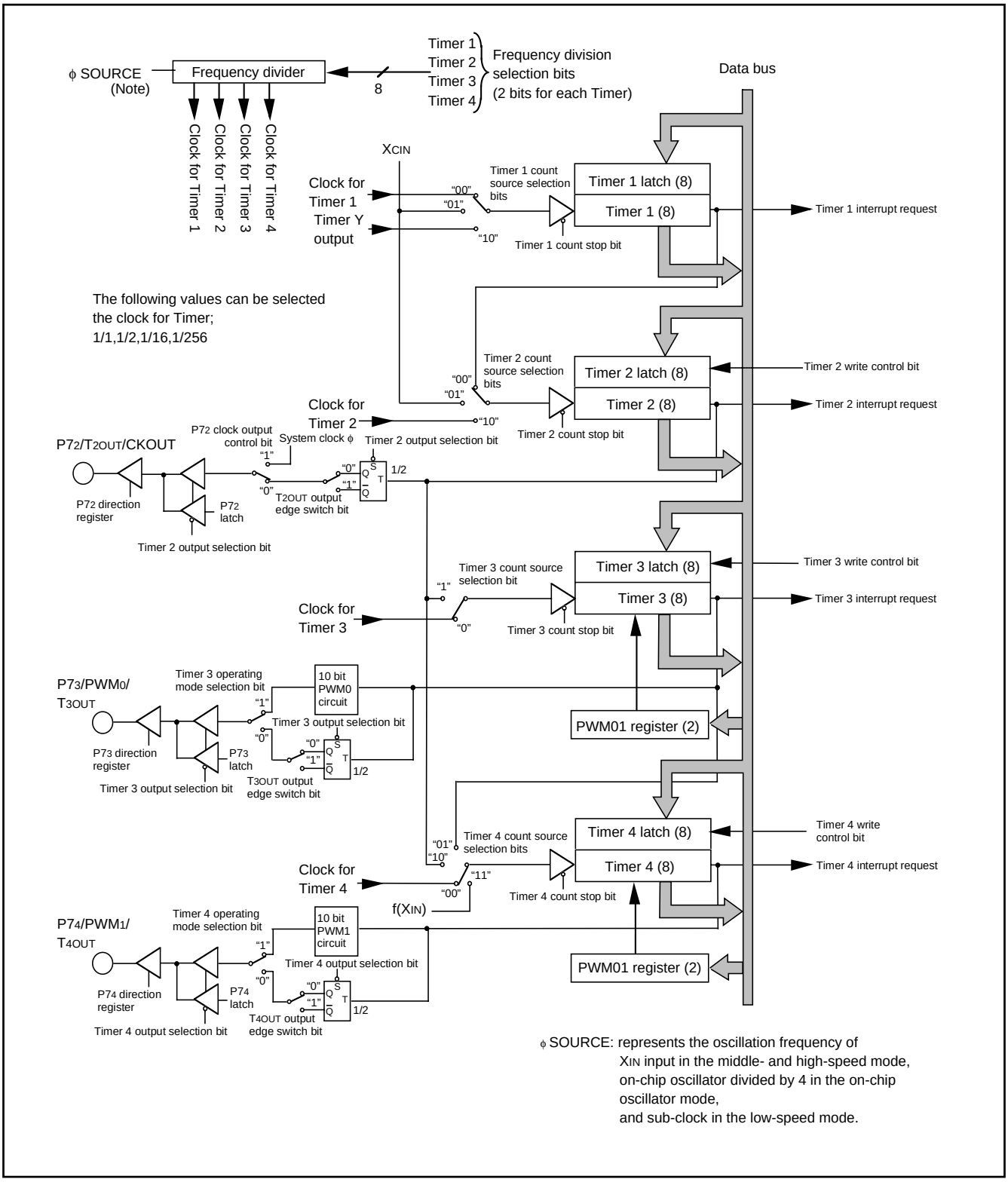


Fig. 22 Structure of timer related register

● Frequency Divider For Timer

Timer 1, timer 2, timer 3 and timer 4 have the frequency divider for the count source. The count source of the frequency divider is switched to XIN, XCIN, or the on-chip oscillator (ROSC) divided by 4 in the on-chip oscillator mode by the CPU mode register. The frequency divider is controlled by each timer division ratio selection bit. The division ratio can be selected from as follows;

1/1, 1/2, 1/16, 1/256 of f(XIN), f(XCIN) or f(ROSC)/4.

Stop a timer to switch the division of frequency.

● Timer 1, Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register.

When XCIN is selected as the count source, a pulse input from XCIN can be counted. Also, by the timer 12 mode register, each time timer 2 underflows, the signal of which polarity is inverted can be output from P72/T2OUT pin.

At reset, all bits of the timer 12 mode register are set to "0," timer 1 is set to "FF16", and timer 2 is set to "0116".

When executing the STP instruction, previously set the wait time at return.

● Timer 3, Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register. Also, by the timer 34 mode register, each time timer 3 or timer 4 underflows, the signal of which polarity is inverted can be output from P73/T3OUT pin or P74/T4OUT pin.

● Timer 3 PWM0 Mode, Timer 4 PWM1 Mode

A PWM rectangular waveform corresponding to the 10-bit accuracy can be output from the P73/PWM0 pin and P74/PWM1 pin by setting the timer 34 mode register and PWM01 register (refer to Figure 23).

One output pulse is the short interval. Four output pulses are the long interval. The "n" is the value set in the timer 3 (address 002216) or the timer 4 (address 002316). The "ts" is one period of timer 3 or timer 4 count source. "H" width of the short interval is obtained by n × ts.

However, in the long interval, "H" width of output pulse is extended for ts which is set by the PWM01 register (address 002416).

■ Notes on Timer 3 PWM0 Mode, Timer 4 PWM1 Mode

- When PWM output is suspended after starting PWM output, depending on the level of the output pulse at that time to resume an output, the delay of the one section of the short interval may be needed.
  - Stop at "H": No output delay
  - Stop at "L": Output is delayed time of 256 × ts
- In the PWM mode, the follows are performed every cycle of the long interval (4 × 256 × ts).
  - •Generation of timer 3, timer 4 interrupt requests
  - •Update of timer 3, timer 4

■ Writing to Timer 2, Timer 3, Timer 4

When writing to the latch only, if the write timing to the reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the reload latch.

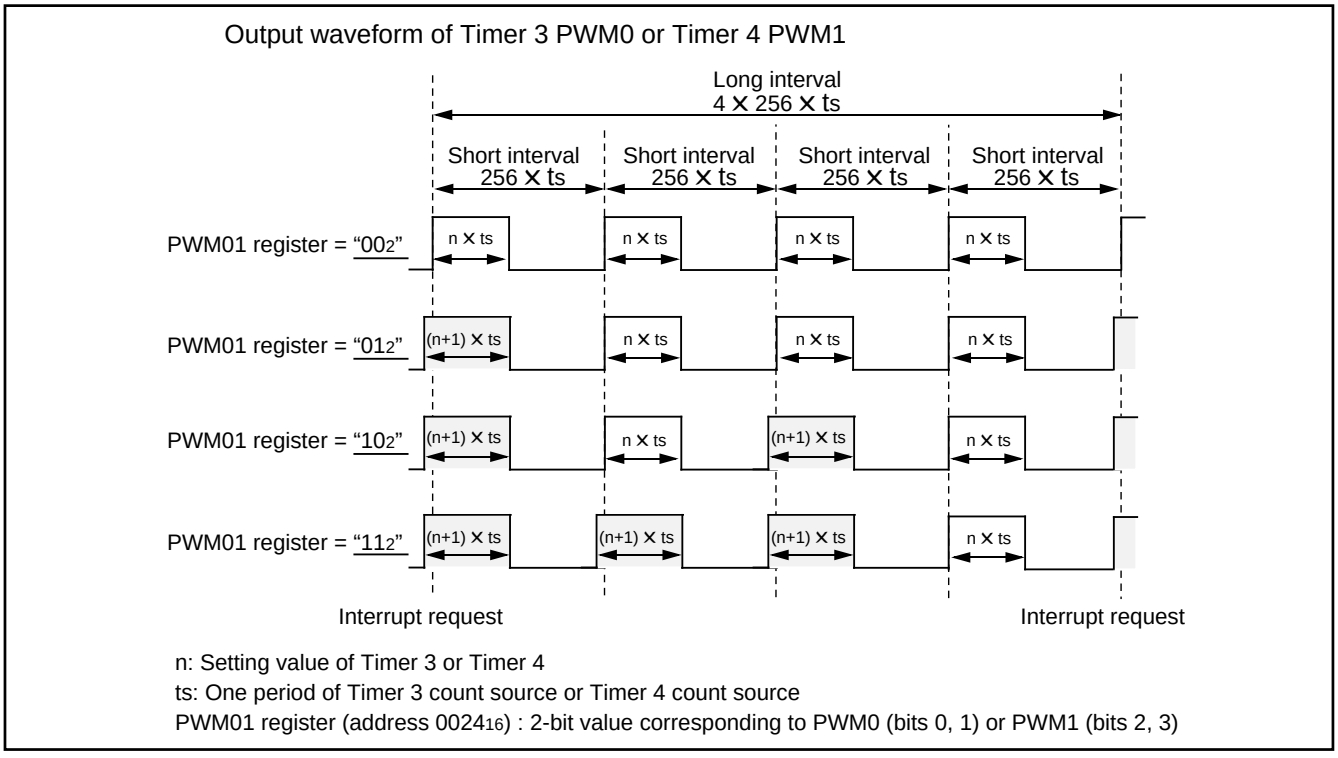


Fig. 23 Waveform of PWM0 and PWM1

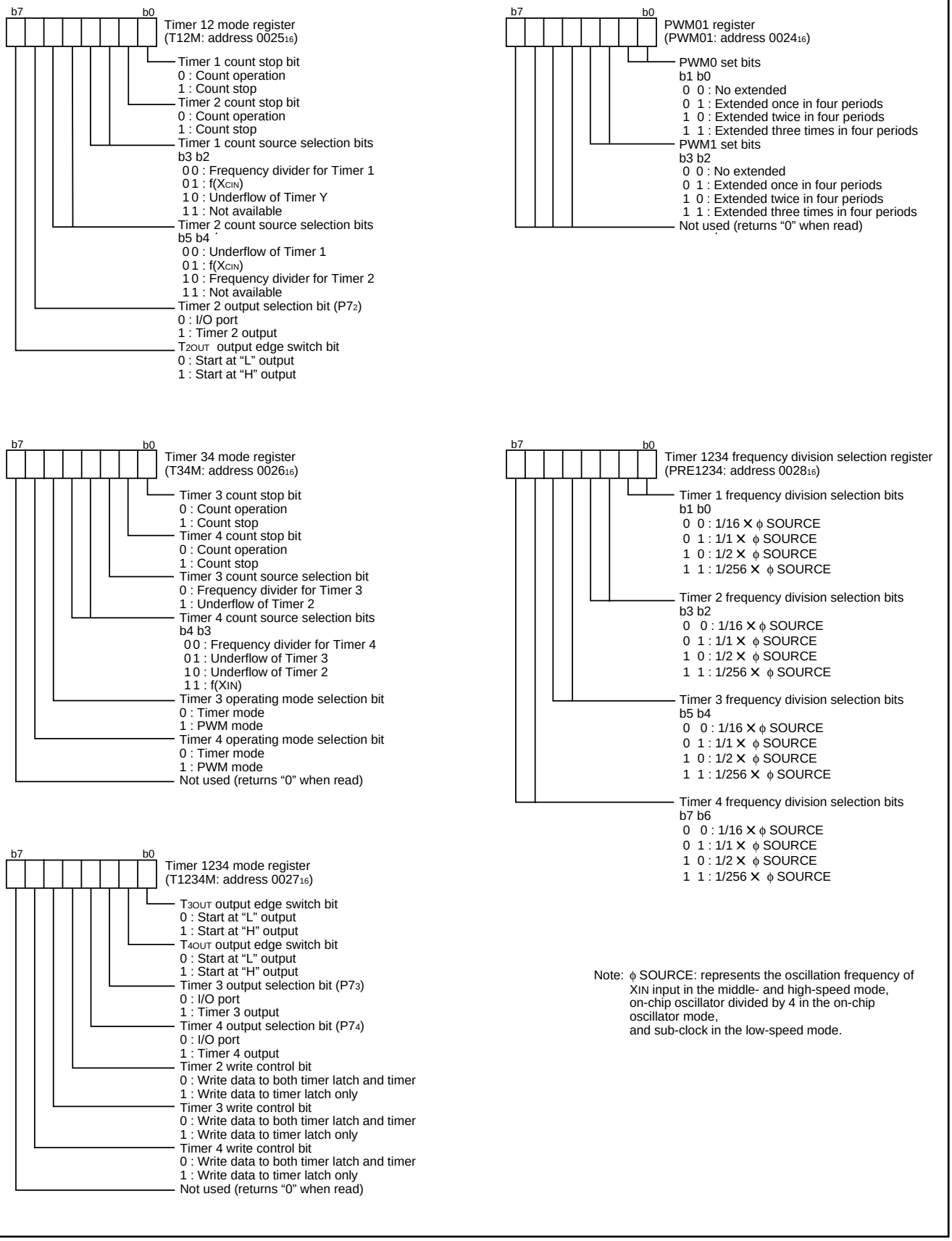


Fig. 24 Structure of Timer 1 to timer 4 related registers

16-bit Timer

Read and write operation on 16-bit timer must be performed for both high and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.

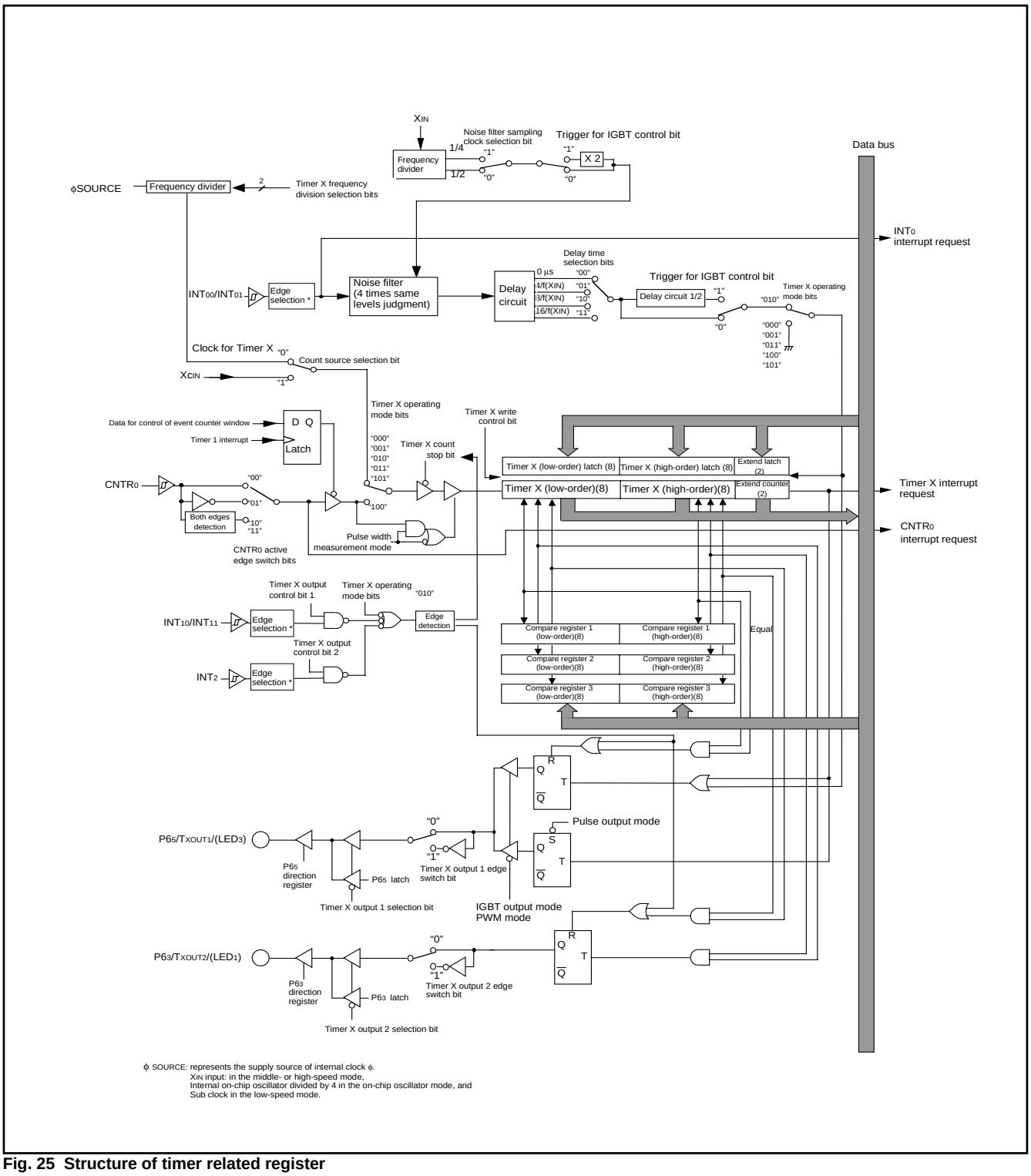


Fig. 25 Structure of timer related register

● Frequency Divider For Timer

Each timer X and timer Y have the frequency dividers for the count source. The count source of the frequency divider is switched to XIN, XCIN, or the on-chip oscillator in the on-chip oscillator mode by the CPU mode register. The division ratio of each timer can be controlled by each timer division ratio selection bit. The division ratio can be selected from as follows;
1/1, 1/2, 1/16, 1/256 of f(XIN), f(XCIN) or f(ROSC)/4.

● Timer X

The timer X count source can be selected by setting the timer X mode register. When XCIN is selected as the count source, a pulse input from XCIN can be counted.
The timer X operates as down-count. When the timer contents reach "0000_{16}", an underflow occurs at the next count pulse and the timer latch contents are reloaded. After that, the timer continues count-down. When the timer underflows, the interrupt request bit corresponding to the timer X is set to "1".
Six operating modes can be selected for timer X by the timer X mode register and timer X control register.

(1) Timer Mode

The count source can be selected by setting the timer X mode register. In this mode, timer X operates as the 18-bit counter by setting the timer X register (extension).

(2) Pulse Output Mode

Pulses of which polarity is inverted each time the timer underflows are output from the TXOUT1 pin. Except for that, this mode operates just as in the timer mode.
When using this mode, set the port sharing the TXOUT1 pin to output mode.

(3) IGBT Output Mode

After dummy output from the TXOUT1 pin, count starts with the INT0 pin input as a trigger. In the case that the timer X1 output edge switch bit is "0", when the trigger is detected or the timer X underflows, "H" is output from the TXOUT1 pin. And then, when the count value corresponds with the compare register 1 value, the TXOUT1 output becomes "L".
After noise is cleared by noise filters, judging continuous 4-time same levels with sampling clocks to be signals, the INT0 signal can use 4 types of delay time by a delay circuit.
When using this mode, set the port sharing the INT0 pin to input mode and set the port sharing the pin used as TXOUT1 or TXOUT2 function to output mode.
When the timer X output control bit 1 or 2 of the timer X control register is set to "1", the timer X count stop bit is fixed to "1" forcibly by the interrupt signal of INT1 or INT2. And then, the TXOUT1 output and TXOUT2 output can be set to "L" forcibly at the same time that the timer X stops counting.
Do not write "1" to the timer X register (extension) when using the IGBT output mode.

(4) PWM Mode

IGBT dummy output, an external trigger with the INT0 pin and output control with pins INT1 and INT2 are not used. Except for those, this mode operates just as in the IGBT output mode.
The period of PWM waveform is specified by the timer X set value. In the case that the timer X1 output edge switch bit is "0", the "H" interval is specified by the compare register 1 set value. In the case that the timer X2 output edge switch bit is "0", the "H" interval is specified by the compare registers 2 and 3 set values.
When using this mode, set the port sharing the pin used as TXOUT1 or TXOUT2 function to output mode.
Do not write "1" to the timer X register (extension) when using the PWM mode.

(5) Event Counter Mode

The timer counts signals input through the CNTR0 pin. In this mode, timer X operates as the 18-bit counter by setting the timer X register (extension). When using this mode, set the port sharing the CNTR0 pin to input mode.
In this mode, the window control can be performed by the timer 1 underflow. When the bit 5 (data for control of event counter window) of the timer X mode register is set to "1", counting is stopped at the next timer 1 underflow. When the bit is set to "0", counting is restarted at the next timer 1 underflow.

(6) Pulse Width Measurement Mode

In this mode, the count source is the output of frequency divider for timer. In this mode, timer X operates as the 18-bit counter by setting the timer X register (extension). When the bit 6 of the CNTR0 active edge switch bits is "0", counting is executed during the "H" interval of CNTR0 pin input. When the bit is "1", counting is executed during the "L" interval of CNTR0 pin input. When using this mode, set the port sharing the CNTR0 pin to input mode.

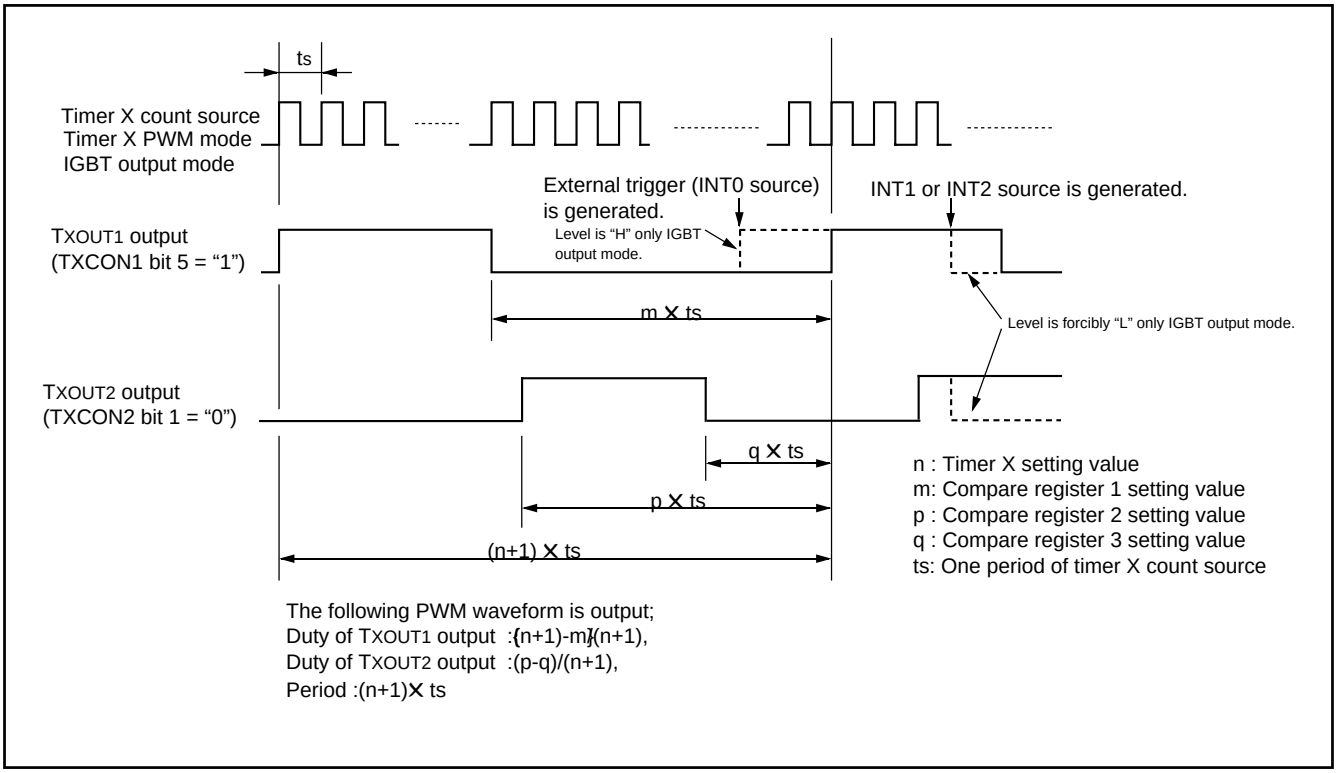


Fig. 26 Waveform of PWM/IGBT

■ Notes on Timer X

(1) Write Order to Timer X

- In the timer mode, pulse output mode, event counter mode and pulse width measurement mode, write to the following registers in the order as shown below;
  the timer X register (extension),
  the timer X register (low-order),
  the timer X register (high-order).
  Do not write to only one of them.
  When the above mode is set and timer X operates as the 16-bit counter, if the timer X register (extension) is never set after reset is released, setting the timer X register (extension) is not required. In this case, write the timer X register (low-order) first and the timer X register (high-order). However, once writing to the timer X register (extension) is executed, note that the value is retained to the reload latch.

- In the IGBT output and PWM modes, do not write "1" to the timer X register (extension). Also, when "1" is already written to the timer X register, be sure to write "0" to the register before using.
  Write to the following registers in the order as shown below;
  the compare registers 1, 2, 3 (high- and low-order),
  the timer X register (extension),
  the timer X register (low-order),
  the timer X register (high-order).
  It is possible to use whichever order to write to the compare registers 1, 2, 3 (high- and low-order). However, write both the compare registers 1, 2, 3 and the timer X register at the same time.

(2) Read Order to Timer X

- In all modes, read the following registers in the order as shown below;
  the timer X register (extension),
  the timer X register (high-order),
  the timer X register (low-order).
  When reading the timer X register (extension) is not required, read the timer X register (high-order) first and the timer X register (low-order).
  Read order to the compare registers 1, 2, 3 is not specified.
- Write to or read from the timer X register by the 16-bit unit. If reading to the timer X register during write operation or writing to it during read operation is performed, normal operation will not be performed.

(3) Write to Timer X

- Which write control can be selected by the timer X write control bit (b3) of the timer X mode register (address $2D_{16}$), writing data to both the latch and the timer at the same time or writing data only to the latch. When writing a value to the timer X address to write to the latch only, the value is set into the reload latch and the timer is updated at the next underflow. After reset release, when writing a value to the timer X address, the value is set into the timer and the timer latch at the same time, because they are written at the same time.
  When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the high-order reload latch.
- Do not switch the timer count source during timer count operation. Stop the timer count before switching it.

(4) Set of Timer X Mode Register

Set the write control bit of the timer X mode register to “1” (write to the latch only) when setting the IGBT output and PWM modes.
Output waveform simultaneously reflects the contents of both registers at the next underflow after writing to the timer X register (high-order).

(5) Output Control Function of Timer X

- When using the output control function (INT_1 and INT_2) in the IGBT output mode, set the levels of INT_1 and INT_2 to “H” in the falling edge active or to “L” in the rising edge active before switching to the IGBT output mode.

(6) Switch of $CNTR_0$ Active Edge

- When the $CNTR_0$ active edge switch bits are set, at the same time, the interrupt active edge is also affected.
- When the pulse width is measured, set the bit 7 of the $CNTR_0$ active edge switch bits to “0”.

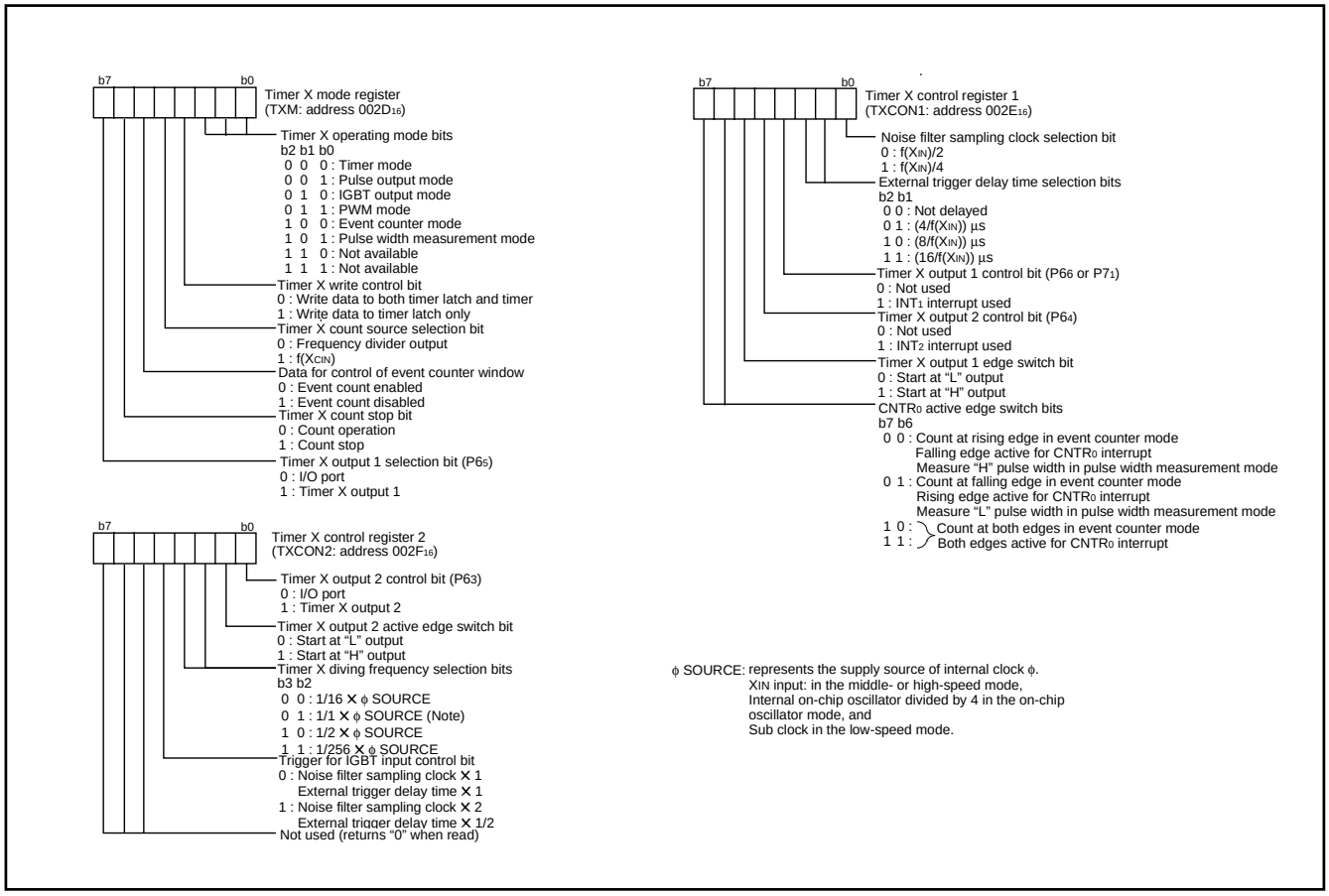


Fig. 27 Structure of Timer X related registers

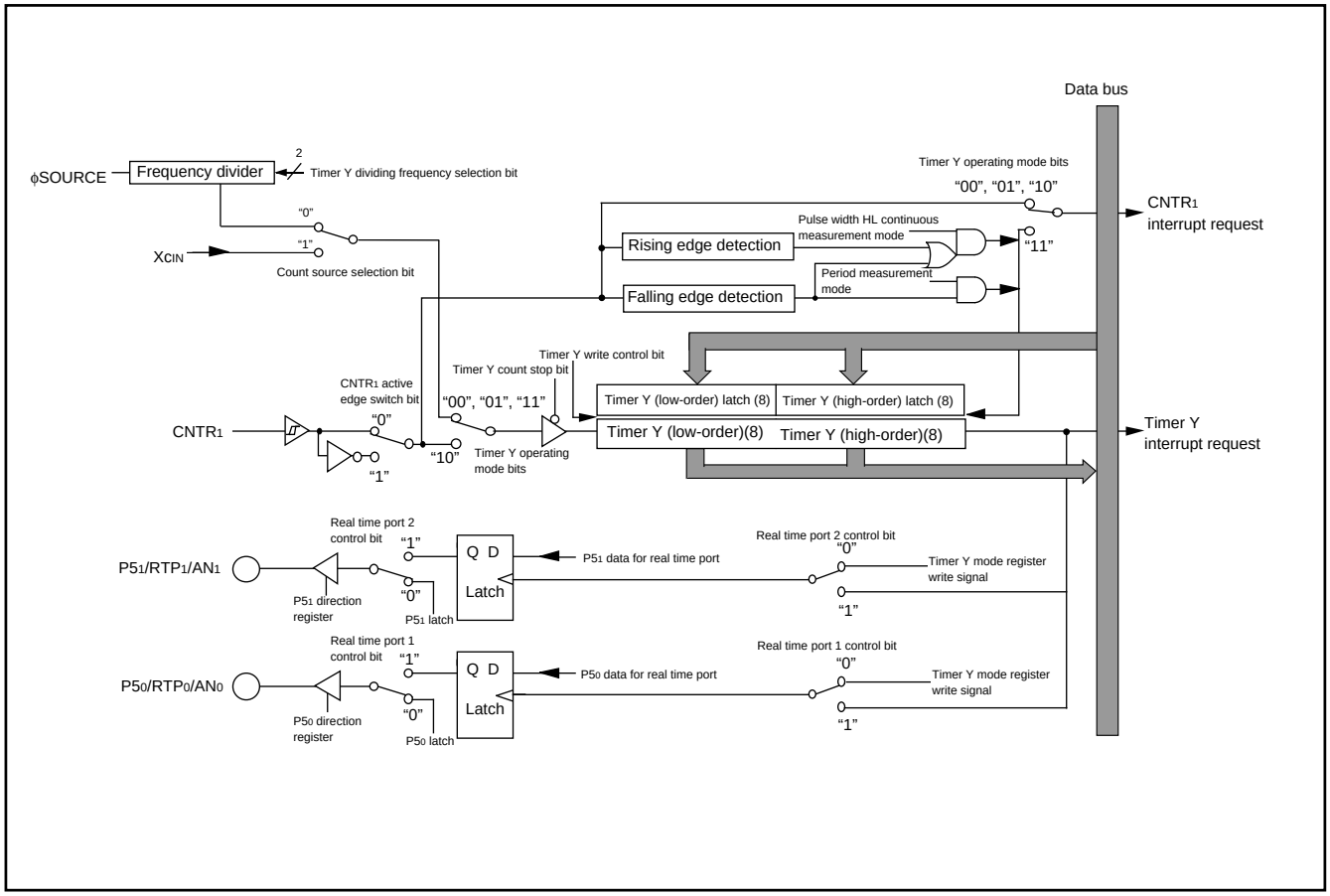


Fig. 28 Block diagram of Timer Y

Timer Y

Timer Y is a 16-bit timer. The timer Y count source can be selected by setting the timer Y mode register. When f(XCIN) is selected as the count source, counting can be performed regardless of XCIN oscillation. However, when XCIN is stopped, the external pulse input from XCIN pin is counted.

Four operating modes can be selected for timer Y by the timer Y mode register. Also, the real time port can be controlled.

(1) Timer Mode

The timer Y count source can be selected by setting the timer Y mode register.

(2) Period Measurement Mode

The interrupt request is generated at rising or falling edge of CNTR1 pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting. Except for that, this mode operates just as in the timer mode.

The timer value just before the reloading at rising or falling of CNTR1 pin input is retained until the timer Y is read once after the reload.

The rising or falling timing of CNTR1 pin input is found by CNTR1 interrupt. When using this mode, set the port sharing the CNTR1 pin to input mode.

(3) Event Counter Mode

The timer counts signals input through the CNTR1 pin.

Except for that, this mode operates just as in the timer mode.

When using this mode, set the port sharing the CNTR1 pin to input mode.

(4) Pulse Width HL Continuously Measurement Mode

The interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for that, this mode operates just as in the period measurement mode. When using this mode, set the port sharing the CNTR1 pin to input mode.

■ Notes on Timer Y

● CNTR1 Interrupt Active Edge Selection

CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit. However, in pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

● Timer Y Read/Write Control

- When reading from/writing to timer Y, read from/write to both the high-order and low-order bytes of timer Y. When the value is read, read the high-order bytes first and the low-order bytes next. When the value is written, write the low-order bytes first and the high-order bytes next.
  Write to or read from the timer X register by the 16-bit unit. If reading from the timer Y register during write operation or writing to it during read operation is performed, normal operation will not be performed.
- Which write control can be selected by the timer Y write control bit (b0) of the timer Y control register (address 0039_{16}), writing data to both the latch and the timer at the same time or writing data only to the latch. When writing a value to the timer Y address to write to the latch only, the value is set into the reload latch and the timer is updated at the next underflow. After reset release, when writing a value to the timer Y address, the value is set into the timer and the timer latch at the same time, because they are set to write at the same time.
  When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the high-order reload latch.
- Do not switch the timer count source during timer count operation. Stop the timer count before switching it.

● Real Time Port Control

When the real time port function is valid, data for the real time port is output from ports P50 and P51 each time the timer Y underflows. (However, if the real time port control bit is changed from “0” to “1” after the data for real time port is set, data is output independent of the timer Y operation.) When the data for the real time port is changed while the real time port function is valid, the changed data is output at the next underflow of timer Y. Before using this function, set the corresponding port direction registers to output mode.

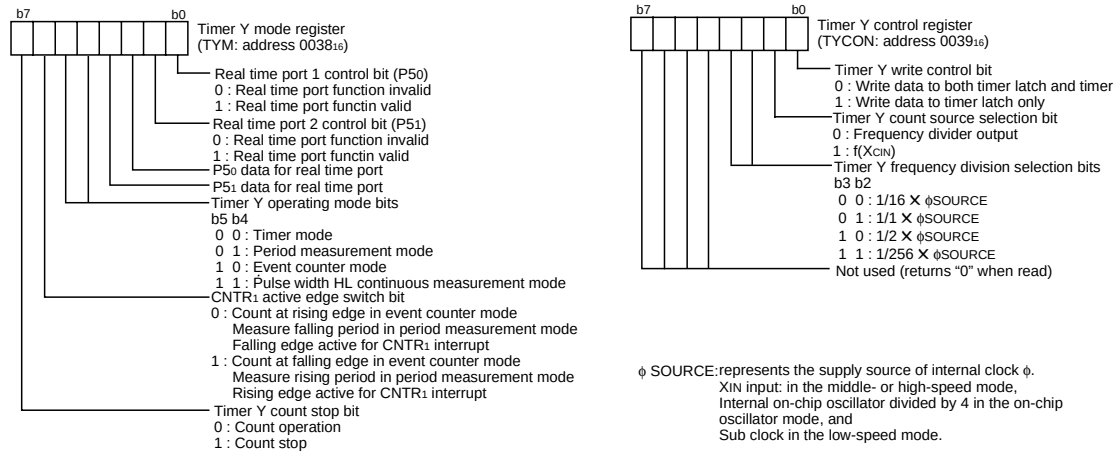


Fig. 29 Structure of Timer X related registers

SERIAL I/O
● Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O mode selection bit of the serial I/O1 control register to “1”. For clock synchronous serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

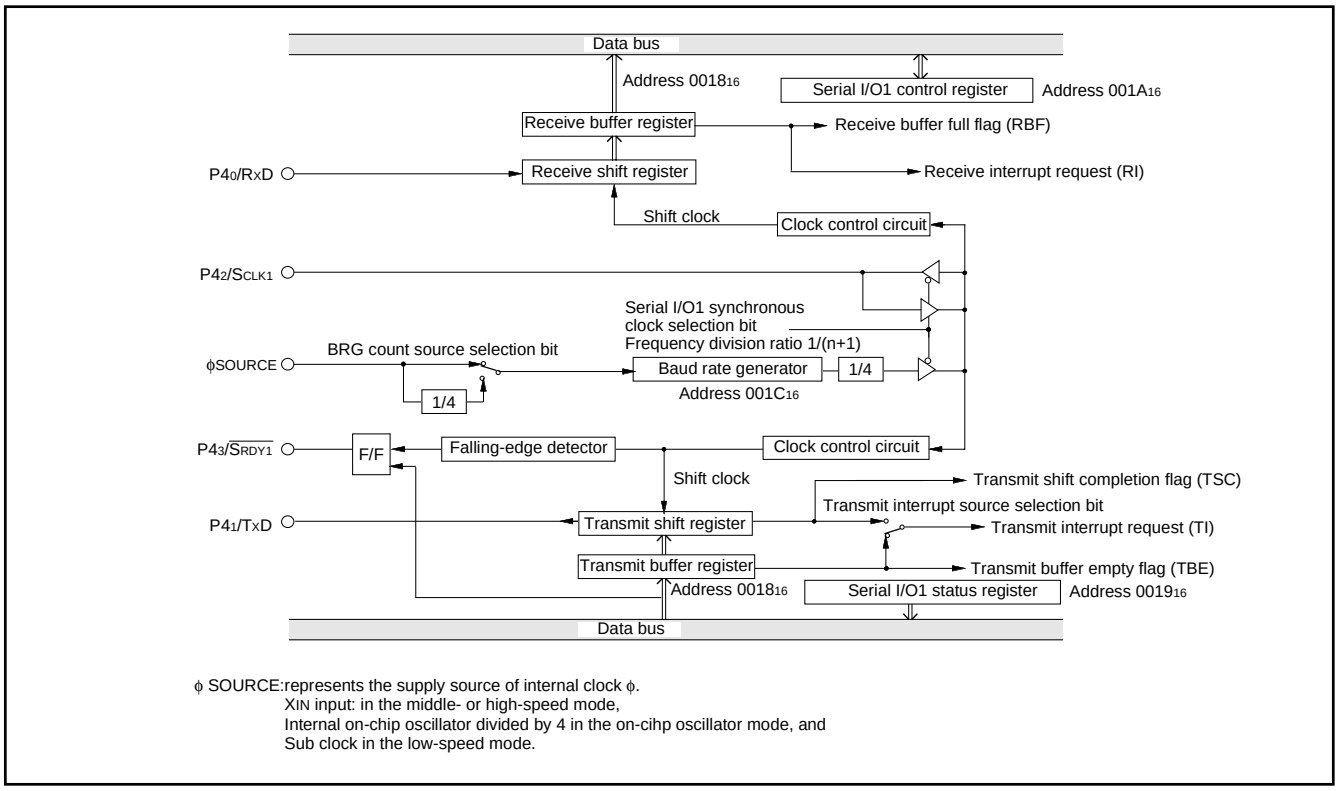
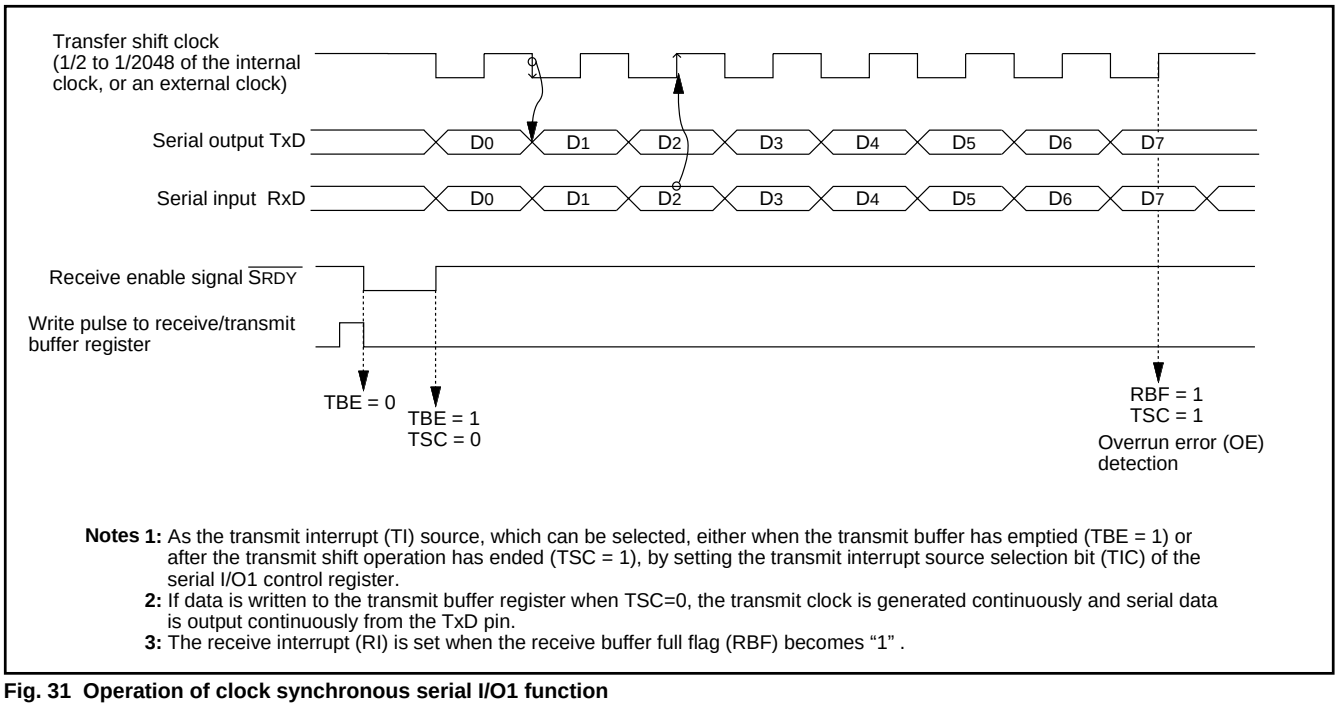


Fig. 30 Block diagram of clock synchronous serial I/O1



Notes 1: As the transmit interrupt (TI) source, which can be selected, either when the transmit buffer has emptied (TBE = 1) or after the transmit shift operation has ended (TSC = 1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes “1” .

Fig. 31 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by setting the serial I/O mode selection bit of the serial I/O1 control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

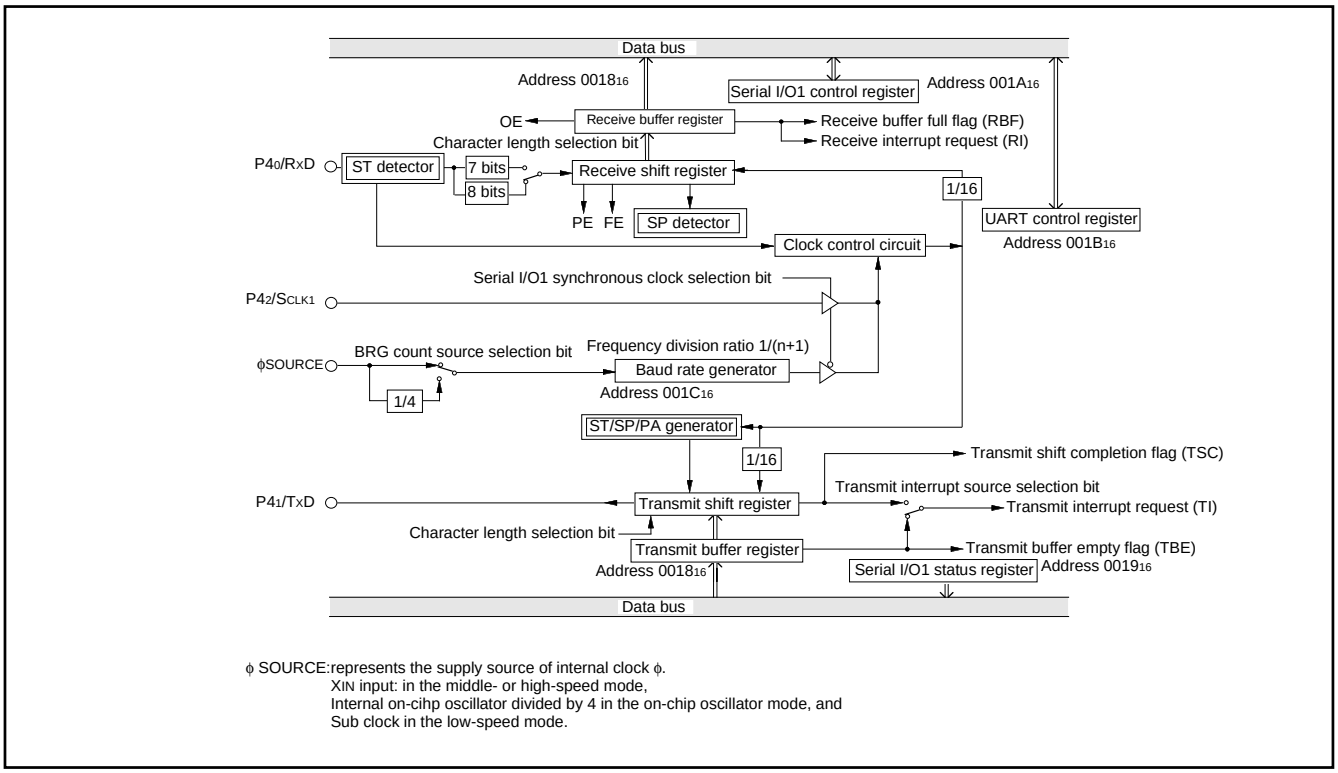
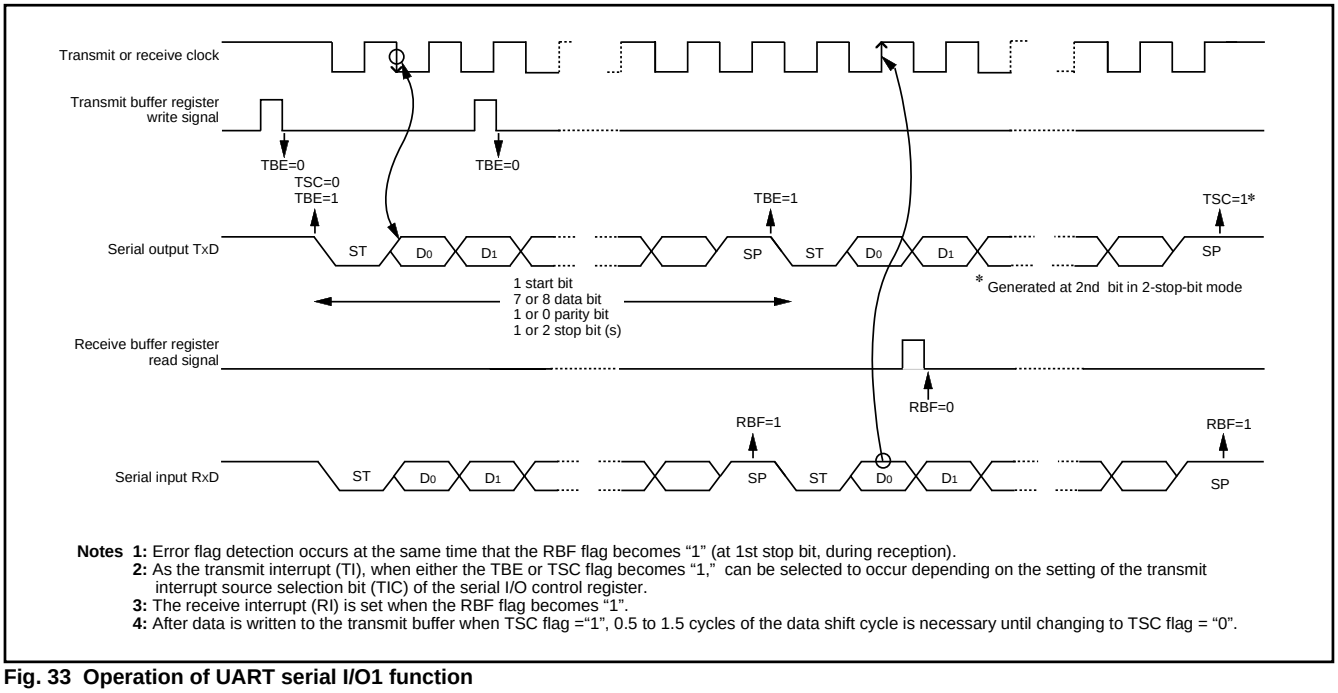


Fig. 32 Block diagram of UART serial I/O1



Notes
1: Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1,” can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1”.
4: After data is written to the transmit buffer when TSC flag =“1”, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC flag = “0”.

Fig. 33 Operation of UART serial I/O1 function

[Transmit Buffer Register/Receive Buffer Register (TB/RB)]

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is “0”.

[Serial I/O1 Status Register (SIO1STS)]

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is set to “0” when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register sets all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively) to “0”. Writing “0” to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also sets all the status flags to “0”, including the error flags.

All bits of the serial I/O1 status register are set to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to “1”, the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O1 Control Register (SIO1CON)]

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART Control Register (UARTCON)]

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P41/TxD pin.

[Baud Rate Generator (BRG)]

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■Notes on serial I/O1

When setting transmit enable bit of serial I/O1 to “1”, the serial I/O1 transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronous with the transmision enabled, take the following sequence.

①Set the serial I/O1 transmit interrupt enable bit to “0” (disabled).

②Set the transmit enable bit to “1”.

③Set the serial I/O1 transmit interrupt request bit to “0” after 1 or more instructions have been executed.

④Set the serial I/O1 transmit interrupt enable bit to “1” (enabled).

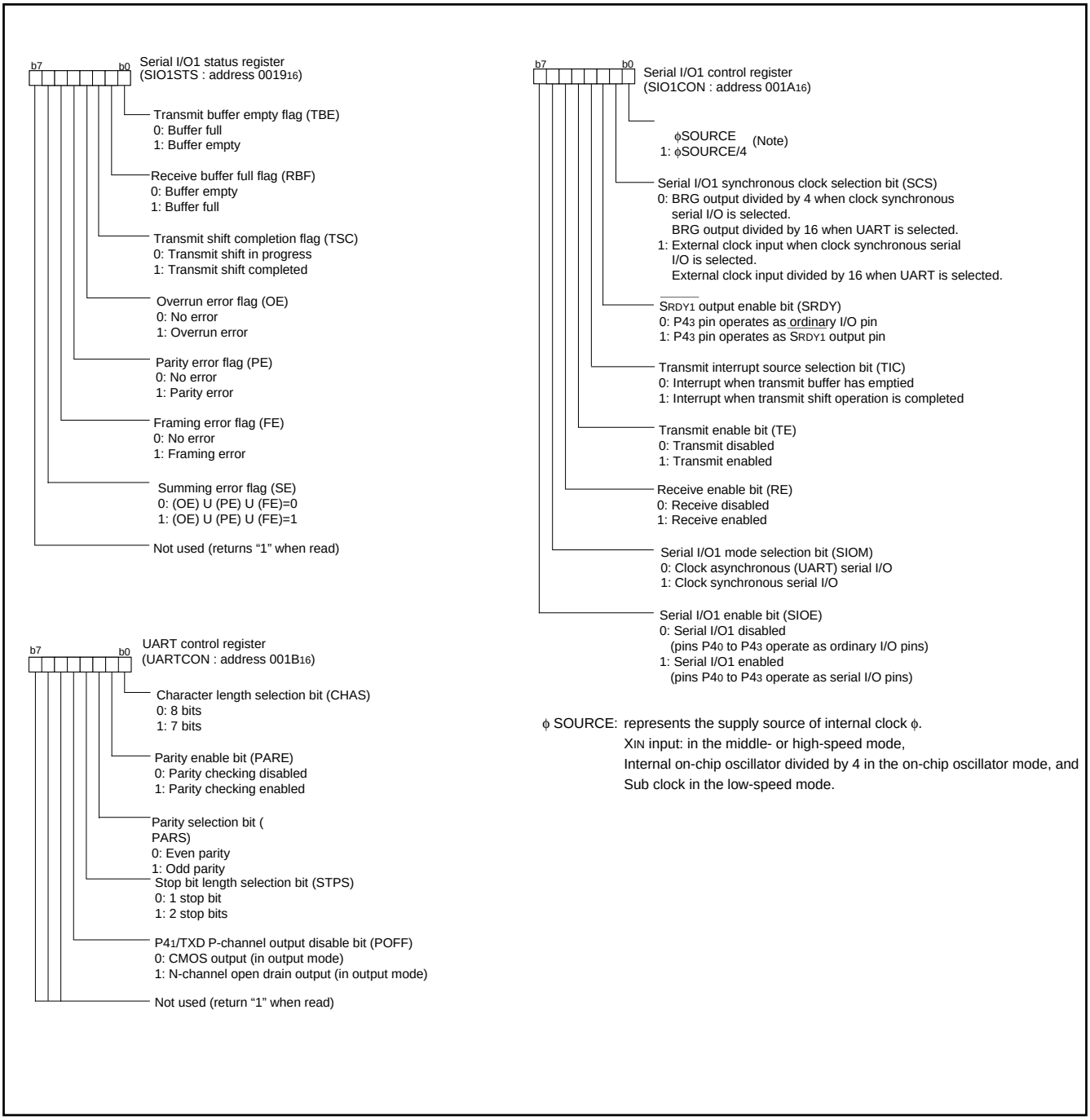


Fig. 34 Structure of serial I/O1 related registers

●Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For serial I/O2, the transmitter and the receiver must use the same clock. When the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

[Serial I/O2 control register] SIO2CON

The serial I/O2 control register contains 8 bits which control various serial I/O functions.

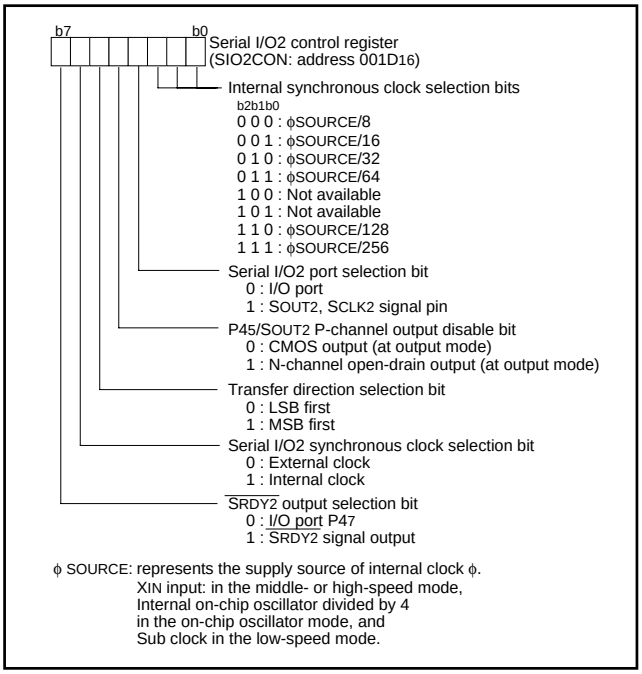


Fig. 35 Structure of serial I/O2 control registers

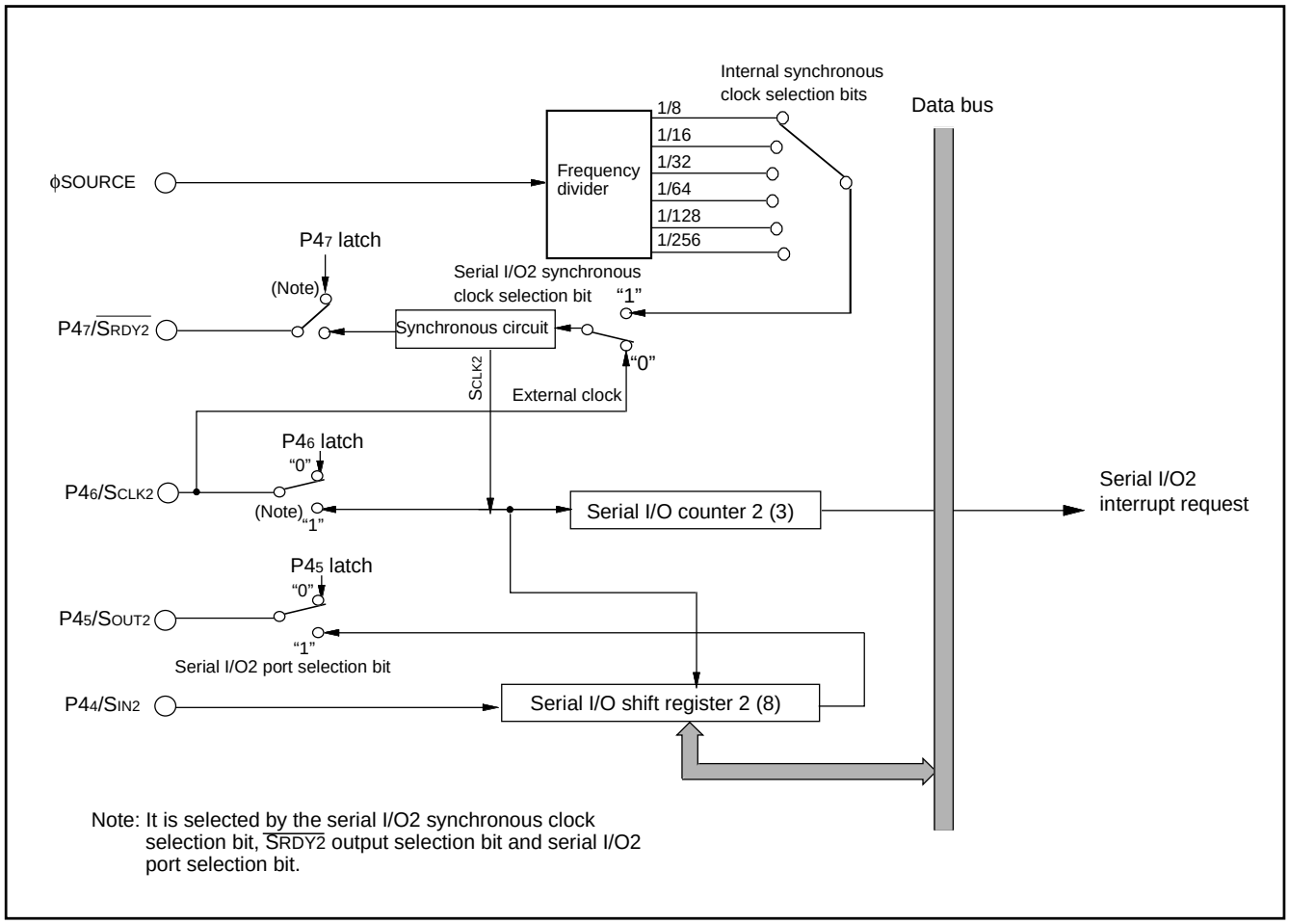
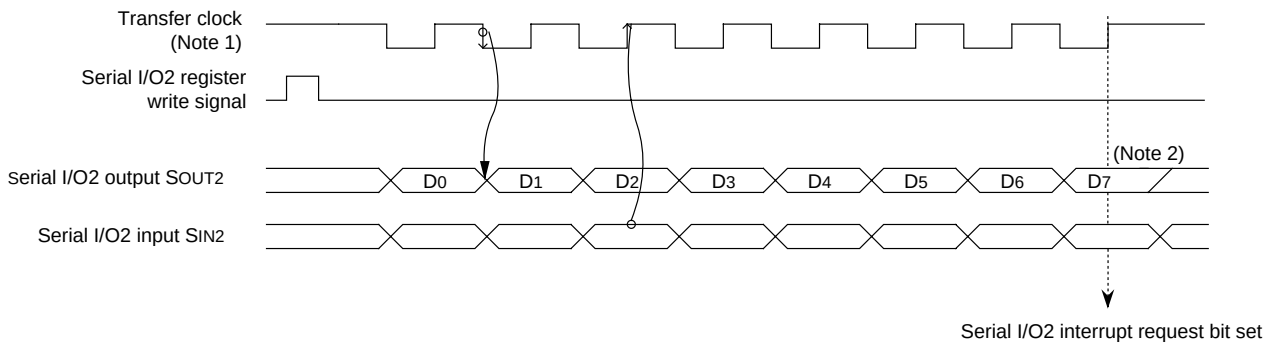


Fig. 36 Block diagram of serial I/O2



1: When the internal clock is selected as the transfer, the dividing frequency of internal clock for transfer clock can be selected by bits 0 to 2 of serial I/O2 control register.
2: When the internal clock is selected as the transfer, the SOUT2 pin is in a high impedance state after the data transfer is completed.
When the external clock is selected as the transfer, the contents of serial I/O shift register keeps shifting during the transmit/receive clock is input.
Also, the SOUT2 pin is not in a high impedance state after the data transfer is completed.

Fig. 37 Serial I/O2 timing

A/D CONVERTER

The 38C5 group has a 10-bit A/D converter. The A/D converter performs successive approximation conversion.The 38C5 group has the ADKEY function which perform A/D conversion of the “L” level analog input from the ADKEY pin automatically.

[A/D Conversion Register (ADL, ADH)]

One of these registers is a high-order register, and the other is a low-order register. The high-order 8 bits of a conversion result is stored in the A/D conversion register (high-order) (address 0017_{16}), and the low-order 2 bits of the same result are stored in bit 7 and bit 6 of the A/D conversion register (low-order) (address 0016_{16}).
During A/D conversion, do not read these registers.
Also, the connection between the resistor ladder and reference voltage input pin (V_{REF}) can be controlled by the V_{REF} input switch bit (bit 0 of address 0016_{16}). When “1” is written to this bit, the resistor ladder is always connected to V_{REF}. When “0” is written to this bit, the resistor ladder is disconnected from V_{REF} except during the A/D conversion.

[A/D Control Register (ADCON)]

This register controls A/D converter. Bits 2 to 0 are analog input pin selection bits. Bit 3 is an AD conversion completion bit and “0” during A/D conversion. This bit is set to “1” upon completion of A/D conversion. A/D conversion is started by setting “0” in this bit.
Bit 5 is the ADKEY enable bit. The ADKEY function is enabled by setting “1” to this bit. When this function is valid, the analog input selection bit is ignored. Also, when bit 5 is “1”, do not set “0” to bit 3 by program.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF}, and outputs the divided voltages.

[Channel Selector]

The channel selector selects one of the input ports $P5_7/AN_7$–$P5_0/AN_0$ and inputs it to the comparator.

[Comparator and Control Circuit]

The comparator and control circuit compare an analog input voltage with the comparison voltage and store the result in the A/D conversion register. When an A/D conversion is completed, the control circuit sets the AD conversion completion bit and the AD conversion interrupt request bit to “1.”
The comparator is constructed linked to a capacitor. The conversion accuracy may be low because the change is lost if the conversion speed is not enough.
Accordingly, set $f(X_{IN})$ to at least 500 kHz during A/D conversion in the middle- or high- speed mode.
Also, do not execute the STP and WIT instructions during the A/D conversion.
In the low-speed mode, since the A/D conversion is executed by the built-in self-oscillation circuit, the minimum value of $f(X_{IN})$ frequency.

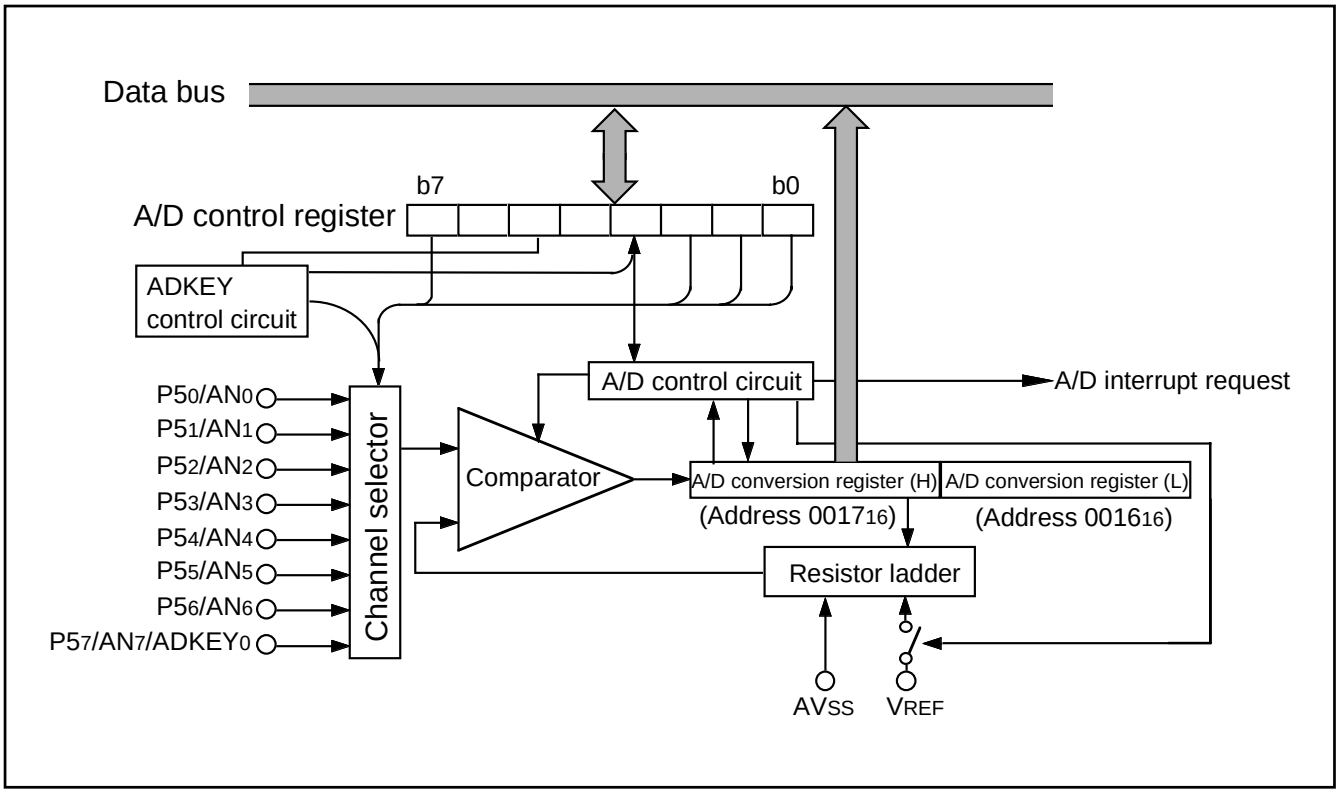


Fig. 38 Block diagram of A/D converter

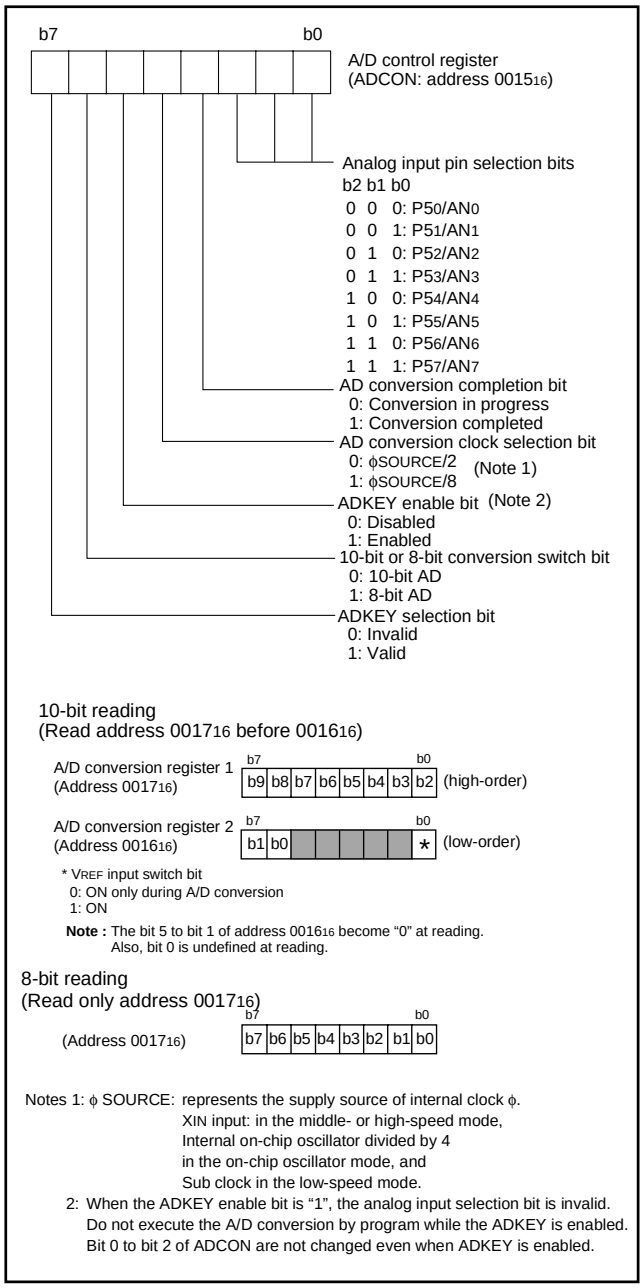


Fig. 39 Structure of A/D control register

ADKEY function

The ADKEY function is used to judge the analog input voltage input from the ADKEY pin. When the A/D converter starts operating after V_{IL} (0.7 × Vcc-0.5) or less is input, the event of analog voltage input can be judged with the A/D conversion interrupt.
This function can be used with the STP and WIT state.
As for the ADKEY function in 38C5 group, the A/D conversion of analog input voltage immediately after starting ADKEY function is not performed.
Therefore, the A/D conversion result immediately after an ADKEY function is undefined. Accordingly, when the A/D conversion result of the analog input voltage input from the ADKEY pin is required, start the A/D conversion by program after the analog input pin corresponding to ADKEY is selected.

• ADKEY Selection

When the ADKEY pin is used, set the ADKEY selection bit to “1”. The ADKEY selection bit is “0”, just after the A/D conversion is started.

• ADKEY Enable

The ADKEY function is enabled by writing “1” to the ADKEY enable bit. Surely, in order to enable ADKEY function, set “1” to the ADKEY enable bit, after setting the ADKEY selection bit to “1”.
When the ADKEY enable bit of the AD control register is “1”, the analog input pin selection bits become invalid. Please do not write “0” in the AD conversion completion bit by the program during ADKEY enabled state.

[ADKEY Control Circuit]

In order to obtain a more exact conversion result, by the A/D conversion with ADKEY, execute the following;

- set the input to the ADKEY pin into a steep falling waveform,
- stabilize the input voltage within 8 clock cycles (1 µs at f(X_{IN}) = 8 MHz) after the input voltage is under V_{IL}, and
- maintain the input voltage until the completion of the A/D conversion.

The threshold voltage with an actual ADKEY pin is the voltage between V_{IH}-V_{IL}.
In order not to make ADKEY operation perform superfluously in a noise etc., in the state of the waiting for an input, set the voltage of an ADKEY pin to V_{IH} (0.9V_{CC}) or more.
When the following operations are performed, the A/D conversion operation cannot be guaranteed.

- When the CPU mode register is operated during A/D conversion operation,
- When the AD conversion control register is operated during A/D conversion operation,
- When the STP or WIT instruction is executed during A/D conversion operation.

LCD DRIVE CONTROL CIRCUIT

The 38C5 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

- LCD display RAM
- Segment output disable register
- LCD mode register
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

A maximum of 36 segment output pins and 8 common output pins can be used.

Up to 256 pixels can be controlled for an LCD display. When the LCD enable bit is set to “1” after data is set in the LCD mode register, the segment output disable register, and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 8 Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixels
1	36 dots or 8 segment LCD 4 digits
2	72 dots or 8 segment LCD 6 digits
3	108 dots or 8 segment LCD 9 digits
4	144 dots or 8 segment LCD 12 digits
8	256 dots or 8 segment LCD 32 digits

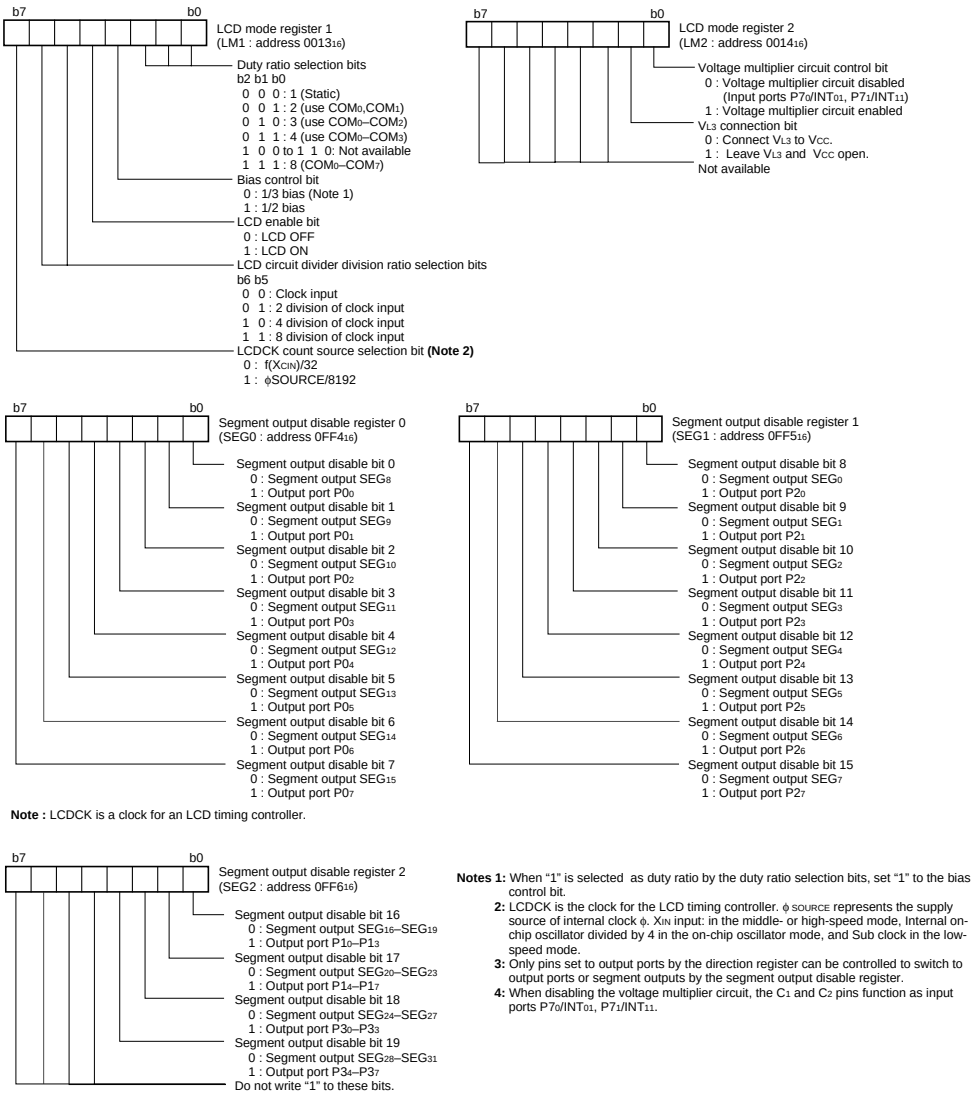
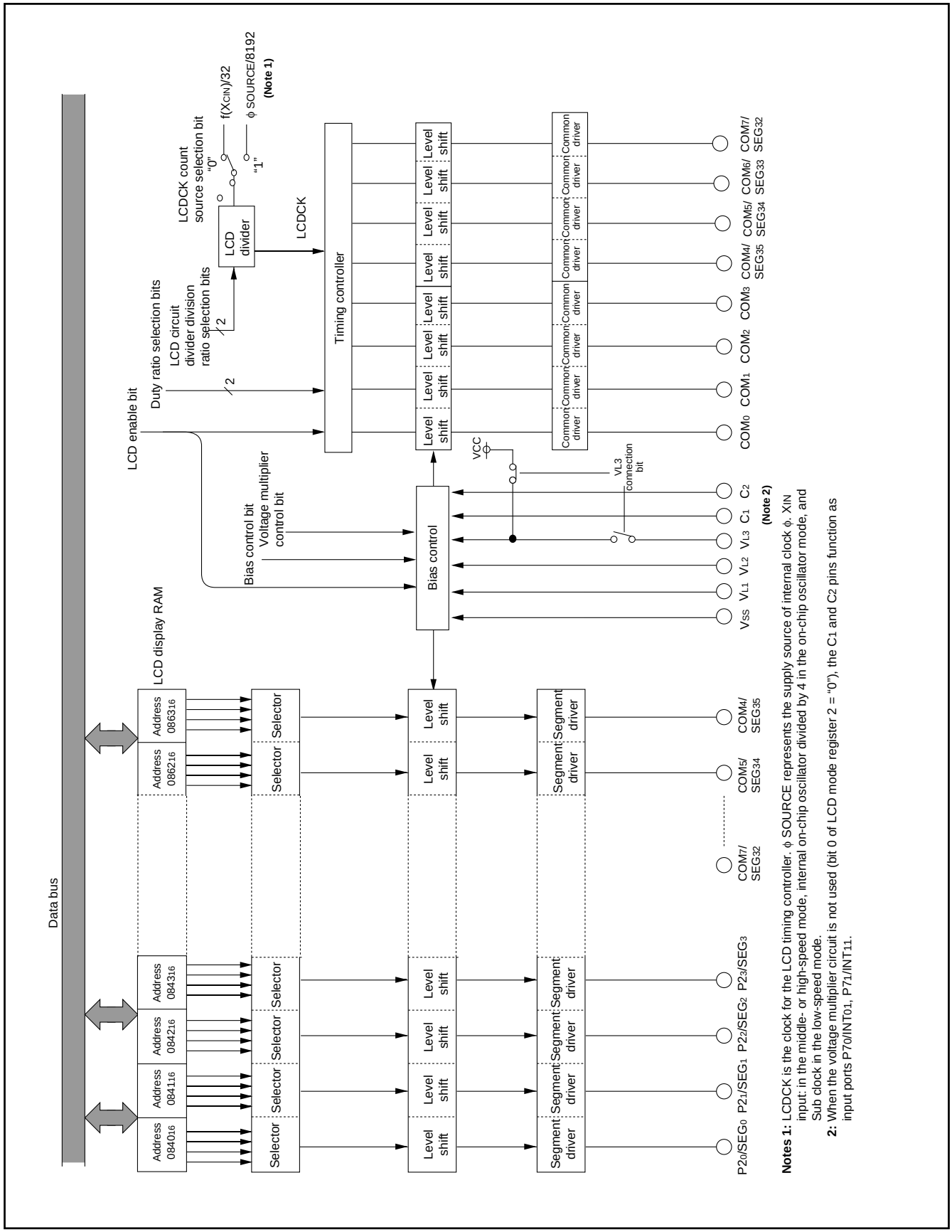


Fig. 40 Structure of LCD related registers



Notes 1: LCDCK is the clock for the LCD timing controller. φ SOURCE represents the supply source of internal clock φ. XIN input: in the middle- or high-speed mode, internal on-chip oscillator divided by 4 in the on-chip oscillator mode, and Sub clock in the low-speed mode.

2: When the voltage multiplier circuit is not used (bit 0 of LCD mode register 2 = "0"), the C1 and C2 pins function as input ports P70/INT01, P71/INT11.

Fig. 41 Block diagram of LCD controller/driver

Voltage Multiplier

The voltage multiplier performs threefold boosting. This circuit inputs a reference voltage for boosting from LCD power input pin V_{L1}. Set each bit of the segment output disable registers and the LCD mode registers in the following order for operating the voltage multiplier.

1. Set the segment output disable bits (bits 0 to 19) of the segment output disable registers (SEG0, 1, 2) to “0” or “1”.
2. Set the duty ratio selection bits (bits 0 to 2), the bias control bit (bit 3), the LCD circuit divider division ratio selection bits (bits 5 and 6), and the LCDCK count source selection bit (bit 7) of the LCD mode register 1 to “0” or “1”.
3. Set the V_{L3} connection bit (bit 1 of the LCD mode register 2 (LM2)) to “1”. Apply the limit voltage or less to the V_{L1} pin.
4. Set the voltage multiplier control bit (bit 0) of the LCD mode register 2 to “1”. However, be sure to select 1/3 bias for bias control.

When voltage is input to the V_{L1} pin during operating the voltage multiplier, voltage that is twice as large as V_{L1} occurs at the V_{L2} pin, and voltage that is three times as large as V_{L1} occurs at the V_{L3} pin.

The voltage multiplier is controlled by the voltage multiplier control bit (bit 0 of the LCD mode register 2).
In addition, when the voltage multiplier is used, set the voltage multiplier control bit to “1” (voltage multiplier enabled) after the voltage 1.3 V or more and 2.1 V or less.
When the voltage multiplier is not used, set the V_{L3} connection bit to “0” (open), and apply the suitable voltage for the power supply input pins for LCD (V_{L1}-V_{L3}).
When V_{L3} connection bit is set to be connected, V_{L3} pin is in a high impedance state.

Bias Control and Applied Voltage to LCD Power Input Pins

Apply the voltage value shown in Table 9 according to the bias value to the LCD power input pins.
Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Table 9 Bias control and applied voltage to V_{L1}–V_{L3}

Bias value	Voltage value
1/4 bias	$V_{L3}=V_{LCD}$ $V_{L2}=3/4$ $V_{L1}=1/4$
1/3 bias	$V_{L3}=V_{LCD}$ $V_{L2}=2/3\ V_{LCD}$ $V_{L1}=1/3\ V_{LCD}$
1/2 bias	$V_{L3}=V_{LCD}$ $V_{L2}=V_{L1}=1/2\ V_{LCD}$

Note : V_{LCD} is the maximum value of supplied voltage for the LCD panel.

Common Pin and Duty Ratio Control

The common pins (COM_0–COM_7) to be used are determined by duty ratio. Select duty ratio by the duty ratio selection bits (bits 0, 1 and 2 of the LCD mode register 1). When reset is released, V_{CC} voltage is output from the common pin.

Table 10 Duty ratio control and common pins used

Duty ratio	Duty ratio selection bits			Common pins used
	Bit 2	Bit 1	Bit 0	
1	0	0	0	COM_0
2	0	0	1	COM_0, COM_1
3	0	1	0	COM_0–COM_2
4	0	1	1	COM_0–COM_3
8	1	1	1	COM_0–COM_7

Note: Unused common pin outputs the unselected waveform.

Segment Signal Output Pin

The segment signal output pins (SEG_0–SEG_{31}) are shared with ports P0–P3. When these pins are used as the segment signal output pins, set the direction registers of the corresponding pins to “1”, and set the segment output disable register to “0”.
Also, these pins are set to the input port after reset, the V_{CC} voltage is output by the pull-up resistor.

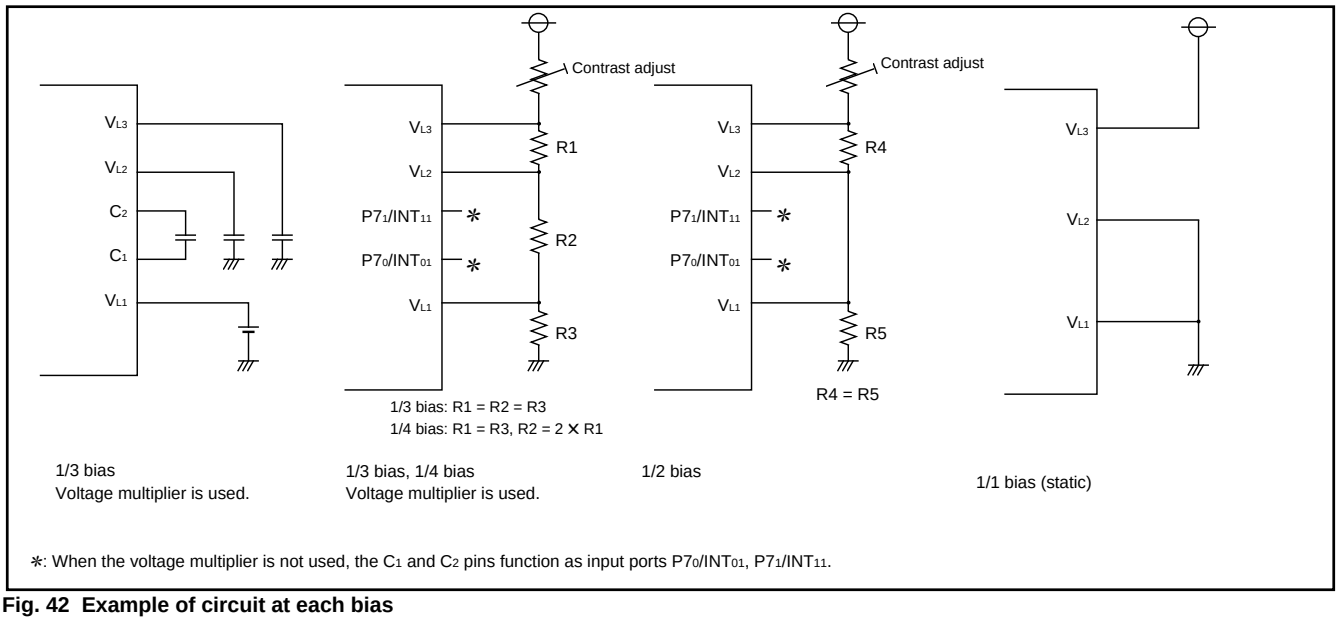


Fig. 42 Example of circuit at each bias

LCD Display RAM

The 36-byte area of address 0840_{16} to 0863_{16} is the designated RAM for the LCD display. When "1" is written to these addresses, the corresponding segments of the LCD display panel are turned on.

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(LCDCK)=\frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency}=\frac{f(LCDCK)}{\text{duty ratio}}$$

at 4COM × 36SEG

Address \ Bits	7	6	5	4	3	2	1	0
0840_{16}	Not used (This area can be used as normal RAM.)				SEG0			
0841_{16}					SEG1			
0842_{16}					SEG2			
0843_{16}					SEG3			
0844_{16}					SEG4			
0845_{16}					SEG5			
0846_{16}					SEG6			
0847_{16}					SEG7			
0848_{16}					SEG8			
0849_{16}					SEG9			
$084A_{16}$					SEG10			
$084B_{16}$					SEG11			
$084C_{16}$					SEG12			
$084D_{16}$					SEG13			
$084E_{16}$					SEG14			
$084F_{16}$					SEG15			
0850_{16}					SEG16			
0851_{16}					SEG17			
0852_{16}					SEG18			
0853_{16}					SEG19			
0854_{16}					SEG20			
0855_{16}					SEG21			
0856_{16}					SEG22			
0857_{16}					SEG23			
0858_{16}					SEG24			
0859_{16}					SEG25			
$085A_{16}$					SEG26			
$085B_{16}$					SEG27			
$085C_{16}$					SEG28			
$085D_{16}$					SEG29			
$085E_{16}$					SEG30			
$085F_{16}$					SEG31			
0860_{16}								
0861_{16}								
0862_{16}								
0863_{16}								
					COM3	COM2	COM1	COM0

at 8COM × 32SEG

Address \ Bits	7	6	5	4	3	2	1	0
0840_{16}	SEG0							
0841_{16}	SEG1							
0842_{16}	SEG2							
0843_{16}	SEG3							
0844_{16}	SEG4							
0845_{16}	SEG5							
0846_{16}	SEG6							
0847_{16}	SEG7							
0848_{16}	SEG8							
0849_{16}	SEG9							
$084A_{16}$	SEG10							
$084B_{16}$	SEG11							
$084C_{16}$	SEG12							
$084D_{16}$	SEG13							
$084E_{16}$	SEG14							
$084F_{16}$	SEG15							
0850_{16}	SEG16							
0851_{16}	SEG17							
0852_{16}	SEG18							
0853_{16}	SEG19							
0854_{16}	SEG20							
0855_{16}	SEG21							
0856_{16}	SEG22							
0857_{16}	SEG23							
0858_{16}	SEG24							
0859_{16}	SEG25							
$085A_{16}$	SEG26							
$085B_{16}$	SEG27							
$085C_{16}$	SEG28							
$085D_{16}$	SEG29							
$085E_{16}$	SEG30							
$085F_{16}$	SEG31							
0860_{16}	Not used (This area can be used as normal RAM.)							
0861_{16}								
0862_{16}								
0863_{16}								
	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0

Fig. 43 LCD display RAM map

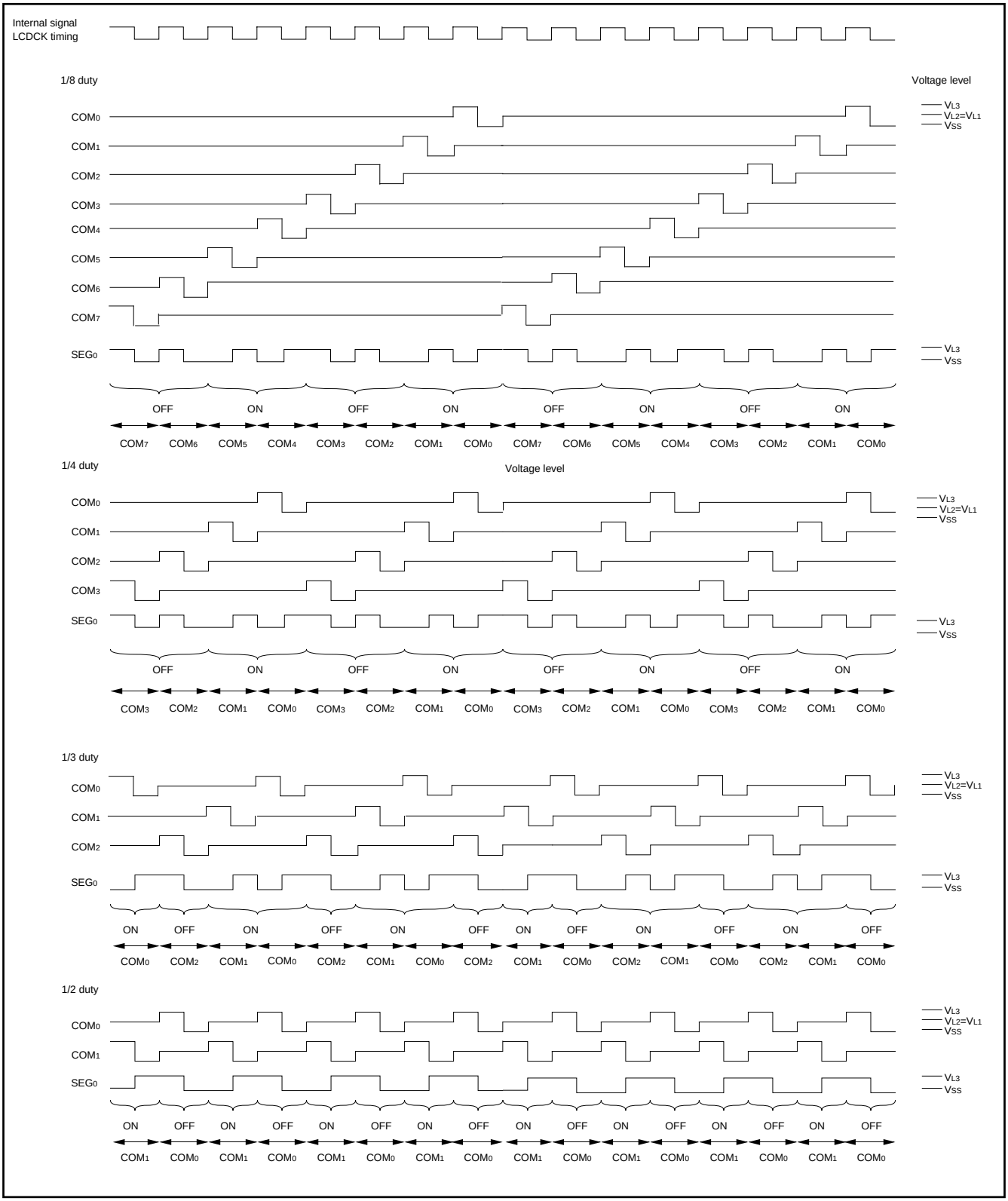


Fig. 44 LCD drive waveform (1/2 bias)

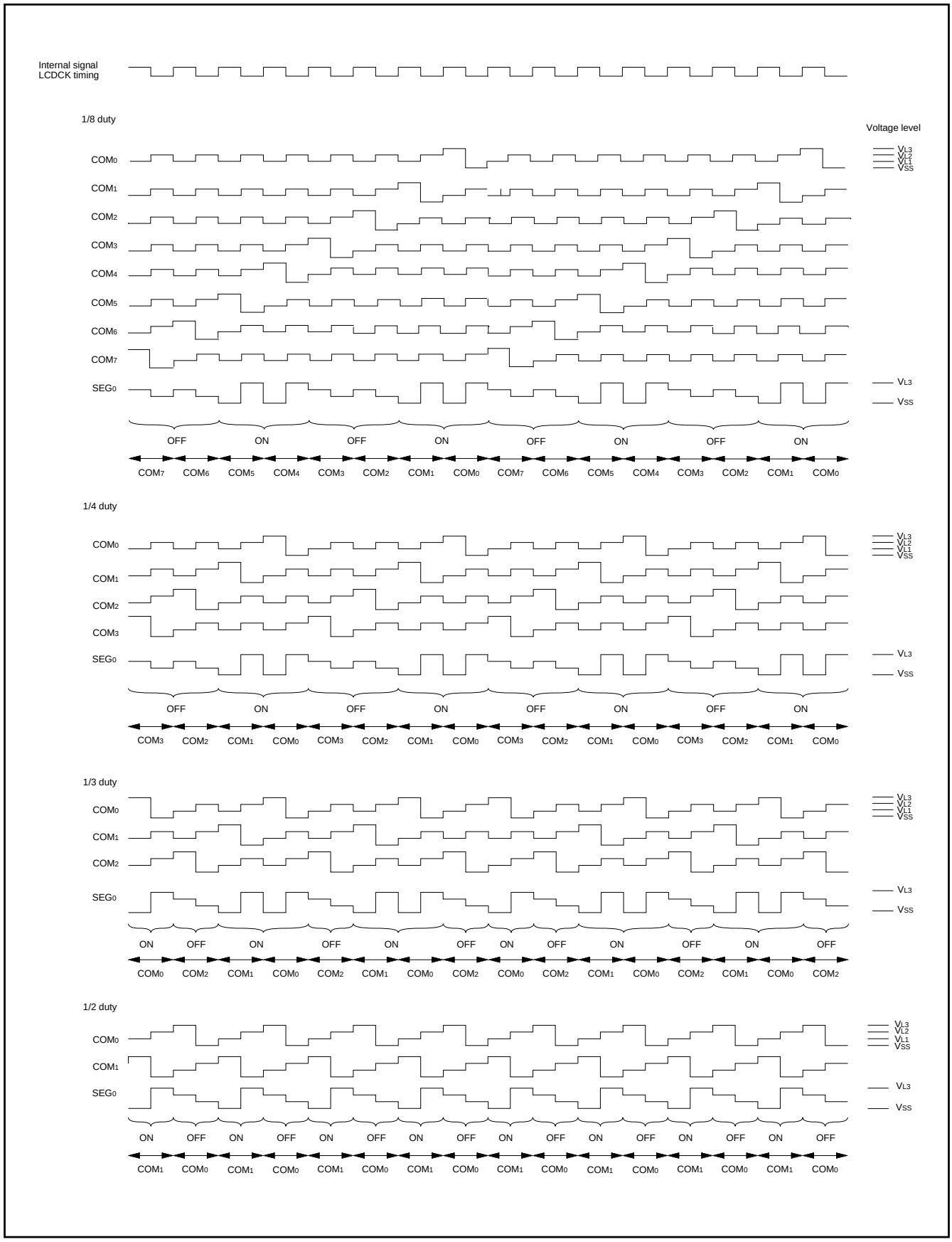


Fig. 45 LCD drive waveform (1/3 bias)

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit counter.

Initial Value of Watchdog Timer

At reset or writing to the watchdog timer control register, each watchdog timer is set to "FF16." Instructions such as STA, LDM and CLB to generate the write signals can be used.
The written data in bits 0 to 5 are not valid, and the above values are set.

Standard Operation of Watchdog Timer

The watchdog timer is in the stop state at reset and the watchdog timer starts to count down by writing an optional value in the watchdog timer control register. An internal reset occurs at an underflow of the watchdog timer. Then, reset is released after the reset release time is elapsed, the program starts from the reset vector address. Normally, writing to the watchdog timer control register before an underflow of the watchdog timer is programmed. If writing to the watchdog timer control register is not executed, the watchdog timer does not operate.

When reading the watchdog timer control register is executed, the contents of the high-order 6-bit counter and the STP instruction disable bit (bit 6), and the count source selection bit (bit 7) are read out. When the STP instruction disable bit is "0", the STP instruction is valid. The STP instruction is disabled by writing to "1" to this bit. In this time, when the STP instruction is executed, it is handled as the undefined instruction, the internal reset occurs. This bit cannot be set to "0" by program. This bit is "0" after reset.
The time until the underflow of the watchdog timer register after writing to the watchdog timer control register is executed is as follows (when the bit 7 of the watchdog timer control register is "0") ;

- at high-speed and middle-speed mode (f(XIN)) = 8 MHz): 32.768 ms
- at low-speed mode (f(XCIN) = 32 KHz): 8.19s

■ Note

The watchdog timer continues to count even during the wait time set by timer 1 and timer 2 to release the stop state and in the wait mode. Accordingly, do not underflow the watchdog timer in this time.

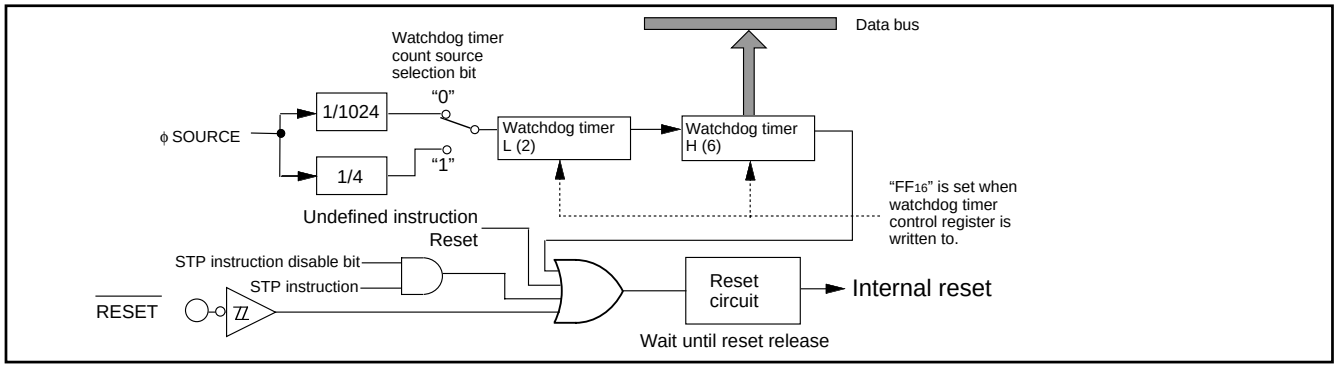


Fig. 46 Block diagram of Watchdog timer

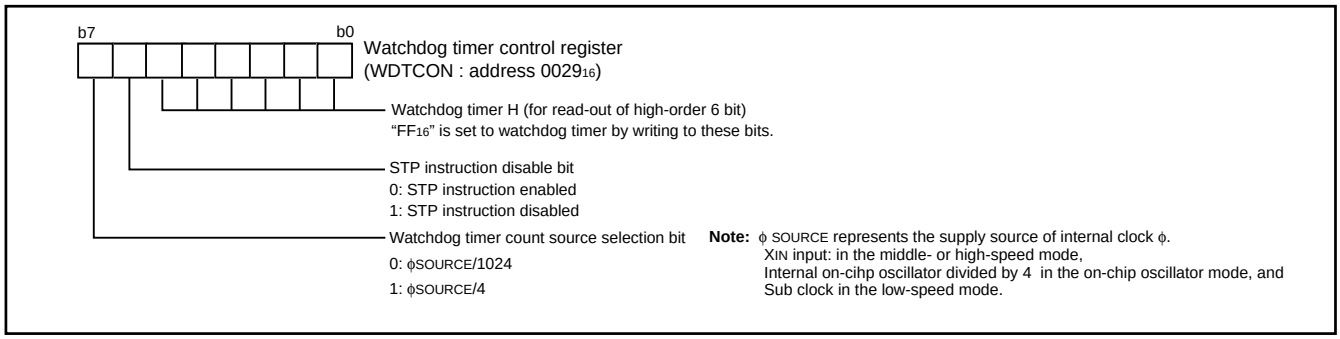


Fig. 47 Structure of Watchdog timer control register

CLOCK OUTPUT FUNCTION

A system clock ϕ can be output from I/O port P7$_2$.The triple function of I/O port, timer 2 output function and system clock ϕ output function are controlled by the clock output control register (address 0FF3$_{16}$) and the timer 2 output selection bit of the timer 12 mode register (address 0025$_{16}$).

In order to output a system clock ϕ from I/O port P7$_2$, set the timer 2 output selection bit to "1" and P7$_2$ clock output control bits of the clock output control register to "01". In order to output the same signal as oscillation frequency of sub clock XCIN, set the P7$_2$ clock output control bits to "10". When the clock output function is selected, a clock is output while the direction register of port P7$_2$ is set to the output mode.

P7$_2$ is switched to the port output or the output (timer 2 output or the clock output) except port at the cycle after the P7$_2$ clock output control bits are switched.

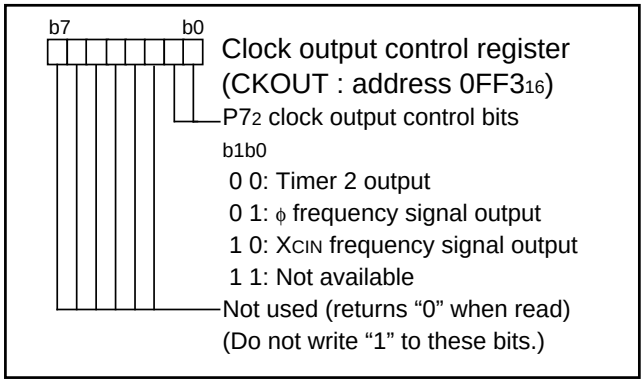


Fig. 48 Structure of clock output control register

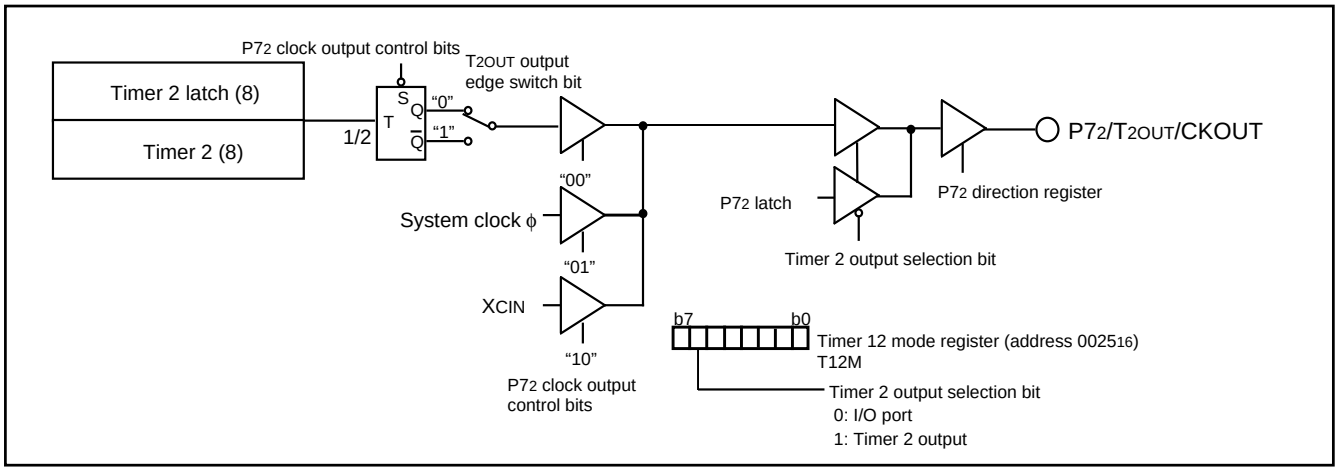


Fig. 49 Block diagram of Clock output function

Other function registers

The RRF register (address 0012_{16}) is the 8-bit register and does not have the control function.

As for the value written in this register, high-order 4 bits and low-order 4 bits interchange.

It is initialized after reset.

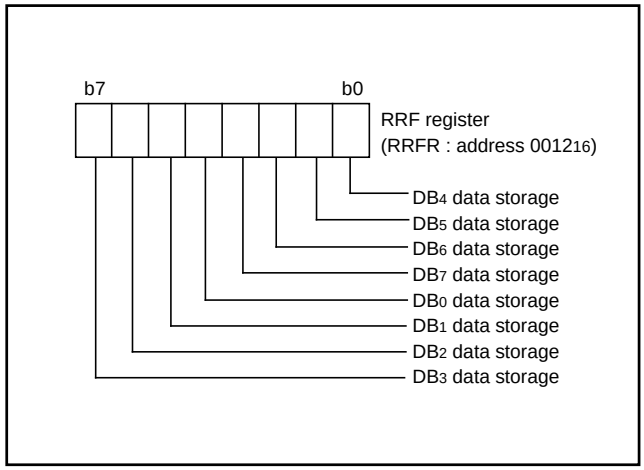


Fig. 50 Structure of RRF register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an “H” level (the power source voltage should be between V_{CC} (min.) and 5.5 V, and the quartz-crystal oscillator should be stable), reset is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage meets V_{IL} spec. when a power source voltage passes V_{CC} (min.).

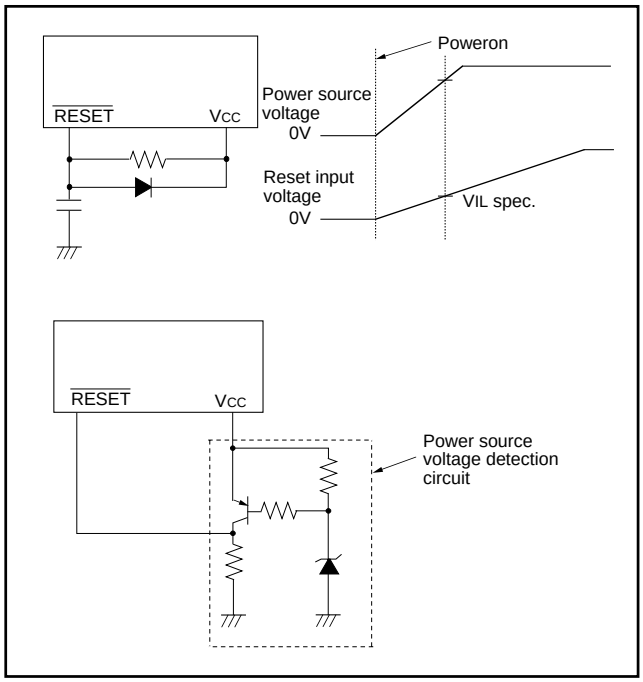
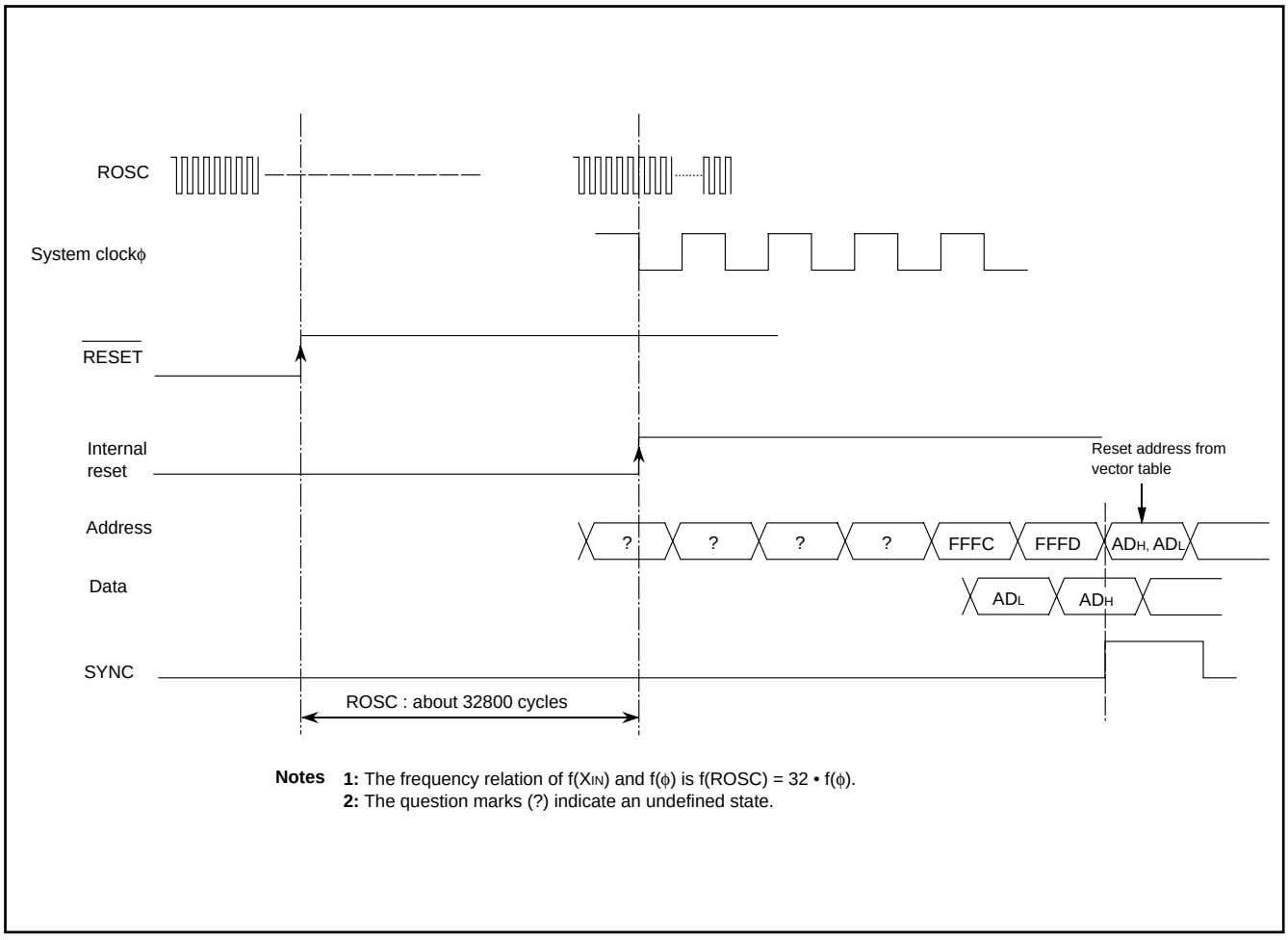


Fig. 51 Reset circuit example



Notes **1:** The frequency relation of $f(X_{IN})$ and $f(\phi)$ is $f(ROSC) = 32 \cdot f(\phi)$.
2: The question marks (?) indicate an undefined state.

Fig. 52 Reset sequence

	Address	Register contents
(1) Port P0	0000_{16}	00_{16}
(2) Port P0 direction register	0001_{16}	00_{16}
(3) Port P1	0002_{16}	00_{16}
(4) Port P1 direction register	0003_{16}	00_{16}
(5) Port P2	0004_{16}	00_{16}
(6) Port P2 direction register	0005_{16}	00_{16}
(7) Port P3	0006_{16}	00_{16}
(8) Port P3 direction register	0007_{16}	00_{16}
(9) Port P4	0008_{16}	00_{16}
(10) Port P4 direction register	0009_{16}	00_{16}
(11) Port P5	$000A_{16}$	00_{16}
(12) Port P5 direction register	$000B_{16}$	00_{16}
(13) Port P6	$000C_{16}$	00_{16}
(14) Port P6 direction register	$000D_{16}$	00_{16}
(15) Port P7	$000E_{16}$	00_{16}
(16) Port P7 direction register	$000F_{16}$	00_{16}
(17) RRF register (RRFR)	0012_{16}	00_{16}
(18) LCD mode register 1	0013_{16}	00_{16}
(19) LCD mode register 2	0014_{16}	00_{16}
(20) A/D control register	0015_{16}	08_{16}
(21) Serial I/O1 status register	0019_{16}	1 0 0 0 0 0 0 0
(22) Serial I/O1 control register	$001A_{16}$	00_{16}
(23) UART control register	$001B_{16}$	1 1 1 0 0 0 0 0
(24) Serial I/O2 control register	$001D_{16}$	00_{16}
(25) Timer 1	0020_{16}	FF_{16}
(26) Timer 2	0021_{16}	01_{16}
(27) Timer 3	0022_{16}	FF_{16}
(28) Timer 4	0023_{16}	FF_{16}
(29) PWM01 register	0024_{16}	00_{16}
(30) Timer 12 mode register	0025_{16}	00_{16}
(31) Timer 34 mode register	0026_{16}	00_{16}
(32) Timer 1234 mode register	0027_{16}	00_{16}
(33) Timer 1234 frequency division selection register	0028_{16}	00_{16}
(34) Watchdog timer control register	0029_{16}	0 0 1 1 1 1 1 1

	Address	Register contents
(35) Timer X (low-order)	$002A_{16}$	FF_{16}
(36) Timer X (high-order)	$002B_{16}$	FF_{16}
(37) Timer X (extension)	$002C_{16}$	00_{16}
(38) Timer X mode register	$002D_{16}$	00_{16}
(39) Timer X control register 1	$002E_{16}$	00_{16}
(40) Timer X control register 2	$002F_{16}$	00_{16}
(41) Compare register 1 (low-order)	0030_{16}	00_{16}
(42) Compare register 1 (high-order)	0031_{16}	00_{16}
(43) Compare register 2 (low-order)	0032_{16}	00_{16}
(44) Compare register 2 (high-order)	0033_{16}	00_{16}
(45) Compare register 3 (low-order)	0034_{16}	00_{16}
(46) Compare register 3 (high-order)	0035_{16}	00_{16}
(47) Timer Y (low-order)	0036_{16}	FF_{16}
(48) Timer Y (high-order)	0037_{16}	FF_{16}
(49) Timer Y mode register	0038_{16}	00_{16}
(50) Timer Y control register	0039_{16}	00_{16}
(51) Interrupt edge selection register	$003A_{16}$	00_{16}
(52) CPU mode register	$003B_{16}$	0 1 1 0 1 0 0 0
(53) Interrupt request register 1	$003C_{16}$	00_{16}
(54) Interrupt request register 2	$003D_{16}$	00_{16}
(55) Interrupt control register 1	$003E_{16}$	00_{16}
(56) Interrupt control register 2	$003F_{16}$	00_{16}
(57) PULL register 1	$0FF0_{16}$	00_{16}
(58) PULL register 2	$0FF1_{16}$	00_{16}
(59) PULL register 3	$0FF2_{16}$	00_{16}
(60) Clock output control register	$0FF3_{16}$	00_{16}
(61) Segment output disable register 0	$0FF4_{16}$	FF_{16}
(62) Segment output disable register 1	$0FF5_{16}$	FF_{16}
(63) Segment output disable register 2	$0FF6_{16}$	$0F_{16}$
(64) Key input control register	$0FF7_{16}$	00_{16}
(65) Flash memory control register	$0FFE_{16}$	X X X 0 0 0 0 1
(66) Processor status register	(PS)	X X X X X 1 X X
(67) Program counter	(PC_H)	$FFFD_{16}$ contents
	(PC_L)	$FFFC_{16}$ contents

X: Not fixed

Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 53 Internal status at reset

CLOCK GENERATING CIRCUIT

The oscillation circuit of 38C5 group can be formed by connecting an oscillator, capacitor and resistor between XIN and XOUT (XCIN and XCOUT). To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open. The clocks that are externally generated cannot be directly input to XCIN. Use the circuit constants in accordance with the oscillator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. (An external feed-back resistor may be needed depending on conditions.) However, an about 10 MΩ external feedback resistor is needed between XCIN and XCOUT.

Immediately after reset is released, only the on-chip oscillator starts oscillating, XIN -XOUT oscillation stops oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency Control
(1) On-chip oscillation Mode

The system clock ϕ is the on-chip oscillator oscillation divided by 32.

(2) Middle-speed Mode

The system clock ϕ is the frequency of XIN divided by 8.

(3)High-speed Mode

The system clock ϕ is half the frequency of XIN.

(4) Low-speed Mode

The system clock ϕ is half the frequency of sub clock.

After reset release and when system returns from the stop mode, the on-chip oscillator mode is selected.

Refer to the clock state transition diagram for the setting of transition to each mode.

The XIN–XOUT oscillation is controlled by the bit 5 of CPUM, and the sub-clock oscillation is controlled by the bit 4 of CPUM. When the mode is switched to the on-chip oscillator mode, set the bit 3 of CPUM to “1”.

In the on-chip oscillator mode, the oscillation by the oscillator can be stopped. In the low-speed mode, the power consumption can be reduced by stopping the XIN–XOUT oscillation.

When the mode is switched from the on-chip oscillator mode to the low-speed mode, the on-chip oscillator is stopped.

Set enough time for oscillation to stabilize by programming to re-start the stopped oscillation and switch the operation mode. Also, set enough time for oscillation to stabilize by programming to switch the timer count source .

■ Notes on Clock Generating Circuit

If you switch the mode between on-chip oscillator mode, middle/high-speed mode and low-speed mode, stabilize both XIN and XCIN oscillations. Especially be careful immediately after power-on and at returning from stop mode. Refer to the clock state transition diagram for the setting of transition to each mode. Set the frequency in the condition that f(XIN) > 3•f(XCIN).

When the middle- and high-speed mode are not used (XIN-XOUT oscillation and external clock input are not performed), connect XIN to VCC through a resistor.

Oscillation Control
(1) Stop Mode

If the STP instruction is executed, the system clock ϕ stops at an “H” level, and main clock and sub-clock oscillators stop.

In this time, values set previously to timer 1 latch and timer 2 latch are loaded automatically to timer 1 and timer 2. Set the values to generate the wait time required for oscillation stabilization to timer 1 latch and timer 2 latch (low-order 8 bits of timer 1 and high-order 8 bits of timer 2) before the STP instruction.

The frequency divider for timer 1 is used for the timer 1 count source, and the output of timer 1 is forcibly connected to timer 2. In this time, bits 0 to 5 of the timer 12 mode register are cleared to “0”.

The values of the timer 12 frequency divider selection register are not changed.

Set the interrupt enable bits of the timer 1 and timer 2 to be disabled (“0”) before executing the STP instruction.

When an external interrupt is received, the clock oscillated before stop mode and the on-chip oscillator start oscillating.

However, bit 3 of CPUM is set to “1” forcibly and system returns to the on-chip oscillator mode.

Oscillator restarts when reset occurs or an interrupt request is received, but the system clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

(2) Wait Mode

If the WIT instruction is executed, only the system clock ϕ stops at an “H” state. The states of main clock, on-chip oscillator and sub clock are the same as the state before executing the WIT instruction, and oscillation does not stop. Since supply of system clock ϕ is started immediately after the interrupt is received, the instruction can be executed immediately.

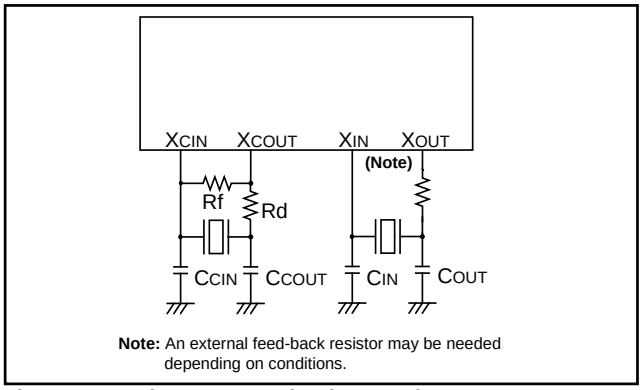


Fig. 54 Ceramic resonator circuit example

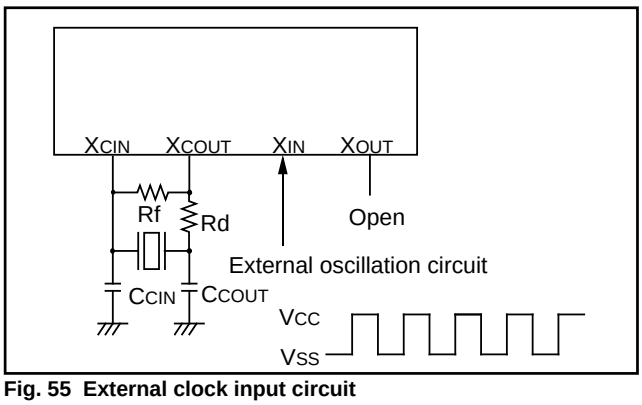
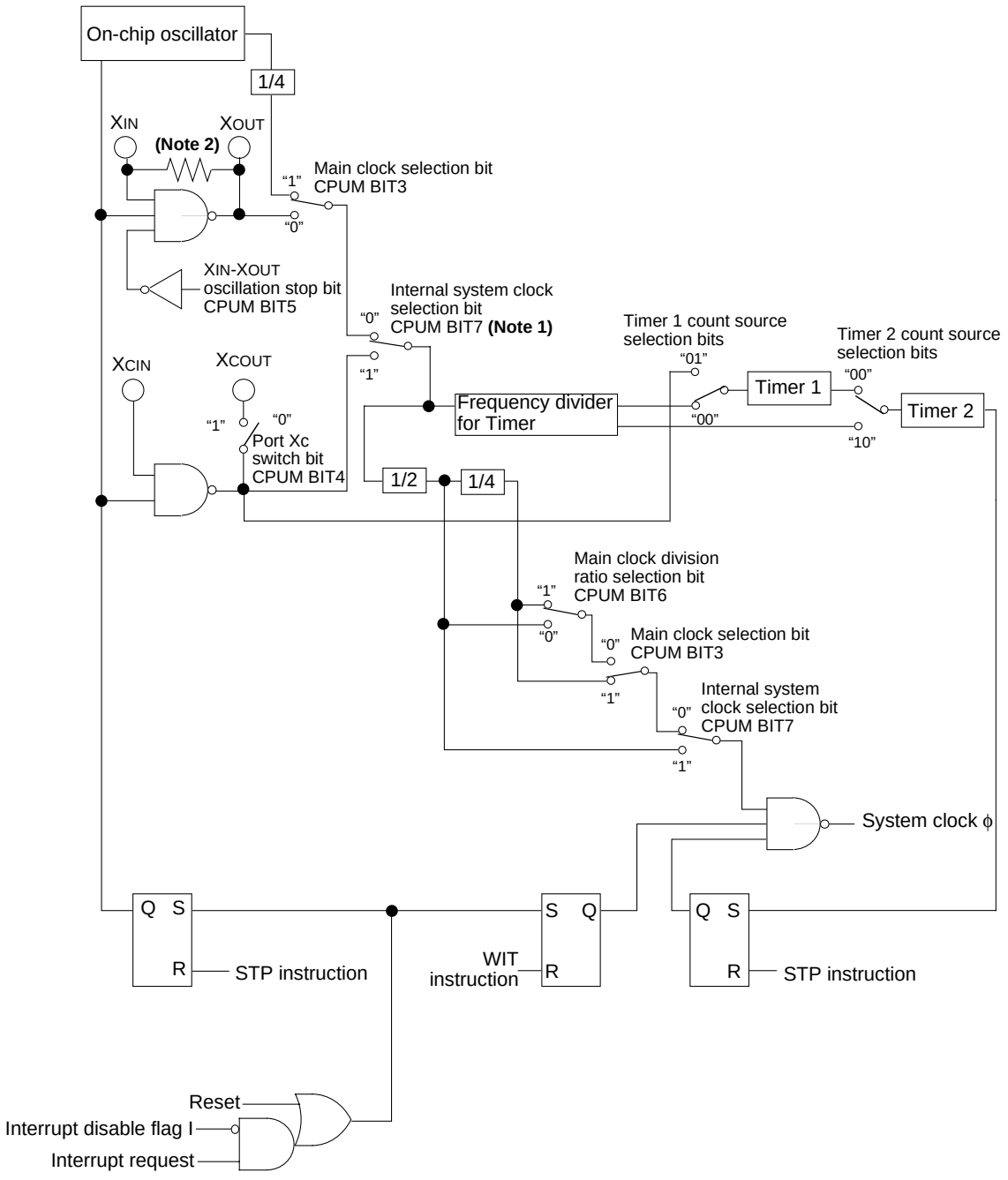
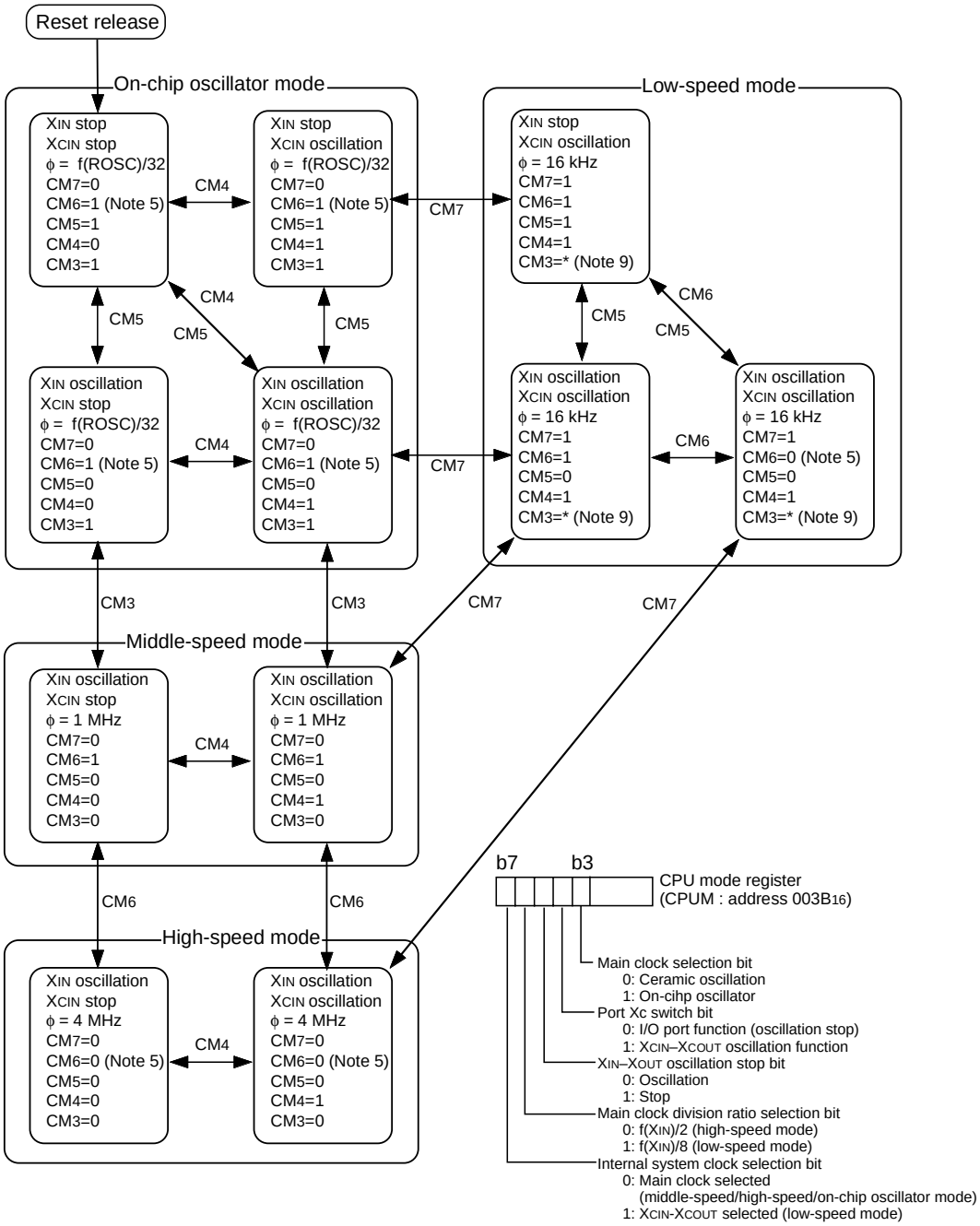


Fig. 55 External clock input circuit



Notes 1: When the XCIN-XCOUT oscillation is selected as the system clock, set the port Xc switch bit to "1".
2: Although a feed-back resistor exists on-chip, an external feed-back resistor may be needed depending on conditions.

Fig. 56 Clock generating circuit block diagram



Notes 1: Switch the mode by the arrows shown between the mode blocks.
The all modes can be switched to the stop mode or the wait mode.
2: Timer and LCD operate in the wait mode. System is returned to the source mode when the wait mode is ended.
3: CM4, CM5 and CM6 are retained in the stop mode.
System is returned to the on-chip oscillator mode (CM3=1, CM7=0).
4: When the stop mode is ended, set the oscillation stabilizing wait time in the on-cihp oscillator mode.
5: When the stop mode is ended, set the initial value to CM6 (CM6=1).
6: Execute the transition after the oscillation used in the destination mode is stabilized.
7: When system goes to on-chip oscillator mode, the oscillation stabilizing wait time is not needed.
8: Do not go to the high-speed mode from the on-cihp oscillator mode.
9: Write the proper values for destination mode beforehand.
10: The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin.
f(ROSC) indicates the oscillation frequency of on-chip oscillator.

Fig. 57 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1," then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing an SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

- If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
- The timers share the one frequency divider to generate the count source. Accordingly, when each timer starts operating, initializing the frequency divider is not executed. Therefore, when the frequency divider is selected for the count source, the delay of the maximum one cycle of the count source is generated until the timer starts counting or the waveform is output from timer starts operating. Also, the count source cannot be checked externally.

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1."
Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

A/D Converter

The comparator is constructed linked to a capacitor. The conversion accuracy may be low because the change is lost if the conversion speed is not enough.
Accordingly, set f(XIN) to at least 500 kHz during A/D conversion in the middle- or high- speed mode.
Also, do not execute the STP and WIT instructions during the A/D conversion.
In the low-speed mode, since the A/D conversion is executed by the built-in self-oscillation circuit, the minimum value of f(XIN) frequency.

Instruction Execution Time

The instruction execution time is obtained by multiplying the number of cycles shown in the list of machine instructions by the period of the internal clock ϕ.

NOTES ON USE

V_{L3} pin

When LCD drive control circuit is not used, connect V_{L3} to V_{CC}.

Countermeasures against noise

The following countermeasures are effective against noise in theory, however, it is necessary not only to take masures as follows but to evaluate before actual use.

(1) Shortest wiring length

① Wiring for $\overline{\text{RESET}}$ pin

Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the V_{SS} pin with the shortest possible wiring (within 20 mm).

● Reason

The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

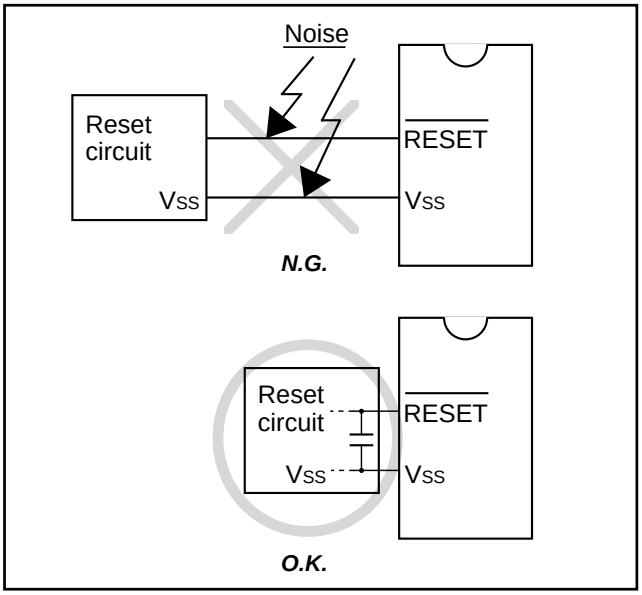


Fig. 58 Wiring for the $\overline{\text{RESET}}$ pin

② Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the V_{SS} pin of a microcomputer as short as possible.
- Separate the V_{SS} pattern only for oscillation from other V_{SS} patterns.

● Reason

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the V_{SS} level of a microcomputer and the V_{SS} level of an oscillator, the correct clock will not be input in the microcomputer.

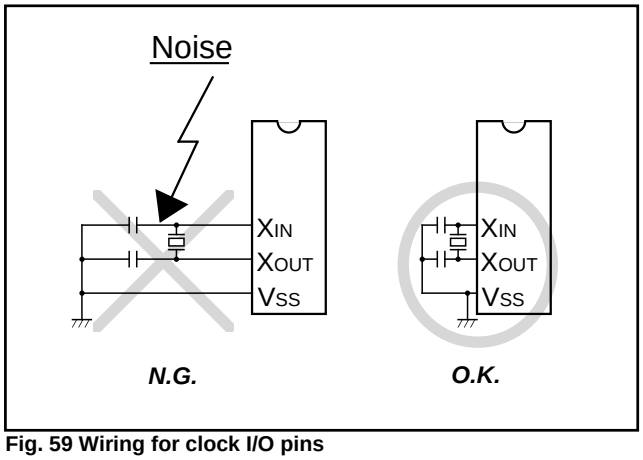


Fig. 59 Wiring for clock I/O pins

(2) Connection of bypass capacitor across V_{SS} line and V_{CC} line

Connect an approximately 0.1 μF bypass capacitor across the V_{SS} line and the V_{CC} line as follows:

- Connect a bypass capacitor across the V_{SS} pin and the V_{CC} pin at equal length.
- Connect a bypass capacitor across the V_{SS} pin and the V_{CC} pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for V_{SS} line and V_{CC} line.
- Connect the power source wiring via a bypass capacitor to the V_{SS} pin and the V_{CC} pin.

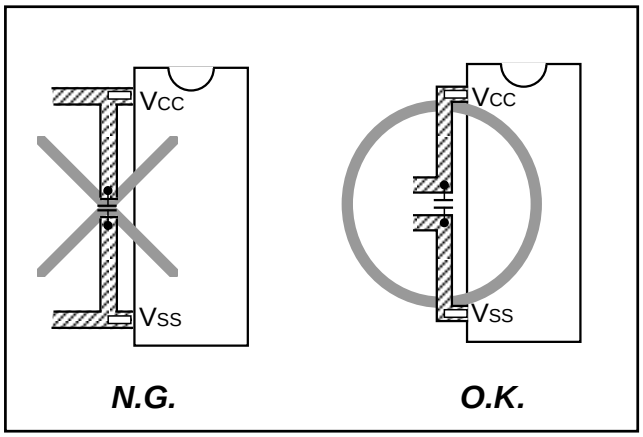


Fig. 60 Bypass capacitor across the V_{SS} line and the V_{CC} line

(3) Oscillator concerns

In order to obtain the stabilized operation clock on the user system and its condition, contact the oscillator manufacturer and select the osillator and oscillation circuit constants. Be careful especially when range of voltage and temperature is wide.

Also, take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

① Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

● Reason

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

② Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

● Reason

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

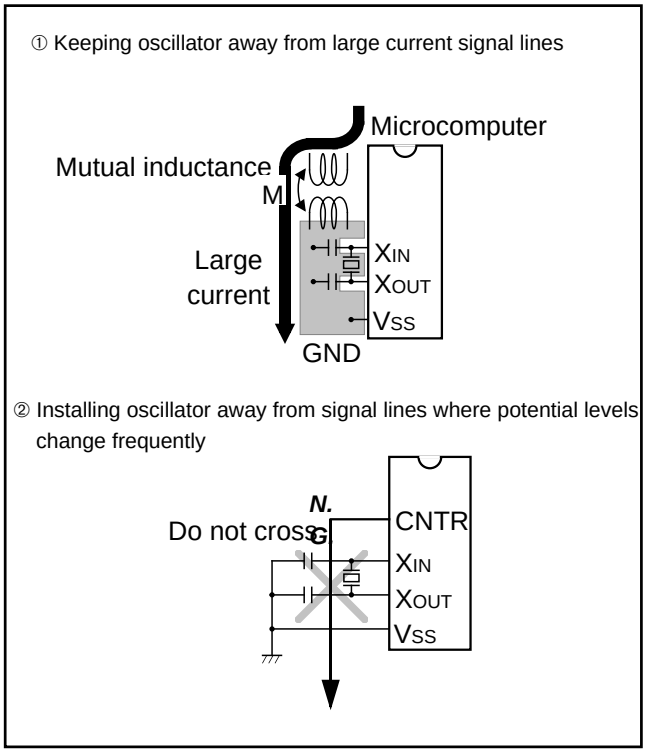


Fig. 61 Wiring for a large current signal line/Writing of signal lines where potential levels change frequently

(4) Analog input

The analog input pin is connected to the capacitor of a voltage comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A/D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A/D covnversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

(5) Difference of memory type and size

When Mask ROM and PROM version and memory size differ in one group, actual values such as an electrical characteristics, A/D conversion accuracy, and the amount of -proof of noise incorrect operation may differ from the ideal values.

When these products are used switching, perform system evaluation for each product of every after confirming product specification.

(6) Wiring to VPP pin of One Time PROM version

Connect an approximately 10 kΩ resistor to the VPP pin at the shortest possible in series and also to the VSS pin.

Note: Even when a circuit which included an approximately 10 kΩ resistor is used in the Mask ROM version, the microcomputer operates correctly.

● Reason

The VPP pin of the One Time PROM version is the power source input pin for the built-in PROM. When programming in the built-in PROM, the impedance of the VPP pin is low to allow the electric current for writing flow into the built-in PROM. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the built-in PROM, which may cause a program runaway.

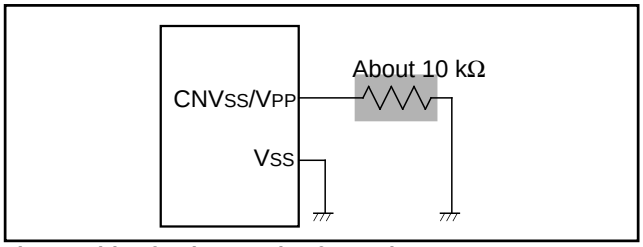


Fig. 62 Wiring for the VPP pin of One Time PROM

Electric Characteristic Differences Between Mask ROM and One Time PROM Version MCUs

There are differences in electric characteristics, operation margin, noise immunity, and noise radiation between the mask ROM and One Time PROM version MCUs due to the difference in the manufacturing processes.

When manufacturing an application system with the One Time PROM version and then switching to use of the Mask ROM version, please perform sufficient evaluations for the commercial samples of the Mask ROM version.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form*
2. Mark Specification Form*
3.Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk

* For the mask ROM confirmation and the mark specifications, refer to the “Renesas Technology” Homepage (http://www.renesas.com/en/rom/).

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Table 11 Absolute maximum ratings (Mask ROM version)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on Vss. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_4$		–0.3 to V_{CC}+0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to 6.5	V
V_I	Input voltage C_1, C_2		–0.3 to 6.5	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC}+0.3	V
V_O	Output voltage C_1, C_2		–0.3 to 6.5	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	At output port	–0.3 to V_{CC}	V
		At segment output	–0.3 to V_{L3}	
V_O	Output voltage $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$		–0.3 to V_{CC}+0.3	V
V_O	Output voltage V_{L3}		–0.3 to 6.5	V
V_O	Output voltage V_{L2}, SEG_{32}–SEG_{35}		–0.3 to V_{L3}	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	Ta = 25°C	300	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Recommended Operating Conditions

Table 12 Recommended operating conditions (Mask ROM version)

(Vcc = 1.8 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Power source voltage **(Note 1)**	High-speed mode	$f(X_{IN})$ = 12.5 MHz	4.5	5.0	5.5	V
			$f(X_{IN})$ = 8 MHz	4.0	5.0	5.5	V
			$f(X_{IN})$ = 6 MHz	3.0	5.0	5.5	V
			$f(X_{IN})$ = 4 MHz	2.0	5.0	5.5	V
		Middle-speed mode	$f(X_{IN})$ = 12.5 MHz	3.0	5.0	5.5	V
			$f(X_{IN})$ = 8 MHz	2.0	5.0	5.5	V
			$f(X_{IN})$ = 6 MHz	1.8	5.0	5.5	V
		Low-speed mode		1.8	5.0	5.5	V
		Oscillation start voltage **(Note 2)**		0.15 × f + 1.3			V
V_{SS}	Power source voltage				0		V
V_{LI}	V_{L1} input voltage	Voltage multiplier is used		1.3	1.8	2.1	V
V_{REF}	A/D converter reference voltage			2.0		V_{CC}	V
AV_{SS}	Analog power source voltage				0		V
V_{IA}	Analog input voltage	AN_0–AN_7		AV_{SS}		V_{CC}	V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_4$–$P2_7$, $P3_0$–$P3_7$, $P4_1$, $P4_3$, $P5_0$–$P5_7$, $P6_0$(CM_4=0), $P6_1$, $P6_5$, $P7_2$–$P7_4$		0.7V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$P2_0$–$P2_3$, $P4_0$, $P4_2$, $P4_4$–$P4_7$, $P6_2$–$P6_4$, $P6_6$–$P6_7$, $P7_0$, $P7_1$		0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$		0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	X_{IN}		0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_4$–$P2_7$, $P3_0$–$P3_7$, $P4_1$, $P4_3$, $P5_0$–$P5_7$, $P6_0$(CM_4=0), $P6_1$, $P6_5$, $P7_2$–$P7_4$		0		0.3V_{CC}	V
V_{IL}	“L” input voltage	$P2_0$–$P2_3$, $P4_0$, $P4_2$, $P4_4$–$P4_7$, $P6_2$–$P6_4$, $P6_6$–$P6_7$, $P7_0$, $P7_1$		0		0.2V_{CC}	V
V_{IL}	“L” input voltage	$\overline{RESET}$		0		0.2V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}		0		0.2V_{CC}	V

Notes 1: When the A/D converter is used, refer to the recommended operating conditions of the A/D converter.

2: The oscillation start voltage and the oscillation start time differ in accordance with an oscillator, a circuit constant, or temperature, etc. When power supply voltage is low and the high frequency oscillator is used, an oscillation start will require sufficient conditions.
f: Oscillation frequency (MHz) of oscillator. When the 8 MHz oscillation is used, assign “8” to “f”.

Table 13 Recommended operating conditions (Mask ROM version)

(Vcc = 1.8 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P7_2$–$P7_4$			–40	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current **(Note 1)** $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$			–40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P7_2$–$P7_4$			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** $P6_2$–$P6_7$			110	mA
$\Sigma I_{OH(avg)}$	"H" total average output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P7_2$–$P7_4$			–20	mA
$\Sigma I_{OH(avg)}$	"H" total average output current **(Note 1)** $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$			–20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P7_2$–$P7_4$			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note 1)** $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note 1)** $P6_2$–$P6_7$			90	mA
$I_{OH(peak)}$	"H" peak output current **(Note 2)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–2	mA
$I_{OH(peak)}$	"H" peak output current **(Note 2)** $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$			–5	mA
$I_{OL(peak)}$	"L" peak output current **(Note 2)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			5.0	mA
$I_{OL(peak)}$	"L" peak output current **(Note 2)** $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_2$–$P7_4$			10	mA
$I_{OL(peak)}$	"L" peak output current **(Note 2)** $P6_2$–$P6_7$			30	mA
$I_{OH(avg)}$	"H" average output current **(Note 3)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–1.0	mA
$I_{OH(avg)}$	"H" average output current **(Note 3)** $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$			–2.5	mA
$I_{OL(avg)}$	"L" average output current **(Note 3)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			2.5	mA
$I_{OL(avg)}$	"L" average output current **(Note 3)** $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_2$–$P7_4$			5.0	mA
$I_{OL(avg)}$	"L" average output current **(Note 3)** $P6_2$–$P6_7$			15	mA

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is average value measured over 100 ms.

Table 14 Recommended operating conditions (Mask ROM version)

(Vcc = 1.8 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
f(CNTR0)	Timer X and Timer Y	(4.5 V ≤ Vcc ≤ 5.5 V)			6.25	MHz
f(CNTR1)	Input frequency (duty cycle 50%)	(4.0 V ≤ Vcc < 4.5 V)			4.0	MHz
		(2.0 V ≤ Vcc < 4.0 V)			Vcc	MHz
		(Vcc < 2.0 V)			5×Vcc–8	MHz
f(XIN)	Main clock input frequency (duty cycle 50%) (**Note 1**)	High-speed mode (4.5 V < Vcc ≤ 5.5 V)			12.5	MHz
		High-speed mode (4.0 V < Vcc ≤ 4.5 V)			9×Vcc–28	MHz
		High-speed mode (2.0 V ≤ Vcc ≤ 4.0 V)			2×Vcc	MHz
		Middle-speed mode (**Notes 3, 4**) (3.0 V ≤ Vcc ≤ 5.5 V)			12.5	MHz
		Middle-speed mode (**Notes 3, 4**) (2.0 V ≤ Vcc ≤ 5.5 V)			8.0	MHz
		Middle-speed mode (**Notes 3, 4**)			6.0	MHz
f(XCIN)	Sub-clock oscillation frequency (duty cycle 50%) (**Notes 2, 4**)			32.768	80	kHz

Notes 1: When the A/D converter is used, refer to the recommended operationg conditions of the A/D converter.

2: When using the microcomputer in low-speed mode, set the clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

3: When the timer X dividing frequency selection bit and timer Y dividing frequency selection bit are "01(1/1 × φSOURCE)" or "10(1/2 × φSOURCE)", the limits at the high-speed mode are suitable for the recommended operating condition of main clock input frequency f(XIN).

4: The oscillation start voltage and the oscillation start time differ in accordance with an oscillator, a circuit constant, or temperature, etc. When power supply voltage is low and the high frequency oscillator is used, an oscillation start will require sufficient conditions.

Electrical Characteristics

Table 15 Electrical characteristics (Mask ROM version)

(Vcc = 4.0 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	I_{OH} = –2.5 mA	V_{CC}–2.0			V
		I_{OH} = –0.6 mA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OH}	"H" output voltage $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$ (Note)	I_{OH} = –5 mA	V_{CC}–2.0			V
		I_{OH} = –1.25 mA	V_{CC}–0.5			V
		I_{OH} = –1.25 mA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	I_{OL} = 5 mA			2.0	V
		I_{OL} = 1.25 mA			0.5	V
		I_{OL} = 1.25 mA V_{CC} = 2.5 V			1.0	V
VOL	"L" output voltage $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_2$–$P7_4$ (Note)	I_{OL} = 10 mA			2.0	V
		I_{OL} = 2.5 mA			0.5	V
		I_{OL} = 2.5 mA V_{CC} = 2.5 V			1.0	V
V_{OL}	"L" output voltage $P6_2$–$P6_7$	I_{OL} = 15 mA			2.0	V
		I_{OL} = 3.0 mA V_{CC} = 2.5 V			0.8	V
V_{T+}–V_{T-}	Hysteresis $INT0_0$, $INT0_1$, $INT1_0$, $INT1_1$, INT_2, $CNTR_0$, $CNTR_1$, KW_0–KW_7			0.5		V
V_{T+}–V_{T-}	Hysteresis S_{IN2}, S_{CLK1}, S_{CLK2}, RxD			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$	V_{CC} = 2.0 V on $\overline{RESET}$		0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_4$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{SS} Pull-up "OFF"			–5.0	µA
		V_{CC} = 5.0 V, V_I = V_{SS} Pull-up "ON"	–60	–120	–240	µA
		V_{CC} = 3.0 V, V_I = V_{SS} Pull-up "ON"	–25	–50	–100	µA
I_{IL}	"L" input current $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$	V_I = V_{SS} Pull-up "OFF"			–5.0	µA
		V_{CC} = 5.0 V, V_I = V_{SS} Pull-up "ON"	–30	–70	–140	µA
		V_{CC} = 3.0 V, V_I = V_{SS} Pull-up "ON"	–6.5	–25	–45	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA
R_{OSC}	On-chip oscillator frequency	V_{CC} = 5 V, Ta = 25 °C	2500	5000	7500	kHz

Note: When the port Xc switch bit (bit 4 of address $003B_{16}$) of CPU mode register is "1", the drivability of $P6_1$ is different from the above.

Table 16 Electrical characteristics (Mask ROM version)

(Vcc = 1.8 to 5.5 V, Ta = –20 to 85°C, f(XCIN) = 32.768 kHz, output transistors in the cut-off state, AD converter stopped, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
VRAM	RAM hold voltage	When clock is stopped			1.8		5.5	V
ICC	Power source current	High-speed mode	Vcc = 5 V	f(XIN) = 12.5 MHz		6.4	13	mA
				f(XIN) = 12.5 MHz (in WIT state)		1.5	3.0	mA
				f(XIN) = 4 MHz		1.5	3.0	mA
			Vcc = 2.5 V	f(XIN) = 4 MHz		0.6	1.2	mA
				f(XIN) = 4 MHz (in WIT state)		0.3	0.6	mA
				f(XIN) = 2 MHz		0.4	0.8	mA
		Middle-speed mode	Vcc = 5 V	f(XIN) = 12.5 MHz		2.5	5.0	mA
				f(XIN) = 12.5 MHz (in WIT state)		1.5	3.0	mA
				f(XIN) = 4 MHz		0.8	1.6	mA
			Vcc = 2.5 V	f(XIN) = 8 MHz		0.5	1.0	mA
				f(XIN) = 8 MHz (in WIT state)		0.3	0.6	mA
				f(XIN) = 4 MHz		0.3	0.6	mA
		Low-speed mode	Vcc = 5 V	f(XIN) = stop		13	26	µA
				in WIT state		5.5	11	µA
			Vcc = 2.5 V	f(XIN) = stop		7.0	14	µA
				in WIT state		3.5	7.0	µA
		On-chip oscillator mode f(XIN), f(XCIN) = stop		VCC = 5 V		270	540	µA
				VCC = 2.5 V		35	90	µA
				VCC = 2.5 V (in WIT state)		25	75	µA
		All oscillations stopped (in STP state)		Ta = 25 °C		0.1	1.0	µA
				Ta = 85 °C			10	µA
		Current increased at A/D converter operating		f(XIN) = 12.5 MHz, VCC = 5 V in middle- or high-speed mode		0.5		mA
				f(XIN) = stop, VCC = 5 V in on-chip oscillator operating		0.5		mA
				f(XIN) = stop, VCC = 5 V in low-speed mode		0.4		mA

A/D Converter Characteristics

Table 17 A/D converter recommended operating condition (Mask ROM version)

(Vcc = 2.0 to 5.5 V, Ta = –20 to 85°C, output transistors in cut-off state, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage		2.0	5.0	5.5	V
V_{IH}	"H" input voltage ADKEY0		0.9Vcc		Vcc	V
V_{IL}	"L" input voltage ADKEY0		0		0.7 × Vcc–0.5	V
f(X_{IN})	AD converter control clock (**Note**) (Low-speed • on-chip oscillator mode excluded)	$V_{CC} \leq 2.2$ V			20 × Vcc–38	MHz
		2.2 V < $V_{CC} \leq 3.0$ V			$\frac{45 \times Vcc-35}{8}$	MHz
		3.0 V < $V_{CC} \leq 5.5$ V			12.5	MHz

Note: Confirm the recommended opearting condition for main clock input frequency.

Table 18 A/D converter characteristics (Mask ROM version)

(Vcc = 2.0 to 5.5 V, Ta = –20 to 85°C, output transistors in cut-off state, low-speed • on-chip oscillator mode included, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
ABS	Absolute accuracy (quantification error excluded)	4.5 < $V_{CC} \leq 5.5$, f(X_{IN}) ≤ 12.5 MHz AD conversion clock = ϕSOURCE/2 10bitAD mode			4	LSB
		2.5 < $V_{CC} \leq 4.5$, f(X_{IN}) ≤ 8 MHz AD conversion clock = ϕSOURCE/2 10bitAD mode				
		2.2 < $V_{CC} \leq 2.5$, f(X_{IN}) ≤ 2 MHz Low-speed mode • on-chip oscillator mode AD conversion clock = ϕSOURCE/2 10bitAD mode			4	
		3.0 < $V_{CC} \leq 5.5$, f(X_{IN}) ≤ 12.5 MHz AD conversion clock = ϕSOURCE/8 8bitAD mode			2	
		2.2 < $V_{CC} \leq 3.0$, f(X_{IN}) ≤ 8 MHz AD conversion clock = ϕSOURCE/8 8bitAD mode				
		2.0 < $V_{CC} \leq 2.2$, f(X_{IN}) ≤ 6 MHz AD conversion clock = ϕSOURCE/8 Low-speed mode • on-chip oscillator mode AD conversion clock = ϕSOURCE/2			2	
T_{conv}	Conversion time	AD conversion clock selection bit : ϕSOURCE/2 10bitAD mode			tc(ϕAD)×121 (Note)	μs
R_{LADDER}	Ladder resistor		12	35	100	kΩ
I_{VREF}	Reference input current	V_{REF} = 5 V	50	150	200	μA
I_{IA}	Analog input current				5.0	μA

Note: When "Frequency/8" is selected by the AD conversion clock selection bit, the above conversion time is multiplied by 4.
The operation clock is XIN in the middle- or high-speed mode, or the on-chip oscillator in the other modes.
When the A/D conversion is executed in the middle- or high-speed mode, set f(X_{IN}) ≤ 500 kHz.
tc(ϕAD): One cycle of control clock for A/D converter. X_{IN} input is used in the middel- or high-speed mode, and on-chip oscillator is used in the low- or on-chip oscillator mode for the control clock.

Timing Requirements And Switching Characteristics

Table 19 Timing requirements 1 (Mask ROM version)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width		2			µs
$t_{C(XIN)}$	Main clock input cycle time	4.5 V to 5.5 V	80			ns
		4.0 V to 4.5 V	125			ns
$t_{WH(XIN)}$	Main clock input “H” pulse width	4.5 V to 5.5 V	32			ns
		4.0 V to 4.5 V	50			ns
$t_{WL(XIN)}$	Main clock input “L” pulse width	4.5 V to 5.5 V	32			ns
		4.0 V to 4.5 V	50			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time		250			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width		105			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width		105			ns
$t_{WH(INT)}$	INT_{00}, INT_{01}, INT_{10}, INT_{11}, INT_2 input “H” pulse width		80			ns
$t_{WL(INT)}$	INT_{00}, INT_{01}, INT_{10}, INT_{11}, INT_2 input “L” pulse width		80			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time (Note)		800			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width (Note)		370			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width (Note)		370			ns
$t_{su(RxD\text{-}SCLK1)}$	Serial I/O1 input setup time		220			ns
$t_{h(SCLK1\text{-}RxD)}$	Serial I/O1 input hold time		100			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time		1000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width		400			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width		400			ns
$t_{su(SIN2\text{-}SCLK2)}$	Serial I/O2 input setup time		200			ns
$t_{h(SCLK2\text{-}SIN2)}$	Serial I/O2 input hold time		200			ns

Note : When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 20 Timing requirements 2 (Mask ROM version)

(Vcc = 1.8 to 4.0 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width		2			µs
$t_{C(XIN)}$	Main clock input cycle time (X_{IN} input)	(2.0 V < V_{CC} ≤ 4.0 V)	125			ns
		(V_{CC} ≤ 2.0 V)	166			ns
$t_{WH(XIN)}$	Main clock input “H” pulse width	(2.0 V < V_{CC} ≤ 4.0 V)	50			ns
		(V_{CC} ≤ 2.0 V)	70			ns
$t_{WL(XIN)}$	Main clock input “L” pulse width	(2.0 V < V_{CC} ≤ 4.0 V)	50			ns
		(V_{CC} ≤ 2.0 V)	70			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	(2.0 V < V_{CC} ≤ 4.0 V)	1000/Vcc			ns
		(V_{CC} ≤ 2.0 V)	1000/(5×Vcc-8)			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width		tc(CNTR)/2-20			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width		tc(CNTR)/2-20			ns
$t_{WH(INT)}$	INT_{00}, INT_{01}, INT_{10}, INT_{11}, INT_2 input “H” pulse width		230			ns
$t_{WL(INT)}$	INT_{00}, INT_{01}, INT_{10}, INT_{11}, INT_2 input “L” pulse width		230			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time (Note)		2000			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width (Note)		950			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width (Note)		950			ns
$t_{su(RxD-SCLK1)}$	Serial I/O1 input setup time		400			ns
$t_{h(SCLK1-RxD)}$	Serial I/O1 input hold time		200			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time		2000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width		950			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width		950			ns
$t_{su(RxD-SCLK2)}$	Serial I/O2 input setup time		400			ns
$t_{h(SCLK2-RxD)}$	Serial I/O2 input hold time		200			ns

Note : When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 21 Switching characteristics 1 (Mask ROM version)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1 clock output “H” pulse width	$t_C(S_{CLK1})/2–30$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock output “L” pulse width	$t_C(S_{CLK1})/2–30$			ns
$t_d(S_{CLK1}\text{-}TxD)$	Serial I/O1 output delay time **(Note)**			140	ns
$t_V(S_{CLK1}\text{-}TxD)$	Serial I/O1 output valid time **(Note)**	–30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time			30	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time			30	ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output “H” pulse width	$t_C(S_{CLK1})/2–30$			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output “L” pulse width	$t_C(S_{CLK1})/2–30$			ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time			40	ns
$t_d(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output delay time			140	ns
$t_V(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output valid time	–30			ns

Note: The $P4_1$/TxD P-channel output disable bit (bit 4 of address $001B_{16}$) of UART control register is “0.”

Table 22 Switching characteristics 2 (Mask ROM version)

(Vcc = 1.8 to 4.0 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1 clock output “H” pulse width	$t_C(S_{CLK1})/2–80$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock output “L” pulse width	$t_C(S_{CLK1})/2–80$			ns
$t_d(S_{CLK1}\text{-}TxD)$	Serial I/O1 output delay time **(Note)**			350	ns
$t_V(S_{CLK1}\text{-}TxD)$	Serial I/O1 output valid time **(Note)**	–30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time			80	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time			80	ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output “H” pulse width	$t_C(S_{CLK1})/2–80$			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output “L” pulse width	$t_C(S_{CLK1})/2–80$			ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time			80	ns
$t_d(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output delay time			350	ns
$t_V(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output valid time	–30			ns

Note: The $P4_1$/TxD P-channel output disable bit (bit 4 of address $001B_{16}$) of UART control register is “0.”

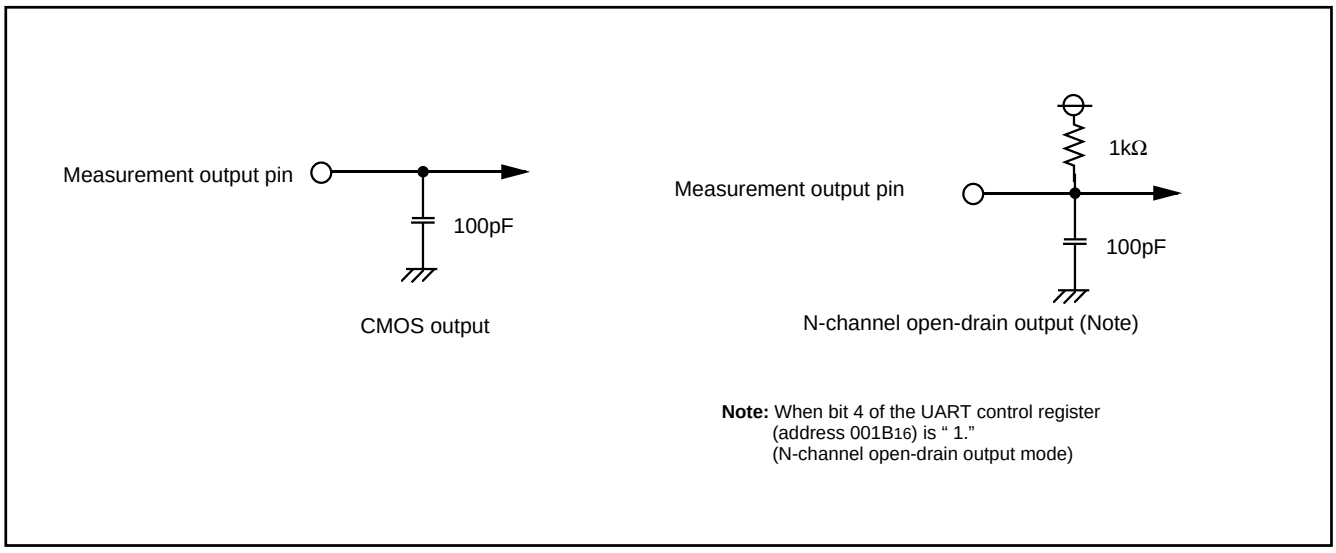


Fig. 63 Circuit for measuring output switching characteristics

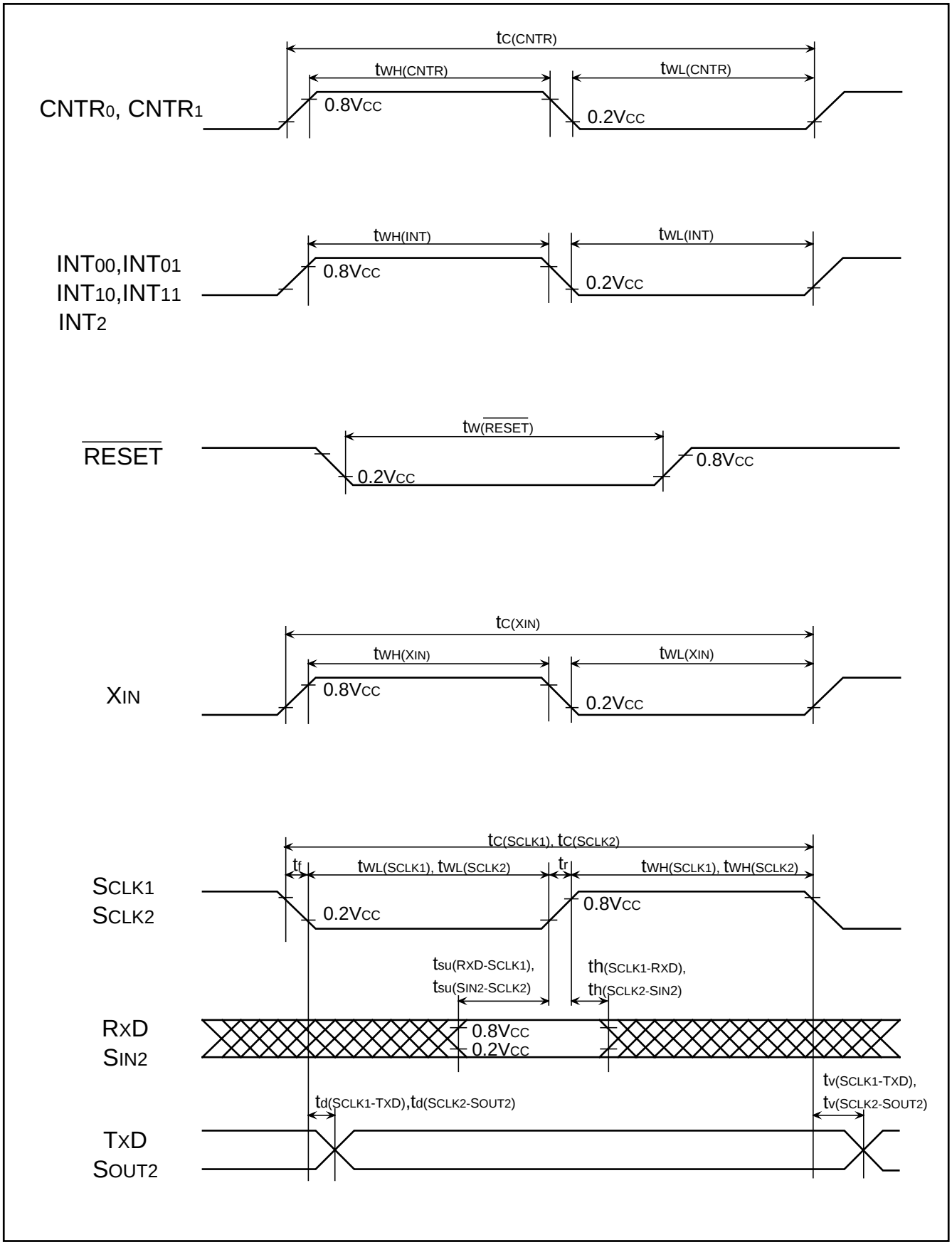


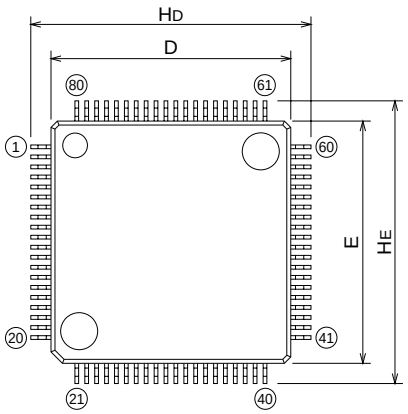
Fig. 64 Timing chart

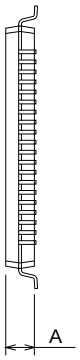
PACKAGE OUTLINE

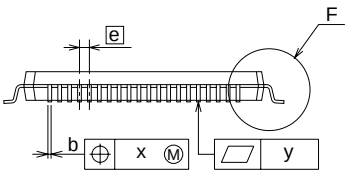
80P6Q-A

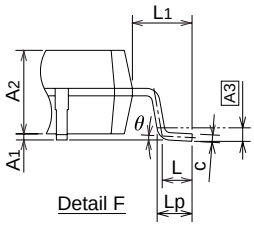
Plastic 80pin 12×12mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.5	–	0.47	Cu Alloy

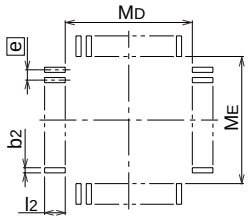








Detail F



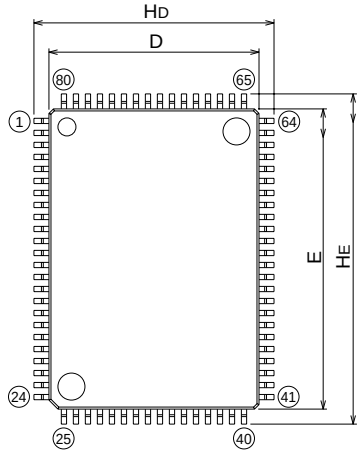
Recommended Mount Pad

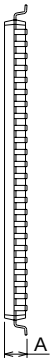
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	–	0.5	–
HD	13.8	14.0	14.2
HE	13.8	14.0	14.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	12.4	–
ME	–	12.4	–

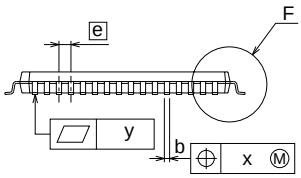
80P6U-A

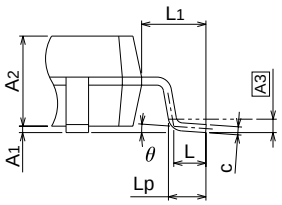
Plastic 80pin 14×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1420-0.8	–		Cu Alloy

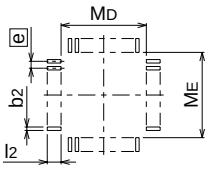








Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.6
A1	0.05	0.125	0.2
A2	–	1.4	–
b	0.32	0.37	0.47
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	19.9	20.0	20.1
e	–	0.8	–
HD	15.8	16.0	16.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.2
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
l2	1.0	–	–
MD	–	14.4	–
ME	–	20.4	–

REVISION HISTORY	38C5 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 31, 2004	–	First edition issued
1.10	Jun. 14, 2004	All pages 8	Words standardized: On-chip oscillator, A/D converter Fig.5: M38C58M8 in mass production.

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