1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Outline

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Shortest instruction execution time	62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2 “Product List”
Peripheral function	Interrupt	Internal: 10 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels
	Watchdog timer	15 bits x 1 (with prescaler)
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel Input capture circuit
	Serial I/O	•1 channel Clock synchronous, UART •1 channel UART
	A-D converter	10-bit A-D converter: 1 circuit, 8 channels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •Ring oscillator
	Oscillation stop detection function	Stop detection of main clock oscillation
	Port	Input/Output: 22 (including LED drive port), Input: 2 (LED drive I/O port: 8, max. 20 mA)
Electrical characteristics	Power supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Power consumption	Typ. 8 mA (VCC = 5.0 V, (f(XIN) = 16 MHz, High-speed mode) Typ. 5 mA (VCC = 3.0 V, (f(XIN) = 10 MHz, High-speed mode) Typ. 35 µA (VCC = 3.0 V, Wait mode, Peripheral clock off) Typ. 0.7 µA (VCC = 3.0 V, Stop mode)
Flash memory	Program/erase voltage	VCC = 2.7 to 5.5 V
	Number of program/erase	100 times
Operating ambient temperature		-20 to 85 °C -40 to 85 °C (option)
Package		32-pin plastic mold LQFP

Option: If you require this option, please specify so.

1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

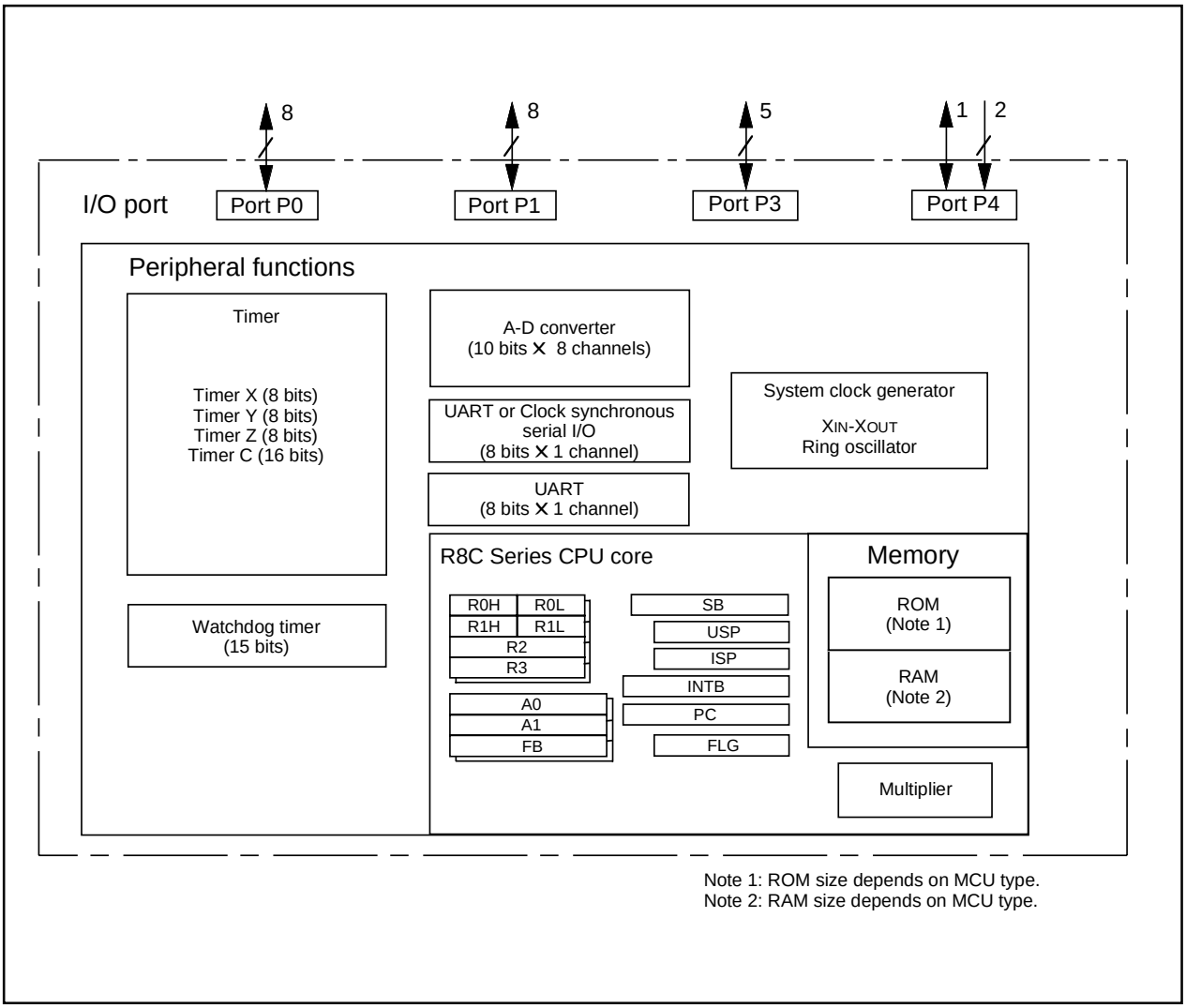


Figure 1.1 Block Diagram

1.4 Product List

Table 1.2 lists the products.

Table 1.2 Product List

As of Oct. 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks
R5F21102FP	8K bytes	512 bytes	32P6U-A	Flash memory version
R5F21103FP	12K bytes	768 bytes	32P6U-A	
R5F21104FP	16K bytes	1K bytes	32P6U-A	
R5F21102DFP **	8K bytes	512 bytes	32P6U-A	D version
R5F21103DFP **	12K bytes	768 bytes	32P6U-A	
R5F21104DFP **	16K bytes	1K bytes	32P6U-A	

** : Under development

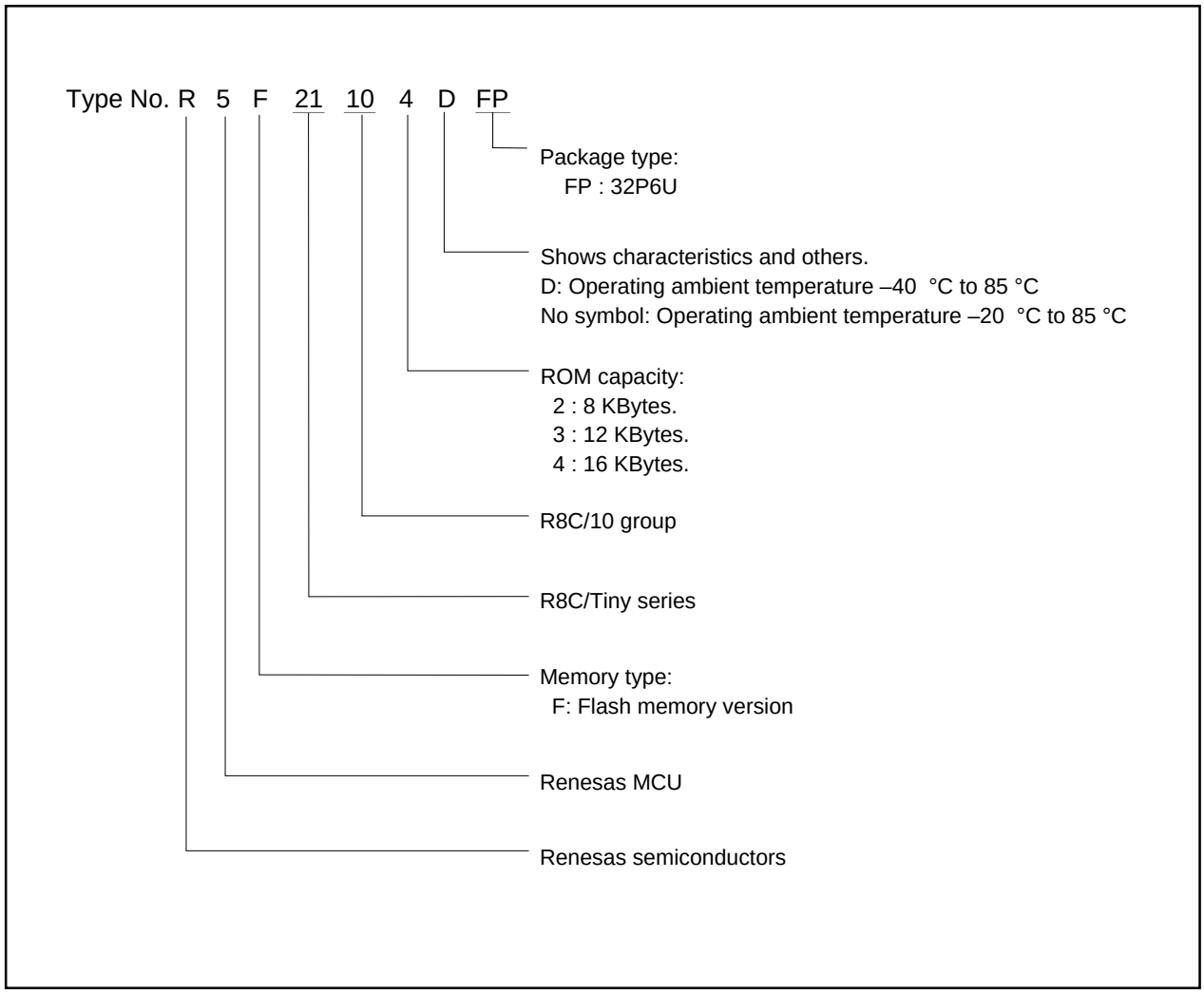
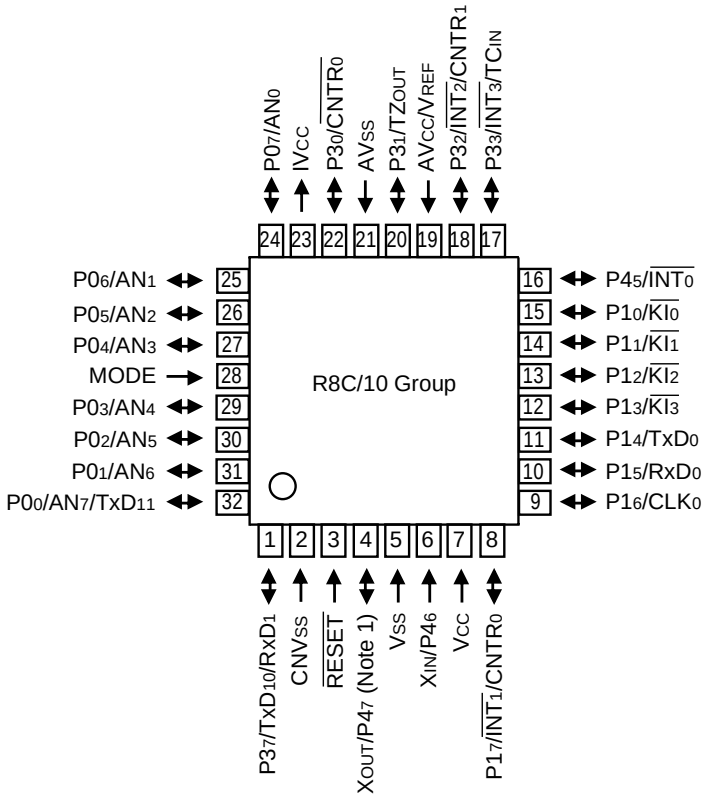


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Configuration

Figure 1.3 shows the pin configuration (top view).

PIN CONFIGURATION (top view)



Notes:
1. P47 functions only as an input port.
2. When using On-chip debugger, do not use pins P00/AN7/TxD11 and P37/TxD10/RxD1.

Package: 32P6U-A

Figure 1.3 Pin Configuration (Top View)

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	Input	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	Output	Connect this pin to Vss via a capacitor (0.1 µF).
Analog power supply input	AVcc, AVss	Input	These are power supply input pins for A-D converter. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	$\overline{\text{RESET}}$	Input	"L" on this input resets the MCU.
CNVss	CNVss	Input	Connect this pin to Vss via a resistor.
MODE	MODE	Input	Connect this pin to Vcc via a resistor.
Main clock input	X_{IN}	Input	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or a crystal oscillator between the X_{IN} and X_{OUT} pins. To use an externally derived clock, input it to the X_{IN} pin and leave the X_{OUT} pin open.
Main clock output	X_{OUT}	Output	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT}}_0$ to $\overline{\text{INT}}_3$	Input	These are $\overline{\text{INT}}$ interrupt input pins.
Key input interrupt input	$\overline{\text{KI}}_0$ to $\overline{\text{KI}}_3$	Input	These are key input interrupt input pins.
Timer X	CNTR_0	Input/Output	This is the timer X I/O pin.
	$\overline{\text{CNTR}}_0$	Output	This is the timer X output pin.
Timer Y	CNTR_1	Input/Output	This is the timer Y I/O pin.
Timer Z	TZ_{OUT}	Output	This is the timer Z output pin.
Timer C	TC_{IN}	Input	This is the timer C input pin.
Serial interface	CLK_0	Input/Output	This is a transfer clock I/O pin.
	RxD_0, RxD_1	Input	These are serial data input pins.
	TxD_0, TxD_{10}, TxD_{11}	Output	These are serial data output pins.
Reference voltage input	V_{REF}	Input	This is a reference voltage input pin for A-D converter.
A-D converter	AN_0 to AN_7	Input	These are analog input pins for A-D converter.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P3_0 to P3_3, P3_7, P4_5	Input/Output	These are 8-bit CMOS I/O ports. Each port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P1_0 to P1_7 also function as LED drive ports.
Input port	P4_6, P4_7	Input	These are input only pins.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

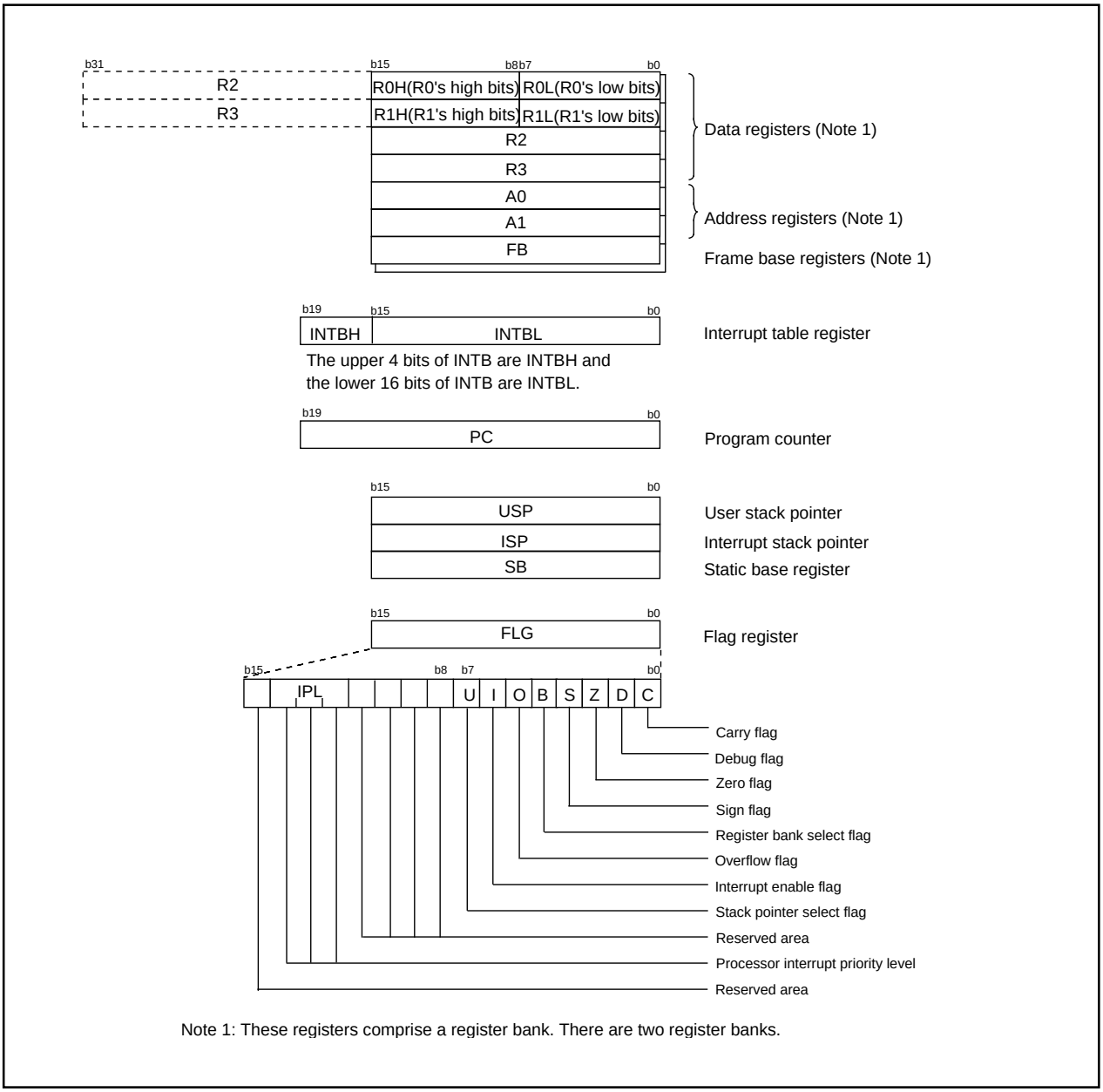


Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is cleared to “0” when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.

The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

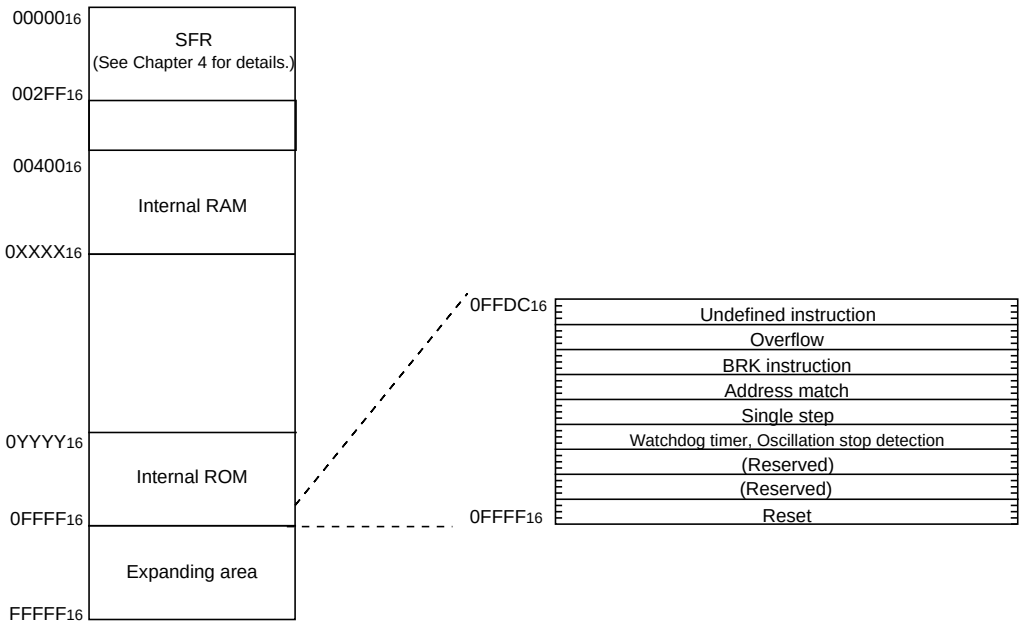
Figure 3.1 is a memory map of this MCU. The address space extends the 1M bytes from address 00000_{16} to $FFFFF_{16}$.

The internal ROM is allocated in a lower address direction beginning with address $0FFFF_{16}$. For example, a 16-Kbyte internal ROM is allocated to the addresses from $0C000_{16}$ to $0FFFF_{16}$.

The fixed interrupt vector table is allocated to the addresses from $0FFDC_{16}$ to $0FFFF_{16}$. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400_{16}. For example, a 1-Kbyte internal RAM is allocated to the addresses from 00400_{16} to $007FF_{16}$. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

Special function registers (SFR) are allocated to the addresses from 00000_{16} to $002FF_{16}$. Peripheral function control registers are located here. Of the SFR, any space which has no functions allocated is reserved for future use and cannot be used by users.



Type name	Internal ROM		Internal RAM	
	Size	Address $0YYYY_{16}$	Size	Address $0XXXX_{16}$
R5F21104FP, R5F21104DFP	16K bytes	$0C000_{16}$	1K bytes	$007FF_{16}$
R5F21103FP, R5F21103DFP	12K bytes	$0D000_{16}$	768 bytes	$006FF_{16}$
R5F21102FP, R5F21102DFP	8K bytes	$0E000_{16}$	512 bytes	$005FF_{16}$

Figure 3.1 Memory Map

4. Special Function Register (SFR)

Address	Register	Symbol	After reset
0000_{16}			
0001_{16}			
0002_{16}			
0003_{16}			
0004_{16}	Processor mode register 0	PM0	00_{16}
0005_{16}	Processor mode register 1	PM1	00_{16}
0006_{16}	System clock control register 0	CM0	01101000_{2}
0007_{16}	System clock control register 1	CM1	00100000_{2}
0008_{16}			
0009_{16}	Address match interrupt enable register	AIER	$XXXXXX00_{2}$
$000A_{16}$	Protect register	PRCR	$00XXX000_{2}$
$000B_{16}$			
$000C_{16}$	Oscillation stop detection register	OCD	00000100_{2}
$000D_{16}$	Watchdog timer reset register	WDTR	XX_{16}
$000E_{16}$	Watchdog timer start register	WDTS	XX_{16}
$000F_{16}$	Watchdog timer control register	WDC	$000XXXXX_{2}$
0010_{16} 0011_{16} 0012_{16}	Address match interrupt register 0	RMAD0	00_{16} 00_{16} $X0_{16}$
0013_{16}			
0014_{16} 0015_{16} 0016_{16}	Address match interrupt register 1	RMAD1	00_{16} 00_{16} $X0_{16}$
0017_{16}			
0018_{16}			
0019_{16}			
$001A_{16}$			
$001B_{16}$			
$001C_{16}$			
$001D_{16}$			
$001E_{16}$	INT0 input filter select register	INT0F	$XXXXX000_{2}$
$001F_{16}$			
0020_{16}			
0021_{16}			
0022_{16}			
0023_{16}			
0024_{16}			
0025_{16}			
0026_{16}			
0027_{16}			
0028_{16}			
0029_{16}			
$002A_{16}$			
$002B_{16}$			
$002C_{16}$			
$002D_{16}$			
$002E_{16}$			
$002F_{16}$			
0030_{16}			
0031_{16}			
0032_{16}			
0033_{16}			
0034_{16}			
0035_{16}			
0036_{16}			
0037_{16}			
0038_{16}			
0039_{16}			
$003A_{16}$			
$003B_{16}$			
$003C_{16}$			
$003D_{16}$			
$003E_{16}$			
$003F_{16}$			

X : Undefined
Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	After reset
0040$_{16}$			
0041$_{16}$			
0042$_{16}$			
0043$_{16}$			
0044$_{16}$			
0045$_{16}$			
0046$_{16}$			
0047$_{16}$			
0048$_{16}$			
0049$_{16}$			
004A$_{16}$			
004B$_{16}$			
004C$_{16}$			
004D$_{16}$	Key input interrupt control register	KUPIC	XXXXX000$_{2}$
004E$_{16}$	A-D conversion interrupt control register	ADIC	XXXXX000$_{2}$
004F$_{16}$			
0050$_{16}$			
0051$_{16}$	UART0 transmit interrupt control register	S0TIC	XXXXX000$_{2}$
0052$_{16}$	UART0 receive interrupt control register	S0RIC	XXXXX000$_{2}$
0053$_{16}$	UART1 transmit interrupt control register	S1TIC	XXXXX000$_{2}$
0054$_{16}$	UART1 receive interrupt control register	S1RIC	XXXXX000$_{2}$
0055$_{16}$	INT2 interrupt control register	INT2IC	XXXXX000$_{2}$
0056$_{16}$	Timer X interrupt control register	TXIC	XXXXX000$_{2}$
0057$_{16}$	Timer Y interrupt control register	TYIC	XXXXX000$_{2}$
0058$_{16}$	Timer Z interrupt control register	TZIC	XXXXX000$_{2}$
0059$_{16}$	INT1 interrupt control register	INT1IC	XXXXX000$_{2}$
005A$_{16}$	INT3 interrupt control register	INT3IC	XXXXX000$_{2}$
005B$_{16}$	Timer C interrupt control register	TCIC	XXXXX000$_{2}$
005C$_{16}$			
005D$_{16}$	INT0 interrupt control register	INT0IC	XX00X000$_{2}$
005E$_{16}$			
005F$_{16}$			
0060$_{16}$			
0061$_{16}$			
0062$_{16}$			
0063$_{16}$			
0064$_{16}$			
0065$_{16}$			
0066$_{16}$			
0067$_{16}$			
0068$_{16}$			
0069$_{16}$			
006A$_{16}$			
006B$_{16}$			
006C$_{16}$			
006D$_{16}$			
006E$_{16}$			
006F$_{16}$			
0070$_{16}$			
0071$_{16}$			
0072$_{16}$			
0073$_{16}$			
0074$_{16}$			
0075$_{16}$			
0076$_{16}$			
0077$_{16}$			
0078$_{16}$			
0079$_{16}$			
007A$_{16}$			
007B$_{16}$			
007C$_{16}$			
007D$_{16}$			
007E$_{16}$			
007F$_{16}$			

X : Undefined
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Address	Register	Symbol	After reset
0080_{16}	Timer Y, Z mode register	TYZMR	00_{16}
0081_{16}	Prescaler Y	PREY	FF_{16}
0082_{16}	Timer Y secondary	TYSC	FF_{16}
0083_{16}	Timer Y primary	TYPR	FF_{16}
0084_{16}	Timer Y, Z waveform output control register	PUM	00_{16}
0085_{16}	Prescaler Z	PREZ	FF_{16}
0086_{16}	Timer Z secondary	TZSC	FF_{16}
0087_{16}	Timer Z primary	TZPR	FF_{16}
0088_{16}			
0089_{16}			
$008A_{16}$	Timer Y, Z output control register	TYZOC	00_{16}
$008B_{16}$	Timer X mode register	TXMR	00_{16}
$008C_{16}$	Prescaler X	PREX	FF_{16}
$008D_{16}$	Timer X register	TX	FF_{16}
$008E_{16}$	Count source set register	TCSS	00_{16}
$008F_{16}$			
0090_{16} 0091_{16}	Timer C register	TC	00_{16} 00_{16}
0092_{16}			
0093_{16}			
0094_{16}			
0095_{16}			
0096_{16}	External input enable register	INTEN	00_{16}
0097_{16}			
0098_{16}	Key input enable register	KIEN	00_{16}
0099_{16}			
$009A_{16}$	Timer C control register 0	TCC0	00_{16}
$009B_{16}$	Timer C control register 1	TCC1	00_{16}
$009C_{16}$ $009D_{16}$	Capture register	TM0	XX_{16} XX_{16}
$009E_{16}$			
$009F_{16}$			
$00A0_{16}$	UART0 transmit/receive mode register	U0MR	00_{16}
$00A1_{16}$	UART0 bit rate generator	U0BRG	XX_{16}
$00A2_{16}$ $00A3_{16}$	UART0 transmit buffer register	U0TB	XX_{16} XX_{16}
$00A4_{16}$	UART0 transmit/receive control register 0	U0C0	00001000_2
$00A5_{16}$	UART0 transmit/receive control register 1	U0C1	00000010_2
$00A6_{16}$ $00A7_{16}$	UART0 receive buffer register	U0RB	XX_{16} XX_{16}
$00A8_{16}$	UART1 transmit/receive mode register	U1MR	00_{16}
$00A9_{16}$	UART1 bit rate generator	U1BRG	XX_{16}
$00AA_{16}$ $00AB_{16}$	UART1 transmit buffer register	U1TB	XX_{16} XX_{16}
$00AC_{16}$	UART1 transmit/receive control register 0	U1C0	00001000_2
$00AD_{16}$	UART1 transmit/receive control register 1	U1C1	00000010_2
$00AE_{16}$ $00AF_{16}$	UART1 receive buffer register	U1RB	XX_{16} XX_{16}
$00B0_{16}$	UART transmit/receive control register 2	UCON	00_{16}
$00B1_{16}$			
$00B2_{16}$			
$00B3_{16}$			
$00B4_{16}$			
$00B5_{16}$			
$00B6_{16}$			
$00B7_{16}$			
$00B8_{16}$			
$00B9_{16}$			
$00BA_{16}$			
$00BB_{16}$			
$00BC_{16}$			
$00BD_{16}$			
$00BE_{16}$			
$00BF_{16}$			

X : Undefined
Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	After reset
$00C0_{16}$	A-D register	AD	XX_{16}
$00C1_{16}$			XX_{16}
$00C2_{16}$			
$00C3_{16}$			
$00C4_{16}$			
$00C5_{16}$			
$00C6_{16}$			
$00C7_{16}$			
$00C8_{16}$			
$00C9_{16}$			
$00CA_{16}$			
$00CB_{16}$			
$00CC_{16}$			
$00CD_{16}$			
$00CE_{16}$			
$00CF_{16}$			
$00D0_{16}$			
$00D1_{16}$			
$00D2_{16}$			
$00D3_{16}$			
$00D4_{16}$	A-D control register 2	ADCON2	00_{16}
$00D5_{16}$			
$00D6_{16}$	A-D control register 0	ADCON0	$00000XXX_2$
$00D7_{16}$	A-D control register 1	ADCON1	00_{16}
$00D8_{16}$			
$00D9_{16}$			
$00DA_{16}$			
$00DB_{16}$			
$00DC_{16}$			
$00DD_{16}$			
$00DE_{16}$			
$00DF_{16}$			
$00E0_{16}$	Port P0 register	P0	XX_{16}
$00E1_{16}$	Port P1 register	P1	XX_{16}
$00E2_{16}$	Port P0 direction register	PD0	00_{16}
$00E3_{16}$	Port P1 direction register	PD1	00_{16}
$00E4_{16}$			
$00E5_{16}$	Port P3 register	P3	XX_{16}
$00E6_{16}$			
$00E7_{16}$	Port P3 direction register	PD3	00_{16}
$00E8_{16}$	Port P4 register	P4	XX_{16}
$00E9_{16}$			
$00EA_{16}$	Port P4 direction register	PD4	00_{16}
$00EB_{16}$			
$00EC_{16}$			
$00ED_{16}$			
$00EE_{16}$			
$00EF_{16}$			
$00F0_{16}$			
$00F1_{16}$			
$00F2_{16}$			
$00F3_{16}$			
$00F4_{16}$			
$00F5_{16}$			
$00F6_{16}$			
$00F7_{16}$			
$00F8_{16}$			
$00F9_{16}$			
$03FA_{16}$			
$00FB_{16}$			
$00FC_{16}$	Pull-up control register 0	PUR0	$00XX0000_2$
$00FD_{16}$	Pull-up control register 1	PUR1	$XXXXXX0X_2$
$00FE_{16}$	Port P1 drivability control register	DRR	00_{16}
$00FF_{16}$			
≈			≈
$01B3_{16}$	Flash memory control register 4	FMR4	$0100000X_2$
$01B4_{16}$			
$01B5_{16}$	Flash memory control register 1	FMR1	$0100XX0X_2$
$01B6_{16}$			
$01B7_{16}$	Flash memory control register 0	FMR0	$XX000001_2$

X : Undefined
Blank columns are all reserved space. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}	Supply voltage	V_{CC}=AV_{CC}	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage	V_{CC}=AV_{CC}	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	Topr=25 °C	300	mW
T_{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			2.7	5.0	5.5	V
AVcc	Analog supply voltage			—	V_{CC}	—	V
Vss	Supply voltage			—	0	—	V
AVss	Analog supply voltage			—	0	—	V
V_{IH}	"H" input voltage			0.8V_{CC}	—	V_{CC}	V
V_{IL}	"L" input voltage			0	—	0.2V_{CC}	V
$I_{OH\ (sum)}$	"H" peak all output currents	Sum of all pins' IOH (peak)		—	—	-60.0	mA
$I_{OH\ (peak)}$	"H" peak output current			—	—	-10.0	mA
$I_{OH\ (avg)}$	"H" average output current			—	—	-5.0	mA
$I_{OL\ (sum)}$	"L" peak all output currents	Sum of all pins' IOL (peak)		—	—	60	mA
$I_{OL\ (peak)}$	"L" peak output current	Except $P1_0$ to $P1_7$		—	—	10	mA
		$P1_0$ to $P1_7$	Drive ability HIGH	—	—	30	mA
			Drive ability LOW	—	—	10	mA
$I_{OL\ (avg)}$	"L" average output current	Except $P1_0$ to $P1_7$		—	—	5	mA
		$P1_0$ to $P1_7$	Drive ability HIGH	—	—	15	mA
			Drive ability LOW	—	—	5	mA
f (X_{IN})	Main clock input oscillation frequency		3.0V ≤ Vcc ≤ 5.5V	0	—	16	MHz
			2.7V ≤ Vcc < 3.0V	0	—	10	MHz

Note
1: Referenced to V_{CC} = AV_{CC} = 2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2: The mean output current is the mean value within 100ms.

Table 5.3 A-D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard Min.	Standard Typ.	Standard Max.	Unit
–	Resolution		V_{ref} =V_{CC}			10	Bit
–	Absolute accuracy	10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V			±3	LSB
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V			±2	LSB
		10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=3.3V			±5	LSB
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=3.3V			±2	LSB
R_{LADDER}	Ladder resistance		V_{REF}=V_{CC}	10		40	kΩ
t_{CONV}	Conversion time	10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V	3.3			µs
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V	2.8			µs
V_{REF}	Reference voltage			2.0		V_{CC}	V
V_{IA}	Analog input voltage			0		V_{ref}	V
–	A-D operation clock frequency[2]	Without sample & hold		0.25		10	MHz
		With sample & hold		1.0		10	MHz

Note
1: Referenced to V_{CC}=AV_{CC}=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2: When f_{AD} is 10 MHz more, divide the f_{AD} and make A-D operation clock frequency ($Ø_{AD}$) lower than 10 MHz.
3: When the Vcc is less than 4.2V, divide the f_{AD} and make A-D operation clock frequency ($Ø_{AD}$) lower than f_{AD}/2.

Table 5.4 Flash Memory Version Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard Min.	Standard Typ.	Standard Max	Unit
–	Program/erase cycle		100	—	—	cycle
–	Byte program time	Vcc=5.0V, Topr=25 °C	—	50	400	µs
–	Block erase time	Vcc=5.0V, Topr=25 °C	—	0.4	9	s
–	Time delay from suspend request until erase suspend		—	—	8	ms
–	Program, Erase voltage		2.7	—	5.5	V
–	Read voltage		2.7	—	5.5	V
–	Program, Erase temperature		0	—	60	°C
–	Data-retention duration	Topr=55 °C	—	—	20	year

Note
1: Referenced to V_{CC1}=AVcc=2.7 to 5.5V at Topr = 0 to 60 °C unless otherwise specified.

Table 5.5 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard Min.	Standard Typ.	Standard Max.	Unit
td(P-R)	Time for internal power supply stabilization during powering-on[2]				2	ms
td(R-S)	STOP release time[3]				150	µs

Note
1: The measureing condition is Vcc=AVcc=2.7 to 5.5 V and Topr=25 °C.
2: This shows the waiting time till the internal power supply generating circuit is stabilized during powering-on.
3: This shows the time till BCLK starts from the interrupt acknowledgement to cancel stop mode.

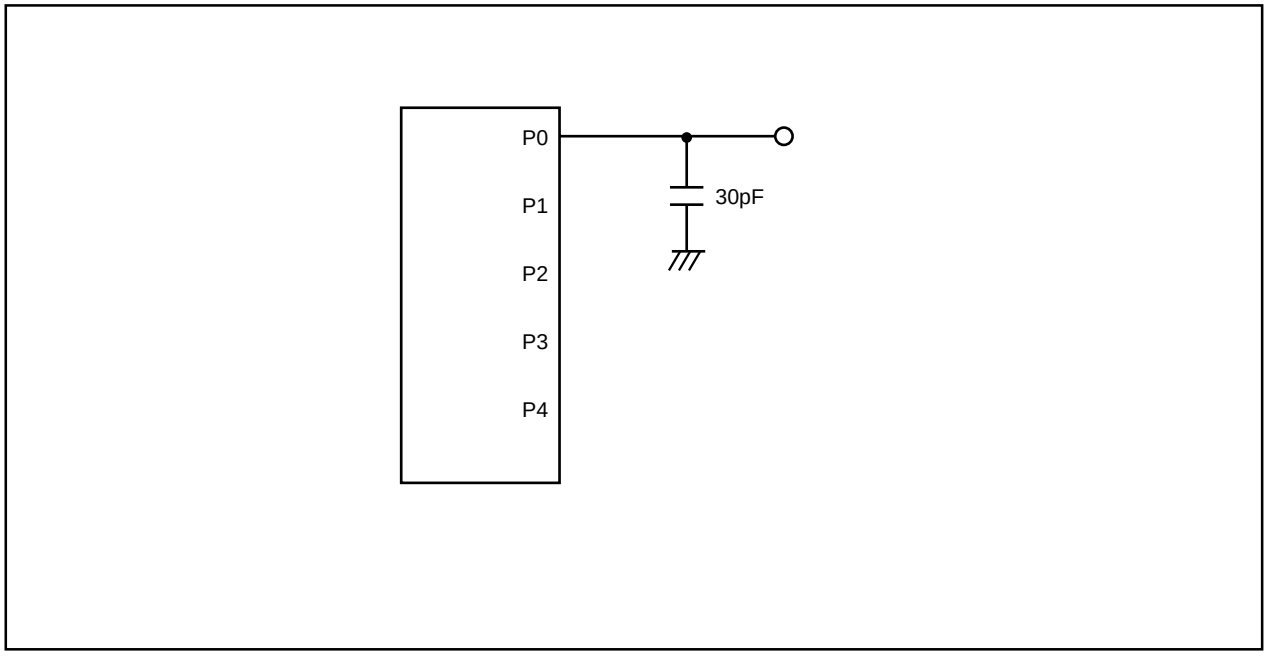


Figure 5.1 Port P0 to P4 measurement circuit

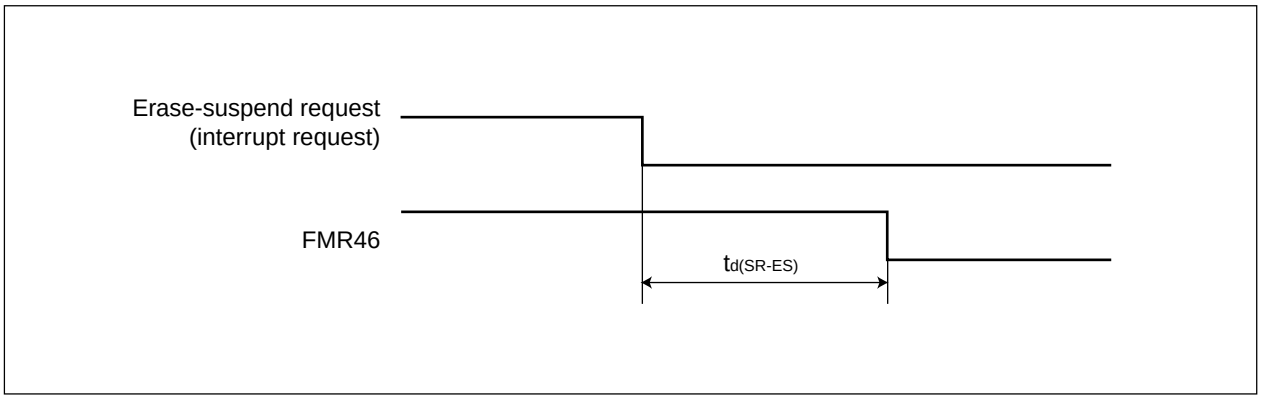


Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Electrical Characteristics (1) [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-5mA		V_{CC}-2.0		V_{CC}	V
			I_{OH}=-200µA		V_{CC}-0.3		V_{CC}	V
		X_{OUT}	Drive ability HIGH	I_{OH}=-1 mA	V_{CC}-2.0		V_{CC}	V
			Drive ability LOW	I_{OH}=-500µA	V_{CC}-2.0		V_{CC}	V
V_{OL}	"L" output voltage	P10 to P17 Except X_{OUT}	I_{OH}= 5 mA				2.0	V
			I_{OH}= 200 µA				0.45	V
		P10 to P17	Drive ability HIGH	I_{OH}= 10 mA			2.0	V
			Drive ability LOW	I_{OH}= 5 mA			2.0	V
		X_{OUT}	Drive ability HIGH	I_{OH}= 1 mA			2.0	V
			Drive ability LOW	I_{OH}=500µA			2.0	V
V_{T+}-V_{T-}	Hysteresis	INT_0, INT_1, INT_2, INT_3, KI_0, KI_1, KI_2, KI_3, $CNTR_0$, $CNTR_1$, TC_{IN}, RxD_0, RxD_1			0.2		1.0	V
		RESET			0.2		2.2	V
I_{IH}	"H" input current		V_I=5V				5.0	µA
I_{IL}	"L" input current		V_I=0V				-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	X_{IN}				1.0		MΩ
f_{RING}	Ring oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0			V

Note
1 : Referenced to V_{CC}=AV_{CC}=4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=20MHz unless otherwise specified.

Table 5.7 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter	Measuring condition		Standard Min.	Typ.	Max.	Unit
I_{CC}	Power supply current (V_{CC}=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V_{SS}	High-speed mode	X_{IN}=16 MHz (square wave) Ring oscillator on=125 kHz No division		8	14	mA
			X_{IN}=10 MHz (square wave) Ring oscillator on=125 kHz No division		5		mA
		Medium-speed mode	X_{IN}=16 MHz (square wave) Ring oscillator on=125 kHz Division by 8		3		mA
			X_{IN}=10 MHz (square wave) Ring oscillator on=125 kHz Division by 8		2		mA
		Ring oscillator mode	Main clock off Ring oscillator on=125 kHz Division by 8		0.4	2.0	mA
		Wait mode	Main clock off Ring oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation		40	80	µA
		Wait mode	Main clock off Ring oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off		38	76	µA
		Stop mode	Main clock off Ring oscillator off CM10="1" Peripheral clock off		0.8	3.0	µA

Note
1: The power supply current measuring is executed using the measuring program on frash memory.
2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: VCC = 5V, VSS = 0V at Ta = 25 °C) [VCC=5V]

Table 5.8 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(XIN)	XIN input cycle time	62.5		ns
twH(XIN)	XIN input HIGH pulse width	30		ns
twL(XIN)	XIN input LOW pulse width	30		ns

Table 5.9 CNTR0 input, CNTR1 input, $\overline{\text{INT2}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CNTR0)	CNTR0 input cycle time	100		ns
twH(CNTR0)	CNTR0 input HIGH pulse width	40		ns
twL(CNTR0)	CNTR0 input LOW pulse width	40		ns

Table 5.10 TCIN input, $\overline{\text{INT3}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TCIN)	TCIN input cycle time	400 [1]		ns
twH(TCIN)	TCIN input HIGH pulse width	200 [2]		ns
twL(TCIN)	TCIN input LOW pulse width	200 [2]		ns

Note
1 : Use the greater value,either (1/ digital filter clock frequency x 6) or min. value.
2 : Use the greater value,either (1/ digital filter clock frequency x 3) or min. value.

Table 5.11 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input HIGH pulse width	100		ns
tw(CKL)	CLKi input LOW pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	35		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.12 External interrupt $\overline{\text{INT0}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{\text{INT0}}$ input HIGH pulse width	250 [1]		ns
tw(INL)	$\overline{\text{INT0}}$ input LOW pulse width	250 [2]		ns

Note
1 : When the $\overline{\text{INT0}}$ input filter select bit selects the digital filter, use the $\overline{\text{INT0}}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or min. value.
2 : When the $\overline{\text{INT0}}$ input filter select bit selects the digital filter, use the $\overline{\text{INT0}}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or min. value.

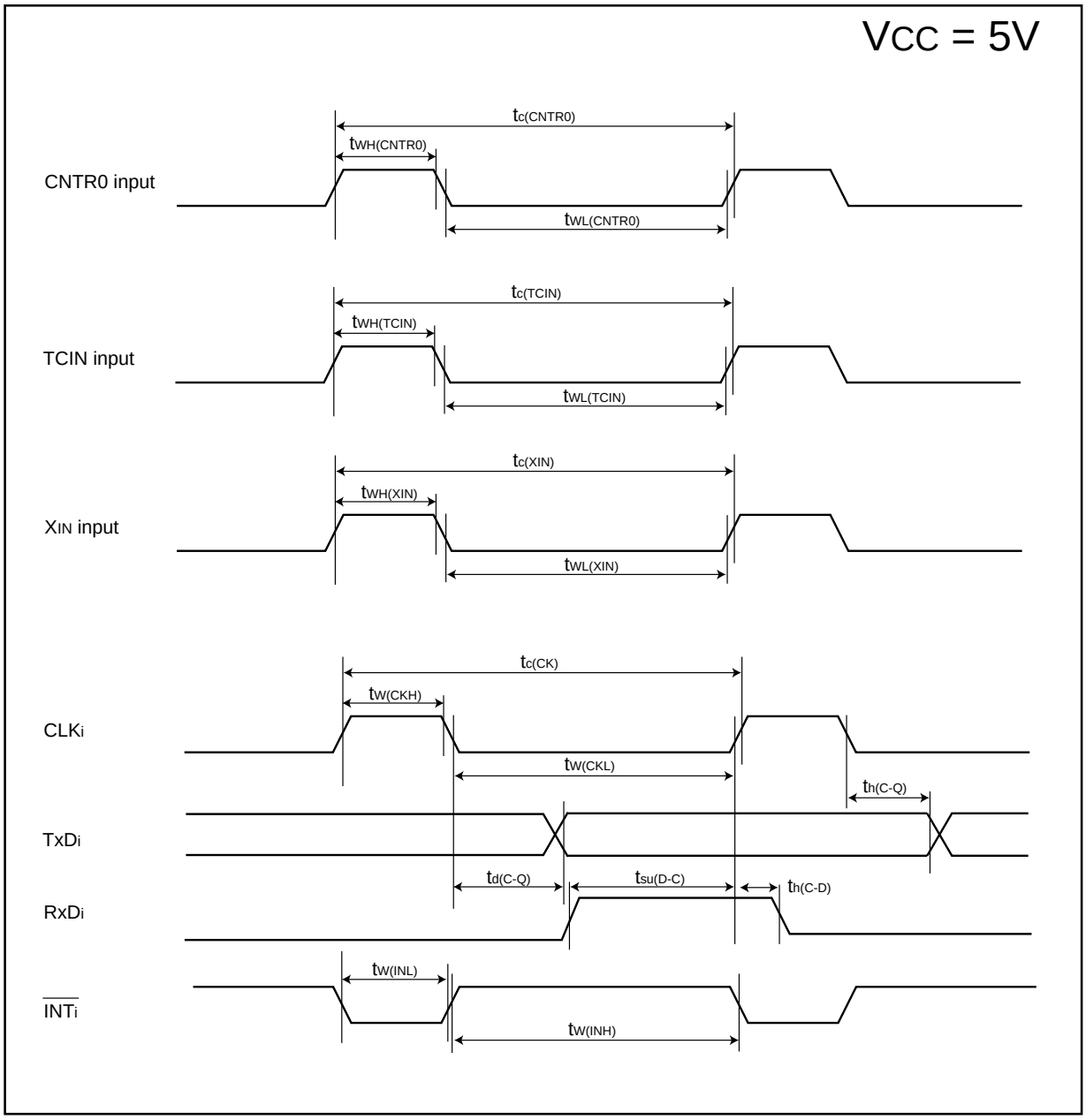


Figure 5.3 Vcc=5V timing diagram

Table 5.13 Electrical Characteristics (3) [Vcc=3V]

Symbol	Parameter		Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-1mA		V_{CC}-0.5		V_{CC}	V
		X_{OUT}	Drive ability HIGH	I_{OH}=-0.1 mA	V_{CC}-0.5		V_{CC}	V
			Drive ability LOW	I_{OH}=-50 µA	V_{CC}-0.5		V_{CC}	V
V_{OL}	"L" output voltage	P10 to P17 Except X_{OUT}	I_{OH}= 1 mA				0.5	V
		P10 to P17	Drive ability HIGH	I_{OH}= 2 mA			0.5	V
			Drive ability LOW	I_{OH}= 1 mA			0.5	V
		X_{OUT}	Drive ability HIGH	I_{OH}= 0.1 mA			0.5	V
			Drive ability LOW	I_{OH}=50 µA			0.5	V
V_{T+}-V_{T-}	Hysteresis	INT_0, INT_1, INT_2, INT_3, KI_0, KI_1, KI_2, KI_3, $CNTR_0$, $CNTR_1$, $TCIN$, RxD_0, RxD_1			0.2		0.8	V
		RESET			0.2		1.8	V
I_{IH}	"H" input current		V_I=3V				4.0	µA
I_{IL}	"L" input current		V_I=0V				-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	X_{IN}				3.0		MΩ
f_{RING}	Ring oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0			V

Note
1 : Referenced to V_{CC}=AV_{CC}=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.

Table 5.14 Electrical Characteristics (4) [Vcc=3V]

Symbol	Parameter	Measuring condition		Standard Min.	Typ.	Max.	Unit
I_{CC}	Power supply current (V_{CC1}=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V_{SS}	High-speed mode	X_{IN}=16 MHz (square wave) Ring oscillator on=125 kHz No division		7	12	mA
			X_{IN}=10 MHz (square wave) Ring oscillator on=125 kHz No division		5		mA
		Medium-speed mode	X_{IN}=16 MHz (square wave) Ring oscillator on=125 kHz Division by 8		2.5		mA
			X_{IN}=10 MHz (square wave) Ring oscillator on=125 kHz Division by 8		1.6		mA
		Ring oscillator mode	Main clock off Ring oscillator on=125 kHz Division by 8		0.4	2.0	mA
		Wait mode	Main clock off Ring oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation		37	74	µA
		Wait mode	Main clock off Ring oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off		35	70	µA
		Stop mode	Main clock off Ring oscillator off CM10="1" Peripheral clock off		0.7	3.0	µA

Note
1: The power supply current measuring is executed using the measuring program on frash memory.
2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: VCC = 3V, VSS = 0V at Ta = 25 °C) [VCC=3V]

Table 5.15 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(XIN)	XIN input cycle time	143		ns
twH(XIN)	XIN input HIGH pulse width	70		ns
twL(XIN)	XIN input LOW pulse width	70		ns

Table 5.16 CNTR0 input, CNTR1 input, $\overline{\text{INT2}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CNTR0)	CNTR0 input cycle time	300		ns
twH(CNTR0)	CNTR0 input HIGH pulse width	120		ns
twL(CNTR0)	CNTR0 input LOW pulse width	120		ns

Table 5.17 TCIN input, $\overline{\text{INT3}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TCIN)	TCIN input cycle time	1200 [1]		ns
twH(TCIN)	TCIN input HIGH pulse width	600 [2]		ns
twL(TCIN)	TCIN input LOW pulse width	600 [2]		ns

Note
1 : Use the greater value,either (1/ digital filter clock frequency x 6) or min. value.
2 : Use the greater value,either (1/ digital filter clock frequency x 3) or min. value.

Table 5.18 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	300		ns
tw(CKH)	CLKi input HIGH pulse width	150		ns
tw(CKL)	CLKi input LOW pulse width	150		ns
td(C-Q)	TxDi output delay time		160	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	55		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.19 External interrupt $\overline{\text{INT0}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{\text{INT0}}$ input HIGH pulse width	380 [1]		ns
tw(INL)	$\overline{\text{INT0}}$ input LOW pulse width	380 [2]		ns

Note
1 : When the $\overline{\text{INT0}}$ input filter select bit selects the digital filter, use the $\overline{\text{INT0}}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or min. value.
2 : When the $\overline{\text{INT0}}$ input filter select bit selects the digital filter, use the $\overline{\text{INT0}}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or min. value.

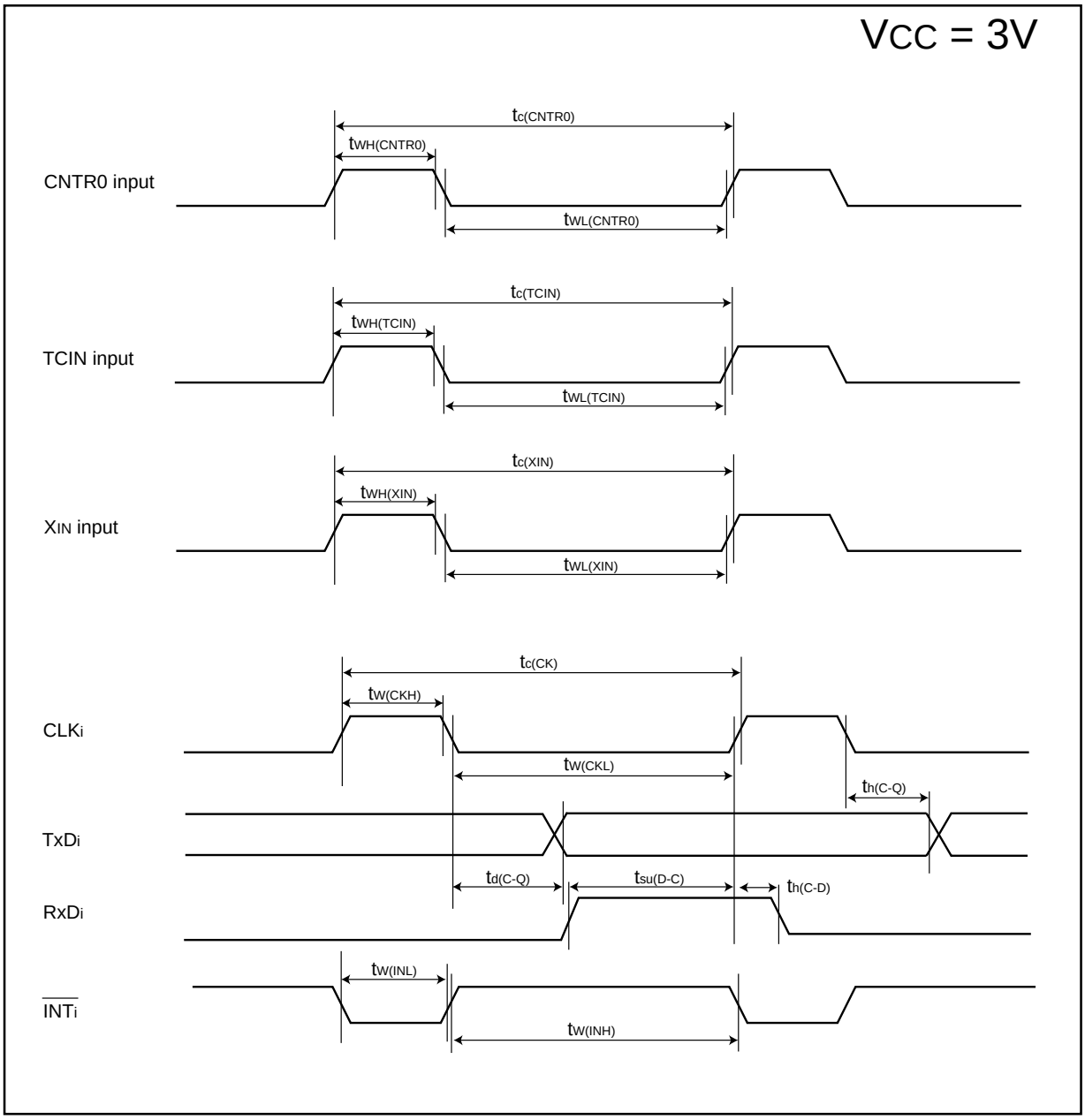
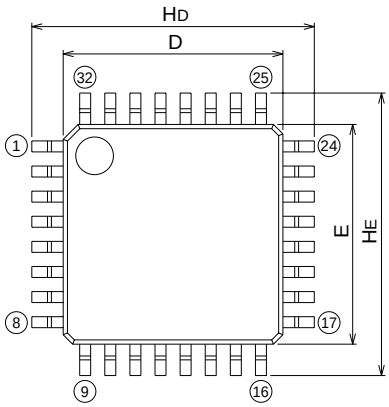


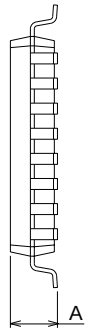
Figure 5.4 Vcc=3V timing diagram

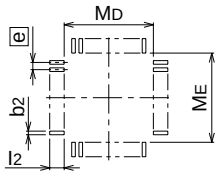
Package Dimensions

32P6U-A (MMP) **Plastic 32pin 7×7mm body LQFP**

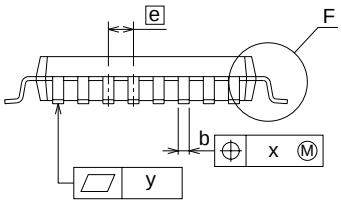
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP32-P-0707-0.80	–		Cu Alloy

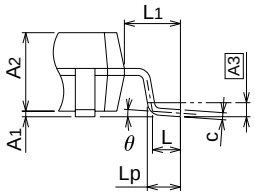






Recommended Mount Pad





Detail F

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.8	–
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.2
y	–	–	0.1
θ	0°	–	10°
b2	–	0.5	–
l2	1.0	–	–
MD	–	7.4	–
ME	–	7.4	–

REVISION HISTORY	R8C/10 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 19, 2003		First edition issued
1.10	Sep. 08, 2003	2 5 6 12 14	Table 1.1: Shortest instruction execution time and f(X_{IN}) changed Figure 1.3: Pin name changed from TX_{OUT} to $\overline{CNTR_0}$ Table 1.3: Pin name changed from TX_{OUT} to $\overline{CNTR_0}$ The value of Time C register after reset changed Chapter “5. Electrical Characteristics” added
1.20	Oct. 31, 2003	2 6 14 15 16 18 19 20 21 22 23 24	Table 1.1: Power consumption values added Table 1.3: Resistor value for CNVss and MODE deleted Table 5.2: Note 3 and Note 4 deleted t_{samp} in Table 5.3 deleted Figure 5.1 added Table 5.7: Vcc changed from “4.2 to 5.5V” to “3.3V to 5.5V”, ring oscillator changed from “on 100kHz” to “125kHz”, X_{IN}=5MHz deleted and X_{IN}=10MHz added in high-speed mode and medium-speed mode, data added and modified Table 5.8 to Table 5.12 added Figure 5.2 added Table 5.13: Note 1, $f_{(BCLK)}$=5 MHz changed to 10 MHz Table 5.14: ring oscillator changed from “on 100kHz” to “125kHz”, X_{IN}=5MHz deleted and X_{IN}=10MHz added in high-speed mode and medium-speed mode, data added and modified Table 5.15 to Table 5.19 added Figure 5.3 added
1.30	Dec 05, 2003	4 15	Table 1.2 : ** deleted Table 5.4 revised
1.30	Dec 05, 2003	15 16	Table 5.4 revised Figure 5.2 added

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