1. Overview

The M32C/84 group (M32C/84, M32C/84T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/84 group (M32C/84, M32C/84T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.
With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.
It incorporates a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.2 Performance Outline

Tables 1.1 and 1.2 list performance outlines of the M32C/84 group (M32C/84, M32C/84T).

Table 1.1 M32C/84 Group (M32C/84, M32C/84T) Performance (144-Pin Package)

Characteristic		Performance	
		M32C/84	M32C/84T
CPU	Basic Instructions	108 instructions	
	Shortest Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V) 41.7 ns (f(BCLK)=24 MHz, V_{CC1}=3.0 V to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V)
	Operation Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	123 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I^2C bus(2)	
	CAN Module	1 channels Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 1 circuit, 34 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	XY Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	38 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generating Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
	Supply Voltage Detect Circuit	Available (optional)	Not available
Electrical Characteristics	Supply Voltage	V_{CC1}=4.2 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=32 MHz) V_{CC1}=3.0 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=24 MHz)	V_{CC1}=V_{CC2}=4.2 V to 5.5 V, (f(BCLK)=32 MHz)(3)
	Power Consumption	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 22 mA (V_{CC1}=V_{CC2}=3.3 V, f(BCLK)=24 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(X_{CIN})=32 kHz, in wait mode)	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(X_{CIN})=32 kHz, in wait mode)
Flash Memory	Program/Erase Supply Voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V	5.0 V ± 0.5 V
	Program and Erase Endurance	100 cycles (all space)	
Operating Ambient Temperature		–20 to 85°C –40 to 85°C (optional)	–40 to 85°C (T version)
Package		144-pin plastic molded LQFP	

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. The supply voltage of M32C/84T (High-reliability version) must be V_{CC1}=V_{CC2}.

All options are on a request basis.

Table 1.2 M32C/84 Group (M32C/84, M32C/84T) Performance (100-Pin Package)

Characteristic		Performance	
		M32C/84	M32C/84T
CPU	Basic Instructions	108 instructions	
	Shortest Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V) 41.7 ns (f(BCLK)=24 MHz, V_{CC1}=3.0 V to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V)
	Operation Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	87 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I^2C bus(2)	
	CAN Module	1 channels Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	XY Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	38 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generating Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
	Supply Voltage Detect Circuit	Available (optional)	Not available
Electrical Characteristics	Supply Voltage	V_{CC1}=4.2 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=32 MHz) V_{CC1}=3.0 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=24 MHz)	V_{CC1}=V_{CC2}=4.2 V to 5.5 V, (f(BCLK)=32 MHz)(3)
	Power Consumption	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 22 mA (V_{CC1}=V_{CC2}=3.3 V, f(BCLK)=24 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(X_{CIN})=32 kHz, wait mode)	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(X_{CIN})=32 kHz, wait mode)
Flash Memory	Program/Erase Supply Voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V	5.0 V ± 0.5 V
	Program and Erase Endurance	100 cycles (all space)	
Operating Ambient Temperature		–20 to 85°C –40 to 85°C (optional)	–40 to 85°C (T version)
Package		100-pin plastic molded LQFP/QFP	

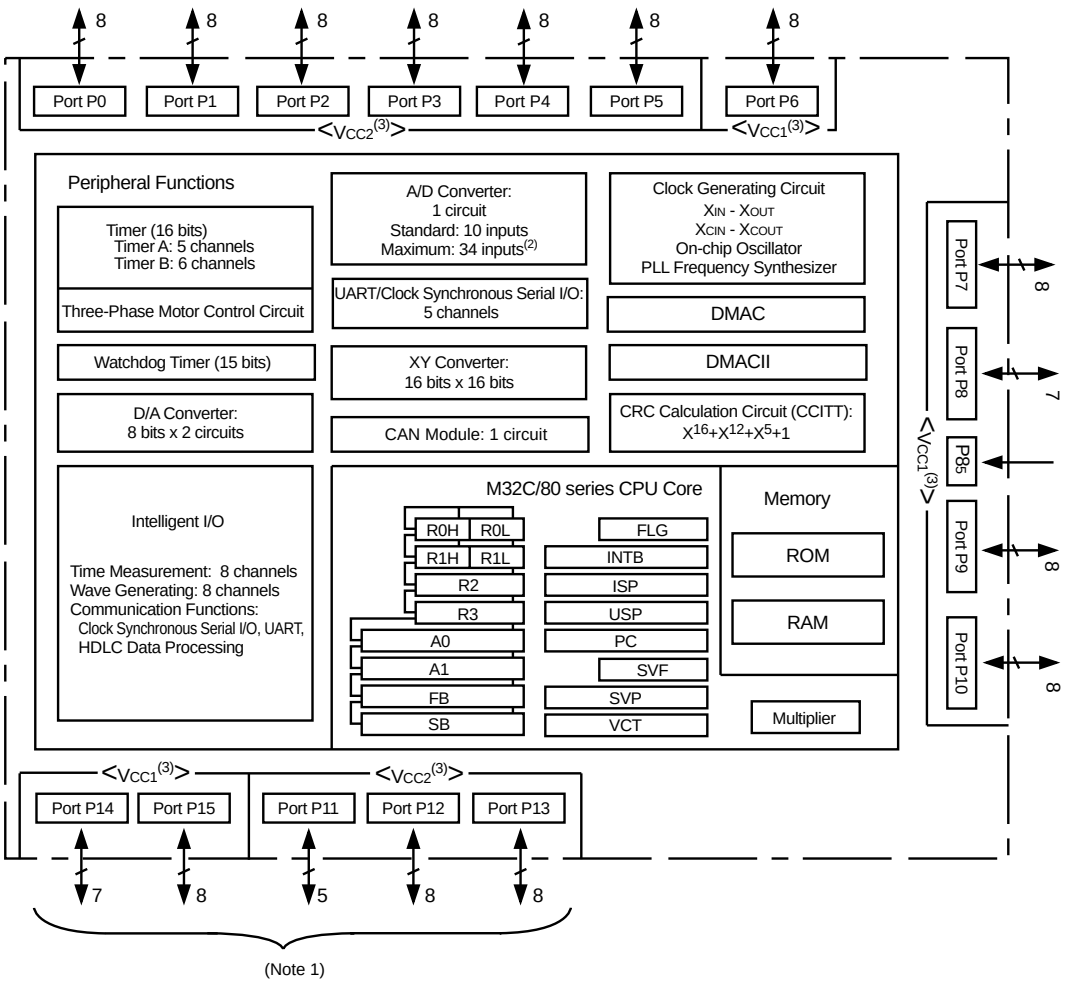
NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
2. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. The supply voltage of M32C/84T (High-reliability version) must be V_{CC1}=V_{CC2}.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/84 group (M32C/84, M32C/84T) microcomputer.



NOTES:
1. Ports P11 to P15 are provided in the 144-pin package only.
2. Included in the 144-pin package only.
3. The supply voltage of M32C/84T (High-reliability version) must be $V_{CC1}=V_{CC2}$.

Figure 1.1 M32C/84 Group (M32C/84, M32C/84T) Block Diagram

1.4 Product Information

Table 1.3 lists product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/84 Group (1) (M32C/84) **As of June, 2004**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks
M30845FJGP (D)	512K+4K	24K	144P6Q-A	Flash Memory
M30843FJGP (D)			100P6Q-A	
M30843FJFP (D)			100P6S-A	
M30845MW-XXXGP	320K	24K	144P6Q-A	Masked ROM
M30843MW-XXXGP			100P6Q-A	
M30843MW-XXXFP			100P6S-A	
M30842ME-XXXGP (P)	192K	16K	144P6Q-A	
M30840ME-XXXGP (P)			100P6Q-A	
M30840ME-XXXFP (P)			100P6S-A	
M30842MC-XXXGP (P)	128K	10K	144P6Q-A	
M30840MC-XXXGP (P)			100P6Q-A	
M30840MC-XXXFP (P)			100P6S-A	

(D): Under development (P): Planning

Table 1.3 M32C/84 Group (2) (T Version, M32C/84T) **As of June, 2004**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	
M30845FJTGP (D)	512K+4K	24K	144P6Q-A	Flash Memory	T version (High-reliability 85°C version)
M30843FJTGP (D)			100P6Q-A		

(D): Under development

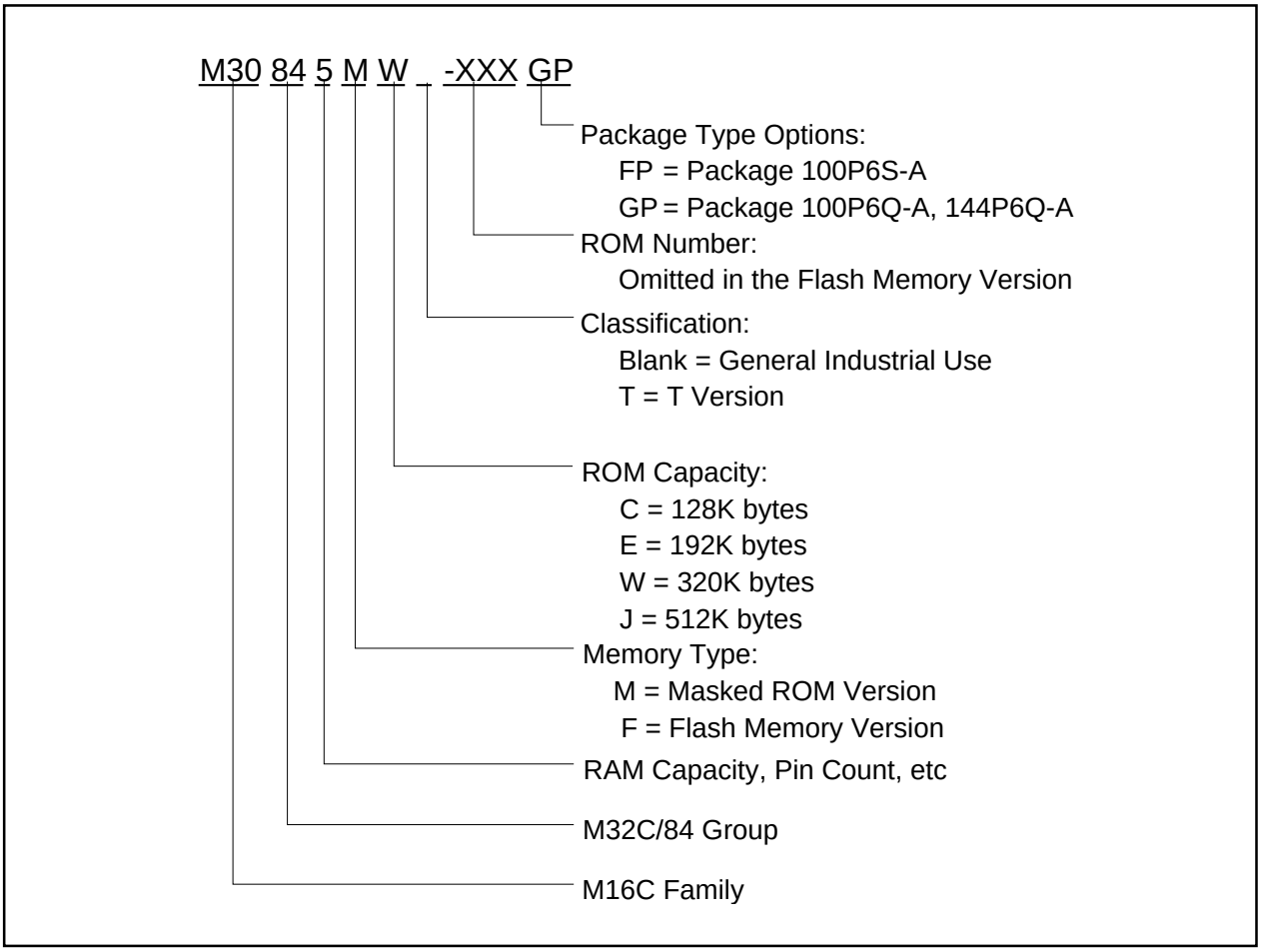


Figure 1.2 Product Numbering System

1.5 Pin Assignments and Descriptions

Figures 1.3 to 1.5 show pin assignments (top view).

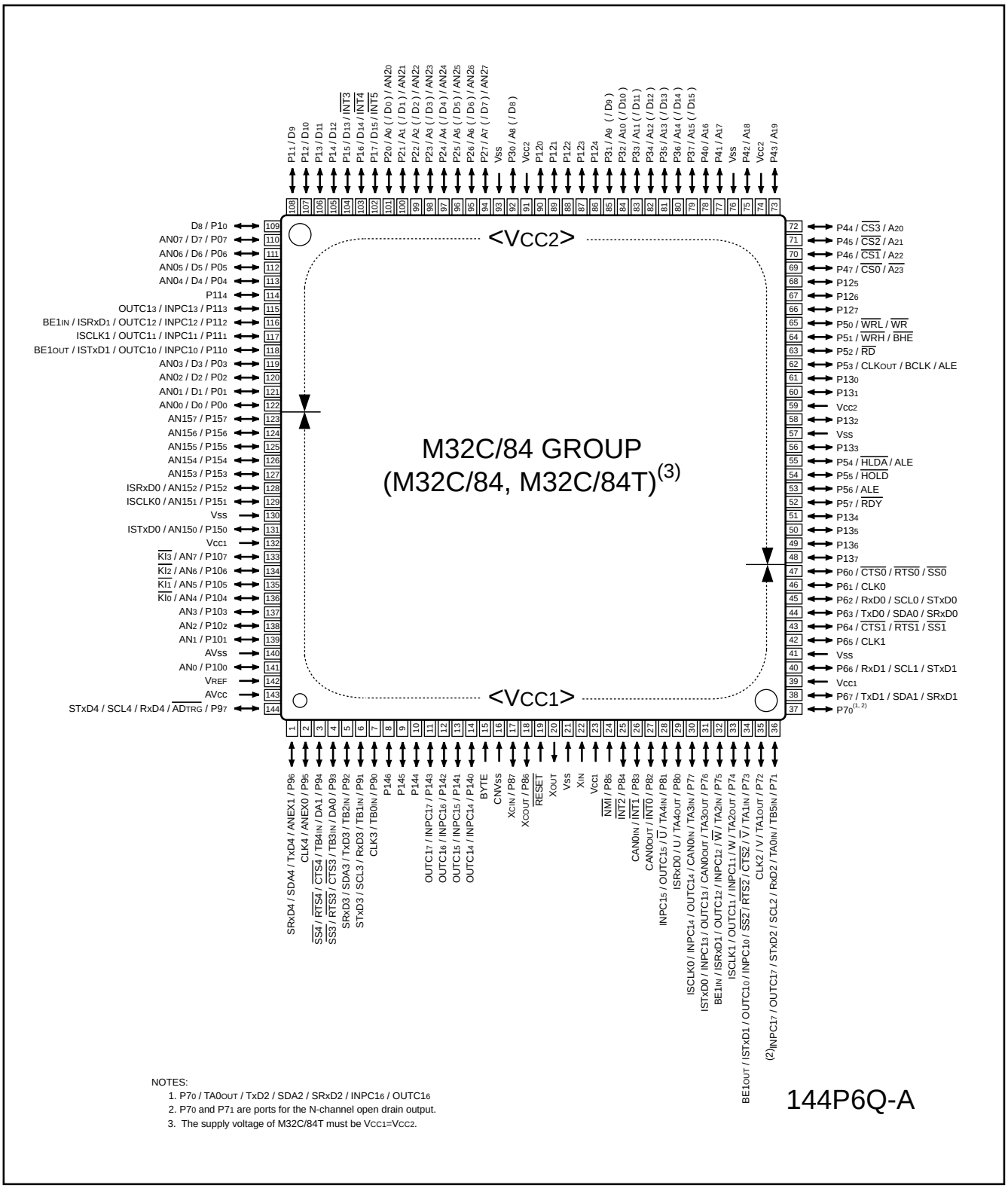


Figure 1.3 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
1		$P9_6$			TxD4/SDA4/SRxD4		ANEX1	
2		$P9_5$			CLK4		ANEX0	
3		$P9_4$		$TB4_{IN}$	$\overline{CTS4}/\overline{RTS4}/\overline{SS4}$		DA1	
4		$P9_3$		$TB3_{IN}$	$\overline{CTS3}/\overline{RTS3}/\overline{SS3}$		DA0	
5		$P9_2$		$TB2_{IN}$	TxD3/SDA3/SRxD3			
6		$P9_1$		$TB1_{IN}$	RxD3/SCL3/STxD3			
7		$P9_0$		$TB0_{IN}$	CLK3			
8		$P14_6$						
9		$P14_5$						
10		$P14_4$						
11		$P14_3$				$INPC1_7/OUTC1_7$		
12		$P14_2$				$INPC1_6/OUTC1_6$		
13		$P14_1$				$INPC1_5/OUTC1_5$		
14		$P14_0$				$INPC1_4/OUTC1_4$		
15	BYTE							
16	CNV_{SS}							
17	X_{CIN}	$P8_7$						
18	X_{COUT}	$P8_6$						
19	$\overline{RESET}$							
20	X_{OUT}							
21	V_{SS}							
22	X_{IN}							
23	V_{CC1}							
24		$P8_5$	$\overline{NMI}$					
25		$P8_4$	$\overline{INT2}$					
26		$P8_3$	$\overline{INT1}$		$CAN0_{IN}$			
27		$P8_2$	$\overline{INT0}$		$CAN0_{OUT}$			
28		$P8_1$		$TA4_{IN}/\overline{U}$		$INPC1_5/OUTC1_5$		
29		$P8_0$		$TA4_{OUT}/U$		ISRxD0		
30		$P7_7$		$TA3_{IN}$	$CAN0_{IN}$	$INPC1_4/OUTC1_4$/ISCLK0		
31		$P7_6$		$TA3_{OUT}$	$CAN0_{OUT}$	$INPC1_3/OUTC1_3$/ISTxD0		
32		$P7_5$		$TA2_{IN}/\overline{W}$		$INPC1_2/OUTC1_2$/ISRxD1/$BE1_{IN}$		
33		$P7_4$		$TA2_{OUT}/W$		$INPC1_1/OUTC1_1$/ISCLK1		
34		$P7_3$		$TA1_{IN}/\overline{V}$	$\overline{CTS2}/\overline{RTS2}/\overline{SS2}$	$INPC1_0/OUTC1_0$/ISTxD1/$BE1_{OUT}$		
35		$P7_2$		$TA1_{OUT}/V$	CLK2			
36		$P7_1$		$TB5_{IN}/TA0_{IN}$	RxD2/SCL2/STxD2	$INPC1_7/OUTC1_7$		
37		$P7_0$		$TA0_{OUT}$	TxD2/SDA2/SRxD2	$INPC1_6/OUTC1_6$		
38		$P6_7$			TxD1/SDA1/SRxD1			
39	V_{CC1}							
40		$P6_6$			RxD1/SCL1/STxD1			
41	V_{SS}							
42		$P6_5$			CLK1			
43		$P6_4$			$\overline{CTS1}/\overline{RTS1}/\overline{SS1}$			
44		$P6_3$			TxD0/SDA0/SRxD0			
45		$P6_2$			RxD0/SCL0/STxD0			
46		$P6_1$			CLK0			
47		$P6_0$			$\overline{CTS0}/\overline{RTS0}/\overline{SS0}$			
48		$P13_7$						

NOTES:

1. Bus control pins in M32C/84T cannot be used.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
49		$P13_6$						
50		$P13_5$						
51		$P13_4$						
52		$P5_7$						$\overline{RDY}$
53		$P5_6$						ALE
54		$P5_5$						$\overline{HOLD}$
55		$P5_4$						$\overline{HLDA}$/ALE
56		$P13_3$						
57	V_{SS}							
58		$P13_2$						
59	V_{CC2}							
60		$P13_1$						
61		$P13_0$						
62		$P5_3$						CLK_{OUT}/BCLK/ALE
63		$P5_2$						$\overline{RD}$
64		$P5_1$						$\overline{WRH}$/$\overline{BHE}$
65		$P5_0$						$\overline{WRL}$/$\overline{WR}$
66		$P12_7$						
67		$P12_6$						
68		$P12_5$						
69		$P4_7$						$\overline{CS0}$/A_{23}
70		$P4_6$						$\overline{CS1}$/A_{22}
71		$P4_5$						$\overline{CS2}$/A_{21}
72		$P4_4$						$\overline{CS3}$/A_{20}
73		$P4_3$						A_{19}
74	V_{CC2}							
75		$P4_2$						A_{18}
76	V_{SS}							
77		$P4_1$						A_{17}
78		$P4_0$						A_{16}
79		$P3_7$						A_{15}(/D_{15})
80		$P3_6$						A_{14}(/D_{14})
81		$P3_5$						A_{13}(/D_{13})
82		$P3_4$						A_{12}(/D_{12})
83		$P3_3$						A_{11}(/D_{11})
84		$P3_2$						A_{10}(/D_{10})
85		$P3_1$						A_9(/D_9)
86		$P12_4$						
87		$P12_3$						
88		$P12_2$						
89		$P12_1$						
90		$P12_0$						
91	V_{CC2}							
92		$P3_0$						A_8(/D_8)
93	V_{SS}							
94		$P2_7$					$AN2_7$	A_7(/D_7)
95		$P2_6$					$AN2_6$	A_6(/D_6)
96		$P2_5$					$AN2_5$	A_5(/D_5)

NOTES:

1. Bus control pins in M32C/84T cannot be used.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin[1]
97		$P2_4$					$AN2_4$	A_4(/D_4)
98		$P2_3$					$AN2_3$	A_3(/D_3)
99		$P2_2$					$AN2_2$	A_2(/D_2)
100		$P2_1$					$AN2_1$	A_1(/D_1)
101		$P2_0$					$AN2_0$	A_0(/D_0)
102		$P1_7$	$\overline{INT5}$					D_{15}
103		$P1_6$	$\overline{INT4}$					D_{14}
104		$P1_5$	$\overline{INT3}$					D_{13}
105		$P1_4$						D_{12}
106		$P1_3$						D_{11}
107		$P1_2$						D_{10}
108		$P1_1$						D_9
109		$P1_0$						D_8
110		$P0_7$					$AN0_7$	D_7
111		$P0_6$					$AN0_6$	D_6
112		$P0_5$					$AN0_5$	D_5
113		$P0_4$					$AN0_4$	D_4
114		$P11_4$						
115		$P11_3$				$INPC1_3$/$OUTC1_3$		
116		$P11_2$				$INPC1_2$/$OUTC1_2$/ISRxD1/$BE1_{IN}$		
117		$P11_1$				$INPC1_1$/$OUTC1_1$/ISCLK1		
118		$P11_0$				$INPC1_0$/$OUTC1_0$/ISTxD1/$BE1_{OUT}$		
119		$P0_3$					$AN0_3$	D_3
120		$P0_2$					$AN0_2$	D_2
121		$P0_1$					$AN0_1$	D_1
122		$P0_0$					$AN0_0$	D_0
123		$P15_7$					$AN15_7$	
124		$P15_6$					$AN15_6$	
125		$P15_5$					$AN15_5$	
126		$P15_4$					$AN15_4$	
127		$P15_3$					$AN15_3$	
128		$P15_2$				ISRxD0	$AN15_2$	
129		$P15_1$				ISCLK0	$AN15_1$	
130	V_{SS}							
131		$P15_0$				ISTxD0	$AN15_0$	
132	V_{CC1}							
133		$P10_7$	$\overline{KI_3}$				AN_7	
134		$P10_6$	$\overline{KI_2}$				AN_6	
135		$P10_5$	$\overline{KI_1}$				AN_5	
136		$P10_4$	$\overline{KI_0}$				AN_4	
137		$P10_3$					AN_3	
138		$P10_2$					AN_2	
139		$P10_1$					AN_1	
140	AV_{SS}							
141		$P10_0$					AN_0	
142	V_{REF}							
143	AV_{CC}							
144		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

NOTES:

1. Bus control pins in M32C/84T cannot be used.

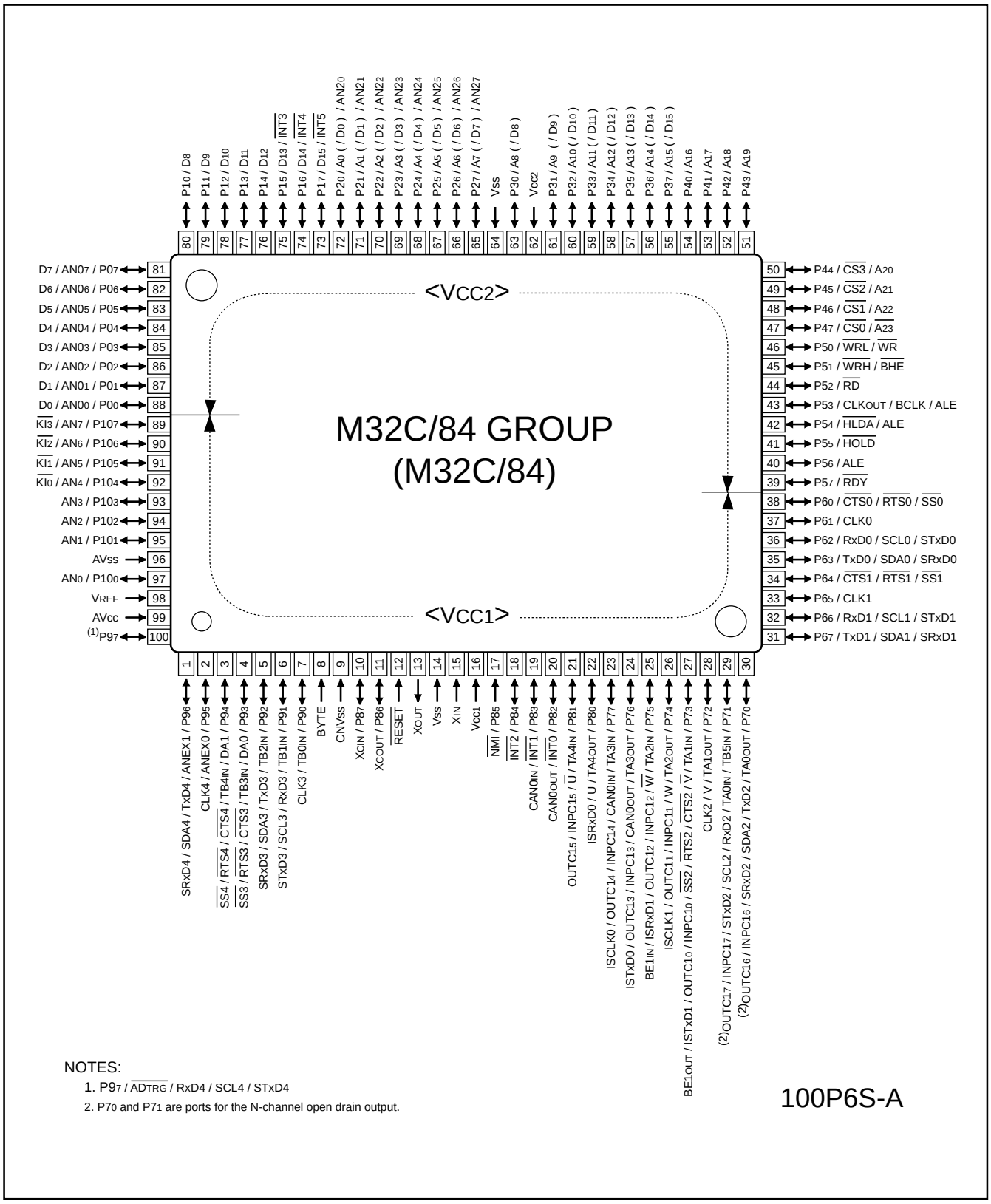
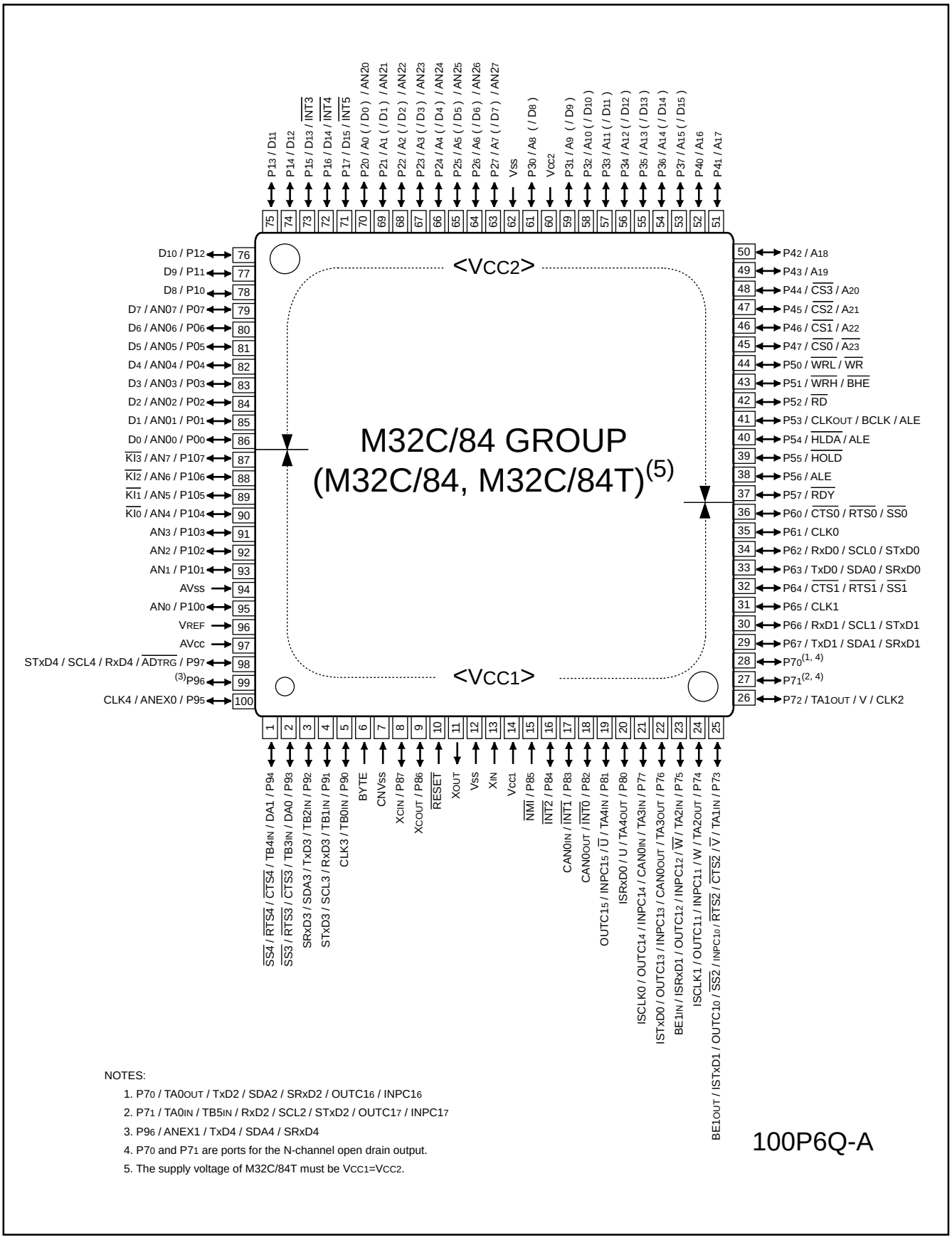


Figure 1.4 Pin Assignment for 100-Pin Package



NOTES:

1. P70 / TA0OUT / TxD2 / SDA2 / SRxD2 / OUTC16 / INPC16
2. P71 / TA0IN / TB5IN / RxD2 / SCL2 / STxD2 / OUTC17 / INPC17
3. P96 / ANEX1 / TxD4 / SDA4 / SRxD4
4. P70 and P71 are ports for the N-channel open drain output.
5. The supply voltage of M32C/84T must be VCC1=VCC2.

Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No. FP	Package Pin No. GP	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
1	99		$P9_6$			TxD4/SDA4/SRxD4		ANEX1	
2	100		$P9_5$			CLK4		ANEX0	
3	1		$P9_4$		$TB4_{IN}$	$\overline{CTS4}/\overline{RTS4}/\overline{SS4}$		DA1	
4	2		$P9_3$		$TB3_{IN}$	$\overline{CTS3}/\overline{RTS3}/\overline{SS3}$		DA0	
5	3		$P9_2$		$TB2_{IN}$	TxD3/SDA3/SRxD3			
6	4		$P9_1$		$TB1_{IN}$	RxD3/SCL3/STxD3			
7	5		$P9_0$		$TB0_{IN}$	CLK3			
8	6	BYTE							
9	7	CNV_{SS}							
10	8	X_{CIN}	$P8_7$						
11	9	X_{COUT}	$P8_6$						
12	10	$\overline{RESET}$							
13	11	X_{OUT}							
14	12	V_{SS}							
15	13	X_{IN}							
16	14	V_{CC1}							
17	15		$P8_5$	$\overline{NMI}$					
18	16		$P8_4$	$\overline{INT2}$					
19	17		$P8_3$	$\overline{INT1}$		$CAN0_{IN}$			
20	18		$P8_2$	$\overline{INT0}$		$CAN0_{OUT}$			
21	19		$P8_1$		$TA4_{IN}/\overline{U}$		$INPC1_5/OUTC1_5$		
22	20		$P8_0$		$TA4_{OUT}/U$		ISRxD0		
23	21		$P7_7$		$TA3_{IN}$	$CAN0_{IN}$	$INPC1_4/OUTC1_4$/ISCLK0		
24	22		$P7_6$		$TA3_{OUT}$	$CAN0_{OUT}$	$INPC1_3/OUTC1_3$/ISTxD0		
25	23		$P7_5$		$TA2_{IN}/\overline{W}$		$INPC1_2/OUTC1_2$/ISRxD1/$BE1_{IN}$		
26	24		$P7_4$		$TA2_{OUT}/W$		$INPC1_1/OUTC1_1$/ISCLK1		
27	25		$P7_3$		$TA1_{IN}/\overline{V}$	$\overline{CTS2}/\overline{RTS2}/\overline{SS2}$	$INPC1_0/OUTC1_0$/ISTxD1/$BE1_{OUT}$		
28	26		$P7_2$		$TA1_{OUT}/V$	CLK2			
29	27		$P7_1$		$TB5_{IN}/TA0_{IN}$	RxD2/SCL2/STxD2	$INPC1_7/OUTC1_7$		
30	28		$P7_0$		$TA0_{OUT}$	TxD2/SDA2/SRxD2	$INPC1_6/OUTC1_6$		
31	29		$P6_7$			TxD1/SDA1/SRxD1			
32	30		$P6_6$			RxD1/SCL1/STxD1			
33	31		$P6_5$			CLK1			
34	32		$P6_4$			$\overline{CTS1}/\overline{RTS1}/\overline{SS1}$			
35	33		$P6_3$			TxD0/SDA0/SRxD0			
36	34		$P6_2$			RxD0/SCL0/STxD0			
37	35		$P6_1$			CLK0			
38	36		$P6_0$			$\overline{CTS0}/\overline{RTS0}/\overline{SS0}$			
39	37		$P5_7$						$\overline{RDY}$
40	38		$P5_6$						ALE
41	39		$P5_5$						$\overline{HOLD}$
42	40		$P5_4$						$\overline{HLDA}$/ALE
43	41		$P5_3$						CLK_{OUT}/BCLK/ALE
44	42		$P5_2$						$\overline{RD}$
45	43		$P5_1$						$\overline{WRH}/\overline{BHE}$
46	44		$P5_0$						$\overline{WRL}/\overline{WR}$
47	45		$P4_7$						$\overline{CS0}/A_{23}$
48	46		$P4_6$						$\overline{CS1}/A_{22}$
49	47		$P4_5$						$\overline{CS2}/A_{21}$
50	48		$P4_4$						$\overline{CS3}/A_{20}$

NOTES:
1. Bus control pins in M32C/84T cannot be used.

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
51	49		$P4_3$						A_{19}
52	50		$P4_2$						A_{18}
53	51		$P4_1$						A_{17}
54	52		$P4_0$						A_{16}
55	53		$P3_7$						A_{15}(/D_{15})
56	54		$P3_6$						A_{14}(/D_{14})
57	55		$P3_5$						A_{13}(/D_{13})
58	56		$P3_4$						A_{12}(/D_{12})
59	57		$P3_3$						A_{11}(/D_{11})
60	58		$P3_2$						A_{10}(/D_{10})
61	59		$P3_1$						A_9(/D_9)
62	60	V_{CC2}							
63	61		$P3_0$						A_8(/D_8)
64	62	V_{SS}							
65	63		$P2_7$					$AN2_7$	A_7(/D_7)
66	64		$P2_6$					$AN2_6$	A_6(/D_6)
67	65		$P2_5$					$AN2_5$	A_5(/D_5)
68	66		$P2_4$					$AN2_4$	A_4(/D_4)
69	67		$P2_3$					$AN2_3$	A_3(/D_3)
70	68		$P2_2$					$AN2_2$	A_2(/D_2)
71	69		$P2_1$					$AN2_1$	A_1(/D_1)
72	70		$P2_0$					$AN2_0$	A_0(/D_0)
73	71		$P1_7$	$\overline{INT5}$					D_{15}
74	72		$P1_6$	$\overline{INT4}$					D_{14}
75	73		$P1_5$	$\overline{INT3}$					D_{13}
76	74		$P1_4$						D_{12}
77	75		$P1_3$						D_{11}
78	76		$P1_2$						D_{10}
79	77		$P1_1$						D_9
80	78		$P1_0$						D_8
81	79		$P0_7$					$AN0_7$	D_7
82	80		$P0_6$					$AN0_6$	D_6
83	81		$P0_5$					$AN0_5$	D_5
84	82		$P0_4$					$AN0_4$	D_4
85	83		$P0_3$					$AN0_3$	D_3
86	84		$P0_2$					$AN0_2$	D_2
87	85		$P0_1$					$AN0_1$	D_1
88	86		$P0_0$					$AN0_0$	D_0
89	87		$P10_7$	$\overline{KI_3}$				AN_7	
90	88		$P10_6$	$\overline{KI_2}$				AN_6	
91	89		$P10_5$	$\overline{KI_1}$				AN_5	
92	90		$P10_4$	$\overline{KI_0}$				AN_4	
93	91		$P10_3$					AN_3	
94	92		$P10_2$					AN_2	
95	93		$P10_1$					AN_1	
96	94	AV_{SS}							
97	95		$P10_0$					AN_0	
98	96	V_{REF}							
99	97	AV_{CC}							
100	98		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

NOTES:

1. Bus control pins in M32C/84T cannot be used.

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
Power Supply	V_{CC1}, V_{CC2} V_{SS}	I I	–	Apply 3.0 to 5.5V to both V_{CC1} and V_{CC2} pins. Apply 0V to the V_{SS} pin. $V_{CC1} \geq V_{CC2}$(1, 2)
Analog Power Supply	AV_{CC} AV_{SS}	I	V_{CC1}	Supplies power to the A/D converter and D/A converter. Connect the AV_{CC} pin to V_{CC1} and the AV_{SS} pin to V_{SS}.
Reset Input	$\overline{RESET}$	I	V_{CC1}	The microcomputer is in a reset state when "L" is applied to the $\overline{RESET}$ pin
CNV_{SS}	CNV_{SS}	I	V_{CC1}	Switches processor mode. Connect the CNV_{SS} pin to V_{SS} to start up in single-chip mode or to V_{CC1} to start up in microprocessor mode
Input to Switch External Data Bus Width(3)	BYTE	I	V_{CC1}	Switches data bus width in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when it is held "H". Set to either. Connect the BYTE pin to V_{SS} to use the microcomputer in single-chip mode
Bus Control Pins(3)	D_0 to D_7	I/O	V_{CC2}	Inputs and outputs data (D_0 to D_7) while accessing an external memory space with the separate bus
	D_8 to D_{15}	I/O	V_{CC2}	Inputs and outputs data (D_8 to D_{15}) while accessing an external memory space with 16-bit separate bus
	A_0 to A_{22}	O	V_{CC2}	Outputs address bits A_0 to A_{22}
	$\overline{A_{23}}$	O	V_{CC2}	Outputs inversed address bit A_{23}
	A_0/D_0 to A_7/D_7	I/O	V_{CC2}	Inputs and outputs data (D_0 to D_7) and outputs 8 low-order address bits (A_0 to A_7) by time-sharing while accessing an external memory space with the multiplexed bus
	A_8/D_8 to A_{15}/D_{15}	I/O	V_{CC2}	Inputs and outputs data (D_8 to D_{15}) and outputs 8 middle-order address bits (A_8 to A_{15}) by time-sharing while accessing an external memory space with 16-bit multiplexed bus
	$\overline{CS0}$ to $\overline{CS3}$	O	V_{CC2}	Outputs $\overline{CS0}$ to $\overline{CS3}$ that are chip-select signals specifying an external space
	$\overline{WRL}$ / $\overline{WR}$ $\overline{WRH}$ / $\overline{BHE}$ $\overline{RD}$	O	V_{CC2}	Outputs $\overline{WRL}$, $\overline{WRH}$, ($\overline{WR}$, $\overline{BHE}$) and $\overline{RD}$ signals. $\overline{WRL}$ and $\overline{WRH}$ can be switched with $\overline{WR}$ and $\overline{BHE}$ by program. ■ $\overline{WRL}$, $\overline{WRH}$ and $\overline{RD}$ selected: If external data bus is 16 bits wide, data is written to an even address in external memory space when $\overline{WRL}$ is held "L". Data is written to an odd address when $\overline{WRH}$ is held "L". Data is read when $\overline{RD}$ is held "L". ■ $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ selected: Data is written to external memory space when $\overline{WR}$ is held "L". Data in an external memory space is read when $\overline{RD}$ is held "L". An odd address is accessed when $\overline{BHE}$ is held "L". Select $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ for external 8-bit data bus.
	ALE	O	V_{CC2}	ALE is a signal latching the address.
	$\overline{HOLD}$	I	V_{CC2}	The microcomputer is placed in a hold state while the $\overline{HOLD}$ pin is held "L".
	$\overline{HLDA}$	O	V_{CC2}	Outputs an "L" signal while the microcomputer is placed in a hold state.
	$\overline{RDY}$	I	V_{CC2}	Bus is placed in a wait state while the $\overline{RDY}$ pin is held "L".

I : Input O : Output I/O : Input and output

NOTES:
1. V_{CC1} is hereinafter referred to as V_{CC} unless otherwise noted.
2. Apply 4.2 to 5.5V to the V_{CC1} and V_{CC2} pins when using M32C/84T. $V_{CC1}=V_{CC2}$.
3. Bus cotrol pins in M32C/84T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
Main Clock Input	X_{IN}	I	V_{CC1}	I/O pins for the main clock oscillation circuit.Connect a crystal oscillator between X_{IN} and X_{OUT}. To apply externally-generated clock, apply it to X_{IN} and leave X_{OUT} open.
Main Clock Output	X_{OUT}	O	V_{CC1}	
Sub Clock Input	X_{CIN}	I	V_{CC1}	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between X_{CIN} and X_{COUT}. To apply externally-generated clock, apply it to X_{CIN} and leave X_{COUT} open.
Sub Clock Output	X_{COUT}	O	V_{CC1}	
BCLK Output(1)	BCLK	O	V_{CC2}	Outputs BCLK signal
Clock Output	CLK_{OUT}	O	V_{CC2}	Outputs the clock having the same frequency as f_C, f_8 or f_{32}
$\overline{INT}$ Interrupt Input	$\overline{INT0}$ to $\overline{INT2}$	I	V_{CC1}	Input pins for the $\overline{INT}$ interrupt
	$\overline{INT3}$ to $\overline{INT5}$	I	V_{CC2}	
$\overline{NMI}$ Interrupt Input	$\overline{NMI}$	I	V_{CC1}	Input pin for the $\overline{NMI}$ interrupt
Key Input Interrupt	$\overline{KI0}$ to $\overline{KI3}$	I	V_{CC1}	Input pins for the key input interrupt
Timer A	$TA0_{OUT}$ to $TA4_{OUT}$	I/O	V_{CC1}	I/O pins for timer A0 to A4 ($TA0_{OUT}$ is a pin for the N-channel open drain output.)
	$TA0_{IN}$ to $TA4_{IN}$	I	V_{CC1}	Input pins for timer A0 to A4
Timer B	$TB0_{IN}$ to $TB5_{IN}$	I	V_{CC1}	Input pins for timer B0 to B5
Three-phase Motor Control Timer Output	U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$	O	V_{CC1}	Output pins for the three-phase motor control timer
Serial I/O	$\overline{CTS0}$ to $\overline{CTS4}$	I	V_{CC1}	Iutput pins for data transmission control
	$\overline{RTS0}$ to $\overline{RTS4}$	O	V_{CC1}	Output pins for data reception control
	CLK0 to CLK4	I/O	V_{CC1}	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	V_{CC1}	Inputs serial data
	TxD0 to TxD4	O	V_{CC1}	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I^2C Mode	SDA0 to SDA4	I/O	V_{CC1}	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4	I/O	V_{CC1}	Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)
Serial I/O Special Function	STxD0 to STxD4	O	V_{CC1}	Outputs serial data when slave mode is selected (STxD2 is a pin for the N-channel open drain output.)
	SRxD0 to SRxD4	I	V_{CC1}	Inputs serial data when slave mode is selected
	$\overline{SS0}$ to $\overline{SS4}$	I	V_{CC1}	Input pins to control serial I/O special function

I : Input O : Output I/O : Input and output

NOTES:

1. Bus control pins in M32C/84T cannot be used.
2. Apply 4.2 to 5.5V to the V_{CC1} and V_{CC2} pins when using M32C/84T. $V_{CC1} = V_{CC2}$.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
Reference Voltage Input	V_{REF}	I	-	Supplies reference voltage to the A/D converter and D/A converter
A/D Converter	AN_0 to AN_7 $AN0_0$ to $AN0_7$ $AN2_0$ to $AN2_7$	I	V_{CC1}	Analog input pins for the A/D converter
	$\overline{ADTRG}$	I	V_{CC1}	Input pin for an external A/D trigger
	ANEX0	I/O	V_{CC1}	Extended analog input pin for the A/D converter and output pin in external op-amp connection mode
	ANEX1	I	V_{CC1}	Extended analog input pin for the A/D converter
D/A Converter	DA0, DA1	O	V_{CC1}	Output pin for the D/A converter
Intelligent I/O	$INPC1_0$ to $INPC1_3$	I	V_{CC1}/V_{CC2}(1)	Input pins for the time measurement function
	$INPC1_4$ to $INPC1_7$	I	V_{CC1}	
	$OUTC1_0$ to $OUTC1_3$	O	V_{CC1}/V_{CC2}(1)	Output pins for the waveform generating function ($OUTC1_6$ and $OUTC1_7$ assgined to $P7_0$ and $P7_1$ are pins for the N-channel open drain output.)
	$OUTC1_4$ to $OUTC1_7$	O	V_{CC1}	
	ISCLK0	I/O	V_{CC1}	Inputs and outputs the clock for the intellignet I/O communication function
	ISCLK1	I/O	V_{CC1}/V_{CC2}(1)	
	ISRXD0	I	V_{CC1}	Inputs data for the intellignet I/O communication function
	ISRXD1	I	V_{CC1}/V_{CC2}(1)	
	ISTXD0	O	V_{CC1}	Outputs data for the intellignet I/O communication function
	ISTXD1	O	V_{CC1}/V_{CC2}(1)	
	$BE1_{IN}$	I	V_{CC1}/V_{CC2}(1)	Inputs data for the intellignet I/O communication function
	$BE1_{OUT}$	O	V_{CC1}/V_{CC2}(1)	Outputs data for the intellignet I/O communication function
CAN	$CAN0_{IN}$	I	V_{CC1}	Input pin for the CAN communication function
	$CAN0_{OUT}$	O	V_{CC1}	Output pin for the CAN communication function
I/O Ports	$P0_0$ to $P0_7$ $P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$ $P4_0$ to $P4_7$ $P5_0$ to $P5_7$	I/O	V_{CC2}	8-bit I/O ports in CMOS. Each port can be programmed to input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	$P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P9_0$ to $P9_7$ $P10_0$ to $P10_7$	I/O	V_{CC1}	8-bit I/O ports having equivalent functions to P0 ($P7_0$ and $P7_1$ are ports for the N-channel open drain output.)
	$P8_0$ to $P8_4$ $P8_6$, $P8_7$	I/O	V_{CC1}	I/O ports having equivalent functions to P0
Input Port	$P8_5$	I	V_{CC1}	Shares a pin with $\overline{NMI}$. $\overline{NMI}$ input state can be got by reading $P8_5$

I : Input O : Output I/O : Input and output

NOTES:

1. V_{CC2} is not available in the 100-pin package. V_{CC1} only available.
2. Apply 4.2 to 5.5V to the V_{CC1} and V_{CC2} pins when using M32C/84T. $V_{CC1} = V_{CC2}$.

Table 1.6 Pin Description (144-Pin Package only) (Continued)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
A/D Converter	$AN15_0$ to $AN15_7$	I	V_{CC1}	Analog input pins for the A/D converter
I/O Ports	$P11_0$ to $P11_4$ $P12_0$ to $P12_7$ $P13_0$ to $P13_7$	I/O	V_{CC2}	8-bit I/O ports having equivalent functions to P0
	$P14_0$ to $P14_6$ $P15_0$ to $P15_7$	I/O	V_{CC1}	8-bit I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

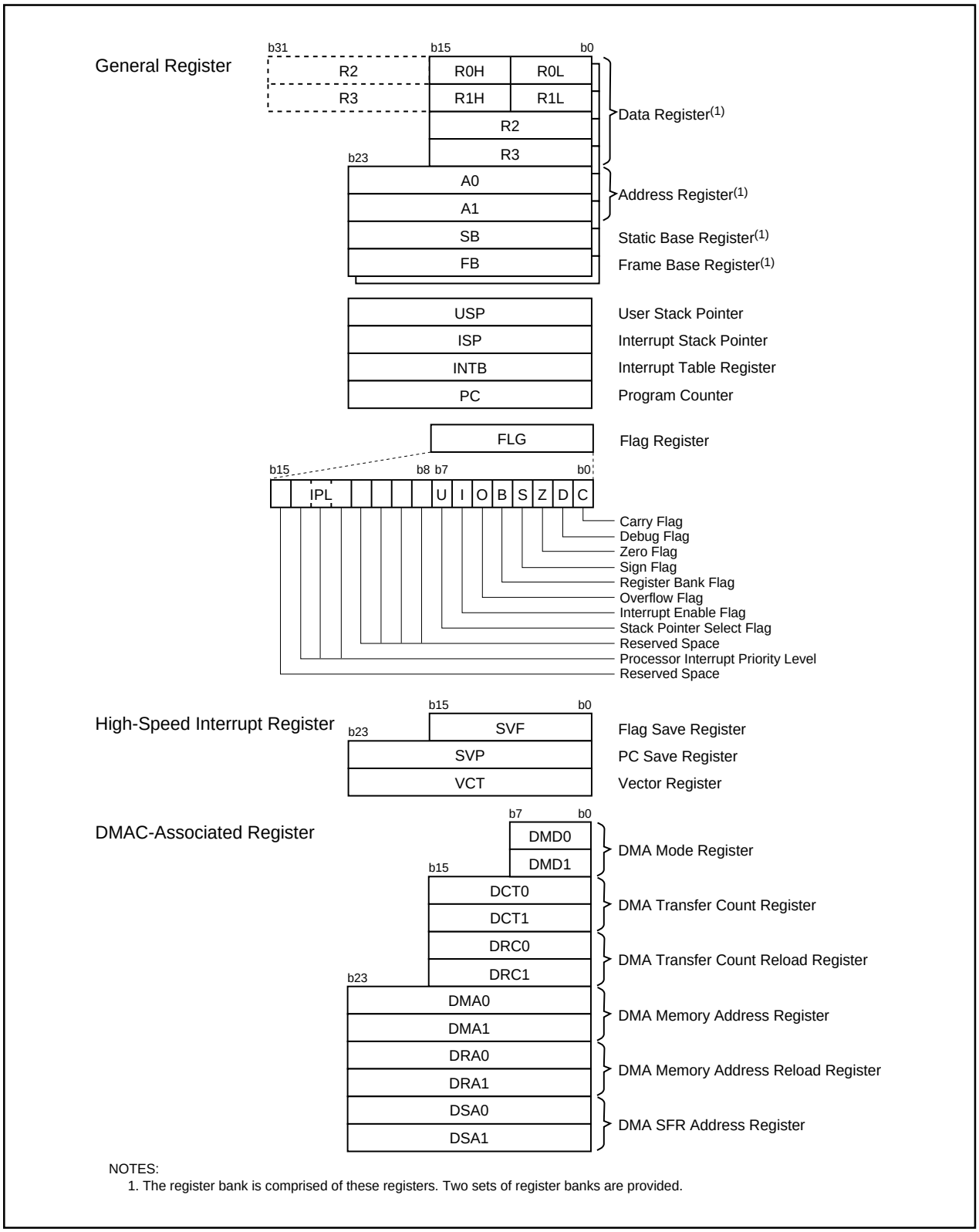
NOTES:

1. Apply 4.2 to 5.5V to the V_{CC1} and V_{CC2} pins when using M32C/84T. $V_{CC1} = V_{CC2}$.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

The register bank is comprised of 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.



NOTES:
1. The register bank is comprised of these registers. Two sets of register banks are provided.

Figure 2.1 CPU Register

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H/R1H) and low-order bits (R0L/R1L) to be used separately as 8-bit data registers.

R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of the next instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of a relocatable vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to **2.1.8 Flag Register (FLG)** for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic calculation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic calculation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
Interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".
The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When reading, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows:
- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows:
- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/84 group (M32C/84, M32C/84T).

The M32C/84 group (M32C/84, M32C/84T) provides 16-Mbyte address space from addresses 000000_{16} to $FFFFFF_{16}$.

The internal ROM is allocated lower addresses beginning with address $FFFFFF_{16}$. For example, a 64-Kbyte internal ROM is allocated in addresses $FF0000_{16}$ to $FFFFFF_{16}$.

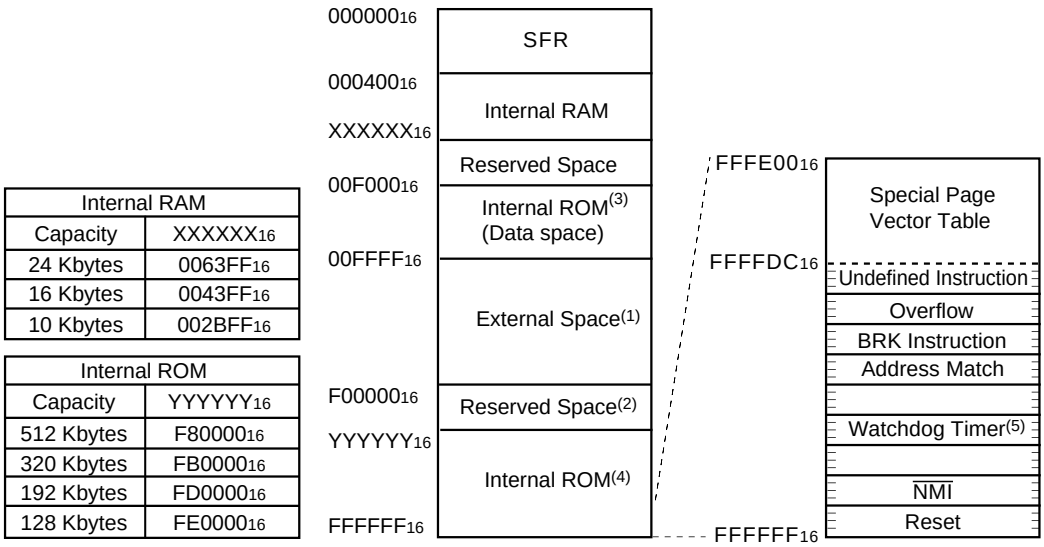
The fixed interrupt vectors are allocated addresses $FFFFDC_{16}$ to $FFFFFF_{16}$. It stores the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 000400_{16}. For example, a 10-Kbyte internal RAM is allocated addresses 000400_{16} to $002BFF_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowleged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D conversion, serial I/O, and timers, is allocated addresses 000000_{16} to $0003FF_{16}$. All blank spaces within SFR are reserved space and cannot be accessed by users.

The special page vectors are allocated addresses $FFFE00_{16}$ to $FFFFDB_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **Software Manual** for details.

In memory expansion mode and microprocessor mode, some spaces are reserved and cannot be accessed by users.



Internal RAM	
Capacity	XXXXXX_{16}
24 Kbytes	$0063FF_{16}$
16 Kbytes	$0043FF_{16}$
10 Kbytes	$002BFF_{16}$

Internal ROM	
Capacity	$YYYYYY_{16}$
512 Kbytes	$F80000_{16}$
320 Kbytes	$FB0000_{16}$
192 Kbytes	$FD0000_{16}$
128 Kbytes	$FE0000_{16}$

NOTES:
1. In memory expansion and microprocessor modes.
2. In memory expansion mode.
   This space becomes an external space in microprocessor mode
3. Additional 4-Kbyte space is provided in flash memory version for storing data.
4. This space can be used in single-chip and memory expansion modes.
   This space becomes an external space in microprocessor mode.
5. Watchdog timer interrupts, oscillation stop detect interrupts, and voltage down detect interrupts share vectors.

Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
0000_{16}			
0001_{16}			
0002_{16}			
0003_{16}			
0004_{16}	Processor Mode Register 0(1)	PM0	$1000\ 0000_2$(CNVss pin ="L") $0000\ 0011_2$(CNVss pin ="H")
0005_{16}	Processor Mode Register 1	PM1	00_{16}
0006_{16}	System Clock Control Register 0	CM0	$0000\ 1000_2$
0007_{16}	System Clock Control Register 1	CM1	$0010\ 0000_2$
0008_{16}			
0009_{16}	Address Match Interrupt Enable Register	AIER	00_{16}
$000A_{16}$	Protect Register	PRCR	$XXXX\ 0000_2$
$000B_{16}$	External Data Bus Width Control Register(2)	DS	$XXXX\ 1000_2$(BYTE pin ="L") $XXXX\ 0000_2$(BYTE pin ="H")
$000C_{16}$	Main Clock Division Register	MCD	$XXX0\ 1000_2$
$000D_{16}$	Oscillation Stop Detection Register	CM2	00_{16}
$000E_{16}$	Watchdog Timer Start Register	WDTS	XX_{16}
$000F_{16}$	Watchdog Timer Control Register	WDC	$000X\ XXXX_2$
0010_{16} 0011_{16} 0012_{16}	Address Match Interrupt Register 0	RMAD0	000000_{16}
0013_{16}	Processor Mode Register 2	PM2	00_{16}
0014_{16} 0015_{16} 0016_{16}	Address Match Interrupt Register 1	RMAD1	000000_{16}
0017_{16}	Voltage Detection Register 2(2)	VCR2	00_{16}
0018_{16} 0019_{16} $001A_{16}$	Address Match Interrupt Register 2	RMAD2	000000_{16}
$001B_{16}$	Voltage Detection Register 1(2)	VCR1	$0000\ 1000_2$
$001C_{16}$ $001D_{16}$ $001E_{16}$	Address Match Interrupt Register 3	RMAD3	000000_{16}
$001F_{16}$			
0020_{16}			
0021_{16}			
0022_{16}			
0023_{16}			
0024_{16}			
0025_{16}			
0026_{16}	PLL Control Register 0	PLC0	$0001\ X010_2$
0027_{16}	PLL Control Register 1	PLC1	$000X\ 0000_2$
0028_{16} 0029_{16} $002A_{16}$	Address Match Interrupt Register 4	RMAD4	000000_{16}
$002B_{16}$			
$002C_{16}$ $002D_{16}$ $002E_{16}$	Address Match Interrupt Register 5	RMAD5	000000_{16}
$002F_{16}$	Voltage Down Detection Interrupt Register(2)	D4INT	00_{16}

X: Indeterminate
Blank spaces are reserved. No access is allowed.
NOTES:
1. The PM00 and PM01 bits in the PM1 register maintain values set before reset even if software reset or watchdog timer reset is performed.
2. These registers in M32C/84T cannot be used.

Address	Register	Symbol	Value after RESET
0030_{16}			
0031_{16}			
0032_{16}			
0033_{16}			
0034_{16}			
0035_{16}			
0036_{16}			
0037_{16}			
0038_{16} 0039_{16} $003A_{16}$	Address Match Interrupt Register 6	RMAD6	000000_{16}
$003B_{16}$			
$003C_{16}$ $003D_{16}$ $003E_{16}$	Address Match Interrupt Register 7	RMAD7	000000_{16}
$003F_{16}$			
0040_{16}			
0041_{16}			
0042_{16}			
0043_{16}			
0044_{16}			
0045_{16}			
0046_{16}			
0047_{16}			
0048_{16}	External Space Wait Control Register 0(1)	EWCR0	$X0X0\ 0011_2$
0049_{16}	External Space Wait Control Register 1(1)	EWCR1	$X0X0\ 0011_2$
$004A_{16}$	External Space Wait Control Register 2(1)	EWCR2	$X0X0\ 0011_2$
$004B_{16}$	External Space Wait Control Register 3(1)	EWCR3	$X0X0\ 0011_2$
$004C_{16}$			
$004D_{16}$			
$004E_{16}$			
$004F_{16}$			
0050_{16}			
0051_{16}			
0052_{16}			
0053_{16}			
0054_{16}			
0055_{16}	Flash Memory Control Register 1	FMR1	$0000\ 0101_2$
0056_{16}			
0057_{16}	Flash Memory Control Register 0	FMR0	$0000\ 0001_2$(Flash memory version) $XXXX\ XXX0_2$(Masked ROM version)
0058_{16}			
0059_{16}			
$005A_{16}$			
$005B_{16}$			
$005C_{16}$			
$005D_{16}$			
$005E_{16}$			
$005F_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. These registers in M32C/84T cannot be used.

Address	Register	Symbol	Value after RESET
0060$_{16}$			
0061$_{16}$			
0062$_{16}$			
0063$_{16}$			
0064$_{16}$			
0065$_{16}$			
0066$_{16}$			
0067$_{16}$			
0068$_{16}$	DMA0 Interrupt Control Register	DM0IC	XXXX X000$_{2}$
0069$_{16}$	Timer B5 Interrupt Control Register	TB5IC	XXXX X000$_{2}$
006A$_{16}$	DMA2 Interrupt Control Register	DM2IC	XXXX X000$_{2}$
006B$_{16}$	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X000$_{2}$
006C$_{16}$	Timer A0 Interrupt Control Register	TA0IC	XXXX X000$_{2}$
006D$_{16}$	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X000$_{2}$
006E$_{16}$	Timer A2 Interrupt Control Register	TA2IC	XXXX X000$_{2}$
006F$_{16}$	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X000$_{2}$
0070$_{16}$	Timer A4 Interrupt Control Register	TA4IC	XXXX X000$_{2}$
0071$_{16}$	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000$_{2}$
0072$_{16}$	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000$_{2}$
0073$_{16}$	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X000$_{2}$
0074$_{16}$	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000$_{2}$
0075$_{16}$	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X000$_{2}$
0076$_{16}$	Timer B1 Interrupt Control Register	TB1IC	XXXX X000$_{2}$
0077$_{16}$	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X000$_{2}$
0078$_{16}$	Timer B3 Interrupt Control Register	TB3IC	XXXX X000$_{2}$
0079$_{16}$	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000$_{2}$
007A$_{16}$	INT5 Interrupt Control Register	INT5IC	XX00 X000$_{2}$
007B$_{16}$			
007C$_{16}$	INT3 Interrupt Control Register	INT3IC	XX00 X000$_{2}$
007D$_{16}$	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X000$_{2}$
007E$_{16}$	INT1 Interrupt Control Register	INT1IC	XX00 X000$_{2}$
007F$_{16}$	Intelligent I/O Interrupt Control Register 10/ CAN Interrupt 1 Control Register	IIO10IC CAN1IC	XXXX X000$_{2}$
0080$_{16}$			
0081$_{16}$	CAN Interrupt 2 Control Register	CAN2IC	XXXX X000$_{2}$
0082$_{16}$			
0083$_{16}$			
0084$_{16}$			
0085$_{16}$			
0086$_{16}$			
0087$_{16}$			
0088$_{16}$	DMA1 Interrupt Control Register	DM1IC	XXXX X000$_{2}$
0089$_{16}$	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X000$_{2}$
008A$_{16}$	DMA3 Interrupt Control Register	DM3IC	XXXX X000$_{2}$
008B$_{16}$	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X000$_{2}$
008C$_{16}$	Timer A1 Interrupt Control Register	TA1IC	XXXX X000$_{2}$
008D$_{16}$	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X000$_{2}$
008E$_{16}$	Timer A3 Interrupt Control Register	TA3IC	XXXX X000$_{2}$
008F$_{16}$	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X000$_{2}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0090_{16}	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX $X000_2$
0091_{16}	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX $X000_2$
0092_{16}	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX $X000_2$
0093_{16}	Key Input Interrupt Control Register	KUPIC	XXXX $X000_2$
0094_{16}	Timer B0 Interrupt Control Register	TB0IC	XXXX $X000_2$
0095_{16}	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX $X000_2$
0096_{16}	Timer B2 Interrupt Control Register	TB2IC	XXXX $X000_2$
0097_{16}	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX $X000_2$
0098_{16}	Timer B4 Interrupt Control Register	TB4IC	XXXX $X000_2$
0099_{16}			
$009A_{16}$	INT4 Interrupt Control Register	INT4IC	XX00 $X000_2$
$009B_{16}$			
$009C_{16}$	INT2 Interrupt Control Register	INT2IC	XX00 $X000_2$
$009D_{16}$	Intelligent I/O Interrupt Control Register 9/ CAN Interrupt 0 Control Register	IIO9IC CAN0IC	XXXX $X000_2$
$009E_{16}$	INT0 Interrupt Control Register	INT0IC	XX00 $X000_2$
$009F_{16}$	Exit Priority Control Register	RLVL	XXXX 0000_2
$00A0_{16}$	Interrupt Request Register 0	IIO0IR	0000 $000X_2$
$00A1_{16}$	Interrupt Request Register 1	IIO1IR	0000 $000X_2$
$00A2_{16}$	Interrupt Request Register 2	IIO2IR	0000 $000X_2$
$00A3_{16}$	Interrupt Request Register 3	IIO3IR	0000 $000X_2$
$00A4_{16}$	Interrupt Request Register 4	IIO4IR	0000 $000X_2$
$00A5_{16}$			
$00A6_{16}$			
$00A7_{16}$			
$00A8_{16}$	Interrupt Request Register 8	IIO8IR	0000 $000X_2$
$00A9_{16}$	Interrupt Request Register 9	IIO9IR	0000 $000X_2$
$00AA_{16}$	Interrupt Request Register 10	IIO10IR	0000 $000X_2$
$00AB_{16}$	Interrupt Request Register 11	IIO11IR	0000 $000X_2$
$00AC_{16}$			
$00AD_{16}$			
$00AE_{16}$			
$00AF_{16}$			
$00B0_{16}$	Interrupt Enable Register 0	IIO0IE	00_{16}
$00B1_{16}$	Interrupt Enable Register 1	IIO1IE	00_{16}
$00B2_{16}$	Interrupt Enable Register 2	IIO2IE	00_{16}
$00B3_{16}$	Interrupt Enable Register 3	IIO3IE	00_{16}
$00B4_{16}$	Interrupt Enable Register 4	IIO4IE	00_{16}
$00B5_{16}$			
$00B6_{16}$			
$00B7_{16}$			
$00B8_{16}$	Interrupt Enable Register 8	IIO8IE	00_{16}
$00B9_{16}$	Interrupt Enable Register 9	IIO9IE	00_{16}
$00BA_{16}$	Interrupt Enable Register 10	IIO10IE	00_{16}
$00BB_{16}$	Interrupt Enable Register 11	IIO11IE	00_{16}
$00BC_{16}$			
$00BD_{16}$			
$00BE_{16}$			
$00BF_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
$00C0_{16}$			
$00C1_{16}$			
$00C2_{16}$			
$00C3_{16}$			
$00C4_{16}$			
$00C5_{16}$			
$00C6_{16}$			
$00C7_{16}$			
$00C8_{16}$			
$00C9_{16}$			
$00CA_{16}$			
$00CB_{16}$			
$00CC_{16}$			
$00CD_{16}$			
$00CE_{16}$			
$00CF_{16}$			
$00D0_{16}$			
$00D1_{16}$			
$00D2_{16}$			
$00D3_{16}$			
$00D4_{16}$			
$00D5_{16}$			
$00D6_{16}$			
$00D7_{16}$			
$00D8_{16}$			
$00D9_{16}$			
$00DA_{16}$			
$00DB_{16}$			
$00DC_{16}$			
$00DD_{16}$			
$00DE_{16}$			
$00DF_{16}$			
$00E0_{16}$			
$00E1_{16}$			
$00E2_{16}$			
$00E3_{16}$			
$00E4_{16}$			
$00E5_{16}$			
$00E6_{16}$			
$00E7_{16}$			
$00E8_{16}$ $00E9_{16}$	SI/O Receive Buffer Register 0	G0RB	$XXXX\ XXXX_2$ $XXX0\ XXXX_2$
$00EA_{16}$	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX_{16}
$00EB_{16}$			
$00EC_{16}$	Receive Input Register 0	G0RI	XX_{16}
$00ED_{16}$	SI/O Communication Mode Register 0	G0MR	00_{16}
$00EE_{16}$	Transmit Output Register 0	G0TO	XX_{16}
$00EF_{16}$	SI/O Communication Control Register 0	G0CR	$0000\ X011_2$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00F0$_{16}$	Data Compare Register 00	G0CMP0	XX$_{16}$
00F1$_{16}$	Data Compare Register 01	G0CMP1	XX$_{16}$
00F2$_{16}$	Data Compare Register 02	G0CMP2	XX$_{16}$
00F3$_{16}$	Data Compare Register 03	G0CMP3	XX$_{16}$
00F4$_{16}$	Data Mask Register 00	G0MSK0	XX$_{16}$
00F5$_{16}$	Data Mask Register 01	G0MSK1	XX$_{16}$
00F6$_{16}$	Communication Clock Select Register	CCS	XXXX 0000$_{2}$
00F7$_{16}$			
00F8$_{16}$ 00F9$_{16}$	Receive CRC Code Register 0	G0RCRC	XX$_{16}$ XX$_{16}$
00FA$_{16}$ 00FB$_{16}$	Transmit CRC Code Register 0	G0TCRC	00$_{16}$ 00$_{16}$
00FC$_{16}$	SI/O Extended Mode Register 0	G0EMR	00$_{16}$
00FD$_{16}$	SI/O Extended Receive Control Register 0	G0ERC	00$_{16}$
00FE$_{16}$	SI/O Special Communication Interrupt Detect Register 0	G0IRF	00$_{16}$
00FF$_{16}$	SI/O Extended Transmit Control Register 0	G0ETC	0000 0XXX$_{2}$
0100$_{16}$ 0101$_{16}$	Time Measurement/Waveform Generating Register 10	G1TM0/G1PO0	XX$_{16}$ XX$_{16}$
0102$_{16}$ 0103$_{16}$	Time Measurement/Waveform Generating Register 11	G1TM1/G1PO1	XX$_{16}$ XX$_{16}$
0104$_{16}$ 0105$_{16}$	Time Measurement/Waveform Generating Register 12	G1TM2/G1PO2	XX$_{16}$ XX$_{16}$
0106$_{16}$ 0107$_{16}$	Time Measurement/Waveform Generating Register 13	G1TM3/G1PO3	XX$_{16}$ XX$_{16}$
0108$_{16}$ 0109$_{16}$	Time Measurement/Waveform Generating Register 14	G1TM4/G1PO4	XX$_{16}$ XX$_{16}$
010A$_{16}$ 010B$_{16}$	Time Measurement/Waveform Generating Register 15	G1TM5/G1PO5	XX$_{16}$ XX$_{16}$
010C$_{16}$ 010D$_{16}$	Time Measurement/Waveform Generating Register 16	G1TM6/G1PO6	XX$_{16}$ XX$_{16}$
010E$_{16}$ 010F$_{16}$	Time Measurement/Waveform Generating Register 17	G1TM7/G1PO7	XX$_{16}$ XX$_{16}$
0110$_{16}$	Waveform Generating Control Register 10	G1POCR0	0000 X000$_{2}$
0111$_{16}$	Waveform Generating Control Register 11	G1POCR1	0X00 X000$_{2}$
0112$_{16}$	Waveform Generating Control Register 12	G1POCR2	0X00 X000$_{2}$
0113$_{16}$	Waveform Generating Control Register 13	G1POCR3	0X00 X000$_{2}$
0114$_{16}$	Waveform Generating Control Register 14	G1POCR4	0X00 X000$_{2}$
0115$_{16}$	Waveform Generating Control Register 15	G1POCR5	0X00 X000$_{2}$
0116$_{16}$	Waveform Generating Control Register 16	G1POCR6	0X00 X000$_{2}$
0117$_{16}$	Waveform Generating Control Register 17	G1POCR7	0X00 X000$_{2}$
0118$_{16}$	Time Measurement Control Register 10	G1TMCR0	00$_{16}$
0119$_{16}$	Time Measurement Control Register 11	G1TMCR1	00$_{16}$
011A$_{16}$	Time Measurement Control Register 12	G1TMCR2	00$_{16}$
011B$_{16}$	Time Measurement Control Register 13	G1TMCR3	00$_{16}$
011C$_{16}$	Time Measurement Control Register 14	G1TMCR4	00$_{16}$
011D$_{16}$	Time Measurement Control Register 15	G1TMCR5	00$_{16}$
011E$_{16}$	Time Measurement Control Register 16	G1TMCR6	00$_{16}$
011F$_{16}$	Time Measurement Control Register 17	G1TMCR7	00$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0120_{16} 0121_{16}	Base Timer Register 1	G1BT	XX_{16} XX_{16}
0122_{16}	Base Timer Control Register 10	G1BCR0	00_{16}
0123_{16}	Base Timer Control Register 11	G1BCR1	00_{16}
0124_{16}	Time Measurement Prescaler Register 16	G1TPR6	00_{16}
0125_{16}	Time Measurement Prescaler Register 17	G1TPR7	00_{16}
0126_{16}	Function Enable Register 1	G1FE	00_{16}
0127_{16}	Function Select Register 1	G1FS	00_{16}
0128_{16} 0129_{16}	SI/O Receive Buffer Register 1	G1RB	$XXXX\ XXXX_2$ $XX00\ XXXX_2$
$012A_{16}$	Transmit Buffer/Receive Data Register 1	G1TB/G1DR	XX_{16}
$012B_{16}$			
$012C_{16}$	Receive Input Register 1	G1RI	XX_{16}
$012D_{16}$	SI/O Communication Mode Register 1	G1MR	00_{16}
$012E_{16}$	Transmit Output Register 1	G1TO	XX_{16}
$012F_{16}$	SI/O Communication Control Register 1	G1CR	$0000\ X011_2$
0130_{16}	Data Compare Register 10	G1CMP0	XX_{16}
0131_{16}	Data Compare Register 11	G1CMP1	XX_{16}
0132_{16}	Data Compare Register 12	G1CMP2	XX_{16}
0133_{16}	Data Compare Register 13	G1CMP3	XX_{16}
0134_{16}	Data Mask Register 10	G1MSK0	XX_{16}
0135_{16}	Data Mask Register 11	G1MSK1	XX_{16}
0136_{16}			
0137_{16}			
0138_{16} 0139_{16}	Receive CRC Code Register 1	G1RCRC	XX_{16} XX_{16}
$013A_{16}$ $013B_{16}$	Transmit CRC Code Register 1	G1TCRC	00_{16} 00_{16}
$013C_{16}$	SI/O Extended Mode Register 1	G1EMR	00_{16}
$013D_{16}$	SI/O Extended Receive Control Register 1	G1ERC	00_{16}
$013E_{16}$	SI/O Special Communication Interrupt Detect Register 1	G1IRF	00_{16}
$013F_{16}$	SI/O Extended Transmit Control Register 1	G1ETC	$0000\ 0XXX_2$
0140_{16}			
0141_{16}			
0142_{16}			
0143_{16}			
0144_{16}			
0145_{16}			
0146_{16}			
0147_{16}			
0148_{16}			
0149_{16}			
$014A_{16}$			
$014B_{16}$			
$014C_{16}$			
$014D_{16}$			
$014E_{16}$			
$014F_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0150$_{16}$			
0151$_{16}$			
0152$_{16}$			
0153$_{16}$			
0154$_{16}$			
0155$_{16}$			
0156$_{16}$			
0157$_{16}$			
0158$_{16}$			
0159$_{16}$			
015A$_{16}$			
015B$_{16}$			
015C$_{16}$			
015D$_{16}$			
015E$_{16}$			
015F$_{16}$			
0160$_{16}$			
0161$_{16}$			
0162$_{16}$			
0163$_{16}$			
0164$_{16}$			
0165$_{16}$			
0166$_{16}$			
0167$_{16}$			
0168$_{16}$			
0169$_{16}$			
016A$_{16}$			
016B$_{16}$			
016C$_{16}$			
016D$_{16}$			
016E$_{16}$			
016F$_{16}$			
0170$_{16}$			
0171$_{16}$			
0172$_{16}$			
0173$_{16}$			
0174$_{16}$			
0175$_{16}$			
0176$_{16}$			
0177$_{16}$			
0178$_{16}$	Input Function Select Register	IPS	00$_{16}$
0179$_{16}$	Input Function Select Register A	IPSA	00$_{16}$
017A$_{16}$			
017B$_{16}$			
017C$_{16}$			
017D$_{16}$ to 01DF$_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
01E0$_{16}$	CAN0 Message Slot Buffer 0 Standard ID0	C0SLOT0_0	XX$_{16}$
01E1$_{16}$	CAN0 Message Slot Buffer 0 Standard ID1	C0SLOT0_1	XX$_{16}$
01E2$_{16}$	CAN0 Message Slot Buffer 0 Extended ID0	C0SLOT0_2	XX$_{16}$
01E3$_{16}$	CAN0 Message Slot Buffer 0 Extended ID1	C0SLOT0_3	XX$_{16}$
01E4$_{16}$	CAN0 Message Slot Buffer 0 Extended ID2	C0SLOT0_4	XX$_{16}$
01E5$_{16}$	CAN0 Message Slot Buffer 0 Data Length Code	C0SLOT0_5	XX$_{16}$
01E6$_{16}$	CAN0 Message Slot Buffer 0 Data 0	C0SLOT0_6	XX$_{16}$
01E7$_{16}$	CAN0 Message Slot Buffer 0 Data 1	C0SLOT0_7	XX$_{16}$
01E8$_{16}$	CAN0 Message Slot Buffer 0 Data 2	C0SLOT0_8	XX$_{16}$
01E9$_{16}$	CAN0 Message Slot Buffer 0 Data 3	C0SLOT0_9	XX$_{16}$
01EA$_{16}$	CAN0 Message Slot Buffer 0 Data 4	C0SLOT0_10	XX$_{16}$
01EB$_{16}$	CAN0 Message Slot Buffer 0 Data 5	C0SLOT0_11	XX$_{16}$
01EC$_{16}$	CAN0 Message Slot Buffer 0 Data 6	C0SLOT0_12	XX$_{16}$
01ED$_{16}$	CAN0 Message Slot Buffer 0 Data 7	C0SLOT0_13	XX$_{16}$
01EE$_{16}$	CAN0 Message Slot Buffer 0 Time Stamp High-Order	C0SLOT0_14	XX$_{16}$
01EF$_{16}$	CAN0 Message Slot Buffer 0 Time Stamp Low-Order	C0SLOT0_15	XX$_{16}$
01F0$_{16}$	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XX$_{16}$
01F1$_{16}$	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XX$_{16}$
01F2$_{16}$	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XX$_{16}$
01F3$_{16}$	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XX$_{16}$
01F4$_{16}$	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XX$_{16}$
01F5$_{16}$	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XX$_{16}$
01F6$_{16}$	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XX$_{16}$
01F7$_{16}$	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XX$_{16}$
01F8$_{16}$	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XX$_{16}$
01F9$_{16}$	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XX$_{16}$
01FA$_{16}$	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XX$_{16}$
01FB$_{16}$	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XX$_{16}$
01FC$_{16}$	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XX$_{16}$
01FD$_{16}$	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XX$_{16}$
01FE$_{16}$	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XX$_{16}$
01FF$_{16}$	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XX$_{16}$
0200$_{16}$ 0201$_{16}$	CAN0 Control Register 0	C0CTLR0	XX01 0X01$_{2}$(1) XXXX 0000$_{2}$(1)
0202$_{16}$ 0203$_{16}$	CAN0 Status Register	C0STR	0000 0000$_{2}$(1) X000 0X01$_{2}$(1)
0204$_{16}$ 0205$_{16}$	CAN0 Extended ID Register	C0IDR	00$_{16}$(1) 00$_{16}$(1)
0206$_{16}$ 0207$_{16}$	CAN0 Configuration Register	C0CONR	0000 XXXX$_{2}$(1) 0000 0000$_{2}$(1)
0208$_{16}$ 0209$_{16}$	CAN0 Time Stamp Register	C0TSR	00$_{16}$(1) 00$_{16}$(1)
020A$_{16}$	CAN0 Transmit Error Count Register	C0TEC	00$_{16}$(1)
020B$_{16}$	CAN0 Receive Error Count Register	C0REC	00$_{16}$(1)
020C$_{16}$ 020D$_{16}$	CAN0 Slot Interrupt Status Register	C0SISTR	00$_{16}$(1) 00$_{16}$(1)
020E$_{16}$			
020F$_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset

Address	Register	Symbol	Value after RESET	
0210_{16} 0211_{16}	CAN0 Slot Interrupt Mask Register	C0SIMKR	00_{16}(2) 00_{16}(2)	
0212_{16}				
0213_{16}				
0214_{16}	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX $X000_2$(2)	
0215_{16}	CAN0 Error Interrupt Status Register	C0EISTR	XXXX $X000_2$(2)	
0216_{16}	CAN0 Error Cause Register	C0EFR	00_{16}(2)	
0217_{16}	CAN0 Baud Rate Prescaler	C0BRP	$0000\ 0001_2$(2)	
0218_{16}				
0219_{16}	CAN0 Mode Register	C0MDR	XXXX $XX00_2$(2)	
$021A_{16}$				
$021B_{16}$				
$021C_{16}$				
$021D_{16}$				
$021E_{16}$				
$021F_{16}$				
0220_{16} 0221_{16}	CAN0 Single Shot Control Register	C0SSCTLR	00_{16}(2) 00_{16}(2)	(Note 1)
0222_{16}				
0223_{16}				
0224_{16} 0225_{16}	CAN0 Single Shot Status Register	C0SSSTR	00_{16}(2) 00_{16}(2)	
0226_{16}				
0227_{16}				
0228_{16}	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000_2(2)	
0229_{16}	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000_2(2)	
$022A_{16}$	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000_2(2)	
$022B_{16}$	CAN0 Global Mask Register Extended ID1	C0GMR3	00_{16}(2)	
$022C_{16}$	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000_2(2)	
$022D_{16}$				
$022E_{16}$				
$022F_{16}$				
0230_{16}	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	$0000\ 0000_2$(2) XXX0 0000_2(2)	
0231_{16}	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	$0000\ 0000_2$(2) XX00 0000_2(2)	
0232_{16}	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	$0000\ 0000_2$(2) XXXX 0000_2(2)	
0233_{16}	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	00_{16}(2) 00_{16}(2)	
0234_{16}	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	$0000\ 0000_2$(2) XX00 0000_2(2)	
0235_{16}	CAN0 Message Slot 5 Control Register	C0MCTL5	00_{16}(2)	
0236_{16}	CAN0 Message Slot 6 Control Register	C0MCTL6	00_{16}(2)	
0237_{16}	CAN0 Message Slot 7 Control Register	C0MCTL7	00_{16}(2)	
0238_{16}	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	$0000\ 0000_2$(2) XXX0 0000_2(2)	

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220_{16} to $023F_{16}$.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET	
0239_{16}	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	$0000\ 0000_2$(2) $XX00\ 0000_2$(2)	(Note 1)
$023A_{16}$	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10/ C0LMBR2	$0000\ 0000_2$(2) $XXXX\ 0000_2$(2)	
$023B_{16}$	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11/ C0LMBR3	00_{16}(2) 00_{16}(2)	
$023C_{16}$	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12/ C0LMBR4	$0000\ 0000_2$(2) $XX00\ 0000_2$(2)	
$023D_{16}$	CAN0 Message Slot 13 Control Register	C0MCTL13	00_{16}(2)	
$023E_{16}$	CAN0 Message Slot 14 Control Register	C0MCTL14	00_{16}(2)	
$023F_{16}$	CAN0 Message Slot 15 Control Register	C0MCTL15	00_{16}(2)	
0240_{16}	CAN0 Slot Buffer Select Register	C0SBS	00_{16}(2)	
0241_{16}	CAN0 Control Register 1	C0CTLR1	$X000\ 00XX_2$(2)	
0242_{16}	CAN0 Sleep Control Register	C0SLPR	$XXXX\ XXX0_2$	
0243_{16}				
0244_{16} 0245_{16}	CAN0 Acceptance Filter Support Register	C0AFS	00_{16}(2) 01_{16}(2)	
0246_{16}				
0247_{16}				
0248_{16}				
0249_{16}				
$024A_{16}$				
$024B_{16}$				
$024C_{16}$				
$024D_{16}$				
$024E_{16}$				
$024F_{16}$				
0250_{16}				
0251_{16}				
0252_{16}				
0253_{16}				
0254_{16}				
0255_{16}				
0256_{16}				
0257_{16}				
0258_{16}				
0259_{16}				
$025A_{16}$				
$025B_{16}$				
$025C_{16}$				
$025D_{16}$ to $02BF_{16}$				

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220_{16} to $023F_{16}$.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02C0$_{16}$ 02C1$_{16}$	X0 Register Y0 Register	X0R,Y0R	XX$_{16}$ XX$_{16}$
02C2$_{16}$ 02C3$_{16}$	X1 Register Y1 Register	X1R,Y1R	XX$_{16}$ XX$_{16}$
02C4$_{16}$ 02C5$_{16}$	X2 Register Y2 Register	X2R,Y2R	XX$_{16}$ XX$_{16}$
02C6$_{16}$ 02C7$_{16}$	X3 Register Y3 Register	X3R,Y3R	XX$_{16}$ XX$_{16}$
02C8$_{16}$ 02C9$_{16}$	X4 Register Y4 Register	X4R,Y4R	XX$_{16}$ XX$_{16}$
02CA$_{16}$ 02CB$_{16}$	X5 Register Y5 Register	X5R,Y5R	XX$_{16}$ XX$_{16}$
02CC$_{16}$ 02CD$_{16}$	X6 Register Y6 Register	X6R,Y6R	XX$_{16}$ XX$_{16}$
02CE$_{16}$ 02CF$_{16}$	X7 Register Y7 Register	X7R,Y7R	XX$_{16}$ XX$_{16}$
02D0$_{16}$ 02D1$_{16}$	X8 Register Y8 Register	X8R,Y8R	XX$_{16}$ XX$_{16}$
02D2$_{16}$ 02D3$_{16}$	X9 Register Y9 Register	X9R,Y9R	XX$_{16}$ XX$_{16}$
02D4$_{16}$ 02D5$_{16}$	X10 Register Y10 Register	X10R,Y10R	XX$_{16}$ XX$_{16}$
02D6$_{16}$ 02D7$_{16}$	X11 Register Y11 Register	X11R,Y11R	XX$_{16}$ XX$_{16}$
02D8$_{16}$ 02D9$_{16}$	X12 Register Y12 Register	X12R,Y12R	XX$_{16}$ XX$_{16}$
02DA$_{16}$ 02DB$_{16}$	X13 Register Y13 Register	X13R,Y13R	XX$_{16}$ XX$_{16}$
02DC$_{16}$ 02DD$_{16}$	X14 Register Y14 Register	X14R,Y14R	XX$_{16}$ XX$_{16}$
02DE$_{16}$ 02DF$_{16}$	X15 Register Y15 Register	X15R,Y15R	XX$_{16}$ XX$_{16}$
02E0$_{16}$	XY Control Register	XYC	XXXX XX00$_{2}$
02E1$_{16}$			
02E2$_{16}$			
02E3$_{16}$			
02E4$_{16}$	UART1 Special Mode Register 4	U1SMR4	00$_{16}$
02E5$_{16}$	UART1 Special Mode Register 3	U1SMR3	00$_{16}$
02E6$_{16}$	UART1 Special Mode Register 2	U1SMR2	00$_{16}$
02E7$_{16}$	UART1 Special Mode Register	U1SMR	00$_{16}$
02E8$_{16}$	UART1 Transmit/Receive Mode Register	U1MR	00$_{16}$
02E9$_{16}$	UART1 Baud Rate Register	U1BRG	XX$_{16}$
02EA$_{16}$ 02EB$_{16}$	UART1 Transmit Buffer Register	U1TB	XX$_{16}$ XX$_{16}$
02EC$_{16}$	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000$_{2}$
02ED$_{16}$	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010$_{2}$
02EE$_{16}$ 02EF$_{16}$	UART1 Receive Buffer Register	U1RB	XX$_{16}$ XX$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
02F0$_{16}$			
02F1$_{16}$			
02F2$_{16}$			
02F3$_{16}$			
02F4$_{16}$	UART4 Special Mode Register 4	U4SMR4	00$_{16}$
02F5$_{16}$	UART4 Special Mode Register 3	U4SMR3	00$_{16}$
02F6$_{16}$	UART4 Special Mode Register 2	U4SMR2	00$_{16}$
02F7$_{16}$	UART4 Special Mode Register	U4SMR	00$_{16}$
02F8$_{16}$	UART4 Transmit/Receive Mode Register	U4MR	00$_{16}$
02F9$_{16}$	UART4 Baud Rate Register	U4BRG	XX$_{16}$
02FA$_{16}$ 02FB$_{16}$	UART4 Transmit Buffer Register	U4TB	XX$_{16}$ XX$_{16}$
02FC$_{16}$	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000$_{2}$
02FD$_{16}$	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010$_{2}$
02FE$_{16}$ 02FF$_{16}$	UART4 Receive Buffer Register	U4RB	XX$_{16}$ XX$_{16}$
0300$_{16}$	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX$_{2}$
0301$_{16}$			
0302$_{16}$ 0303$_{16}$	Timer A1-1 Register	TA11	XX$_{16}$ XX$_{16}$
0304$_{16}$ 0305$_{16}$	Timer A2-1 Register	TA21	XX$_{16}$ XX$_{16}$
0306$_{16}$ 0307$_{16}$	Timer A4-1 Register	TA41	XX$_{16}$ XX$_{16}$
0308$_{16}$	Three-Phase PWM Control Register 0	INVC0	00$_{16}$
0309$_{16}$	Three-Phase PWM Control Register 1	INVC1	00$_{16}$
030A$_{16}$	Three-Phase Output Buffer Register 0	IDB0	0011 1111$_{2}$
030B$_{16}$	Three-Phase Output Buffer Register 1	IDB1	0011 1111$_{2}$
030C$_{16}$	Dead Time Timer	DTT	XX$_{16}$
030D$_{16}$	Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	XX$_{16}$
030E$_{16}$			
030F$_{16}$			
0310$_{16}$ 0311$_{16}$	Timer B3 Register	TB3	XX$_{16}$ XX$_{16}$
0312$_{16}$ 0313$_{16}$	Timer B4 Register	TB4	XX$_{16}$ XX$_{16}$
0314$_{16}$ 0315$_{16}$	Timer B5 Register	TB5	XX$_{16}$ XX$_{16}$
0316$_{16}$			
0317$_{16}$			
0318$_{16}$			
0319$_{16}$			
031A$_{16}$			
031B$_{16}$	Timer B3 Mode Register	TB3MR	00XX 0000$_{2}$
031C$_{16}$	Timer B4 Mode Register	TB4MR	00XX 0000$_{2}$
031D$_{16}$	Timer B5 Mode Register	TB5MR	00XX 0000$_{2}$
031E$_{16}$			
031F$_{16}$	External Interrupt Cause Select Register	IFSR	00$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0320$_{16}$			
0321$_{16}$			
0322$_{16}$			
0323$_{16}$			
0324$_{16}$	UART3 Special Mode Register 4	U3SMR4	00$_{16}$
0325$_{16}$	UART3 Special Mode Register 3	U3SMR3	00$_{16}$
0326$_{16}$	UART3 Special Mode Register 2	U3SMR2	00$_{16}$
0327$_{16}$	UART3 Special Mode Register	U3SMR	00$_{16}$
0328$_{16}$	UART3 Transmit/Receive Mode Register	U3MR	00$_{16}$
0329$_{16}$	UART3 Baud Rate Register	U3BRG	XX$_{16}$
032A$_{16}$ 032B$_{16}$	UART3 Transmit Buffer Register	U3TB	XX$_{16}$ XX$_{16}$
032C$_{16}$	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000$_{2}$
032D$_{16}$	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010$_{2}$
032E$_{16}$ 032F$_{16}$	UART3 Receive Buffer Register	U3RB	XX$_{16}$ XX$_{16}$
0330$_{16}$			
0331$_{16}$			
0332$_{16}$			
0333$_{16}$			
0334$_{16}$	UART2 Special Mode Register 4	U2SMR4	00$_{16}$
0335$_{16}$	UART2 Special Mode Register 3	U2SMR3	00$_{16}$
0336$_{16}$	UART2 Special Mode Register 2	U2SMR2	00$_{16}$
0337$_{16}$	UART2 Special Mode Register	U2SMR	00$_{16}$
0338$_{16}$	UART2 Transmit/Receive Mode Register	U2MR	00$_{16}$
0339$_{16}$	UART2 Baud Rate Register	U2BRG	XX$_{16}$
033A$_{16}$ 033B$_{16}$	UART2 Transmit Buffer Register	U2TB	XX$_{16}$ XX$_{16}$
033C$_{16}$	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000$_{2}$
033D$_{16}$	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010$_{2}$
033E$_{16}$ 033F$_{16}$	UART2 Receive Buffer Register	U2RB	XX$_{16}$ XX$_{16}$
0340$_{16}$	Count Start Flag	TABSR	00$_{16}$
0341$_{16}$	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX$_{2}$
0342$_{16}$	One-Shot Start Flag	ONSF	00$_{16}$
0343$_{16}$	Trigger Select Register	TRGSR	00$_{16}$
0344$_{16}$	Up-Down Flag	UDF	00$_{16}$
0345$_{16}$			
0346$_{16}$ 0347$_{16}$	Timer A0 Register	TA0	XX$_{16}$ XX$_{16}$
0348$_{16}$ 0349$_{16}$	Timer A1 Register	TA1	XX$_{16}$ XX$_{16}$
034A$_{16}$ 034B$_{16}$	Timer A2 Register	TA2	XX$_{16}$ XX$_{16}$
034C$_{16}$ 034D$_{16}$	Timer A3 Register	TA3	XX$_{16}$ XX$_{16}$
034E$_{16}$ 034F$_{16}$	Timer A4 Register	TA4	XX$_{16}$ XX$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0350_{16} 0351_{16}	Timer B0 Register	TB0	XX_{16} XX_{16}
0352_{16} 0353_{16}	Timer B1 Register	TB1	XX_{16} XX_{16}
0354_{16} 0355_{16}	Timer B2 Register	TB2	XX_{16} XX_{16}
0356_{16}	Timer A0 Mode Register	TA0MR	00_{16}
0357_{16}	Timer A1 Mode Register	TA1MR	00_{16}
0358_{16}	Timer A2 Mode Register	TA2MR	00_{16}
0359_{16}	Timer A3 Mode Register	TA3MR	00_{16}
$035A_{16}$	Timer A4 Mode Register	TA4MR	00_{16}
$035B_{16}$	Timer B0 Mode Register	TB0MR	$00XX\ 0000_2$
$035C_{16}$	Timer B1 Mode Register	TB1MR	$00XX\ 0000_2$
$035D_{16}$	Timer B2 Mode Register	TB2MR	$00XX\ 0000_2$
$035E_{16}$	Timer B2 Special Mode Register	TB2SC	$XXXX\ XXX0_2$
$035F_{16}$	Count Source Prescaler Register(1)	TCSPR	00_{16}
0360_{16}			
0361_{16}			
0362_{16}			
0363_{16}			
0364_{16}	UART0 Special Mode Register 4	U0SMR4	00_{16}
0365_{16}	UART0 Special Mode Register 3	U0SMR3	00_{16}
0366_{16}	UART0 Special Mode Register 2	U0SMR2	00_{16}
0367_{16}	UART0 Special Mode Register	U0SMR	00_{16}
0368_{16}	UART0 Transmit/Receive Mode Register	U0MR	00_{16}
0369_{16}	UART0 Baud Rate Register	U0BRG	XX_{16}
$036A_{16}$ $036B_{16}$	UART0 Transmit Buffer Register	U0TB	XX_{16} XX_{16}
$036C_{16}$	UART0 Transmit/Receive Control Register 0	U0C0	$0000\ 1000_2$
$036D_{16}$	UART0 Transmit/Receive Control Register 1	U0C1	$0000\ 0010_2$
$036E_{16}$ $036F_{16}$	UART0 Receive Buffer Register	U0RB	XX_{16} XX_{16}
0370_{16}			
0371_{16}			
0372_{16}			
0373_{16}			
0374_{16}			
0375_{16}			
0376_{16}			
0377_{16}			
0378_{16}	DMA0 Factor Select Register	DM0SL	00_{16}
0379_{16}	DMA1 Factor Select Register	DM1SL	00_{16}
$037A_{16}$	DMA2 Factor Select Register	DM2SL	00_{16}
$037B_{16}$	DMA3 Factor Select Register	DM3SL	00_{16}
$037C_{16}$ $037D_{16}$	CRC Data Register	CRCD	XX_{16} XX_{16}
$037E_{16}$	CRC Input Register	CRCIN	XX_{16}
$037F_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The TCSPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
0380_{16} 0381_{16}	A/D0 Register 0	AD00	XXXX XXXX_2 0000 0000_2
0382_{16} 0383_{16}	A/D0 Register 1	AD01	XX_{16} XX_{16}
0384_{16} 0385_{16}	A/D0 Register 2	AD02	XX_{16} XX_{16}
0386_{16} 0387_{16}	A/D0 Register 3	AD03	XX_{16} XX_{16}
0388_{16} 0389_{16}	A/D0 Register 4	AD04	XX_{16} XX_{16}
$038A_{16}$ $038B_{16}$	A/D0 Register 5	AD05	XX_{16} XX_{16}
$038C_{16}$ $038D_{16}$	A/D0 Register 6	AD06	XX_{16} XX_{16}
$038E_{16}$ $038F_{16}$	A/D0 Register 7	AD07	XX_{16} XX_{16}
0390_{16}			
0391_{16}			
0392_{16}	A/D0 Control Register 4	AD0CON4	XXXX $00XX_2$
0393_{16}			
0394_{16}	A/D0 Control Register 2	AD0CON2	XX0X $X000_2$
0395_{16}	A/D0 Control Register 3	AD0CON3	XXXX $X000_2$
0396_{16}	A/D0 Control Register 0	AD0CON0	00_{16}
0397_{16}	A/D0 Control Register 1	AD0CON1	00_{16}
0398_{16}	D/A Register 0	DA0	XX_{16}
0399_{16}			
$039A_{16}$	D/A Register 1	DA1	XX_{16}
$039B_{16}$			
$039C_{16}$	D/A Control Register	DACON	XXXX $XX00_2$
$039D_{16}$			
$039E_{16}$			
$039F_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin Package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$	Function Select Register A8	PS8	X000 0000$_2$
03A1$_{16}$	Function Select Register A9	PS9	00$_{16}$
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function Select Register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function Select Register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function Select Register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function Select Register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function Select Register A0	PS0	00$_{16}$
03B1$_{16}$	Function Select Register A1	PS1	00$_{16}$
03B2$_{16}$	Function Select Register B0	PSL0	00$_{16}$
03B3$_{16}$	Function Select Register B1	PSL1	00$_{16}$
03B4$_{16}$	Function Select Register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function Select Register A3	PS3	00$_{16}$
03B6$_{16}$	Function Select Register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function Select Register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$	Function Select Register A5	PS5	XXX0 0000$_2$
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 Register	P6	XX$_{16}$
03C1$_{16}$	Port P7 Register	P7	XX$_{16}$
03C2$_{16}$	Port P6 Direction Register	PD6	00$_{16}$
03C3$_{16}$	Port P7 Direction Register	PD7	00$_{16}$
03C4$_{16}$	Port P8 Register	P8	XX$_{16}$
03C5$_{16}$	Port P9 Register	P9	XX$_{16}$
03C6$_{16}$	Port P8 Direction Register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 Direction Register	PD9	00$_{16}$
03C8$_{16}$	Port P10 Register	P10	XX$_{16}$
03C9$_{16}$	Port P11 Register	P11	XX$_{16}$
03CA$_{16}$	Port P10 Direction Register	PD10	00$_{16}$
03CB$_{16}$	Port P11 Direction Register	PD11	XXX0 0000$_2$
03CC$_{16}$	Port P12 Register	P12	XX$_{16}$
03CD$_{16}$	Port P13 Register	P13	XX$_{16}$
03CE$_{16}$	Port P12 Direction Register	PD12	00$_{16}$
03CF$_{16}$	Port P13 Direction Register	PD13	00$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin Package>

Address	Register	Symbol	Value after RESET
03D0$_{16}$	Port P14 Register	P14	XX$_{16}$
03D1$_{16}$	Port P15 Register	P15	XX$_{16}$
03D2$_{16}$	Port P14 Direction Register	PD14	X000 0000$_{2}$
03D3$_{16}$	Port P15 Direction Register	PD15	00$_{16}$
03D4$_{16}$			
03D5$_{16}$			
03D6$_{16}$			
03D7$_{16}$			
03D8$_{16}$			
03D9$_{16}$			
03DA$_{16}$	Pull-Up Control Register 2	PUR2	00$_{16}$
03DB$_{16}$	Pull-Up Control Register 3	PUR3	00$_{16}$
03DC$_{16}$	Pull-Up Control Register 4	PUR4	XXXX 0000$_{2}$
03DD$_{16}$			
03DE$_{16}$			
03DF$_{16}$			
03E0$_{16}$	Port P0 Register	P0	XX$_{16}$
03E1$_{16}$	Port P1 Register	P1	XX$_{16}$
03E2$_{16}$	Port P0 Direction Register	PD0	00$_{16}$
03E3$_{16}$	Port P1 Direction Register	PD1	00$_{16}$
03E4$_{16}$	Port P2 Register	P2	XX$_{16}$
03E5$_{16}$	Port P3 Register	P3	XX$_{16}$
03E6$_{16}$	Port P2 Direction Register	PD2	00$_{16}$
03E7$_{16}$	Port P3 Direction Register	PD3	00$_{16}$
03E8$_{16}$	Port P4 Register	P4	XX$_{16}$
03E9$_{16}$	Port P5 Register	P5	XX$_{16}$
03EA$_{16}$	Port P4 Direction Register	PD4	00$_{16}$
03EB$_{16}$	Port P5 Direction Register	PD5	00$_{16}$
03EC$_{16}$			
03ED$_{16}$			
03EE$_{16}$			
03EF$_{16}$			
03F0$_{16}$	Pull-Up Control Register 0	PUR0	00$_{16}$
03F1$_{16}$	Pull-Up Control Register 1	PUR1	XXXX 0000$_{2}$
03F2$_{16}$			
03F3$_{16}$			
03F4$_{16}$			
03F5$_{16}$			
03F6$_{16}$			
03F7$_{16}$			
03F8$_{16}$			
03F9$_{16}$			
03FA$_{16}$			
03FB$_{16}$			
03FC$_{16}$			
03FD$_{16}$			
03FE$_{16}$			
03FF$_{16}$	Port Control Register	PCR	XXXX XXX0$_{2}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin Package>

Address	Register	Symbol	Value after RESET
$03A0_{16}$			
$03A1_{16}$			
$03A2_{16}$			
$03A3_{16}$			
$03A4_{16}$			
$03A5_{16}$			
$03A6_{16}$			
$03A7_{16}$	Function Select Register D1	PSD1	$X0XX\ XX00_2$
$03A8_{16}$			
$03A9_{16}$			
$03AA_{16}$			
$03AB_{16}$			
$03AC_{16}$	Function Select Register C2	PSC2	$XXXX\ X00X_2$
$03AD_{16}$	Function Select Register C3	PSC3	$X0XX\ XXXX_2$
$03AE_{16}$			
$03AF_{16}$	Function Select Register C	PSC	$0X00\ 0000_2$
$03B0_{16}$	Function Select Register A0	PS0	00_{16}
$03B1_{16}$	Function Select Register A1	PS1	00_{16}
$03B2_{16}$	Function Select Register B0	PSL0	00_{16}
$03B3_{16}$	Function Select Register B1	PSL1	00_{16}
$03B4_{16}$	Function Select Register A2	PS2	$00X0\ 0000_2$
$03B5_{16}$	Function Select Register A3	PS3	00_{16}
$03B6_{16}$	Function Select Register B2	PSL2	$00X0\ 0000_2$
$03B7_{16}$	Function Select Register B3	PSL3	00_{16}
$03B8_{16}$			
$03B9_{16}$			
$03BA_{16}$			
$03BB_{16}$			
$03BC_{16}$			
$03BD_{16}$			
$03BE_{16}$			
$03BF_{16}$			
$03C0_{16}$	Port P6 Register	P6	XX_{16}
$03C1_{16}$	Port P7 Register	P7	XX_{16}
$03C2_{16}$	Port P6 Direction Register	PD6	00_{16}
$03C3_{16}$	Port P7 Direction Register	PD7	00_{16}
$03C4_{16}$	Port P8 Register	P8	XX_{16}
$03C5_{16}$	Port P9 Register	P9	XX_{16}
$03C6_{16}$	Port P8 Direction Register	PD8	$00X0\ 0000_2$
$03C7_{16}$	Port P9 Direction Register	PD9	00_{16}
$03C8_{16}$	Port P10 Register	P10	XX_{16}
$03C9_{16}$			
$03CA_{16}$	Port P10 Direction Register	PD10	00_{16}
$03CB_{16}$	Set default value to "FF_{16}"		
$03CC_{16}$			
$03CD_{16}$			
$03CE_{16}$	Set default value to "FF_{16}"		
$03CF_{16}$	Set default value to "FF_{16}"		

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin Package>

Address	Register	Symbol	Value after RESET
03D0$_{16}$			
03D1$_{16}$			
03D2$_{16}$	Set default value to "FF$_{16}$"		
03D3$_{16}$	Set default value to "FF$_{16}$"		
03D4$_{16}$			
03D5$_{16}$			
03D6$_{16}$			
03D7$_{16}$			
03D8$_{16}$			
03D9$_{16}$			
03DA$_{16}$	Pull-Up Control Register 2	PUR2	00$_{16}$
03DB$_{16}$	Pull-Up Control Register 3	PUR3	00$_{16}$
03DC$_{16}$	Set default value to "00$_{16}$"		
03DD$_{16}$			
03DE$_{16}$			
03DF$_{16}$			
03E0$_{16}$	Port P0 Register	P0	XX$_{16}$
03E1$_{16}$	Port P1 Register	P1	XX$_{16}$
03E2$_{16}$	Port P0 Direction Register	PD0	00$_{16}$
03E3$_{16}$	Port P1 Direction Register	PD1	00$_{16}$
03E4$_{16}$	Port P2 Register	P2	XX$_{16}$
03E5$_{16}$	Port P3 Register	P3	XX$_{16}$
03E6$_{16}$	Port P2 Direction Register	PD2	00$_{16}$
03E7$_{16}$	Port P3 Direction Register	PD3	00$_{16}$
03E8$_{16}$	Port P4 Register	P4	XX$_{16}$
03E9$_{16}$	Port P5 Register	P5	XX$_{16}$
03EA$_{16}$	Port P4 Direction Register	PD4	00$_{16}$
03EB$_{16}$	Port P5 Direction Register	PD5	00$_{16}$
03EC$_{16}$			
03ED$_{16}$			
03EE$_{16}$			
03EF$_{16}$			
03F0$_{16}$	Pull-up Control Register 0	PUR0	00$_{16}$
03F1$_{16}$	Pull-up Control Register 1	PUR1	XXXX 0000$_{2}$
03F2$_{16}$			
03F3$_{16}$			
03F4$_{16}$			
03F5$_{16}$			
03F6$_{16}$			
03F7$_{16}$			
03F8$_{16}$			
03F9$_{16}$			
03FA$_{16}$			
03FB$_{16}$			
03FC$_{16}$			
03FD$_{16}$			
03FE$_{16}$			
03FF$_{16}$	Port Control Register	PCR	XXXX XXX0$_{2}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

5. Electrical Characteristics

5.1 Electrical Characteristics (M32C/84)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V_{CC1}, V_{CC2}	Supply Voltage		V_{CC1}=AV_{CC}	-0.3 to 6.0	V
V_{CC2}	Supply Voltage		-	-0.3 to V_{CC1}	V
AV_{CC}	Analog Supply Voltage		V_{CC1}=AV_{CC}	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNV_{SS}, BYTE, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), V_{REF}, X_{IN}		-0.3 to V_{CC1}+0.3	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(1)		-0.3 to V_{CC2}+0.3	
		$P7_0$, $P7_1$		-0.3 to 6.0	
V_O	Output Voltage	$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{OUT}		-0.3 to V_{CC1}+0.3	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(1)		-0.3 to V_{CC2}+0.3	
Pd	Power Dissipation		Topr=25° C	500	mW
Topr	Operating Ambient Temperature	during CPU operation		-20 to 85/ -40 to 85(2)	° C
		during flash memory program and erase operation		0 to 60	
Tstg	Storage Temperature			-65 to 150	° C

NOTES:
1. P11 to P15 are provided in the 144-pin package only.
2. Contact Renesas Technology Sales Co., Ltd, if temperature range of -40 to 85° C is required.

Table 5.2 Recommended Operating Conditions
(V_{CC1}= V_{CC2}=3.0V to 5.5V at Topr=– 20 to 85°C unless otherwise specified)

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply Voltage ($V_{CC1} \geq V_{CC2}$)	3.0	5.0	5.5	V
AV_{CC}	Analog Supply Voltage		V_{CC1}		V
V_{SS}	Supply Voltage		0		V
AV_{SS}	Analog Supply Voltage		0		V

Table 5.2 Recommended Operating Conditions (Continued)
(V_{CC1}=V_{CC2}=3.0V to 5.5V at Topr=–20 to 85°C unless otherwise specified)

Symbol	Parameter	Accommodating Pins	Standard			Unit
			Min.	Typ.	Max.	
V_{IH}	Input High ("H") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0.8V_{CC2}		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0.8V_{CC1}		V_{CC1}	
		$P7_0$, $P7_1$	0.8V_{CC1}		6.0	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)	0.8V_{CC2}		V_{CC2}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)	0.5V_{CC2}		V_{CC2}	V
V_{IL}	Input Low ("L") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0		0.2V_{CC2}	V
		$P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0		0.2V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)	0		0.2V_{CC2}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)	0		0.16V_{CC2}	V
$I_{OH(peak)}$	Peak Output High ("H") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			5.0	mA

NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, and P11 must be -40mA or less.
   Total $I_{OH(peak)}$ for $P8_6$, $P8_7$, P9, P10, P14 and P15 must be -40mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P12 and P13 must be -40mA or less.
   Total $I_{OH(peak)}$ for P6, P7, and $P8_0$ to $P8_4$ must be -40mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply when $P8_7$ is used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

Table 5.2 Recommended Operating Conditions (Continued)
(V_{CC1}=V_{CC2}=3.0V to 5.5V at Topr=–20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f(X_{IN})$	Main Clock Input Frequency	V_{CC1}=4.2 to 5.5V	0		32	MHz
		V_{CC1}=3.0 to 5.5V	0		24	MHz
$f(X_{CIN})$	Sub Clock Frequency			32.768	50	kHz
$f(_{Ring})$	On-chip Oscillator Frequency			1		MHz
$f(_{PLL})$	PLL Clock Frequency	V_{CC1}=4.2 to 5.5V	10		32	MHz
		V_{CC1}=3.0 to 5.5V	10		24	MHz
$t_{SU(PLL)}$	PLL Lock Time	V_{CC1}=5.0V			5	ms
		V_{CC1}=3.3V			10	ms

$V_{CC1}=V_{CC2}=5V$

Table 5.3 Electrical Characteristics

($V_{CC1}=V_{CC2}$=4.2 to 5.5V, V_{SS}=0V at Topr= –20 to 85°C, f(X_{IN})=32MHz unless otherwise specified)

Symbol	Parameter			Condition		Standard			Unit
						Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$		I_{OH}=-5mA		3.0		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OH}=-5mA		3.0		V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$		I_{OH}=-200µA		4.7		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$,$P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OH}=-200µA		4.7		V_{CC1}	
		X_{OUT}		I_{OH}=-1mA		3.0			V
		X_{COUT}	High Power	No load applied			2.5		V
			Low Power	No load applied			1.6		
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OL}=5mA				2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OL}=200µA				0.45	V
		X_{OUT}		I_{OL}=1mA				2.0	V
		X_{COUT}	High Power	No load applied			0		V
			Low Power	No load applied			0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{AD_{TRG}}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4				0.2		1.0	V
		$\overline{RESET}$				0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		V_I=5V				5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		V_I=0V				-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		V_I=0V	Flash Memory	30	50	167	kΩ
					Masked ROM	20	40	167	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}					1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}					10		MΩ
V_{RAM}	RAM Standby Voltage	In stop mode				2.0			V
I_{CC}	Power Supply Current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(X_{IN})=32 MHz, square wave, no division				28	45	mA
			f(X_{CIN})=32 kHz, in wait mode, Topr=25° C				10		µA
			Topr=25° C (while clock is stopped)				0.8	5	µA
			Topr=85° C (while clock is stopped)					50	µA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=5V$

Table 5.4 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}$=4.2 to 5.5V, V_{SS}= AV_{SS} = 0V at Topr=–20 to 85°C, f(X_{IN}) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}$=5V	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8.00		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2.00		V_{CC1}	V
V_{IA}	Analog Input Voltage			0.00		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. Sample and hold function available.

Table 5.5 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}$=4.2 to 5.5V, $V_{SS}=AV_{SS}$=0V at Topr=–20 to 85°C, f(X_{IN}) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Table 5.6 Flash Memory Version Electrical Characteristics(1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and Erase Endurance(3)		100			cycles
-	Word Program Time (V_{CC1}=5.0V, Topr=25° C)			25	200	µs
-	Lock Bit Program Time			25	200	µs
-	Block Erase Time (V_{CC1}=5.0V, Topr=25° C)	4-Kbyte Block		0.3	4	s
		8-Kbyte Block		0.3	4	s
		32-Kbyte Block		0.5	4	s
		64-Kbyte Block		0.8	4	s
-	All-Unlocked-Block Erase Time(2)				4 x *n*	s
t_{PS}	Flash Memory Circuit Stabilization Wait Time				15	µs
-	Data Hold Time(4)		10			years

NOTES:
1. Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at Topr = 0 to 60 ° C unless otherwise specified.
2. n denotes the number of block to be erased.
3. Number of program-erase cycles per block.
   If Program and Erase Endurance is *n* cycle (*n*=100), each block can be erased and programmed *n* cycles.
   For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (Rewrite prohibited).
4. Topr = -40 to 85 ° C

$V_{CC1}=V_{CC2}=5V$

Table 5.7 Low Voltage Detect Circuit Electrical Characteristics ($V_{CC1}=V_{CC2}$=3.0 to 5.5V, Vss= AV_{SS}=0V at Topr=–20 to 85°C unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Voltage Down Detect Voltage(1)	V_{CC1}=3.0 to 5.5V		3.8		V
Vdet3	Reset Space Detect Voltage(1)			3.0		V
Vdet3s	Low Voltage Reset Hold Voltage		2.0			V
Vdet3r	Low Voltage Reset Release Voltage(2)			3.1		V

NOTES:
1. Vdet4 >Vdet3
2. Vdet3r >Vdet3 is not guaranteed.

Table 5.8 Power Supply Timing

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time for Stable Internal Supply Voltage when Power-on	V_{CC1}=3.0 to 5.5V			2	ms
td(S-R)	Wait Time to Release Voltage Voltage Down Detect Reset	V_{CC1}=Vdet3r to 5.5V		6(1)	20	ms
td(E-A)	Start-up Time for Low Voltage Detect Circuit Operation	V_{CC1}=3.0 to 5.5V			20	µs

NOTES:
1. V_{CC1}=5V

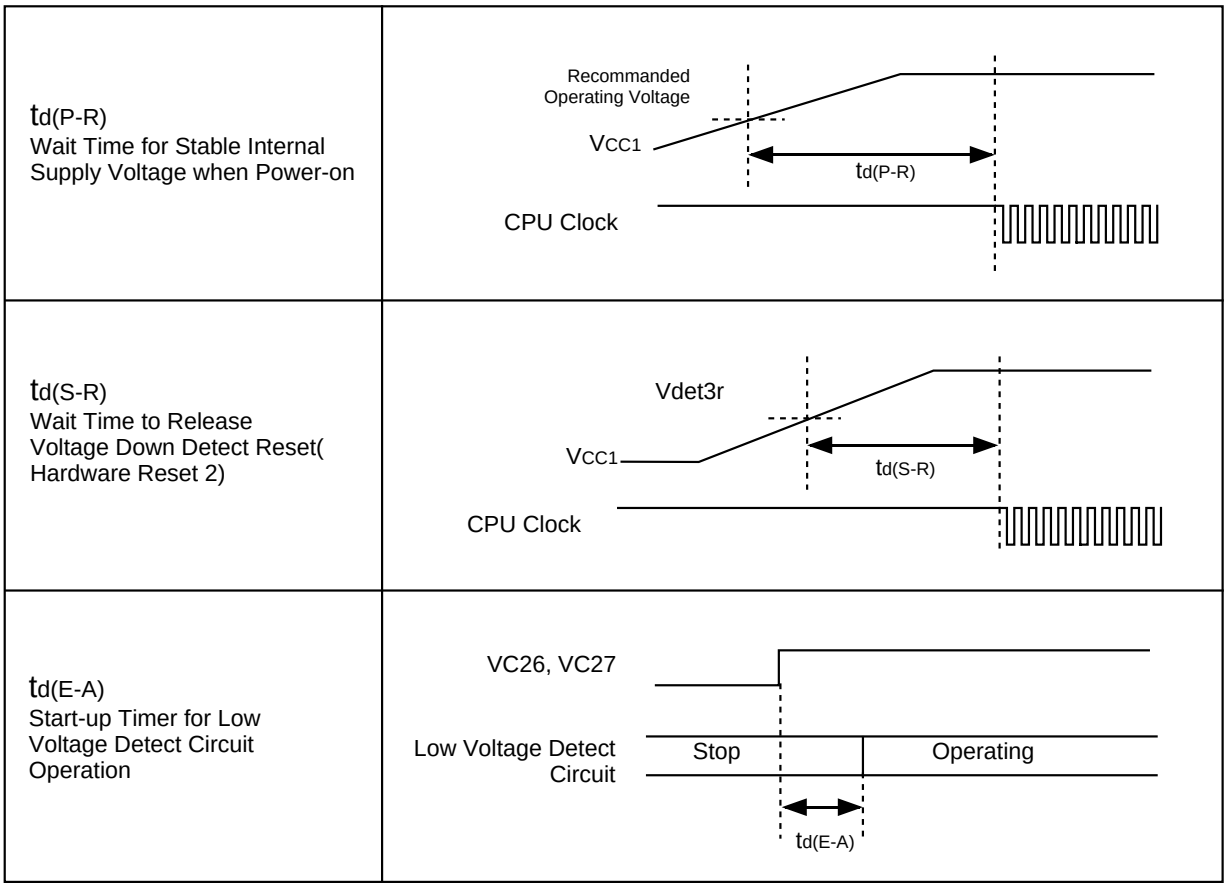


Figure 5.1 Power Supply Timing Diagram

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}$=4.2 to 5.5V, V_{SS}=0V at Topr=–20 to 85°C unless otherwise specified)

Table 5.9 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$t_{w(H)}$	External Clock Input High ("H") Width	13.75		ns
$t_{w(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.10 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	26		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	26		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	30		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequecncy and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)+1)

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, n=a+b)

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, p={(a+b-1)x2}+1)

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr=–20 to 85°C unless otherwise specified)

Table 5.11 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	40		ns

Table 5.12 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	200		ns

Table 5.13 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.14 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.15 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

(V_{CC1} = V_{CC2} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.16 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on both edges)	80		ns

Table 5.17 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.18 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.19 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ Input Cycle Time (required for re-trigger)	1000		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ Input Low ("L") Width	125		ns

Table 5.20 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.21 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.22 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-5		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n=(bx2)-1)

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, m= b)

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics

(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.23 Memory Expansion Mode and Microprocessor Mode (when accessing an external memory space with the multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$td_{(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$th_{(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$th_{(RD-AD)}$	Address Output Hold Time (RD standard)		(Note 1)		ns
$th_{(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$td_{(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$th_{(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
$th_{(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		(Note 1)		ns
$th_{(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$td_{(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$th_{(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$td_{(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$th_{(BCLK-WR)}$	WR Signal Output Hold Time		-5		ns
$td_{(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$th_{(DB-WR)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$td_{(BCLK-ALE)}$	ALE Signal Output Delay Time (BCLK standard)			18	ns
$th_{(BCLK-ALE)}$	ALE Signal Output Hold Time (BCLK standard)		-2		ns
$td_{(AD-ALE)}$	ALE Signal Output Delay Time (address standard)		(Note 3)		ns
$th_{(ALE-AD)}$	ALE Signal Output Hold Time (address standard)		(Note 4)		ns
$tdz_{(RD-AD)}$	Address Output Float Start Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$th_{(RD-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th_{(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th_{(RD-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th_{(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th_{(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$td_{(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi,\ m = (bx2)-1)$$

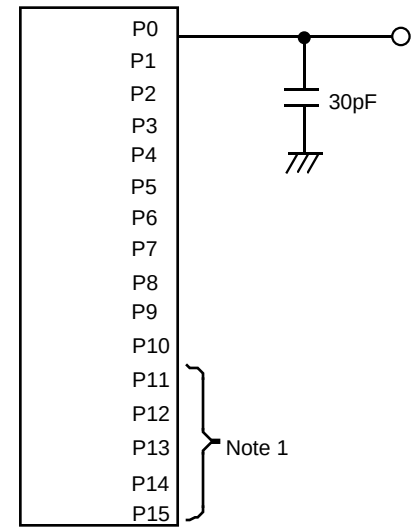
3. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$td_{(AD-ALE)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 20 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi,\ n = a)$$

4. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$th_{(ALE-AD)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 10 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi,\ n = a)$$

$V_{CC1}=V_{CC2}=5V$



NOTES:

1. P11 to P15 are provided in the 144-pin package only.

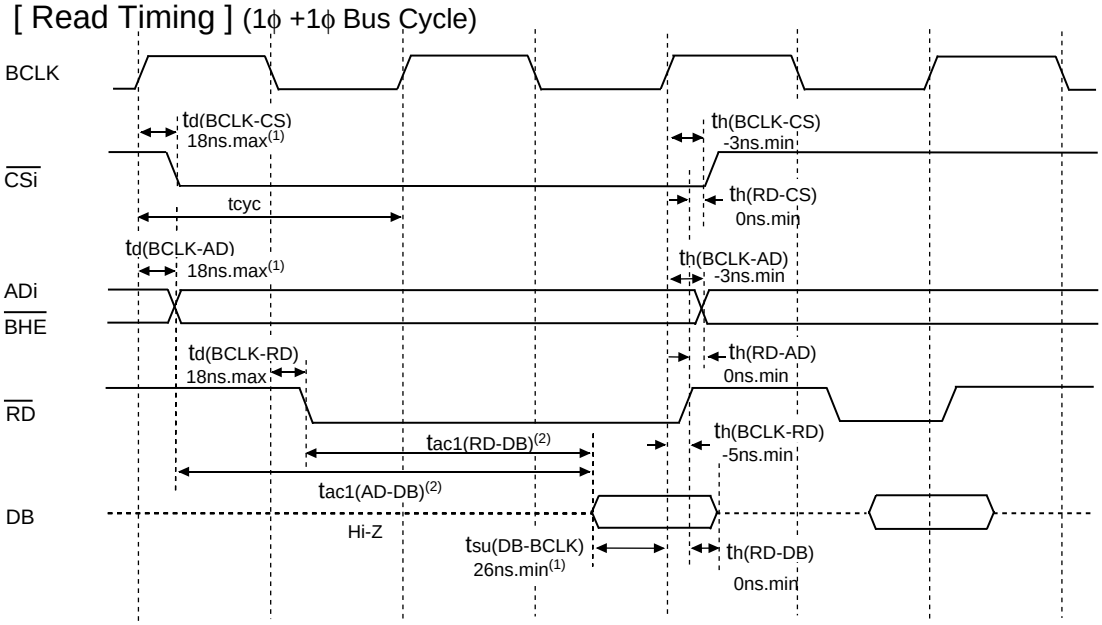
Figure 5.2 P0 to P15 Measurement Circuit

Vcc1=Vcc2=5V

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space)

[Read Timing] (1ϕ +1ϕ Bus Cycle)



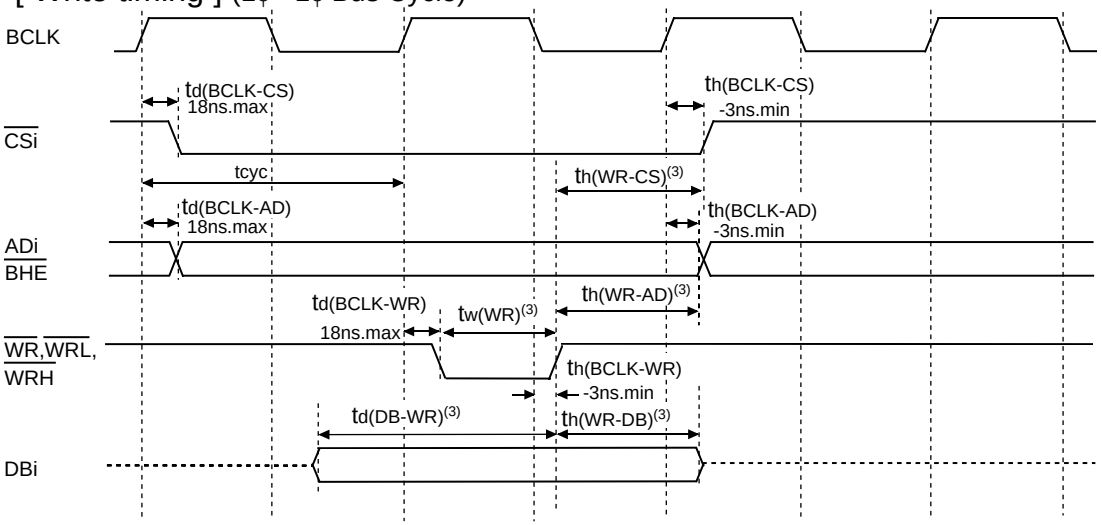
NOTES:

1. Values guaranteed only when the microcomputer is used independently.
A maximum of 35ns is guaranteed for td(BCLK-AD)+tsu(DB-BCLK).
2. Varies with operation frequency:

tac1(RD-DB)=(tcyc/2 x m-35)ns.max (if external bus cycle is aϕ + bϕ, m=(b x 2)+1)

tac1(AD-DB)=(tcyc x n-35)ns.max (if external bus cycle is aϕ + bϕ, n=a+b)

[Write timing] (1ϕ +1ϕ Bus Cycle)



NOTES:

3. Varies with operation frequency:
td(DB-WR)=(tcyc x m-20)ns.min
(if external bus cycle is aϕ+bϕ, m=b)
th(WR-DB)=(tcyc/2-10)ns.min
th(WR-AD)=(tcyc/2-10)ns.min
th(WR-CS)=(tcyc/2-10)ns.min
tw(WR)=(tcyc/2 x n-15)ns.min
(if external bus cycle is aϕ+bϕ , n=(bx2)+1)

Measurement Conditions:

- Vcc1=Vcc2=4.2 to 5.5V
- Input high and low voltage: VIH=2.5V, VIL=0.8V
- Output high and low voltage: VOH=2.0V, VOL=0.8V

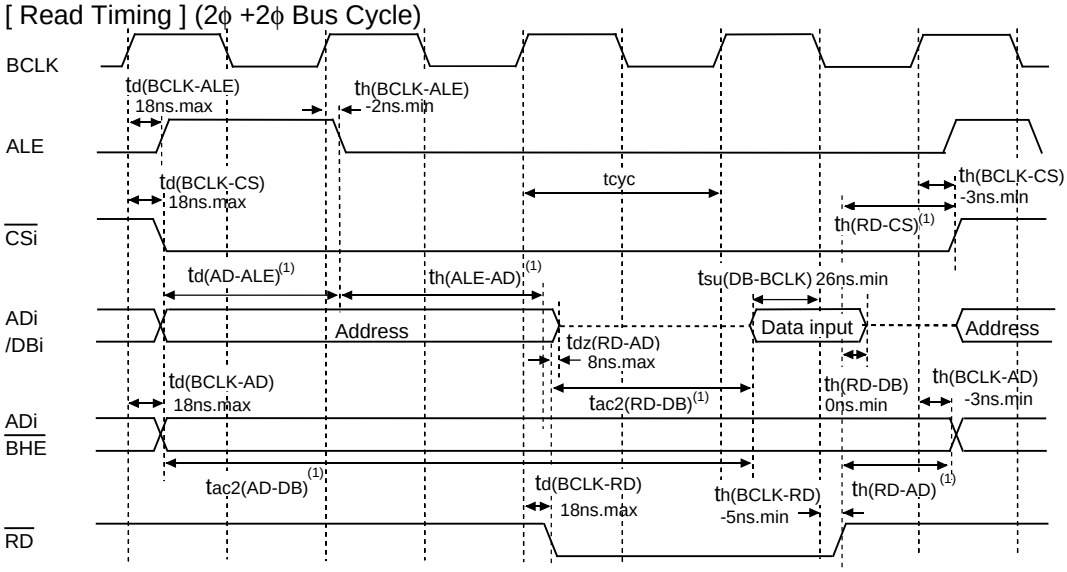
Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (1)

Vcc1=Vcc2=5V

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space with the multiplexed bus)

[Read Timing] (2ϕ +2ϕ Bus Cycle)



NOTES:

1. Varies with operation frequency:

td(AD-ALE)=(tcyc/2 x n-20)ns.min (if external bus cycle is aϕ + bϕ, n=a)

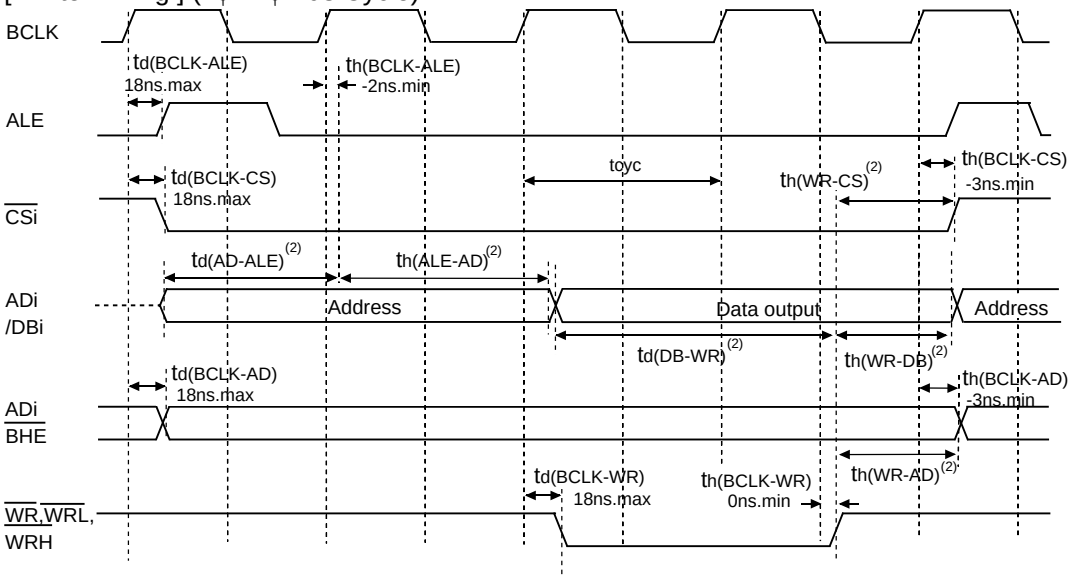
th(ALE-AD)=(tcyc x n-10)ns.min (if external bus cycle is aϕ + bϕ, n=a)

th(RD-AD)=(tcyc/2-10)ns.min, th(RD-CS)=(tcyc/2-10)ns.min

tac2(RD-DB)=(tcyc/2 x m-35)ns.max (if external bus cycle is aϕ + bϕ, m=(b x 2)+1)

tac2(AD-DB)=(tcyc/2 x p-35)ns.max (if external bus cycle is aϕ + bϕ, p={(a+b-1) x 2}-1)

[Write Timing] (2ϕ +2ϕ Bus Cycle)



NOTES:

2. Varies with operation frequency:

td(AD-ALE)=(tcyc/2 x n - 20)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

th(ALE-AD)=(tcyc x n -10)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

th(WR-AD)=(tcyc/2-10)ns.min,

th(WR-CS)=(tcyc/2-10)ns.min, th(WR-DB)=(tcyc/2-10)ns.min

td(DB-WR)=(tcyc/2 x m-25)ns.min

(if external bus cycle is aϕ + bϕ, m=(b x 2)+1)

Measurement Conditions:

- Vcc1=Vcc2=4.2 to 5.5V
- Input high and low voltage:
  VIH=2.5V, VIL=0.8V
- Output high and low voltage:
  VOH=2.0V, VOL=0.8V

Figure 5.4 Vcc1=Vcc2=5V Timing Diagram (2)

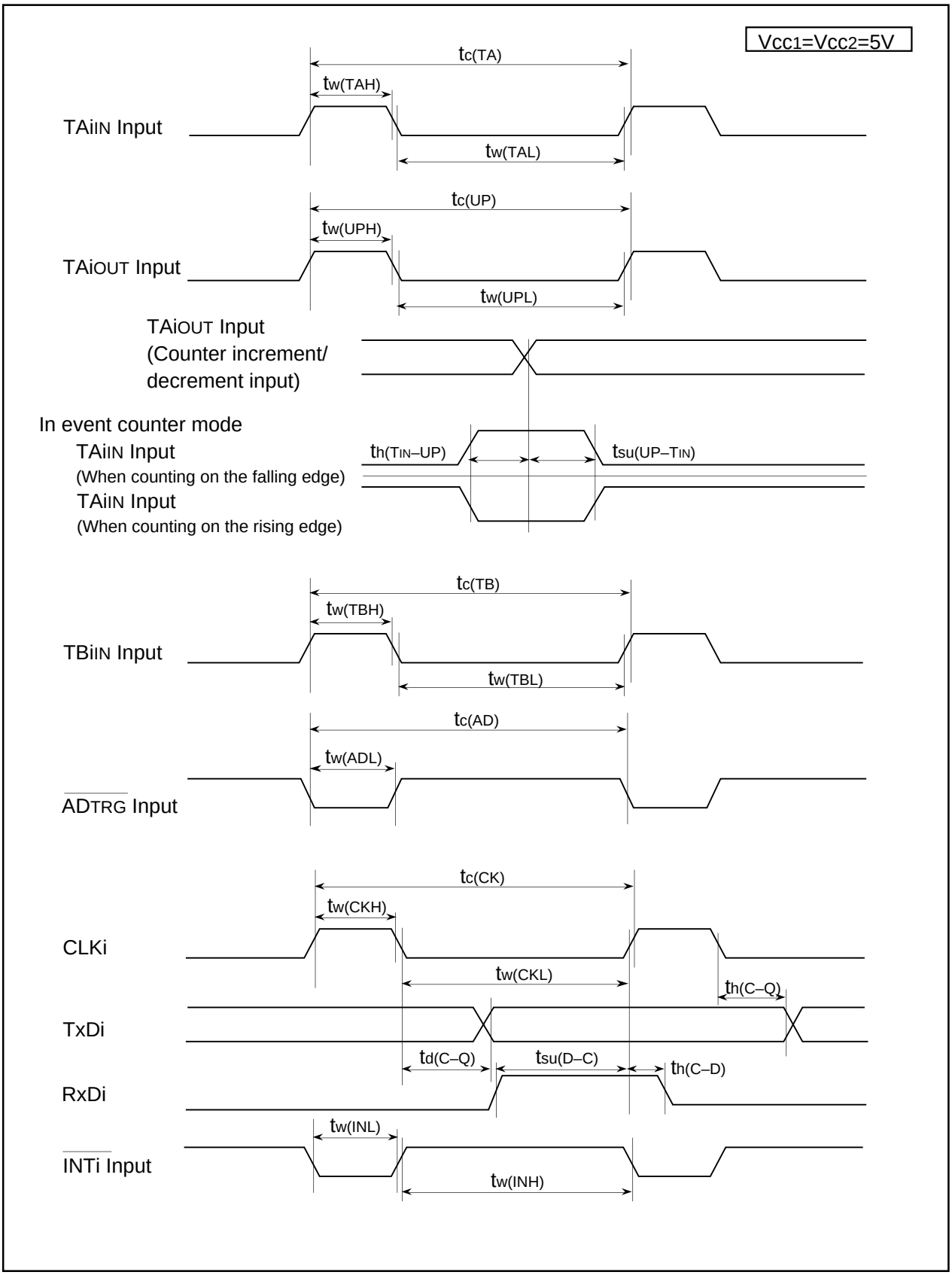
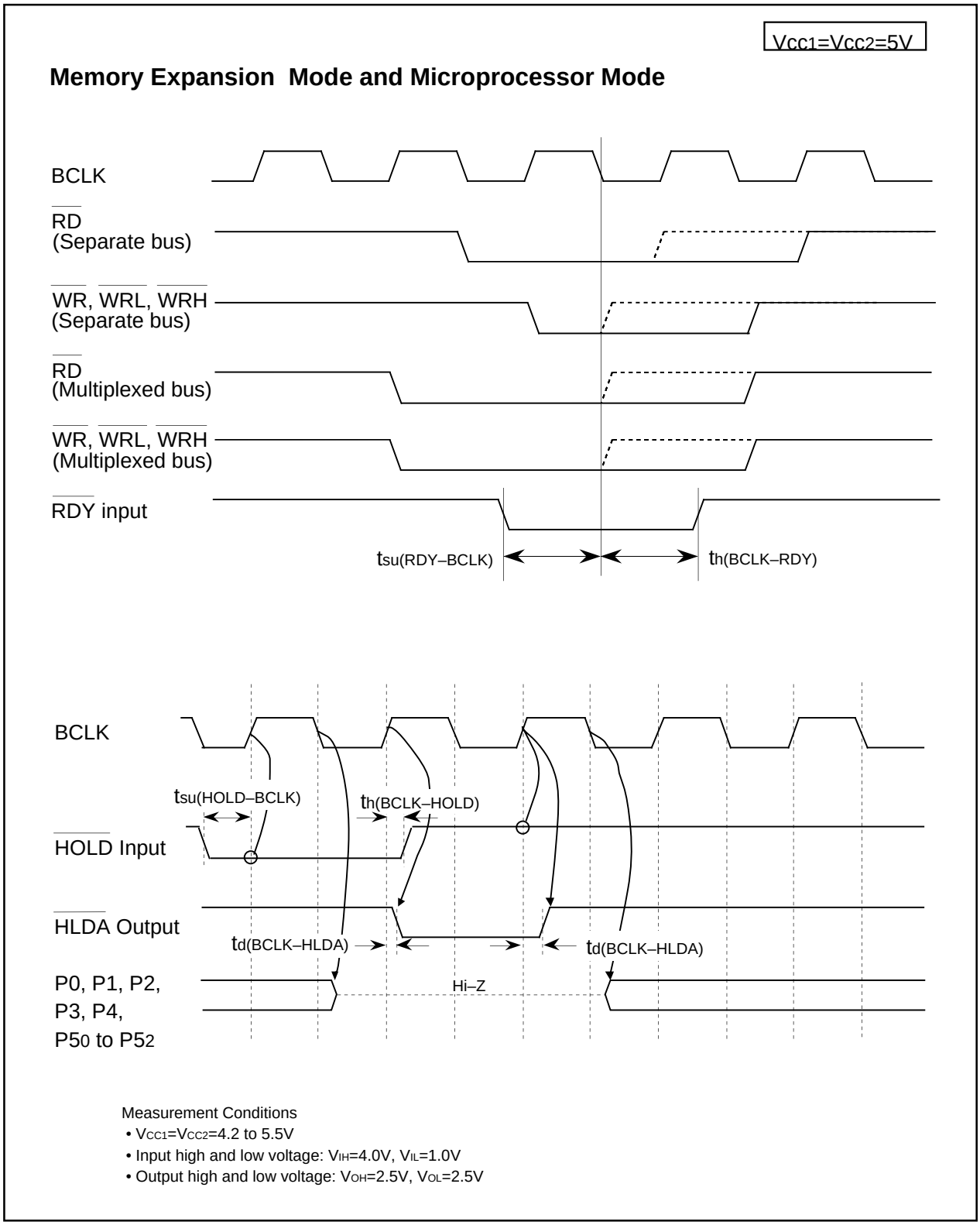


Figure 5.5 Vcc1=Vcc2=5V Timing Diagram (3)



Measurement Conditions
- $V_{CC1}=V_{CC2}$=4.2 to 5.5V
- Input high and low voltage: V_{IH}=4.0V, V_{IL}=1.0V
- Output high and low voltage: V_{OH}=2.5V, V_{OL}=2.5V

Figure 5.6 $V_{CC1}=V_{CC2}$=5V Timing Diagram (4)

$V_{CC1}=V_{CC2}=3.3V$

Table 5.24 Electrical Characteristics

($V_{CC1}=V_{CC2}$=3.0 to 3.6V, V_{SS}=0V at Topr = –20 to 85°C, f(X_{IN})=24MHz unless otherwise specified)

Symbol	Parameter			Condition		Standard			Unit
						Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$		I_{OH}=-1mA		2.7		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)				2.7		V_{CC1}	V
		X_{OUT}		I_{OH}=-0.1mA		2.7		V_{CC1}	V
		X_{COUT}	High Power	No load applied			2.5		V
			Low Power	No load applied			1.6		V
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OL}=1mA				0.5	V
		X_{OUT}		I_{OL}=0.1mA				0.5	V
		X_{COUT}	High Power	No load applied			0		V
			Low Power	No load applied			0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4				0.2		1.0	V
		$\overline{RESET}$				0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		V_I=3V				4.0	μA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		V_I=0V				-4.0	μA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		V_I=0V	Flash Memory	66	120	500	kΩ
					Masked ROM	40	70	500	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}					3.0		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}					20.0		MΩ
V_{RAM}	RAM Standby Voltage	in stop mode				2.0			V
I_{CC}	Power Supply Current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(X_{IN})=24 MHz, square wave, no division				22	35	mA
			f(X_{CIN})=32 kHz, in wait mode, Topr=25° C				10		μA
			Topr=25° C when the clock stops				0.8	5	μA
			Topr=85° C when the clock stops					50	μA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=3.3V$

Table 5.25 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}$= 3.0 to 3.6V, $V_{SS}=AV_{SS}$=0V at Topr = –20 to 85°C, f(X_{IN}) = 24MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
-	Resolution		$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	No S&H function (8-bit)	$V_{CC1}=V_{CC2}=V_{REF}$=3.3V			±2	LSB
DNL	Differential Nonlinearity Error	No S&H function (8-bit)				±1	LSB
-	Offset Error	No S&H function (8-bit)				±2	LSB
-	Gain Error	No S&H function (8-bit)				±2	LSB
R_{LADDER}	Resistor Ladder		$V_{REF}=V_{CC1}$	8		40	kΩ
t_{CONV}	8-bit Conversion Time(1, 2)			6.1			µs
V_{REF}	Reference Voltage			3.0		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

S&H: Sample and Hold

NOTES:
1. Divide f(X_{IN}), if exceeding 10 MHz, to keep ϕAD frequency at 10 MHz or less.
2. S&H function not available.

Table 5.26 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}$=3.0 to 3.6V, $V_{SS}=AV_{SS}$=0V at Topr = –20 to 85°C, f(X_{IN}) = 24MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.0	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.27 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	41		ns
$t_{w(H)}$	External Clock Input High ("H") Width	18		ns
$t_{w(L)}$	External Clock Input Low ("L") Width	18		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.28 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	30		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	40		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	60		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequecncy and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m= (b x 2)+1)

$$t_{ac1(AD-DB)} = \frac{10^9}{f_{(BCLK)}} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, n= a+b)

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)}} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, p={(a+b-1) x 2})

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS}= 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.29 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	40		ns

Table 5.30 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	200		ns

Table 5.31 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.32 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.33 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.34 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on both edges)	80		ns

Table 5.35 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Wdth	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.36 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.37 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ Input Cycle Time (required for re-trigger)	1000		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ Input Low ("L") Width	125		ns

Table 5.38 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.39 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

$V_{CC1}=V_{CC2}=3.3V$

Switching Characteristics

($V_{CC1}=V_{CC2}$=3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.40 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi,\ m=b)$$

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi,\ n=(b \times 2)-1)$$

$V_{CC1}=V_{CC2}=3.3V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.41 Memory Expansion Mode and Microprocessor Mode (when accessing an external memory space with the multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.2		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		0		ns
th(RD-AD)	Address Output Hold Time (RD standard)		(Note 1)		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-Select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
th(RD-CS)	Chip-Select Signal Output Hold Time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-AD)	RD Signal Output Hold Time		-3		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(DB-WR)	Data Output delay Time (WR standard)		(Note 2)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (BCLK standard)		-2		ns
td(AD-ALE)	ALE Signal Output Delay Time (address standard)		(Note 3)		ns
th(ALE-AD)	ALE Signal Output Hold Time (address standard)		(Note 4)		ns
tdz(RD-AD)	Address Output Float Start Time			8	ns

NOTES:

1. Values can be obtained by the following equations, according to BLCK frequency.

$$th(RD-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

2. Values can be obtained by the following equations, according to BLCK frequency and external bus cycles.

$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, m=(b+2)-1)

3. Values can be obtained by the following equations, according to BLCK frequency and external bus cycles.

$$td(AD-ALE) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n=a)

4. Values can be obtained by the following equations, according to BLCK frequency and external bus cycles.

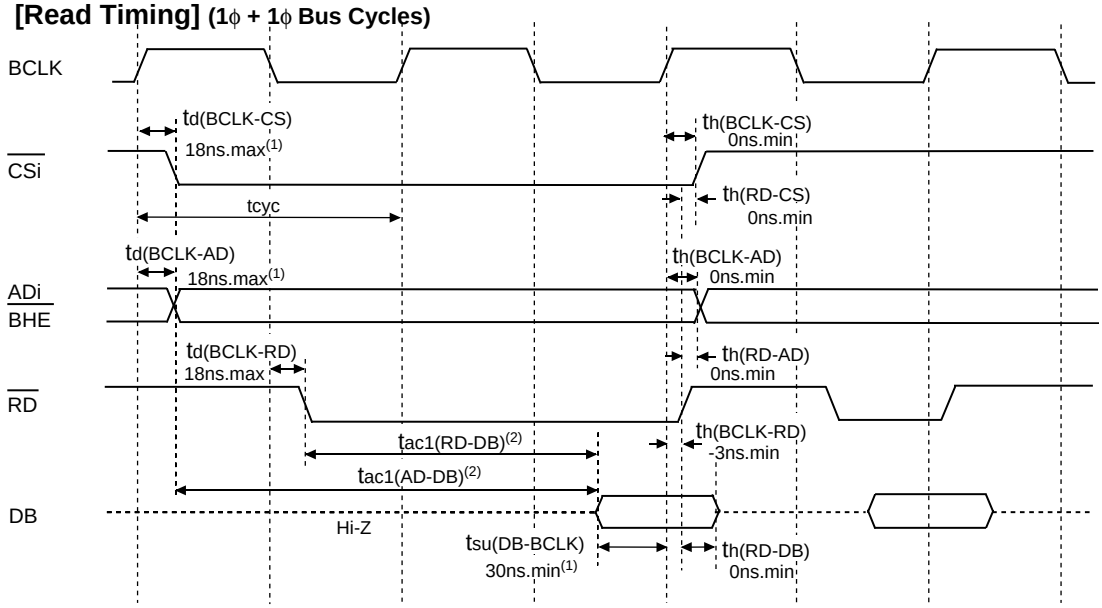
$$th(ALE-AD) = \frac{10^9 \times m}{f(BCLK) \times 2} - 10 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n=a)

Vcc1=Vcc2=3.3V

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space)

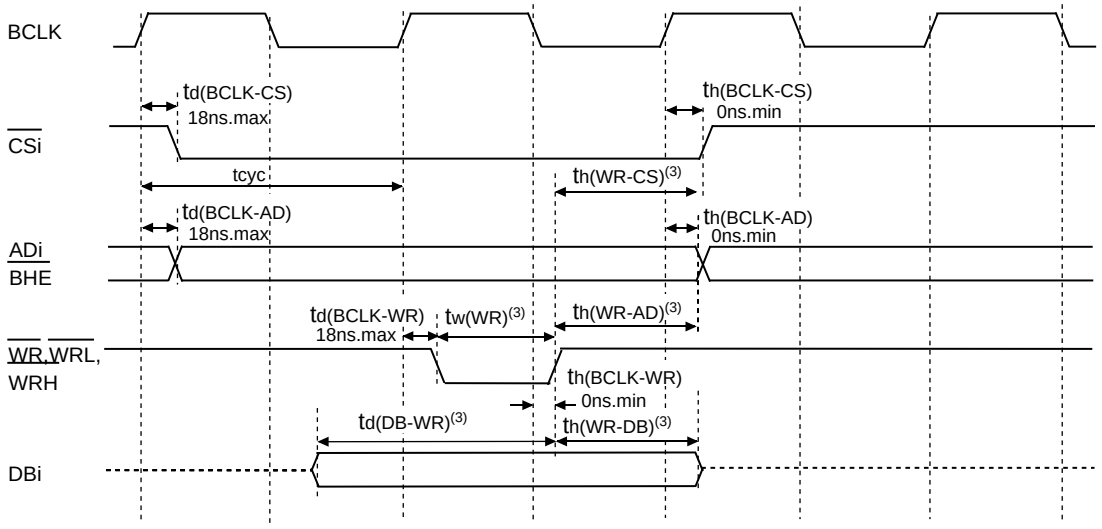
[Read Timing] (1ϕ + 1ϕ Bus Cycles)



NOTES:

1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for td(BCLK-AD)+tsu(DB-BCLK).
2. Varies with operation frequency.
   tac1(RD-DB)=(tcyc/2 x m-35)ns.max (if external bus cycle is aϕ + bϕ, m=(b x 2) + 1)
   tac1(AD-DB)=(tcyc x n-35)ns.max (if external bus cycle is aϕ + bϕ, n = a + b)

[Write Timing] (1ϕ + 1ϕ Bus Cycles)



NOTES:

3. Varies with operation frequency.
   td(DB-WR)=(tcyc x m-20)ns.min
   (if external bus cycle is aϕ + bϕ, m=b)
   th(WR-DB)=(tcyc/2-10)ns.min
   th(WR-AD)=(tcyc/2-10)ns.min
   th(WR-CS)=(tcyc/2-10)ns.min
   tw(WR)=(tcyc/2 x n-15)ns.min
   (if external bus cycle is aϕ + bϕ, n=(bx2)+1)

Measurement Conditions

- Vcc1=Vcc2=3.0 to 3.6V
- Input high and low voltage: VIH=1.5V, VIL=0.5V
- Output high and low voltage: VOH=1.5V, VOL=1.5V

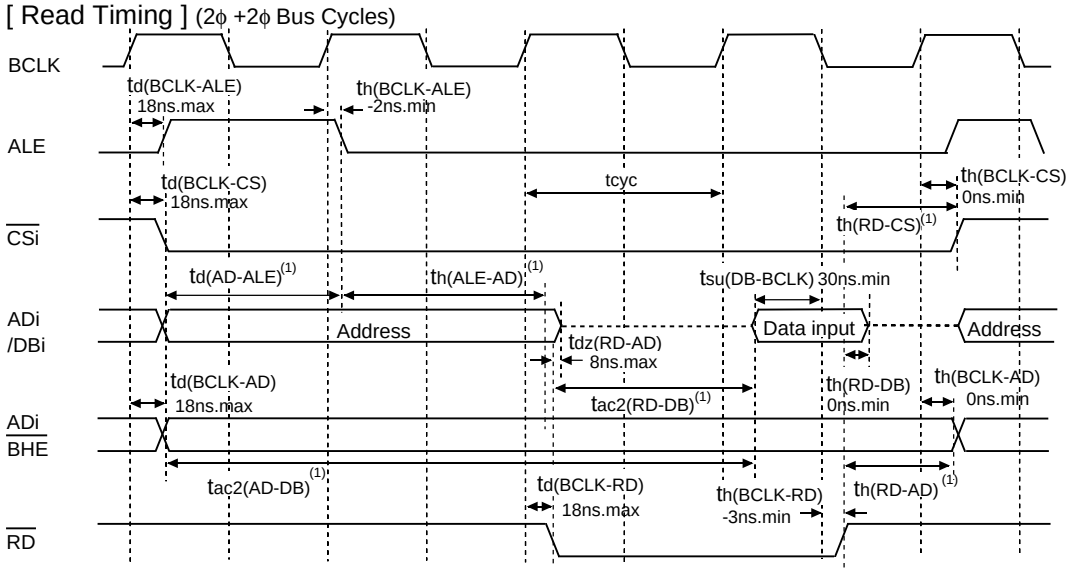
Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (1)

Memory Expansion Mode and Microprocessor Mode

Vcc1=Vcc2=3.3V

(when accessing external memory space and using the multiplexed bus)

[Read Timing] (2ϕ +2ϕ Bus Cycles)



NOTES:

1. Varies with operation frequency:

td(AD-ALE)=(tcyc/2 x n-20)ns.min (if external bus cycle is aϕ + bϕ, n=a)

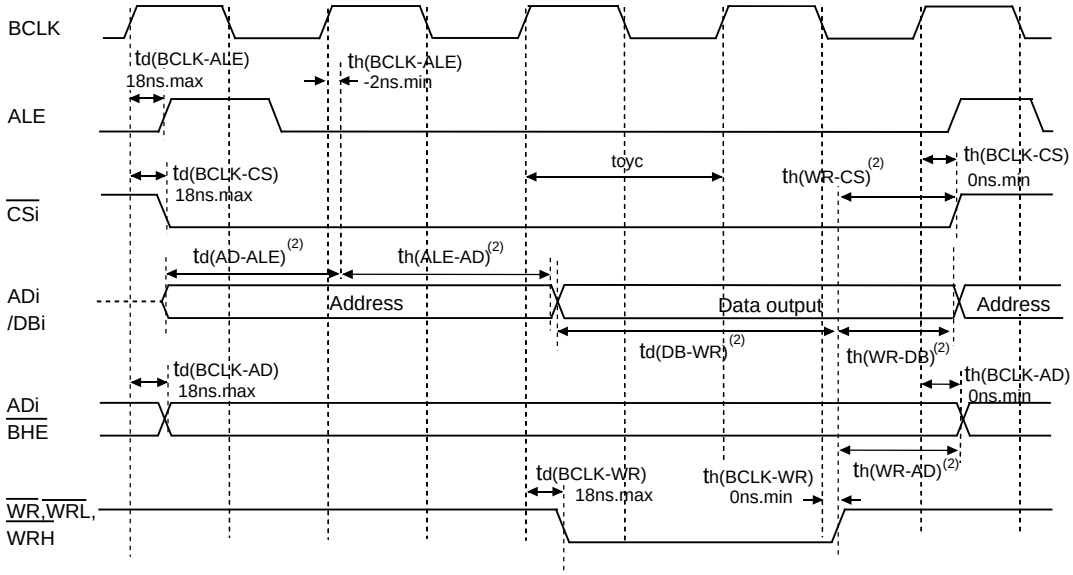
th(ALE-AD)=(tcyc x n-10)ns.min (if external bus cycle is aϕ + bϕ, n=a)

th(RD-AD)=(tcyc/2-10)ns.min, th(RD-CS)=(tcyc/2-10)ns.min

tac2(RD-DB)=(tcyc/2 x m-35)ns.max (if external bus cycle is aϕ + bϕ, m=(b x 2)+1)

tac2(AD-DB)=(tcyc/2 x p-35)ns.max (if external bus cycle is aϕ + bϕ, p={(a+b-1) x 2}-1)

[Write Timing] (2ϕ +2ϕ Bus Cycles)



NOTES:

2. Varies with operation frequency:

td(AD-ALE)=(tcyc/2 x n - 20)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

th(ALE-AD)=(tcyc x n -10)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

th(WR-AD)=(tcyc/2-10)ns.min,

th(WR-CS)=(tcyc/2-10)ns.min, th(WR-DB)=(tcyc/2-10)ns.min

td(DB-WR)=(tcyc/2 x m-25)ns.min

(if external bus cycle is aϕ + bϕ, m=(b x 2)+1)

Measurement Conditions:

- Vcc1=Vcc2=3.0 to 3.6V
- Input high and low voltage:
  VIH=1.5V, VIL=0.5V
- Output high and low voltage:
  VOH=1.5V, VOL=1.5V

Figure 5.8 Vcc1=Vcc2=3.3V Timing Diagram (2)

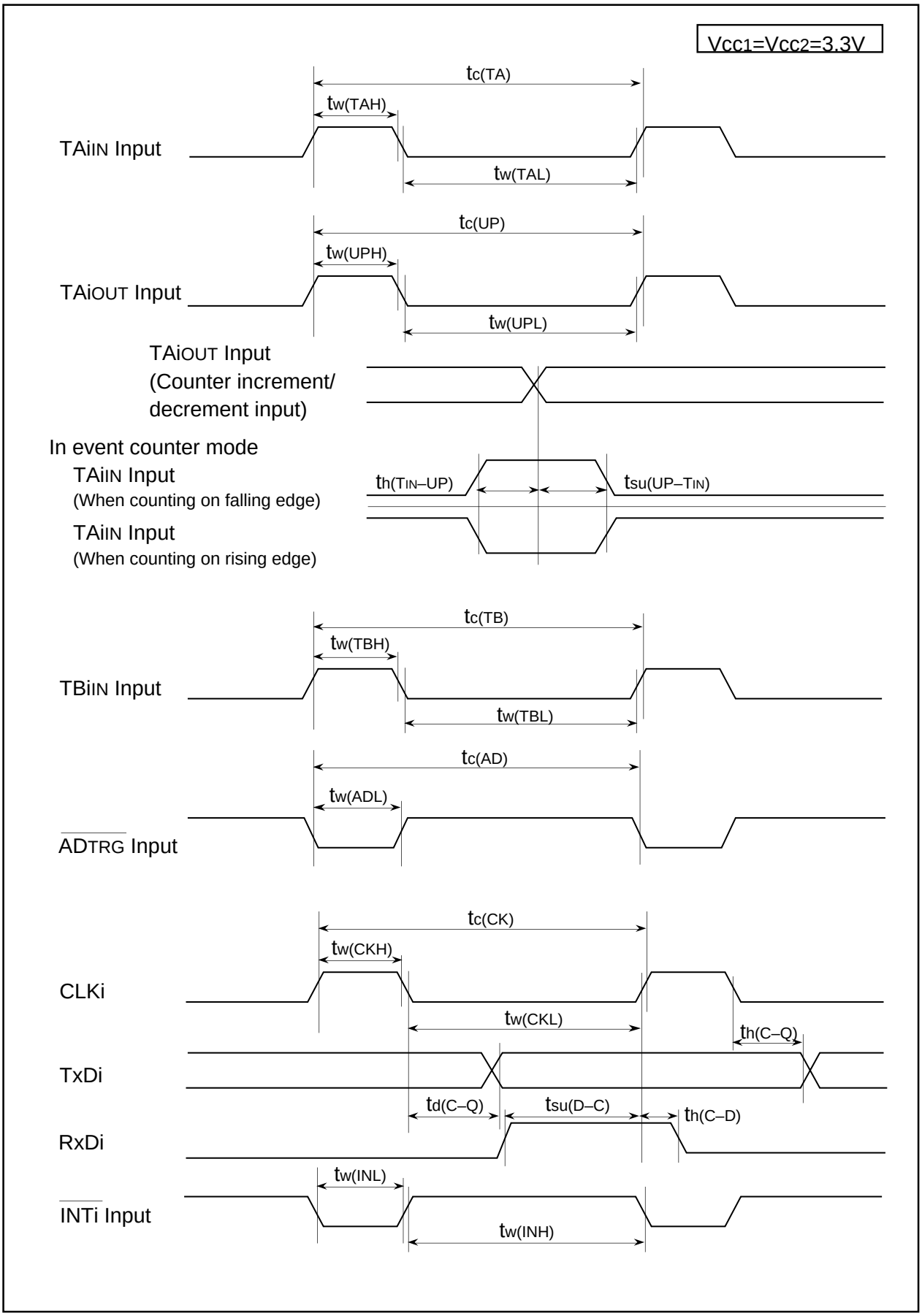


Figure 5.9 Vcc1=Vcc2=3.3V Timing Diagram (3)

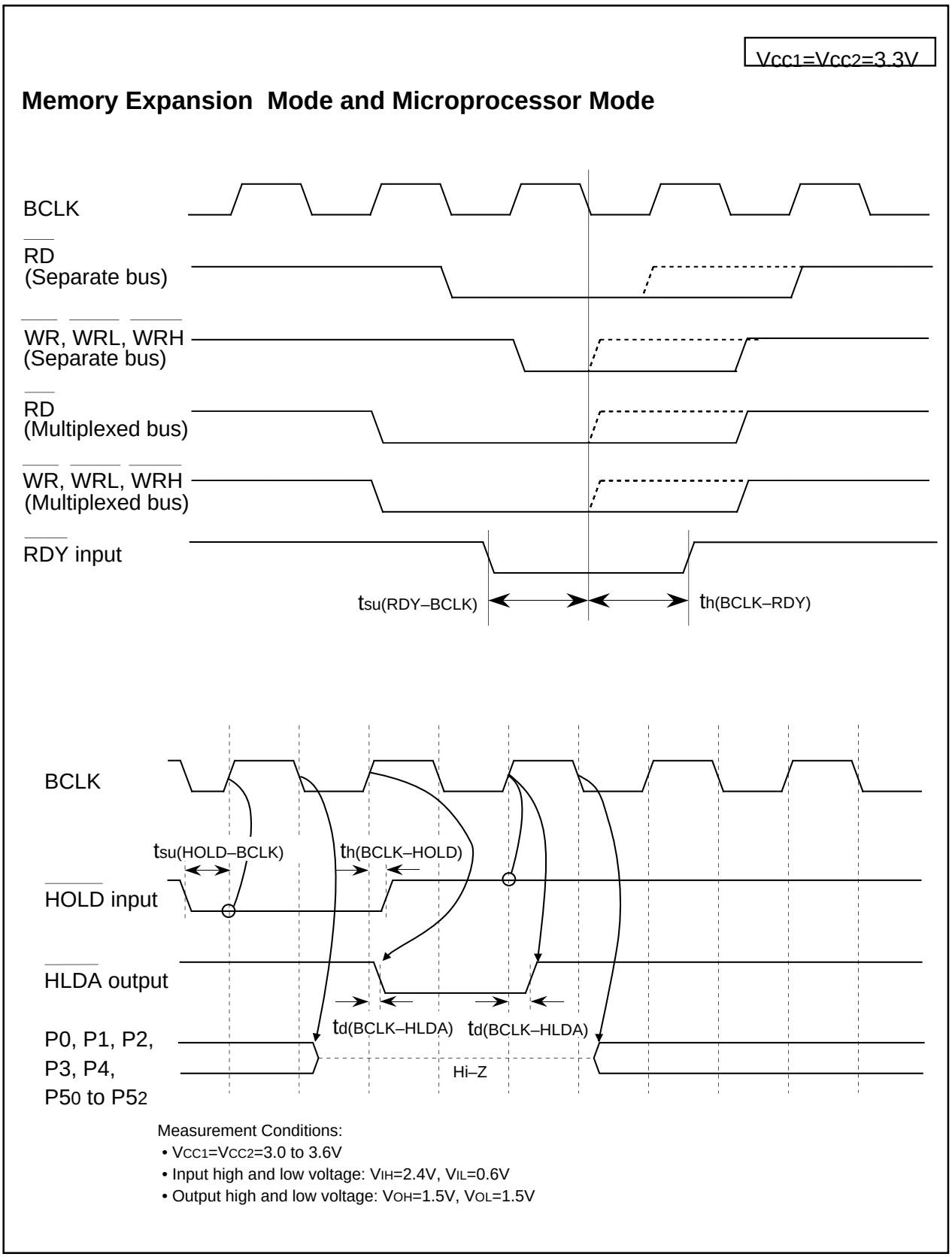


Figure 5.10 Vcc1=Vcc2=3.3V Timing Diagram (4)

5.2 Electrical Characteristics (M32C/84T)

Table 5.42 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V_{CC1}, V_{CC2}	Supply Voltage		V_{CC1}=V_{CC2}=AV_{CC}	-0.3 to 6.0	V
AV_{CC}	Analog Supply Voltage		V_{CC1}=V_{CC2}=AV_{CC}	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNV_{SS}, BYTE, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), V_{REF}, X_{IN}		-0.3 to V_{CC1}+0.3	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(1)		-0.3 to V_{CC2}+0.3	
		$P7_0$, $P7_1$		-0.3 to 6.0	
V_O	Output Voltage	$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{OUT}		-0.3 to V_{CC1}+0.3	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(1)		-0.3 to V_{CC2}+0.3	
Pd	Power Dissipation		Topr=25° C	500	mW
Topr	Operating Ambient Temperature	during CPU operation	T version	-40 to 85	° C
		during flash memory program and erase operation		0 to 60	
Tstg	Storage Temperature			-65 to 150	° C

NOTES:
1. P11 to P15 are provided in the 144-pin package only.

Table 5.43 Recommended Operating Conditions

(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr= -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply Voltage (V_{CC1}=V_{CC2})	4.2	5.0	5.5	V
AV_{CC}	Analog Supply Voltage		V_{CC1}		V
V_{SS}	Supply Voltage		0		V
AV_{SS}	Analog Supply Voltage		0		V

Table 5.43 Recommended Operating Conditions (Continued)

(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter	Accommodating Pins	Standard			Unit
			Min.	Typ.	Max.	
V_{IH}	Input High ("H") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0.8V_{CC2}		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0.8V_{CC1}		V_{CC1}	
		$P7_0$, $P7_1$	0.8V_{CC1}		6.0	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$	0.8V_{CC2}		V_{CC2}	V
V_{IL}	Input Low ("L") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0		0.2V_{CC2}	V
		$P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE			0.2V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$	0		0.2V_{CC2}	V
$I_{OH(peak)}$	Peak Output High ("H") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			5.0	mA

NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, and P11 must be -40mA or less.
   Total $I_{OH(peak)}$ for $P8_6$, $P8_7$, P9, P10, P14 and P15 must be -40mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P12 and P13 must be -40mA or less.
   Total $I_{OH(peak)}$ for P6, P7, and $P8_0$ to $P8_4$ must be -40mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply when $P8_7$ is used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

Table 5.43 Recommended Operating Conditions (Continued)

(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f(X_{IN})$	Main Clock Input Frequency	V_{CC1}=4.2 to 5.5V	0		32	MHz
$f(X_{CIN})$	Sub Clock Frequency			32.768	50	kHz
$f(_{Ring})$	On-chip Oscillator Frequency			1		MHz
$f(_{PLL})$	PLL Clock Frequency	V_{CC1}=4.2 to 5.5V	10		32	MHz
$t_{SU(PLL)}$	PLL Lock Time	V_{CC1}=5.0V			5	ms

$V_{CC1}=V_{CC2}=5V$

Table 5.44 Electrical Characteristics
($V_{CC1}=V_{CC2}$=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version), f(X_{IN})=32MHz unless otherwise specified)

Symbol	Parameter			Measurement Condition		Standard Min.	Standard Typ.	Standard Max.	Unit
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$		I_{OH}=-5mA		3.0		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OH}=-5mA		3.0		V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$		I_{OH}=-200μA		4.7		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$,$P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OH}=-200μA		4.7		V_{CC1}	
		X_{OUT}		I_{OH}=-1mA		3.0			V
		X_{COUT}	High Power	No load applied			2.5		V
			Low Power	No load applied			1.6		
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OL}=5mA				2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OL}=200μA				0.45	V
		X_{OUT}		I_{OL}=1mA				2.0	V
		X_{COUT}	High Power	No load applied			0		V
			Low Power	No load applied			0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{AD_{TRG}}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4				0.2		1.0	V
		$\overline{RESET}$				0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		V_I=5V				5.0	μA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		V_I=0V				-5.0	μA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		V_I=0V	Flash Memory	30	50	167	kΩ
					Masked ROM	20	40	167	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}					1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}					10		MΩ
V_{RAM}	RAM Standby Voltage	in stop mode				2.0			V
I_{CC}	Power Supply Current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(X_{IN})=32 MHz, square wave, no division				28	50	mA
			f(X_{CIN})=32 kHz, in wait mode, Topr=25° C				10		μA
			Topr=25° C (while clock is stopped)				0.8	5	μA
			Topr=85° C (while clock is stopped)					50	μA

NOTES:
1. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=5V$

Table 5.45 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}$=4.2 to 5.5V, V_{SS}=0V at Topr= -40 to 85°C (T version), f(X_{IN})=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}$=5V	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, AN_{EX0}, AN_{EX1}			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8.00		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2.00		V_{CC1}	V
V_{IA}	Analog Input Voltage			0.00		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. Sample and Hold function is available.

Table 5.46 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}$=4.2 to 5.5V, V_{SS}=0V at Topr= -40 to 85°C (T version), f(X_{IN})=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Table 5.47 Flash Memory Version Electrical Characteristics(1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and Erase Endurance(3)		100			cycles
-	Word Program Time (V_{CC1}=5.0V,Topr=25° C)			25	200	µs
-	Lock Bit Program Time			25	200	µs
-	Block Erase Time (V_{CC1}=5.0V,Topr=25° C)	4-Kbyte Block		0.3	4	s
		8-Kbyte Block		0.3	4	s
		32-Kbyte Block		0.5	4	s
		64-Kbyte Block		0.8	4	s
-	All-Unlocked-Block Erase Time(2)				4 x *n*	s
t_{PS}	Flash Memory Circuit Stabilization Wait Time				15	µs
-	Data Hold Time(4)		10			years

NOTES:
1. Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at Topr = 0 to 60 ° C unless otherwise specified.
2. n denotes the number of block to be erased.
3. Number of program-erase cycles per block.
   If Program and Erase Endurance is *n* cycle (*n*=100), each block can be erased and programmed *n* cycles.
   For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (Rewrite prohibited).
4. Topr = -40 to 85 ° C

$V_{CC1}=V_{CC2}=5V$

Table 5.48 Power Supply Timing

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time for Stable Internal Supply Voltage when Power-on	V_{CC1}=3.0 to 5.5V			2	ms

td(P-R)
Wait Time for Stable Internal Supply Voltage when Power-on

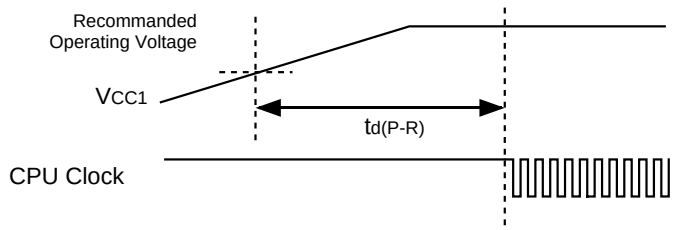


Figure 5.11 Power Supply Timing Diagram

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version) unless otherwise specified)

Table 5.49 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$tw_{(H)}$	External Clock Input High ("H") Width	13.75		ns
$tw_{(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}$=4.2 to 5.5V, V_{SS}=0V at Topr= -40 to 85°C (T version) unless otherwise specified)

Table 5.50 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	40		ns

Table 5.51 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	200		ns

Table 5.52 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.53 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.54 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}$=4.2 to 5.5V, V_{SS}=0V at Topr= -40 to 85°C (T version) unless otherwise specified)

Table 5.55 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on both edges)	80		ns

Table 5.56 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.57 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.58 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ Input Cycle Time (required for re-trigger)	1000		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ Input Low ("L") Pulse Width	125		ns

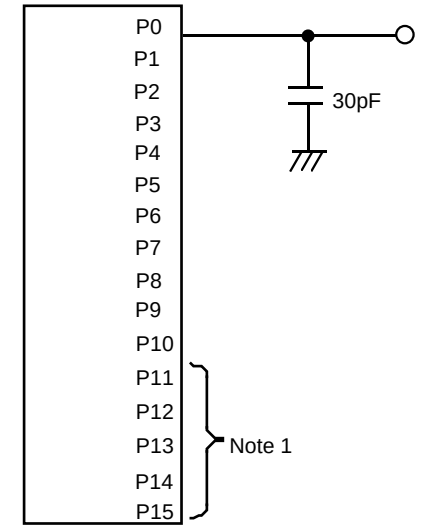
Table 5.59 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.60 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

$V_{CC1}=V_{CC2}=5V$



NOTES:
1. P11 to P15 are provided in the 144-pin package only.

Figure 5.12 P0 to P15 Measurement Circuit

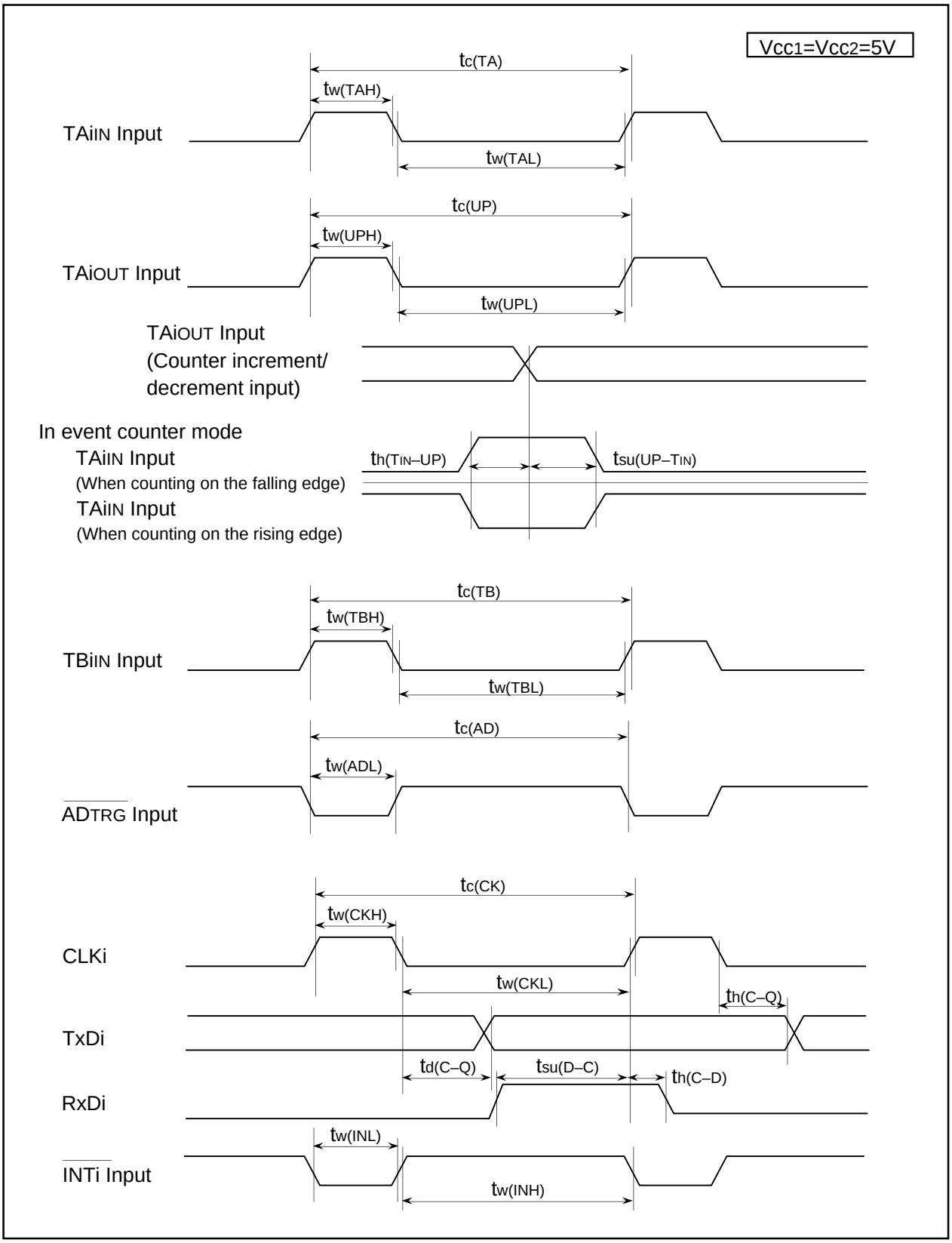


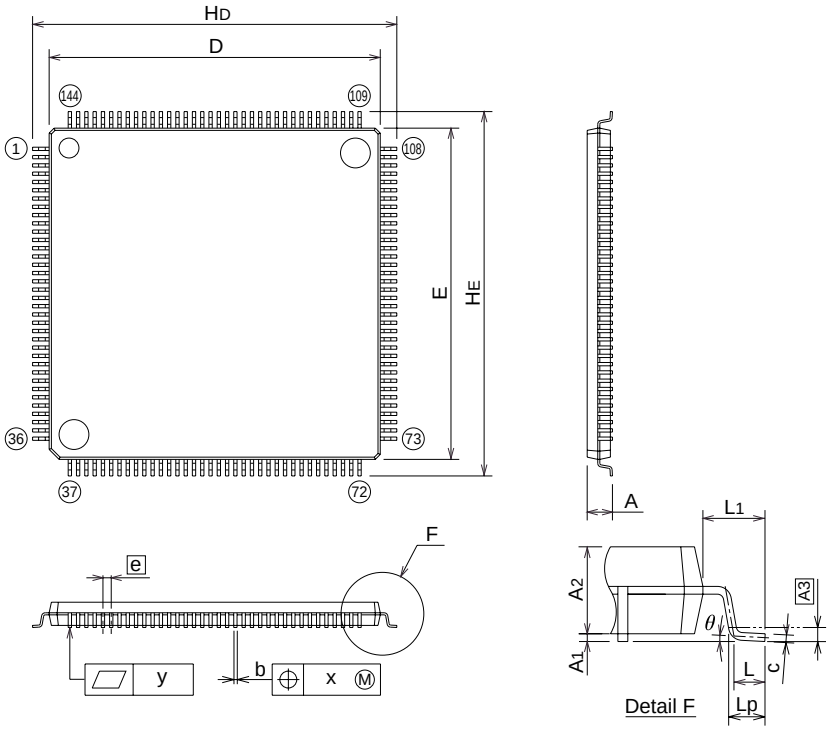
Figure 5.13 Vcc1=Vcc2=5V Timing Diagram

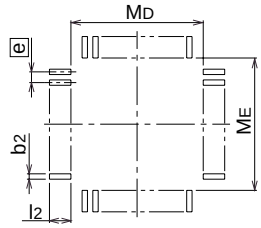
Package Dimensions

144P6Q-A Recommended

Plastic 144pin 20×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP144-P-2020-0.50	–	1.23	Cu Alloy





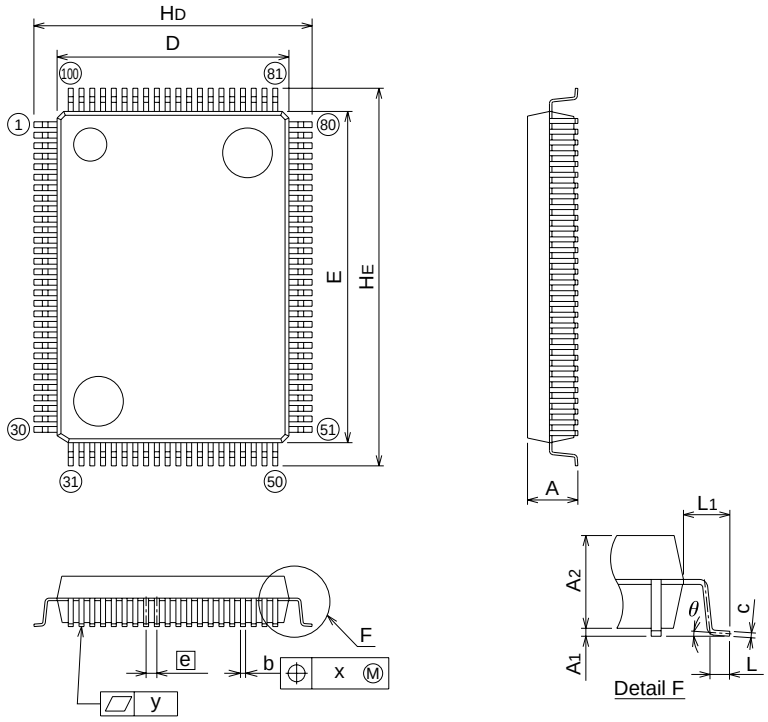
Recommended Mount Pad

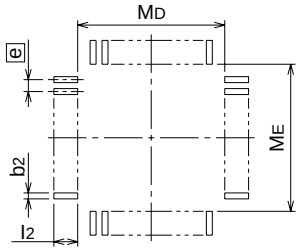
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0.05	0.125	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	–	0.5	–
HD	21.8	22.0	22.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
l2	0.95	–	–
MD	–	20.4	–
ME	–	20.4	–

100P6S-A Recommended

Plastic 100pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	–	1.58	Alloy 42





Recommended Mount Pad

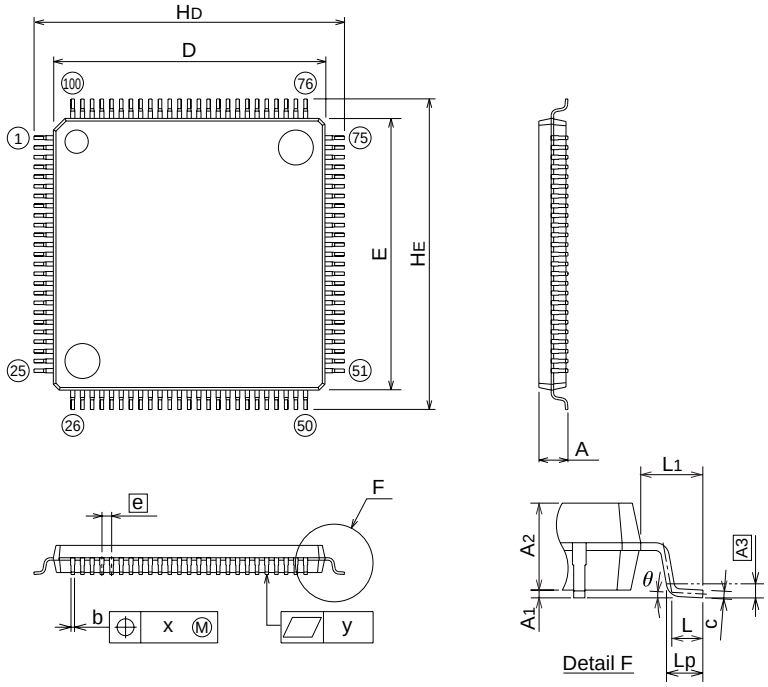
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	–	1.4	–
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b2	–	0.35	–
l2	1.3	–	–
MD	–	14.6	–
ME	–	20.6	–

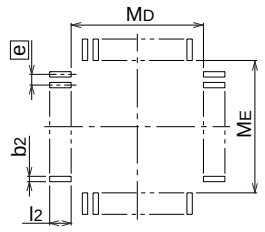
100P6Q-A

Recommended

Plastic 100pin 14×14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	–	0.63	Cu Alloy





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
L	0.3	0.5	0.7
L_1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
l_2	0.9	–	–
M_D	–	14.4	–
M_E	–	14.4	–

REVISION HISTORY	M32C/84 Group (M32C/84, M32C/84T) Data Sheet

Rev.	Date	Description	
		Page	Summary
0.40	Sep. 30, 2003	–	New Document
0.50	Feb. 05, 2004		**Overview**
		2, 3	• **Table 1.1** and **Table 1.2 M32C/84 Group Performance** Values for Shortest Instruction Execution Time and Power Consumption" modified
		5	• **Figure 1.2 ROM/RAM Capacity** Products added
			• **Table 1.3 M32C/84 Group** Products added
		6	• **Figure 1.3 Product Numbering System** 128-Kbytes added to ROM capacity Memory
		23	• **Figure 3.1 Memory Map** Diagram modified; products added
			SFR
		24	• "Values after RESET" for the PM1, PM2, D4INT, G0IRF, G1IRF, IDB0 to IDB1, TA0MR to TA4MR, TCSPR, DM0SL to DM3SL registers revised
			• The IPSA register added to address 0179_{16}
			• NOTES added to the PM0 and TCSPR register
			Electrical Characteristics
		44	• Newly added
0.51	Feb. 09, 2004		**Electrical Characteristics**
		50	• **Table 5.6 Flash Memory Version Electrical Characteristics** Note 4 revised
		57	• **Figure 5.2 V_{CC1}=V_{CC2}=5V Timing Diagram (1)** Notes 1 and 2 revised
		68	• **Figure 5.3 V_{CC1}=V_{CC2}=5V Timing Diagram (2)** Notes 1, 2, and 3 revised
		68	• **Figure 5.6 V_{CC1}=V_{CC2}=3.3V Timing Diagram (1)** Notes 1, 2, and 3 revised
		69	• **Figure 5.7 V_{CC1}=V_{CC2}=3.3V Timing Diagram (2)** Notes 1 and 2 revised
0.52	Mar.12, 2004		**Overview**
		2, 3	•**Table 1.1 and 1.2 M32C/84 Group Performance** Values for Power Consumption modified
			Electrical Characteristics
		48	• **Table 5.3 Electrical Characteristics** Maximum values for Power Supply Current modified
		50	• **Table 5.6 Flash Memory Version Electrical Characteristics** Note 1. 100-cycle Products (D3, D5, U3, U5) deleted; Note 4 modified
			• **Table 5.7 Flash Memory Version Program and Erase Voltage and Read Operation Voltage Characteristics (at Topr=0 to 60°C)** deleted
		61	• **Table 5.22 Electrical Characteristics** Maximum values for Power Supply Consumption modified and standard values when "Topr=85°C while clock is stopped" deleted

REVISION HISTORY	M32C/84 Group (M32C/84, M32C/84T) Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Jun.01, 2004	-	**M32C/84T (High-reliability version)** added
		All Pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
			Overview
		1	• **1.1 Applications** Automobiles added
		2, 3	• **Table 1.1** and **Table 1.2 M32C/84 Group (M32C/84, M32C/84T) Performance** M32C/84T added; note 3 added
		4	• **Figure 1.1 M32C/84 Group (M32C/84, M32C/84T) Block Diagram** Note 3 added
		5	• **1.4 Product Information** Description modified
			• **Figure 1.2 ROM/RAM Capacity** figure modified
		6	• **Table 1.3 M32C/84 Group** M32C/84T added
		6	• **Figure 1.3 Product Numbering System** M32C/84T added
		7	• **Figure 1.4 Pin Assignment for 144-Pin Package** Note 3 added
		12	• **Figure 1.6 Pin Assignment for 100-Pin Pacakage** Note 5 added
		8 to 10	• **Table 1.5 Pin Characteristics for 144-Pin Package** Note 1 added
		13, 14	• **Table 1.6 Pin Characteristics for 100-Pin Package** Note 1 added
		15 to 18	• **Table 1.7 Pin Description** Notes added
			Memory
		22	• **Figure 3.1 Memory Map** Tables of internal ROM/internal RAM modified; note 2 modified; notes 4 and 5 added
			SFR
		23	• Note 2 added
		24	• PWCR0 and PWCR1 registers deleted
			• “Values after RESET” of the masked ROM version added to the FMR0 register
			• Note 1 added
			Electrical Characteristics
		44	• **Table 5.2 Recommended Operating Conditions** $f_{(ripple)}$, $V_{p-p(ripple)}$, V_{CC}, SV_{CC} and note 1 deleted
		47	• **Table 5.3 Electrical Characteristics** R_{PULLUP} value for the masked ROM version added
		48	• **Table 5.4 A/D Conversion Characteristics** t_{SMP} value modified; note 1 added
		50	• **Table 5.7 Low Voltage Detect Circuit Electrical Characteristics** added
			• **Table 5.8 Power Supply Timing** added
			• **Figure 5.1 Power Supply Timing Diagram** added
		55	• **Table 5.23 Memory Expassion Mode and Microprocessor Mode** $t_{h(BCLK-ALE)}$ value modified
		61	• **Table 5.24 Electrical Characteristics** R_{PULLUP} value for the masked ROM version added
		62	• **Table 5.25 A/D Conversion Characteristics** t_{CONV} value modified

Rev.	Date	Description	
		Page	Summary
		63	• **Table 5.28 Memory Expassion Mode and Microprocessor Mode** tsu(DB-BCLK), tsu(RDY-BCLK) and tsu(HOLD-BCLK) value modified
		66	• **Table 5.40 Memory Expassion Mode and Microprocessor Mode** equetion of th(WR-DB) modified
		67	• **Table 5.41 Memory Expassion Mode and Microprocessor Mode** th(BCLK-ALE) value modified; equetion of th(WR-DB) modified
		72	• **5.2 Electrical Characteristics (M32C/84T)** added
1.10	Jun.28, 2004	-	**High-reliability version (U version)** deleted
			Overview
		5	• **Table 1.3 M32C/84 Group (1) (2)** development status modified
		6	• **Figure 1.2 Product Numbering System** figure modified

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Colophon .1.0