

## 1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

The data flash ROM (2 KB X 2 blocks) is embedded.

### 1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

## 1.2 Performance Outline

Table 1.1. lists the performance outline of this MCU.

**Table 1.1 Performance outline**

Item		Performance
CPU	Number of basic instructions	89 instructions
	Shortest instruction execution time	62.5 ns ( $f(XIN) = 16$ MHz, $VCC = 3.0$ to $5.5$ V) 100 ns ( $f(XIN) = 10$ MHz, $VCC = 2.7$ to $5.5$ V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2 "Product List"
Peripheral function	Interrupt	Internal: 10 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels
	Watchdog timer	15 bits x 1 (with prescaler) Reset start function selectable
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel Input capture circuit
	Serial I/O	•1 channel Clock synchronous, UART •1 channel UART
	A-D converter	10-bit A-D converter: 1 circuit, 8 channels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •Ring oscillator
	Oscillation stop detection function	Stop detection of main clock oscillation
	Port	Input/Output: 22 (including LED drive port), Input: 2 (LED drive I/O port: 8, max. 20 mA)
Electrical characteristics	Power supply voltage	$VCC = 3.0$ to $5.5$ V ( $f(XIN) = 16$ MHz) $VCC = 2.7$ to $5.5$ V ( $f(XIN) = 10$ MHz)
	Power consumption	Typ. 8 mA ( $VCC = 5.0$ V, ( $f(XIN) = 16$ MHz, High-speed mode) Typ. 5 mA ( $VCC = 3.0$ V, ( $f(XIN) = 10$ MHz, High-speed mode) TBD ( $VCC = 3.0$ V, Wait mode) Typ. 0.7 $\mu$ A ( $VCC = 3.0$ V, Stop mode)
Flash memory	Program/erase voltage	$VCC = 2.7$ to $5.5$ V
	Number of program/erase	10000 times (Data area) 100 times (Program area)
Operating ambient temperature		-20 to 85 °C -40 to 85 °C (option)
Package		32-pin plastic mold LQFP

If you require this option, please specify so.

### 1.3 Block Diagram

Figure 1.1. shows this MCU block diagram.

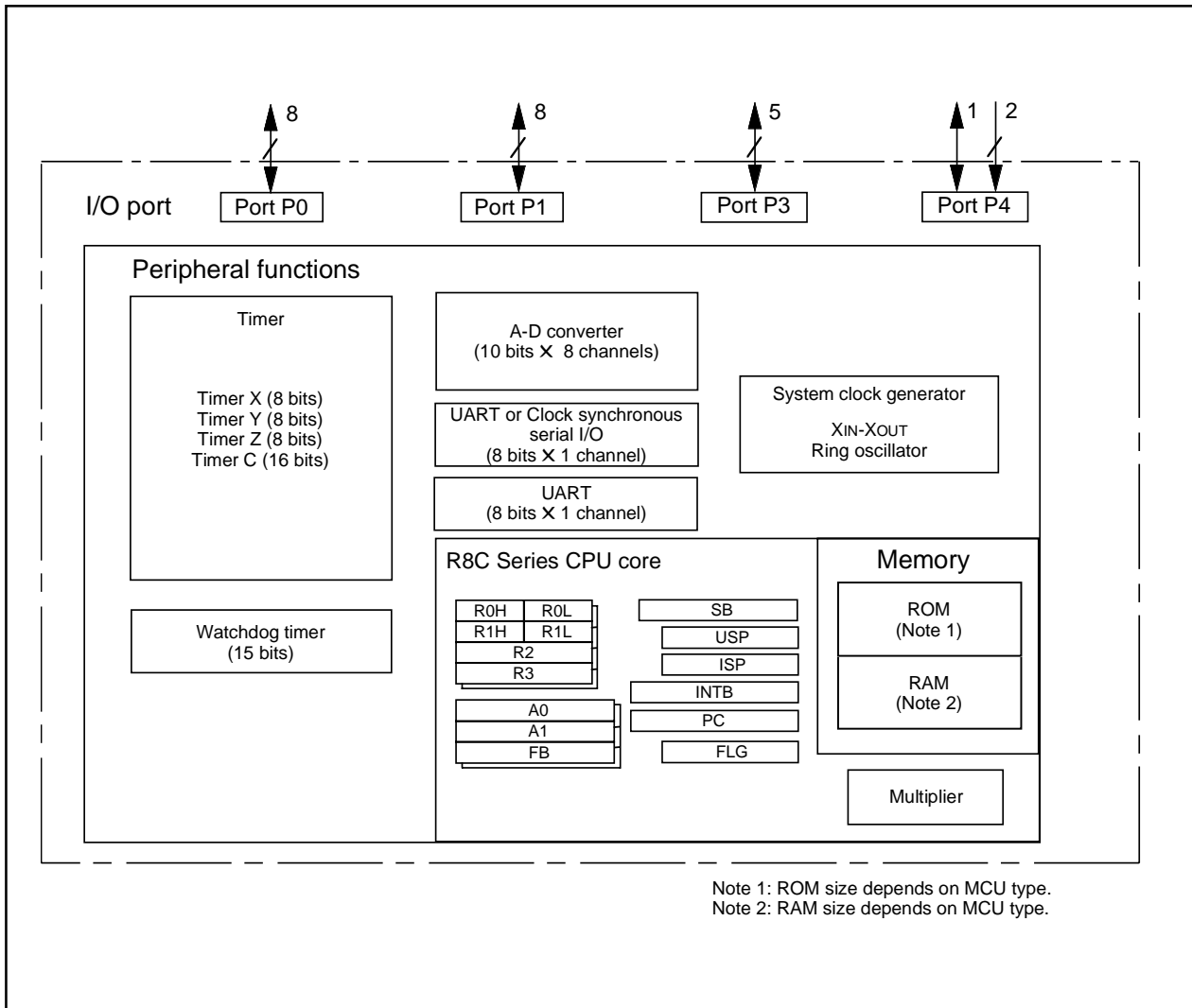


Figure 1.1 Block Diagram

## 1.4 Product Information

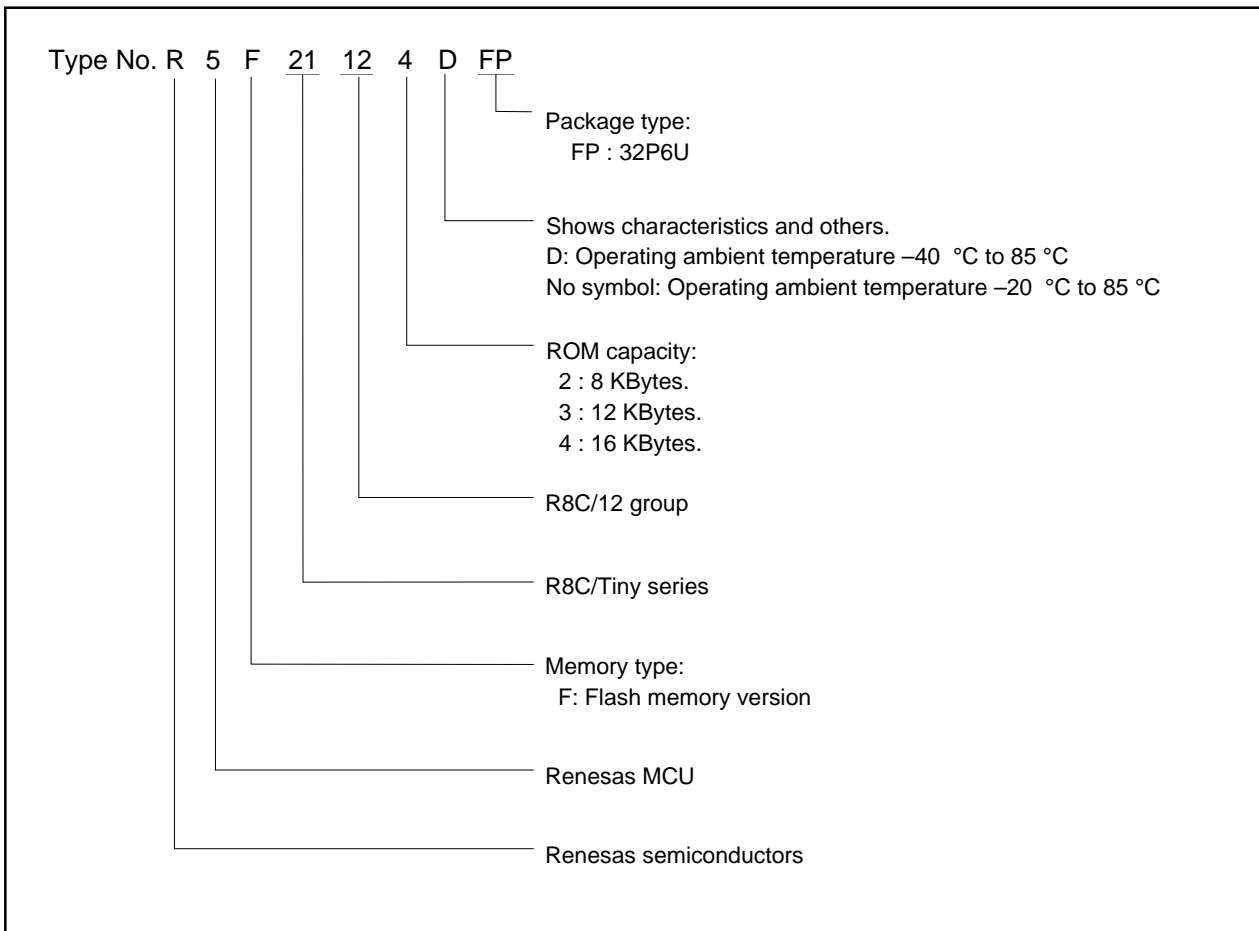
Table 1.2 lists the products.

**Table 1.2 Product List**

As of October 2003

Type No.	ROM capacity		RAM capacity	Package type	Remarks
	Program area	Data area			
R5F21122FP **	8K bytes	2K bytes x 2	512 bytes	32P6U-A	Flash memory version
R5F21123FP **	12K bytes	2K bytes x 2	768 bytes	32P6U-A	
R5F21124FP **	16K bytes	2K bytes x 2	1K bytes	32P6U-A	
R5F21122DFP **	8K bytes	2K bytes x 2	512 bytes	32P6U-A	D version
R5F21123DFP **	12K bytes	2K bytes x 2	768 bytes	32P6U-A	
R5F21124DFP **	16K bytes	2K bytes x 2	1K bytes	32P6U-A	

\*\* : Under development



**Figure 1.2 Type No., Memory Size, and Package**

## 1.5 Pin Configuration

Figure 1.3 shows the pin configuration (top view).

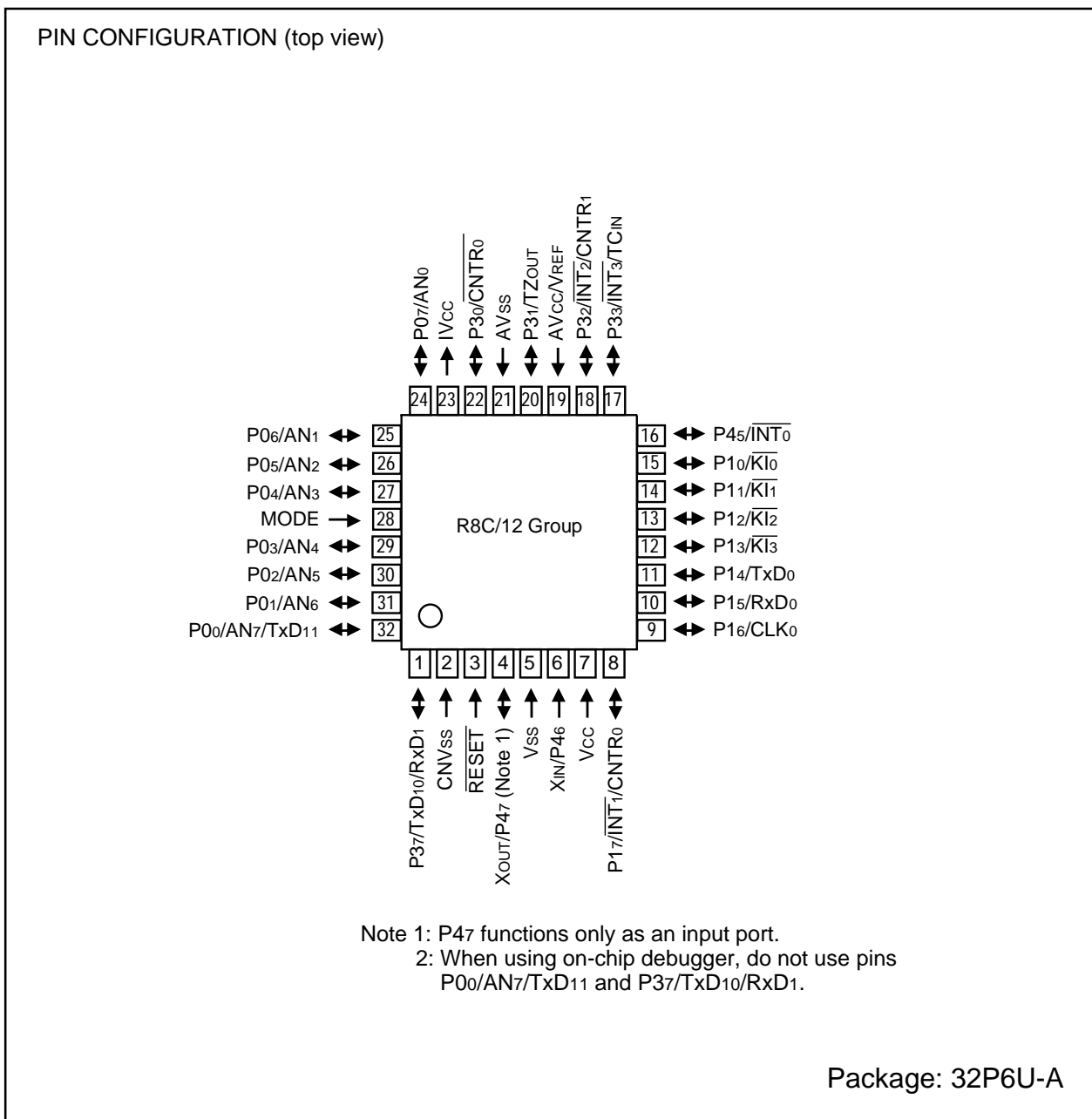


Figure 1.3 Pin Configuration (Top View)

- Note 1: P47 functions only as an input port.  
 Note 2: When using on-chip debugger, do not use pins P00/AN7/TxD11 and P37/TxD10/RxD1.

## 1.6 Pin Description

Table 1.3 shows the pin description

**Table 1.3 Pin description**

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	Input	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	Output	Connect this pin to Vss via a capacitor.
Analog power supply input	AVcc, AVss	Input	These are power supply input pins for A-D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss.
Reset input	RESET	Input	"L" on this input resets the MCU.
CNVss	CNVss	Input	Connect this pin to Vss via a resistor.
MODE	MODE	Input	Connect this pin to Vcc via a resistor.
Main clock input	XIN	Input	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	Output	
INT interrupt input	INT0 to INT3	Input	These are INT interrupt input pins.
Key input interrupt input	KI0 to KI3	Input	These are key input interrupt input pins.
Timer X	CNTR0	Input/Output	This is the timer X I/O pin.
	CNTR0	Output	This is the timer X output pin.
Timer Y	CNTR1	Input/Output	This is the timer Y I/O pin.
Timer Z	TZOUT	Output	This is the timer Z output pin.
Timer C	TCIN	Input	This is the timer C input pin.
Serial interface	CLK0	Input/Output	This is a transfer clock I/O pin.
	RxD0, RxD1	Input	These are serial data input pins.
	TxD0, TxD10, TxD11	Output	These are serial data output pins.
Reference voltage input	VREF	Input	This is a reference voltage input pin for A-D converter. Connect the VREF pin to Vcc.
A-D converter	AN0 to AN7	Input	These are analog input pins for A-D converter.
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	Input/Output	These are 8-bit CMOS I/O ports. Each port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	Input	These are input only pins.

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

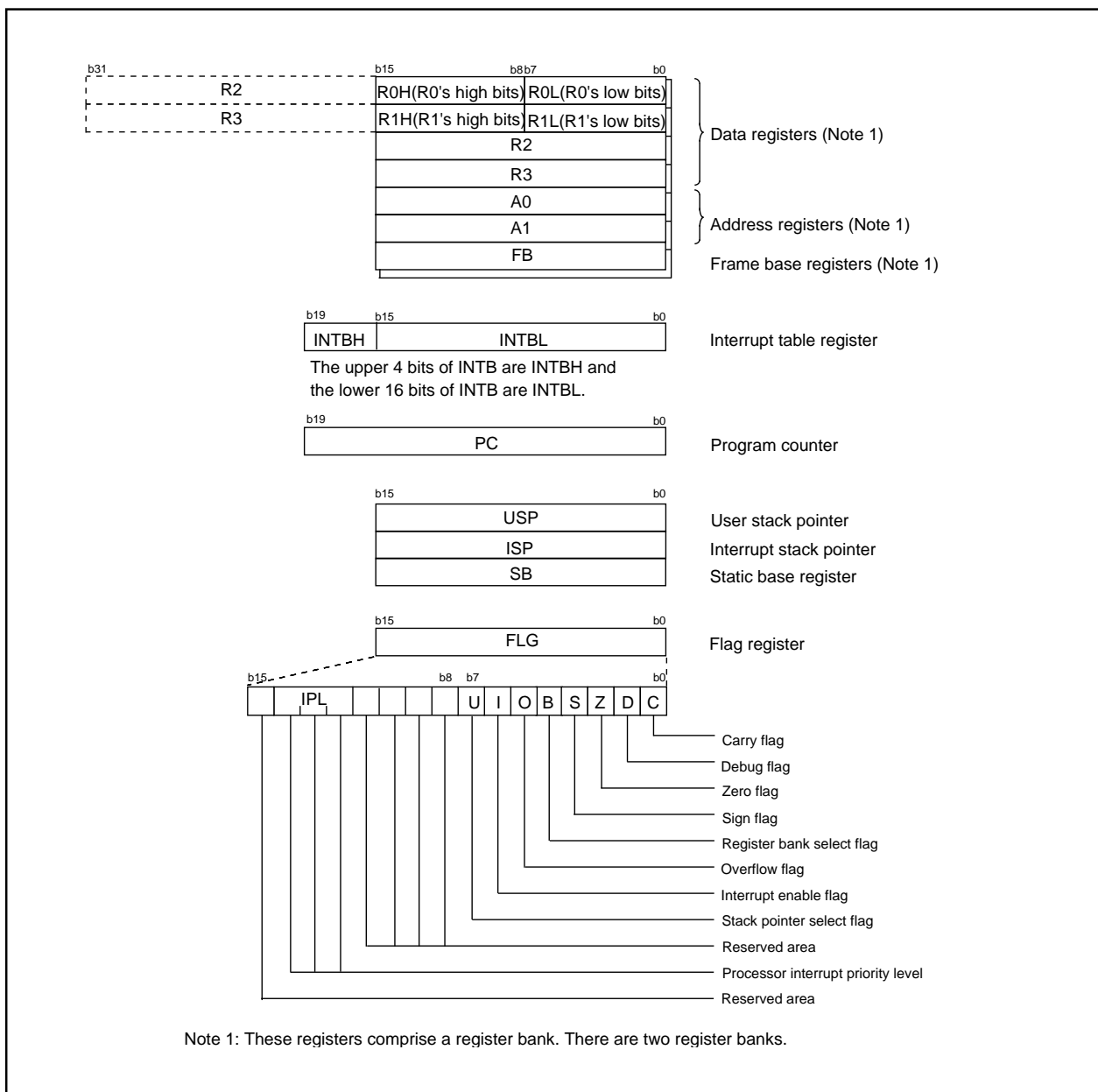


Figure 2.1 Central Processing Unit Register

### 2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

## 2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0. In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

## 2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

### 2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

### 2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

### 2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

### 2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

### 2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

### 2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

### 2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

### 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

### 2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.



### 3. Memory

Figure 3.1 is a memory map of this MCU. The address space extends the 1M bytes from address 00000<sub>16</sub> to FFFFF<sub>16</sub>.

The internal ROM (program area) is allocated in a lower address direction beginning with address 0FFFF<sub>16</sub>. For example, a 16-Kbyte internal ROM is allocated to the addresses from 0C000<sub>16</sub> to 0FFFF<sub>16</sub>. The fixed interrupt vector table is allocated to the addresses from 0FFDC<sub>16</sub> to 0FFFF<sub>16</sub>. Therefore, store the start address of each interrupt routine here.

The internal ROM (data area) is allocated to the addresses from 02000<sub>16</sub> to 02FFF<sub>16</sub>.

The internal RAM is allocated in an upper address direction beginning with address 00400<sub>16</sub>. For example, a 1-Kbyte internal RAM is allocated to the addresses from 00400<sub>16</sub> to 007FF<sub>16</sub>. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

Special function registers (SFR) are allocated to the addresses from 00000<sub>16</sub> to 002FF<sub>16</sub>. Peripheral function control registers are located here. Of the SFR, any space which has no functions allocated is reserved for future use and cannot be used by users.

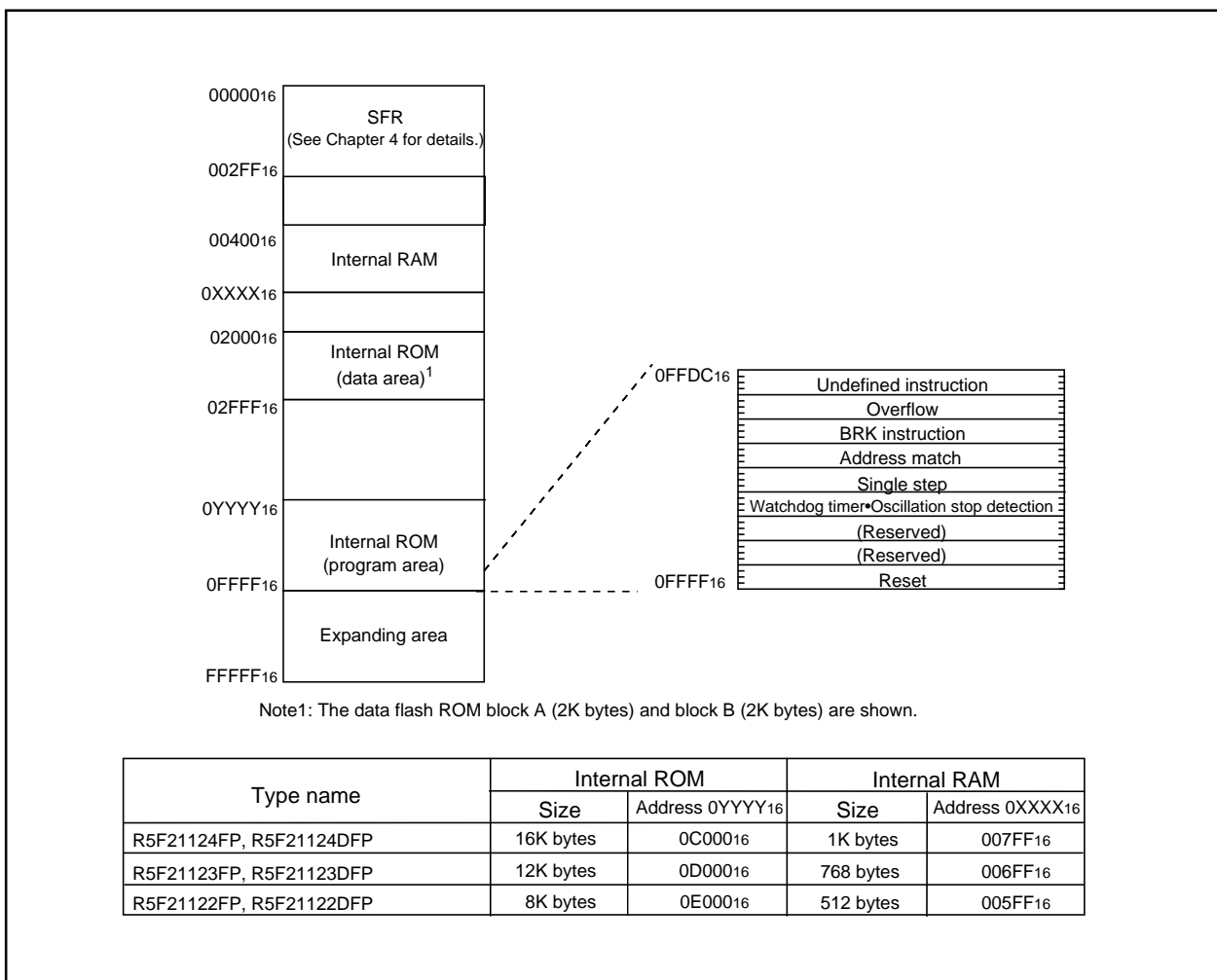


Figure 3.1 Memory Map

## 4. Special Function Register (SFR)

Address	Register	Symbol	After reset
0000 <sub>16</sub>			
0001 <sub>16</sub>			
0002 <sub>16</sub>			
0003 <sub>16</sub>			
0004 <sub>16</sub>	Processor mode register 0	PM0	XXXX0X002
0005 <sub>16</sub>	Processor mode register 1	PM1	00XXXX0X02
0006 <sub>16</sub>	System clock control register 0	CM0	011010002
0007 <sub>16</sub>	System clock control register 1	CM1	001000002
0008 <sub>16</sub>			
0009 <sub>16</sub>	Address match interrupt enable register	AIER	XXXXXX002
000A <sub>16</sub>	Protect register	PRCR	00XXX0002
000B <sub>16</sub>			
000C <sub>16</sub>	Oscillation stop detection register	OCD	000001002
000D <sub>16</sub>	Watchdog timer reset register	WDTR	XX <sub>16</sub>
000E <sub>16</sub>	Watchdog timer start register	WDTS	XX <sub>16</sub>
000F <sub>16</sub>	Watchdog timer control register	WDC	000XXXXX2
0010 <sub>16</sub>	Address match interrupt register 0	RMAD0	00 <sub>16</sub>
0011 <sub>16</sub>			00 <sub>16</sub>
0012 <sub>16</sub>			X0 <sub>16</sub>
0013 <sub>16</sub>			
0014 <sub>16</sub>	Address match interrupt register 1	RMAD1	00 <sub>16</sub>
0015 <sub>16</sub>			00 <sub>16</sub>
0016 <sub>16</sub>			X0 <sub>16</sub>
0017 <sub>16</sub>			
0018 <sub>16</sub>			
0019 <sub>16</sub>			
001A <sub>16</sub>			
001B <sub>16</sub>			
001C <sub>16</sub>			
001D <sub>16</sub>			
001E <sub>16</sub>	INT0 input filter select register	INT0F	XXXXX0002
001F <sub>16</sub>			
0020 <sub>16</sub>			
0021 <sub>16</sub>			
0022 <sub>16</sub>			
0023 <sub>16</sub>			
0024 <sub>16</sub>			
0025 <sub>16</sub>			
0026 <sub>16</sub>			
0027 <sub>16</sub>			
0028 <sub>16</sub>			
0029 <sub>16</sub>			
002A <sub>16</sub>			
002B <sub>16</sub>			
002C <sub>16</sub>			
002D <sub>16</sub>			
002E <sub>16</sub>			
002F <sub>16</sub>			
0030 <sub>16</sub>			
0031 <sub>16</sub>			
0032 <sub>16</sub>			
0033 <sub>16</sub>			
0034 <sub>16</sub>			
0035 <sub>16</sub>			
0036 <sub>16</sub>			
0037 <sub>16</sub>			
0038 <sub>16</sub>			
0039 <sub>16</sub>			
003A <sub>16</sub>			
003B <sub>16</sub>			
003C <sub>16</sub>			
003D <sub>16</sub>			
003E <sub>16</sub>			
003F <sub>16</sub>			

Note 1: The blank areas are reserved and cannot be used by users.

X : Undefined

Address	Register	Symbol	After reset
0040 <sub>16</sub>			
0041 <sub>16</sub>			
0042 <sub>16</sub>			
0043 <sub>16</sub>			
0044 <sub>16</sub>			
0045 <sub>16</sub>			
0046 <sub>16</sub>			
0047 <sub>16</sub>			
0048 <sub>16</sub>			
0049 <sub>16</sub>			
004A <sub>16</sub>			
004B <sub>16</sub>			
004C <sub>16</sub>			
004D <sub>16</sub>	Key input interrupt control register	KUPIC	XXXXX0002
004E <sub>16</sub>	A-D conversion interrupt control register	ADIC	XXXXX0002
004F <sub>16</sub>			
0050 <sub>16</sub>			
0051 <sub>16</sub>	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052 <sub>16</sub>	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053 <sub>16</sub>	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054 <sub>16</sub>	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055 <sub>16</sub>	INT2 interrupt control register	INT2IC	XXXXX0002
0056 <sub>16</sub>	Timer X interrupt control register	TXIC	XXXXX0002
0057 <sub>16</sub>	Timer Y interrupt control register	TYIC	XXXXX0002
0058 <sub>16</sub>	Timer Z interrupt control register	TZIC	XXXXX0002
0059 <sub>16</sub>	INT1 interrupt control register	INT1IC	XXXXX0002
005A <sub>16</sub>	INT3 interrupt control register	INT3IC	XXXXX0002
005B <sub>16</sub>	Timer C interrupt control register	TCIC	XXXXX0002
005C <sub>16</sub>			
005D <sub>16</sub>	INT0 interrupt control register	INT0IC	XX00X0002
005E <sub>16</sub>			
005F <sub>16</sub>			
0060 <sub>16</sub>			
0061 <sub>16</sub>			
0062 <sub>16</sub>			
0063 <sub>16</sub>			
0064 <sub>16</sub>			
0065 <sub>16</sub>			
0066 <sub>16</sub>			
0067 <sub>16</sub>			
0068 <sub>16</sub>			
0069 <sub>16</sub>			
006A <sub>16</sub>			
006B <sub>16</sub>			
006C <sub>16</sub>			
006D <sub>16</sub>			
006E <sub>16</sub>			
006F <sub>16</sub>			
0070 <sub>16</sub>			
0071 <sub>16</sub>			
0072 <sub>16</sub>			
0073 <sub>16</sub>			
0074 <sub>16</sub>			
0075 <sub>16</sub>			
0076 <sub>16</sub>			
0077 <sub>16</sub>			
0078 <sub>16</sub>			
0079 <sub>16</sub>			
007A <sub>16</sub>			
007B <sub>16</sub>			
007C <sub>16</sub>			
007D <sub>16</sub>			
007E <sub>16</sub>			
007F <sub>16</sub>			

Note 1: The blank areas are reserved and cannot be used by users.

X : Undefined

Address	Register	Symbol	After reset
0080 <sub>16</sub>	Timer Y, Z mode register	TYZMR	00 <sub>16</sub>
0081 <sub>16</sub>	Prescaler Y	PREY	FF <sub>16</sub>
0082 <sub>16</sub>	Timer Y secondary	TYSC	FF <sub>16</sub>
0083 <sub>16</sub>	Timer Y primary	TYPR	FF <sub>16</sub>
0084 <sub>16</sub>	Timer Y, Z waveform output control register	PUM	00 <sub>16</sub>
0085 <sub>16</sub>	Prescaler Z	PREZ	FF <sub>16</sub>
0086 <sub>16</sub>	Timer Z secondary	TZSC	FF <sub>16</sub>
0087 <sub>16</sub>	Timer Z primary	TZPR	FF <sub>16</sub>
0088 <sub>16</sub>			
0089 <sub>16</sub>			
008A <sub>16</sub>	Timer Y, Z output control register	TYZOC	00 <sub>16</sub>
008B <sub>16</sub>	Timer X mode register	TXMR	00 <sub>16</sub>
008C <sub>16</sub>	Prescaler X	PREX	FF <sub>16</sub>
008D <sub>16</sub>	Timer X register	TX	FF <sub>16</sub>
008E <sub>16</sub>	Count source set register	TCSS	00 <sub>16</sub>
008F <sub>16</sub>			
0090 <sub>16</sub>	Timer C register	TC	00 <sub>16</sub>
0091 <sub>16</sub>			00 <sub>16</sub>
0092 <sub>16</sub>			
0093 <sub>16</sub>			
0094 <sub>16</sub>			
0095 <sub>16</sub>			
0096 <sub>16</sub>	External input enable register	INTEN	00 <sub>16</sub>
0097 <sub>16</sub>			
0098 <sub>16</sub>	Key input enable register	KIEN	00 <sub>16</sub>
0099 <sub>16</sub>			
009A <sub>16</sub>	Timer C control register 0	TCC0	00 <sub>16</sub>
009B <sub>16</sub>	Timer C control register 1	TCC1	00 <sub>16</sub>
009C <sub>16</sub>	Capture register	TM0	XX <sub>16</sub>
009D <sub>16</sub>			XX <sub>16</sub>
009E <sub>16</sub>			
009F <sub>16</sub>			
00A0 <sub>16</sub>	UART0 transmit/receive mode register	U0MR	00 <sub>16</sub>
00A1 <sub>16</sub>	UART0 bit rate generator	U0BRG	XX <sub>16</sub>
00A2 <sub>16</sub>	UART0 transmit buffer register	U0TB	XX <sub>16</sub>
00A3 <sub>16</sub>			XX <sub>16</sub>
00A4 <sub>16</sub>	UART0 transmit/receive control register 0	U0C0	00001000 <sub>2</sub>
00A5 <sub>16</sub>	UART0 transmit/receive control register 1	U0C1	00000010 <sub>2</sub>
00A6 <sub>16</sub>	UART0 receive buffer register	U0RB	XX <sub>16</sub>
00A7 <sub>16</sub>			XX <sub>16</sub>
00A8 <sub>16</sub>	UART1 transmit/receive mode register	U1MR	00 <sub>16</sub>
00A9 <sub>16</sub>	UART1 bit rate generator	U1BRG	XX <sub>16</sub>
00AA <sub>16</sub>	UART1 transmit buffer register	U1TB	XX <sub>16</sub>
00AB <sub>16</sub>			XX <sub>16</sub>
00AC <sub>16</sub>	UART1 transmit/receive control register 0	U1C0	00001000 <sub>2</sub>
00AD <sub>16</sub>	UART1 transmit/receive control register 1	U1C1	00000010 <sub>2</sub>
00AE <sub>16</sub>	UART1 receive buffer register	U1RB	XX <sub>16</sub>
00AF <sub>16</sub>			XX <sub>16</sub>
00B0 <sub>16</sub>	UART transmit/receive control register 2	UCON	00 <sub>16</sub>
00B1 <sub>16</sub>			
00B2 <sub>16</sub>			
00B3 <sub>16</sub>			
00B4 <sub>16</sub>			
00B5 <sub>16</sub>			
00B6 <sub>16</sub>			
00B7 <sub>16</sub>			
00B8 <sub>16</sub>			
00B9 <sub>16</sub>			
00BA <sub>16</sub>			
00BB <sub>16</sub>			
00BC <sub>16</sub>			
00BD <sub>16</sub>			
00BE <sub>16</sub>			
00BF <sub>16</sub>			

Note : The blank areas are reserved and cannot be used by users.

X : Undefined

Address	Register	Symbol	After reset
00C0 <sub>16</sub> 00C1 <sub>16</sub>	A-D register	AD	XXXXXXXX2 XXXXXXXX2
00C2 <sub>16</sub>			
00C3 <sub>16</sub>			
00C4 <sub>16</sub>			
00C5 <sub>16</sub>			
00C6 <sub>16</sub>			
00C7 <sub>16</sub>			
00C8 <sub>16</sub>			
00C9 <sub>16</sub>			
00CA <sub>16</sub>			
00CB <sub>16</sub>			
00CC <sub>16</sub>			
00CD <sub>16</sub>			
00CE <sub>16</sub>			
00CF <sub>16</sub>			
00D0 <sub>16</sub>			
00D1 <sub>16</sub>			
00D2 <sub>16</sub>			
00D3 <sub>16</sub>			
00D4 <sub>16</sub>	A-D control register 2	ADCON2	0016
00D5 <sub>16</sub>			
00D6 <sub>16</sub>	A-D control register 0	ADCON0	0000XXX2
00D7 <sub>16</sub>	A-D control register 1	ADCON1	0016
00D8 <sub>16</sub>			
00D9 <sub>16</sub>			
00DA <sub>16</sub>			
00DB <sub>16</sub>			
00DC <sub>16</sub>			
00DD <sub>16</sub>			
00DE <sub>16</sub>			
00DF <sub>16</sub>			
00E0 <sub>16</sub>	Port P0 register	P0	XX16
00E1 <sub>16</sub>	Port P1 register	P1	XX16
00E2 <sub>16</sub>	Port P0 direction register	PD0	0016
00E3 <sub>16</sub>	Port P1 direction register	PD1	0016
00E4 <sub>16</sub>			
00E5 <sub>16</sub>	Port P3 register	P3	XX16
00E6 <sub>16</sub>			
00E7 <sub>16</sub>	Port P3 direction register	PD3	0016
00E8 <sub>16</sub>	Port P4 register	P4	XX16
00E9 <sub>16</sub>			
00EA <sub>16</sub>	Port P4 direction register	PD4	0016
00EB <sub>16</sub>			
00EC <sub>16</sub>			
00ED <sub>16</sub>			
00EE <sub>16</sub>			
00EF <sub>16</sub>			
00F0 <sub>16</sub>			
00F1 <sub>16</sub>			
00F2 <sub>16</sub>			
00F3 <sub>16</sub>			
00F4 <sub>16</sub>			
00F5 <sub>16</sub>			
00F6 <sub>16</sub>			
00F7 <sub>16</sub>			
00F8 <sub>16</sub>			
00F9 <sub>16</sub>			
03FA <sub>16</sub>			
00FB <sub>16</sub>			
00FC <sub>16</sub>	Pull-up control register 0	PUR0	00XX00002
00FD <sub>16</sub>	Pull-up control register 1	PUR1	XXXXXXXX0X2
00FE <sub>16</sub>	Port P1 drivability control register	DRR	0016
00FF <sub>16</sub>			
01B3 <sub>16</sub>	Flash memory control register 4	FMR4	0100000X2
01B4 <sub>16</sub>			
01B5 <sub>16</sub>	Flash memory control register 1	FMR1	1000000X2
01B6 <sub>16</sub>			
01B7 <sub>16</sub>	Flash memory control register 0	FMR0	XX0000012

Note 1: The blank areas are reserved and cannot be used by users.

X : Undefined

## 5. Electrical Characteristics

**Table 5.1 Absolute Maximum Ratings**

Symbol	Parameter	Condition	Rated value	Unit
V <sub>CC</sub>	Supply voltage	V <sub>CC</sub> =AV <sub>CC</sub>	-0.3 to 6.5	V
AV <sub>CC</sub>	Analog supply voltage	V <sub>CC</sub> =AV <sub>CC</sub>	-0.3 to 6.5	V
V <sub>I</sub>	Input voltage		-0.3 to V <sub>CC</sub> +0.3	V
V <sub>O</sub>	Output voltage		-0.3 to V <sub>CC</sub> +0.3	V
P <sub>d</sub>	Power dissipation	T <sub>opr</sub> =25 °C	300	mW
T <sub>opr</sub>	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T <sub>stg</sub>	Storage temperature		-65 to 150	°C

**Table 5.2 Recommended Operating Conditions**

Symbol	Parameter	Conditions	Standard			Unit	
			Min.	Typ.	Max.		
V <sub>CC</sub>	Supply voltage		2.7	5.0	5.5	V	
AV <sub>CC</sub>	Analog supply voltage		—	V <sub>CC</sub>	—	V	
V <sub>SS</sub>	Supply voltage		—	0	—	V	
AV <sub>SS</sub>	Analog supply voltage		—	0	—	V	
V <sub>IH</sub>	"H" input voltage		0.8V <sub>CC</sub>	—	V <sub>CC</sub>	V	
V <sub>IL</sub>	"L" input voltage		0	—	0.2V <sub>CC</sub>	V	
I <sub>OH</sub> (sum)	"H" peak all output currents	Sum of all pins' I <sub>OH</sub> (peak)	—	—	-60.0	mA	
I <sub>OH</sub> (peak)	"H" peak output current		—	—	-10.0	mA	
I <sub>OH</sub> (avg)	"H" average output current		—	—	-5.0	mA	
I <sub>OL</sub> (sum)	"L" peak all output currents	Sum of all pins' I <sub>OL</sub> (peak)	—	—	60	mA	
I <sub>OL</sub> (peak)	"L" peak output current	Except P10 to P17	—	—	10	mA	
		P10 to P17	Drive ability HIGH	—	—	30	mA
			Drive ability LOW	—	—	10	mA
I <sub>OL</sub> (avg)	"L" average output current	Except P10 to P17	—	—	5	mA	
		P10 to P17	Drive ability HIGH	—	—	15	mA
			Drive ability LOW	—	—	5	mA
f (XIN)	Main clock input oscillation frequency	3.0V ≤ V <sub>CC</sub> ≤ 5.5V	0	—	16	MHz	
		2.7V ≤ V <sub>CC</sub> < 3.0V	0	—	10	MHz	

**Note**

1: Referenced to V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 to 5.5V at T<sub>opr</sub> = -20 to 85 °C / -40 to 85 °C unless otherwise specified.

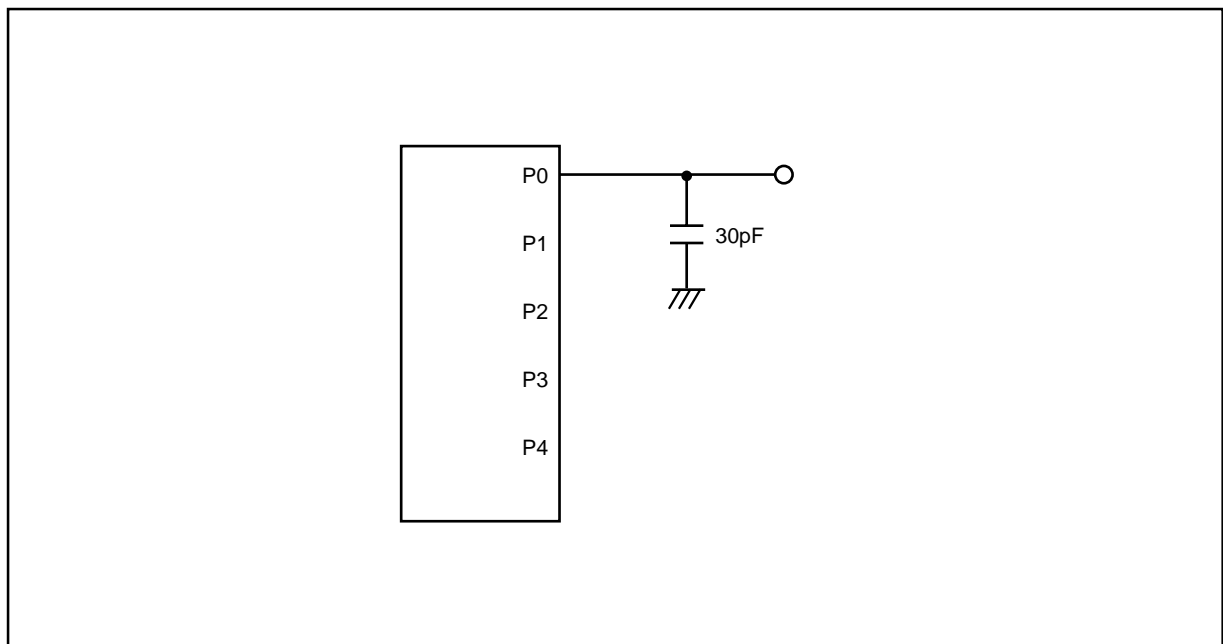
2: The mean output current is the mean value within 100ms.

**Table 5.3 A-D Conversion Characteristics**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		$V_{ref} = V_{CC}$			10	Bit
–	Absolute accuracy	10 bit mode	$f(XIN) = \phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 5.0 \text{ V}$			$\pm 3$	LSB
		8 bit mode	$f(XIN) = \phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 5.0 \text{ V}$			$\pm 2$	LSB
		10 bit mode	$f(XIN) = \phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 3.3 \text{ V}$			$\pm 5$	LSB
		8 bit mode	$f(XIN) = \phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 3.3 \text{ V}$			$\pm 2$	LSB
$R_{LADDER}$	Ladder resistance		$V_{REF} = V_{CC}$	10		40	$k\Omega$
$t_{CONV}$	Conversion time	10 bit mode	$f(XIN) = \phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 5.0 \text{ V}$	3.3			$\mu\text{s}$
		8 bit mode	$f(XIN) = \phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 5.0 \text{ V}$	2.8			$\mu\text{s}$
$V_{REF}$	Reference voltage			2.0		$V_{CC}$	V
$V_{IA}$	Analog input voltage			0		$V_{ref}$	V
–	A-D operation clock frequency <sup>2</sup>	Without sample & hold		0.25		10	MHz
		With sample & hold		1.0		10	MHz

**Note**

- 1: Referenced to  $V_{CC} = AV_{CC} = 2.7$  to  $5.5 \text{ V}$  at  $T_{opr} = -20$  to  $85 \text{ }^\circ\text{C}$  /  $-40$  to  $85 \text{ }^\circ\text{C}$  unless otherwise specified.
- 2: When  $f_{AD}$  is 10 MHz more, divide the  $f_{AD}$  and make A-D operation clock frequency ( $\phi_{AD}$ ) lower than 10 MHz.
- 3: When the  $V_{CC}$  is less than 4.2V, divide the  $f_{AD}$  and make A-D operation clock frequency ( $\phi_{AD}$ ) lower than  $f_{AD}/2$ .

**Figure 5.1 Port P0 to P4 measurement circuit**

**Table 5.4 Flash Memory (Program area) Electrical Characteristics**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase cycle <sup>2</sup>		100 <sup>3</sup>	—	—	cycle
–	Byte program time	V <sub>CC</sub> = 5.0 V at Topr = 25 °C	—	50	—	μs
–	Block erase time	V <sub>CC</sub> = 5.0 V at Topr = 25 °C	—	0.4	—	s
t <sub>d(SR-ES)</sub>	Time delay from Suspend Request until Erase Suspend		—	—	TBD	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program, Erase Temperature		0	—	60	°C

**Table 5.5 Flash Memory (Data area Block A, Block B) Electrical Characteristics<sup>4</sup>**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase endurance <sup>2</sup>		10000 <sup>3</sup>	—	—	times
–	Byte program time(program/erase endurance ≤1000 times)	V <sub>CC</sub> = 5.0 V at Topr = 25 °C	—	50	400	μs
–	Byte program time(program/erase endurance >1000 times)	V <sub>CC</sub> = 5.0 V at Topr = 25 °C	—	65	—	μs
–	Block erase time(program/erase endurance ≤1000 times)	V <sub>CC</sub> = 5.0 V at Topr = 25 °C	—	0.2	9	s
–	Block erase time(program/erase endurance >1000 times)	V <sub>CC</sub> = 5.0 V at Topr = 25 °C	—	0.3	—	s
t <sub>d(SR-ES)</sub>	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program/Erase Temperature		-20(-40) <sup>8</sup>	—	85	°C
–	Data-retention duration	Topr = 55 °C	—	—	20	year

**Note**

1: Referenced to V<sub>CC</sub>=AV<sub>CC</sub>=2.7 to 5.5V at Topr = 0 to 60 °C unless otherwise specified.

2: Definition of Program/Erase

The cycle of Program/Erase shows a cycle for each block.

If the program/erase number is “n” (n = 100, 10000), “n” times erase can be performed for each block.

For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.

However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).

3: Maximum numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.

4: Table 5.5 applies for Block A or B when the Program/Erase cycles are more than 1000. The byte program time and block erase time up to 1000 cycles are the same as that of the program area (see Table 5.4).

5: To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.

6: If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.

7: Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.

8: -40 °C for D version.



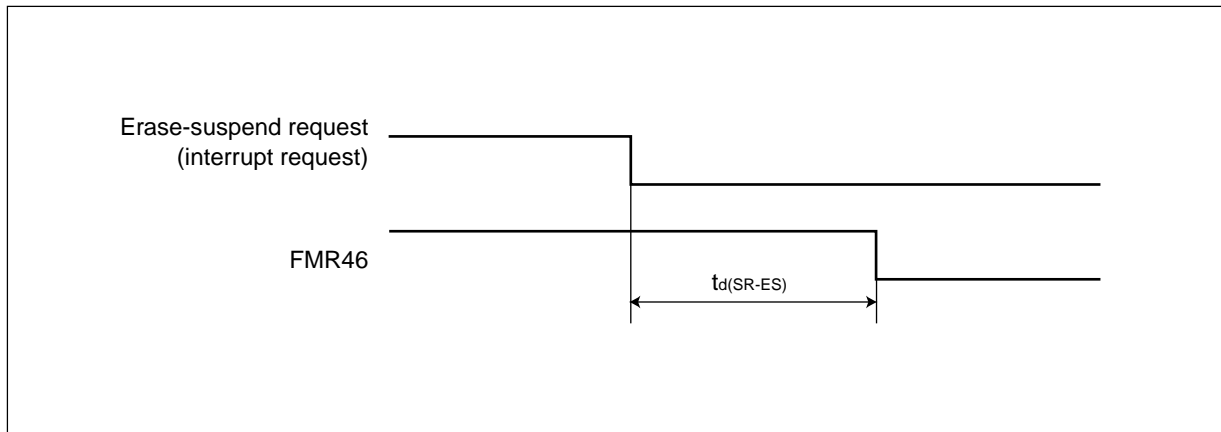


Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on <sup>2</sup>				2	ms
td(R-S)	STOP release time <sup>3</sup>				150	μs

## Note

- 1: The measuring condition is  $V_{CC}=AV_{CC}=2.7$  to  $5.5$  V and  $T_{opr}=25$  °C.
- 2: This shows the waiting time till the internal power supply generating circuit is stabilized during powering-on.
- 3: This shows the time till BCLK starts from the interrupt acknowledgement to cancel stop mode.

Table 5.7 Electrical Characteristics (1) [V<sub>CC</sub>=5V]

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V <sub>OH</sub>	"H" output voltage	Except X <sub>OUT</sub>	I <sub>OH</sub> =5mA	V <sub>CC</sub> -2.0		V <sub>CC</sub>	V
			I <sub>OH</sub> =-200μA	V <sub>CC</sub> -0.3		V <sub>CC</sub>	V
	X <sub>OUT</sub>		Drive ability HIGH I <sub>OH</sub> =1 mA	V <sub>CC</sub> -2.0		V <sub>CC</sub>	V
			Drive ability LOW I <sub>OL</sub> =-500μA	V <sub>CC</sub> -2.0		V <sub>CC</sub>	V
V <sub>OL</sub>	"L" output voltage	P10 to P17 Except X <sub>OUT</sub>	I <sub>OH</sub> = 5 mA			2.0	V
			I <sub>OH</sub> = 200 μA			0.45	V
	P10 to P17		Drive ability HIGH I <sub>OH</sub> = 10 mA			2.0	V
			Drive ability LOW I <sub>OL</sub> = 5 mA			2.0	V
	X <sub>OUT</sub>		Drive ability HIGH I <sub>OH</sub> = 1 mA			2.0	V
			Drive ability LOW I <sub>OL</sub> =500μA			2.0	V
V <sub>T+</sub> -V <sub>T-</sub>	Hysteresis	INT0, INT1, INT2, INT3, K10, K11, K12, K13, CNTR0, CNTR1, TCIN, RxD0, RxD1		0.2		1.0	V
		RESET		0.2		2.2	V
I <sub>IH</sub>	"H" input current		V <sub>I</sub> =5V			5.0	μA
I <sub>IL</sub>	"L" input current		V <sub>I</sub> =0V			-5.0	μA
R <sub>PULLUP</sub>	Pull-up resistance		V <sub>I</sub> =0V	30	50	167	kΩ
R <sub>XIN</sub>	Feedback resistance	X <sub>IN</sub>			1.0		MΩ
f <sub>RING</sub>	Ring oscillator frequency			40	125	250	kHz
V <sub>RAM</sub>	RAM retention voltage		At stop mode	2.0			V

## Note

- 1 : Referenced to  $V_{CC}=AV_{CC}=4.2$  to  $5.5$  V at  $T_{opr} = -20$  to  $85$  °C /  $-40$  to  $85$  °C,  $f(\text{BCLK})=20$  MHz unless otherwise specified.

**Table 5.8 Electrical Characteristics (2) [Vcc=5V]**

Symbol	Parameter	Measuring condition		Min.	Standard	Max.	Unit
					Typ.		
I <sub>CC</sub>	Power supply current (V <sub>CC</sub> =3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V <sub>SS</sub>	High-speed mode	X <sub>IN</sub> =16 MHz (square wave) Ring oscillator on=125 kHz No division		8	14	mA
			X <sub>IN</sub> =10 MHz (square wave) Ring oscillator on=125 kHz No division		5		mA
		Medium-speed mode	X <sub>IN</sub> =16 MHz (square wave) Ring oscillator on=125 kHz Division by 8		3		mA
			X <sub>IN</sub> =10 MHz (square wave) Ring oscillator on=125 kHz Division by 8		2		mA
		Ring oscillator mode	Main clock off Ring oscillator on=125 kHz Division by 8		0.4	2.0	mA
		Wait mode	Main clock off Ring oscillator on=125 kHz When a WAIT instruction is executed <sup>2</sup> Peripheral clock operation		TBD	TBD	μA
		Wait mode	Main clock off Ring oscillator on=125 kHz When a WAIT instruction is executed <sup>2</sup> Peripheral clock off		TBD	TBD	μA
Stop mode	Main clock off Ring oscillator off CM10="1" Peripheral clock off		0.8	3.0	μA		

## Note

- 1: The power supply current measuring is executed using the measuring program on flash memory.  
2: Timer Y is operated with timer mode.

**Timing requirements (Unless otherwise noted: Vcc = 5V, Vss = 0V at Ta = 25 °C) [Vcc=5V]****Table 5.9 XIN input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	62.5		ns
tWH(XIN)	XIN input HIGH pulse width	30		ns
tWL(XIN)	XIN input LOW pulse width	30		ns

**Table 5.10 CNTR0 input, CNTR1 input, INT2 input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	100		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	40		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	40		ns

**Table 5.11 TCIN input, INT3 input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	400 <sup>1</sup>		ns
tWH(TCIN)	TCIN input HIGH pulse width	200 <sup>2</sup>		ns
tWL(TCIN)	TCIN input LOW pulse width	200 <sup>2</sup>		ns

**Note**

- 1 : Use the greater value, either ( 1 / digital filter clock frequency x 6) or min. value.  
 2 : Use the greater value, either ( 1 / digital filter clock frequency x 3) or min. value.

**Table 5.12 Serial I/O**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	200		ns
tW(CKH)	CLKi input HIGH pulse width	100		ns
tW(CKL)	CLKi input LOW pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	35		ns
th(C-D)	RxDi input hold time	90		ns

**Table 5.13 External interrupt INT0 input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	INT0 input HIGH pulse width	250 <sup>1</sup>		ns
tW(INL)	INT0 input LOW pulse width	250 <sup>2</sup>		ns

**Note**

- 1 : When the INT0 input filter select bit selects the digital filter, use the INT0 input HIGH pulse width to the greater value, either ( 1 / digital filter clock frequency x 3) or min. value.  
 2 : When the INT0 input filter select bit selects the digital filter, use the INT0 input LOW pulse width to the greater value, either ( 1 / digital filter clock frequency x 3) or min. value.

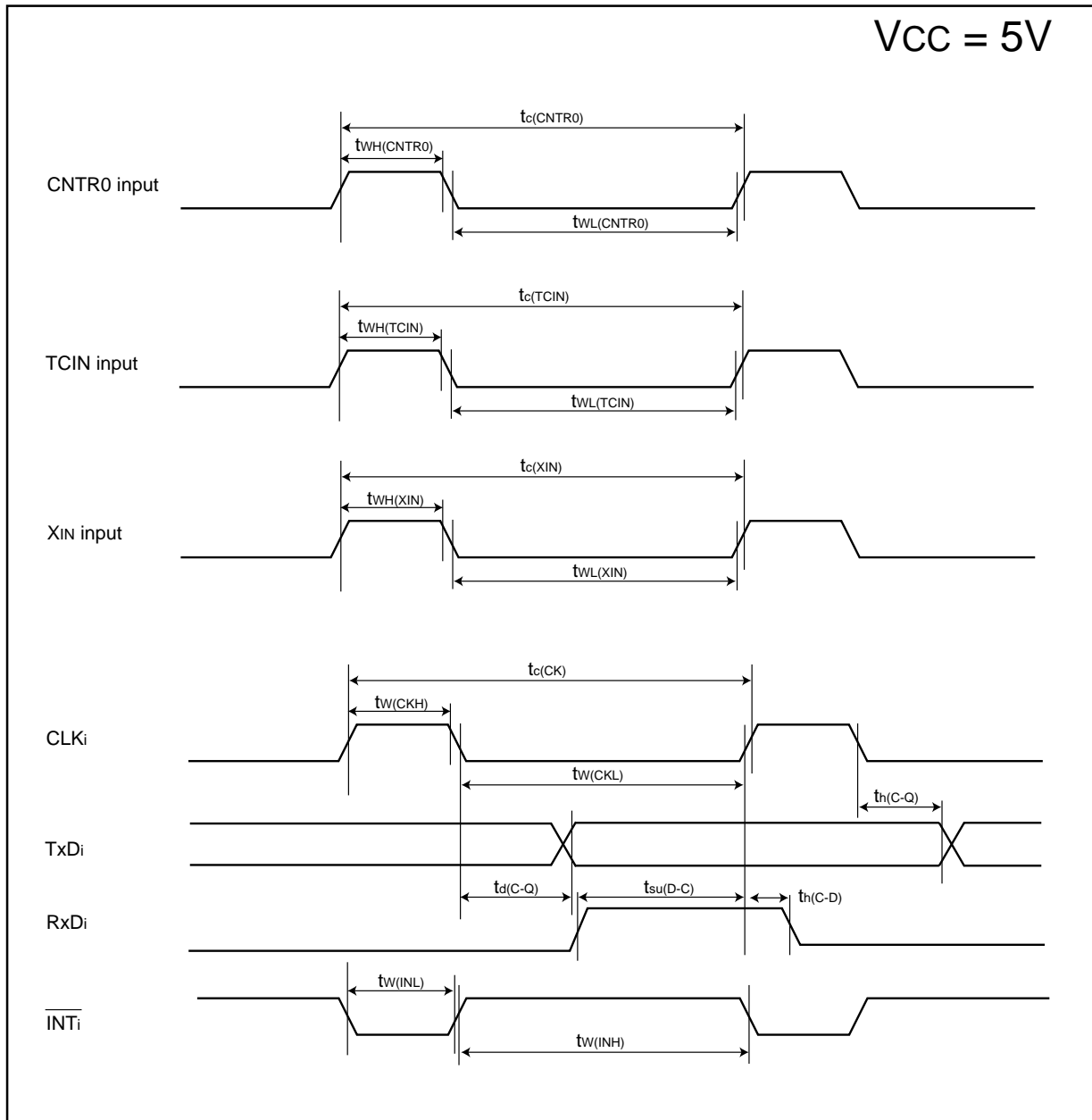


Figure 5.3  $V_{CC}=5V$  timing diagram

**Table 5.14 Electrical Characteristics (3) [Vcc=3V]**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	"H" output voltage	Except XOUT	IOH=-1mA	Vcc-0.5		Vcc	V
		XOUT	Drive ability HIGH IOH=-0.1 mA	Vcc-0.5		Vcc	v
			Drive ability LOW IOL=-50 μA	Vcc-0.5		Vcc	v
VOL	"L" output voltage	P10 to P17	IOH= 1 mA			0.5	V
		Except XOUT	Drive ability HIGH IOH= 2 mA			0.5	V
			Drive ability LOW IOL= 1 mA			0.5	V
		P10 to P17	Drive ability HIGH IOH= 0.1 mA			0.5	V
			Drive ability LOW IOL=50 μA			0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, K10, K11, K12, K13, CNTRo, CNTR1, TCIN, RxD0, RxD1		0.2		0.8	V
		RESET		0.2		1.8	V
IiH	"H" input current		Vi=3V			4.0	μA
IiL	"L" input current		Vi=0V			-4.0	μA
RPULLUP	Pull-up resistance		Vi=0V	66	160	500	kΩ
RiXIN	Feedback resistance	XIN			3.0		MΩ
fRING	Ring oscillator frequency			40	125	250	kHz
VRAM	RAM retention voltage		At stop mode	2.0			V

## Note

1 : Referenced to Vcc=AVcc=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.

**Table 5.15 Electrical Characteristics (4) [V<sub>CC</sub>=3V]**

Symbol	Parameter	Measuring condition		Standard			Unit
				Min.	Typ.	Max.	
I <sub>CC</sub>	Power supply current (V <sub>CC1</sub> =2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V <sub>SS</sub>	High-speed mode	X <sub>IN</sub> =16 MHz (square wave) Ring oscillator on=125 kHz No division		7	12	mA
			X <sub>IN</sub> =10 MHz (square wave) Ring oscillator on=125 kHz No division		5		mA
		Medium-speed mode	X <sub>IN</sub> =16 MHz (square wave) Ring oscillator on=125 kHz Division by 8		2.5		mA
			X <sub>IN</sub> =10 MHz (square wave) Ring oscillator on=125 kHz Division by 8		1.6		mA
		Ring oscillator mode	Main clock off Ring oscillator on=125 kHz Division by 8		0.4	2.0	mA
		Wait mode	Main clock off Ring oscillator on=125 kHz When a WAIT instruction is executed <sup>2</sup> Peripheral clock operation		TBD	TBD	μA
		Wait mode	Main clock off Ring oscillator on=125 kHz When a WAIT instruction is executed <sup>2</sup> Peripheral clock off		TBD	TBD	μA
Stop mode	Main clock off Ring oscillator off CM10="1" Peripheral clock off		0.7	3.0	μA		

## Note

- 1: The power supply current measuring is executed using the measuring program on flash memory.  
2: Timer Y is operated with timer mode.

**Timing requirements (Unless otherwise noted:  $V_{CC} = 3V$ ,  $V_{SS} = 0V$  at  $T_a = 25\text{ }^\circ\text{C}$ ) [ $V_{CC}=3V$ ]****Table 5.16 XIN input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	143		ns
tWH(XIN)	XIN input HIGH pulse width	70		ns
tWL(XIN)	XIN input LOW pulse width	70		ns

**Table 5.17 CNTR0 input, CNTR1 input,  $\overline{\text{INT2}}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	300		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	120		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	120		ns

**Table 5.18 TCIN input,  $\overline{\text{INT3}}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	1200 <sup>1</sup>		ns
tWH(TCIN)	TCIN input HIGH pulse width	600 <sup>2</sup>		ns
tWL(TCIN)	TCIN input LOW pulse width	600 <sup>2</sup>		ns

Note

- 1 : Use the greater value, either ( 1 / digital filter clock frequency x 6 ) or min. value.  
 2 : Use the greater value, either ( 1 / digital filter clock frequency x 3 ) or min. value.

**Table 5.19 Serial I/O**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	300		ns
tW(CKH)	CLKi input HIGH pulse width	150		ns
tW(CKL)	CLKi input LOW pulse width	150		ns
td(C-Q)	TxDi output delay time		160	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	55		ns
th(C-D)	RxDi input hold time	90		ns

**Table 5.20 External interrupt  $\overline{\text{INT0}}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	$\overline{\text{INT0}}$ input HIGH pulse width	380 <sup>1</sup>		ns
tW(INL)	$\overline{\text{INT0}}$ input LOW pulse width	380 <sup>2</sup>		ns

Note

- 1 : When the  $\overline{\text{INT0}}$  input filter select bit selects the digital filter, use the  $\overline{\text{INT0}}$  input HIGH pulse width to the greater value, either ( 1 / digital filter clock frequency x 3 ) or min. value.  
 2 : When the  $\overline{\text{INT0}}$  input filter select bit selects the digital filter, use the  $\overline{\text{INT0}}$  input LOW pulse width to the greater value, either ( 1 / digital filter clock frequency x 3 ) or min. value.

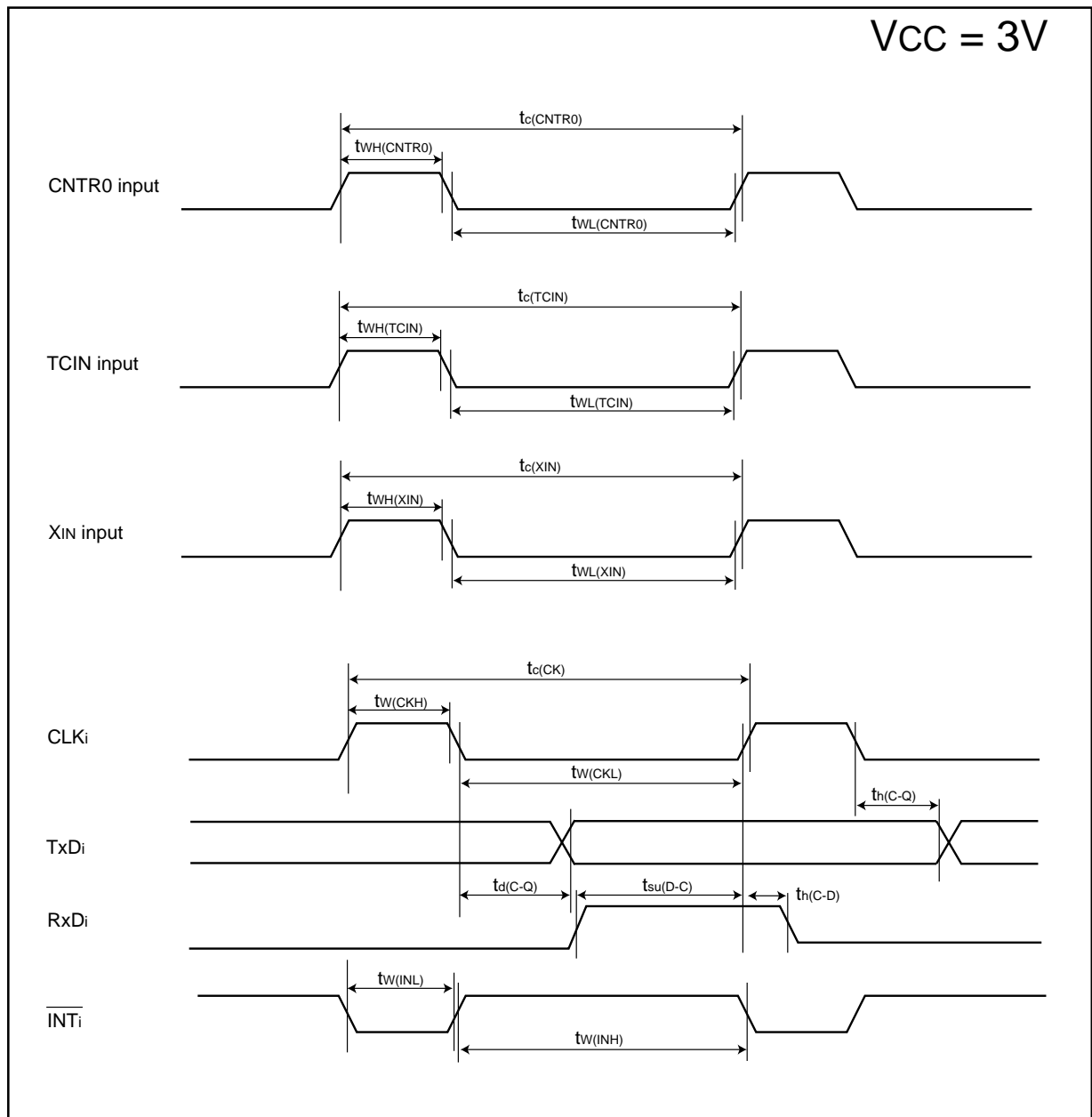


Figure 5.4 Vcc=3V timing diagram

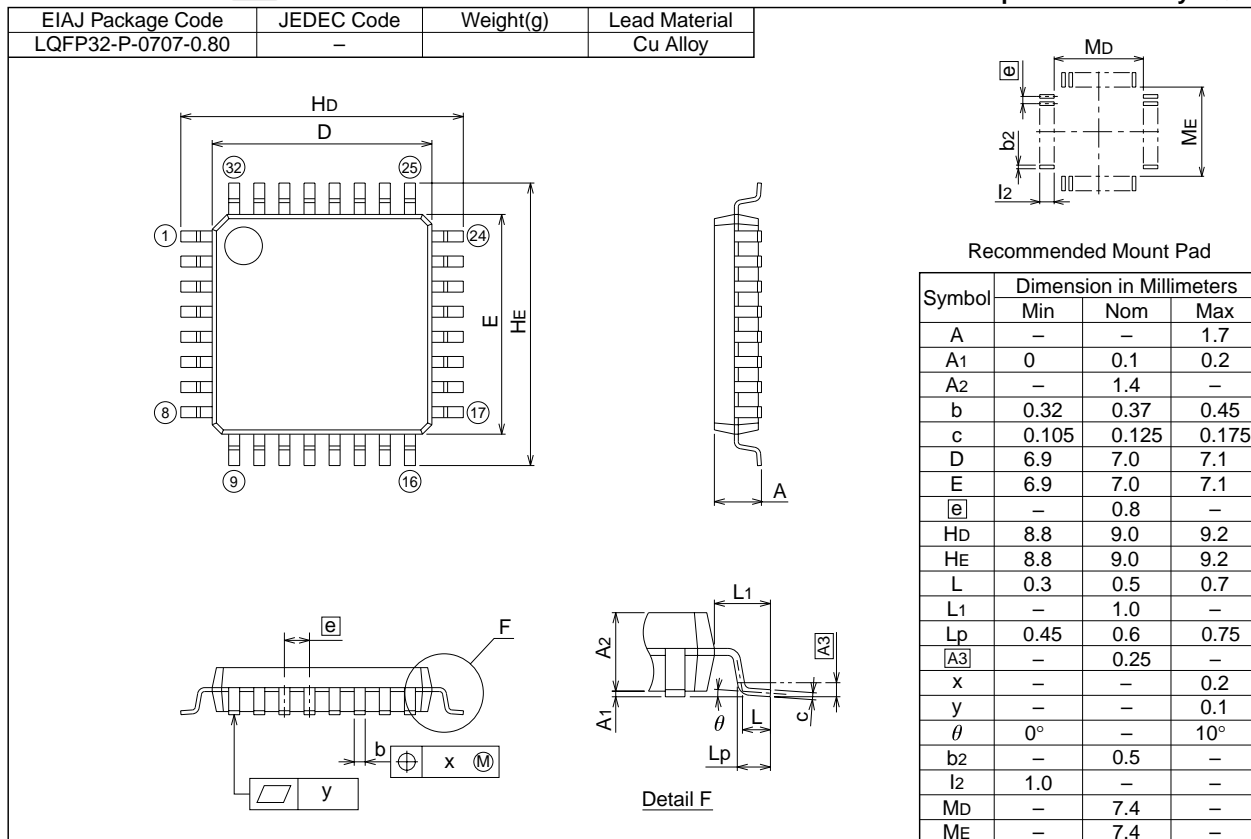


## Package Dimensions

### 32P6U-A

(MMP)

Plastic 32pin 7X7mm body LQFP





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