RENESAS

R8C/13 Group
SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0069-0020Z
Rev.0.20
2003.12.05

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

The data flash ROM (2 KB X 2 blocks) is embedded.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

Under development Preliminary specification
                    Specifications in this manual are tentative and subject to change.

R8C/13 Group   1. Overview

1.2 Performance Outline

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

	Item	Performance
CPU	Number of basic instructions	89 instructions
	Shortest instruction execution time	50 ns (f(X_{IN}) = 20 MHz, V_{CC} = 3.0 to 5.5 V)
		100 ns (f(X_{IN}) = 10 MHz, V_{CC} = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2.
Peripheral function	Interrupt	Internal: 10 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels
	Watchdog timer	15 bits x 1 (with prescaler) Reset start function selectable
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel Circuits of input capture and output compare.
	Serial I/O	•1 channel Clock synchronous, UART •1 channel UART
	A-D converter	10-bit A-D converter: 1 circuit, 12 channels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •Ring oscillator (high speed, low speed) On High-speed ring oscillator the frequency adjustment function is usable.
	Oscillation stop detection function	Stop detection of main clock oscillation
	Voltage detection circuit	Included
	Power on reset circuit	Included
	Port	Input/Output: 22 (including LED drive port), Input: 2 (LED drive I/O port: 8, max. 20 mA)
Electrical characteristics	Power supply voltage	V_{CC} = 3.0 to 5.5 V (f(X_{IN}) = 20 MHz) V_{CC} = 2.7 to 5.5 V (f(X_{IN}) = 10 MHz)
	Power consumption	Typ. 9 mA (V_{CC} = 5.0 V, (f(X_{IN}) = 20 MHz, High-speed mode) Typ. 5 mA (V_{CC} = 3.0 V, (f(X_{IN}) = 10 MHz, High-speed mode) TBD (V_{CC} = 3.0 V, Wait mode) Typ. 0.7 µA (V_{CC} = 3.0 V, Stop mode)
Flash memory	Program/erase voltage	V_{CC} = 2.7 to 5.5 V
	Number of program/erase	10000 times (Data area)
		100 times (Program area)
Operating ambient temperature		-20 to 85 °C -40 to 85 °C (option)
Package		32-pin plastic mold LQFP

Option: If you require this option, please specify so.

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R8C/13 Group   1. Overview

1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

Figure 1.1 Block Diagram

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R8C/13 Group   1. Overview
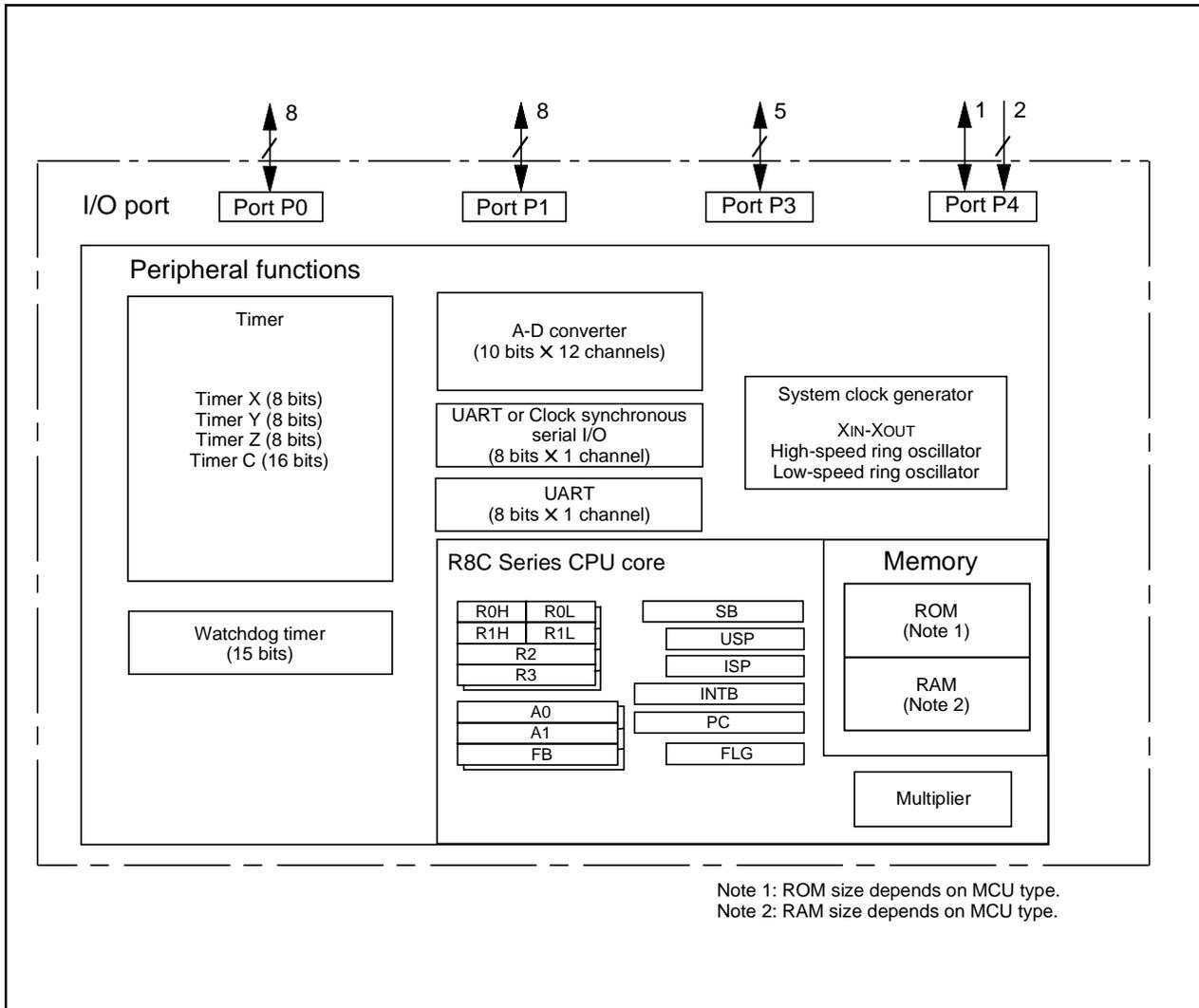
1.4 Product Information

Table 1.2 lists the products.

Table 1.2 Product List

As of October 2003

Type No.		ROM capacity		RAM capacity	Package type	Remarks
		Program area	Data area			
R5F21132FP	✶✶	8K bytes	2K bytes x 2	512 bytes	32P6U-A	Flash memory version
R5F21133FP	✶✶	12K bytes	2K bytes x 2	768 bytes	32P6U-A	
R5F21134FP	✶✶	16K bytes	2K bytes x 2	1K bytes	32P6U-A	
R5F21132DFP	✶✶	8K bytes	2K bytes x 2	512 bytes	32P6U-A	D version
R5F21133DFP	✶✶	12K bytes	2K bytes x 2	768 bytes	32P6U-A	
R5F21134DFP	✶✶	16K bytes	2K bytes x 2	1K bytes	32P6U-A	

✶✶ : Under development

Type No. R 5 F 21 13 4 D FP

Package type:
    FP : 32P6U

Shows characteristics and others.
D: Operating ambient temperature –40 °C to 85 °C
No symbol: Operating ambient temperature –20 °C to 85 °C

ROM capacity:
    2 : 8 KBytes.
    3 : 12 KBytes.
    4 : 16 KBytes.

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R8C/Tiny series

Memory type:
    F: Flash memory version

Renesas MCU

Renesas semiconductors
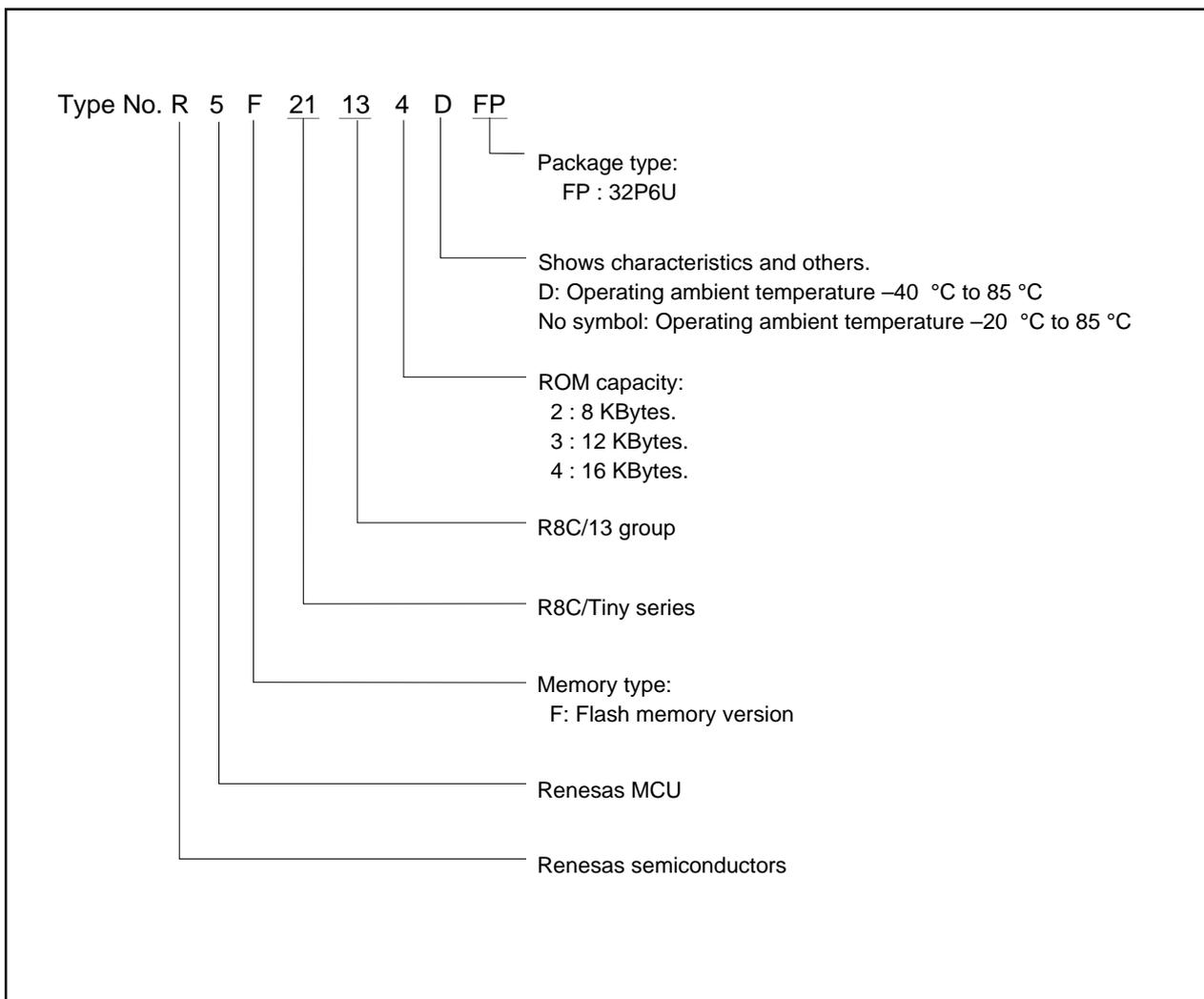
Figure 1.2 Type No., Memory Size, and Package

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R8C/13 Group

1. Overview

1.5 Pin Assignments

Figure 1.3 shows the pin configuration (top view).
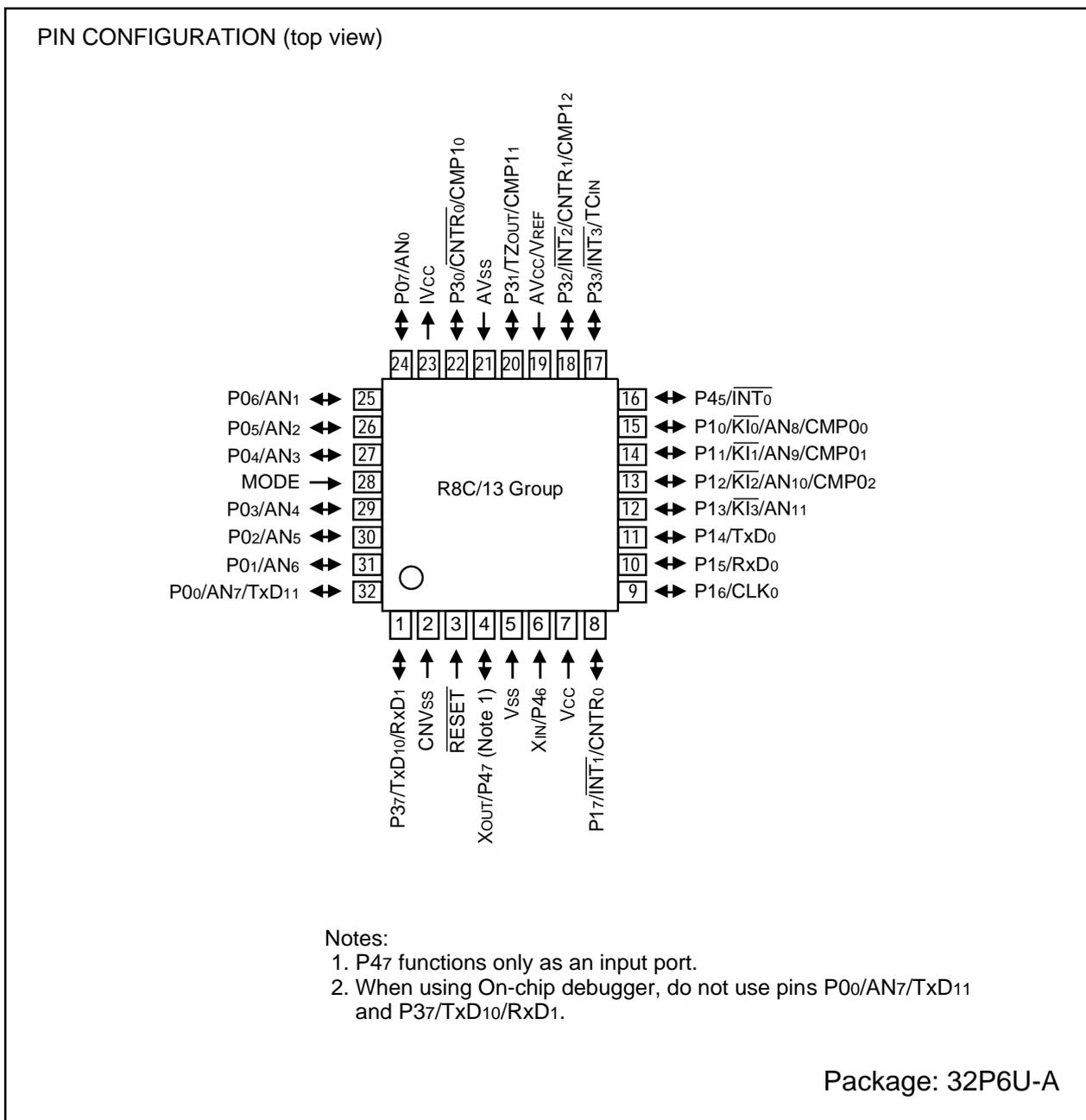
Figure 1.3 Pin Configuration (Top View)

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R8C/13 Group   1. Overview

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	Input	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	Output	Connect this pin to Vss via a capacitor.
Analog power supply input	AVcc, AVss	Input	These are power supply input pins for A-D converter. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	$\overline{RESET}$	Input	"L" on this input resets the MCU.
CNVss	CNVss	Input	Connect this pin to Vss via a resistor.
MODE	MODE	Input	Connect this pin to Vcc via a resistor.
Main clock input	X_{IN}	Input	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or a crystal oscillator between the X_{IN} and X_{OUT} pins. To use an externally derived clock, input it to the X_{IN} pin and leave the X_{OUT} pin open.
Main clock output	X_{OUT}	Output	
$\overline{INT}$ interrupt input	$\overline{INT_0}$ to $\overline{INT_3}$	Input	These are $\overline{INT}$ interrupt input pins.
Key input interrupt input	KI_0 to KI_3	Input	These are key input interrupt input pins.
Timer X	$CNTR_0$	Input/Output	This is the timer X I/O pin.
	$\overline{CNTR_0}$	Output	This is the timer X output pin.
Timer Y	$CNTR_1$	Input/Output	This is the timer Y I/O pin.
Timer Z	TZ_{OUT}	Output	This is the timer Z output pin.
Timer C	TC_{IN}	Input	This is the timer C input pin.
	$CMP0_0$ to $CMP0_3$, $CMP1_0$ to $CMP1_3$	Output	These are the timer C output pins.
Serial interface	CLK_0	Input/Output	This is a transfer clock I/O pin.
	RxD_0, RxD_1	Input	These are serial data input pins.
	TxD_0, $TxD1_0$, $TxD1_1$	Output	These are serial data output pins.
Reference voltage input	V_{REF}	Input	This is a reference voltage input pin for A-D converter.
A-D converter	AN_0 to AN_{11}	Input	These are analog input pins for A-D converter.
I/O port	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P3_0$ to $P3_3$, $P3_7$, $P4_5$	Input/Output	These are 8-bit CMOS I/O ports. Each port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. $P1_0$ to $P1_7$ also function as LED drive ports.
Input port	$P4_6$, $P4_7$	Input	These are input only pins.

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R8C/13 Group   2. Central Processing Unit (CPU)

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.
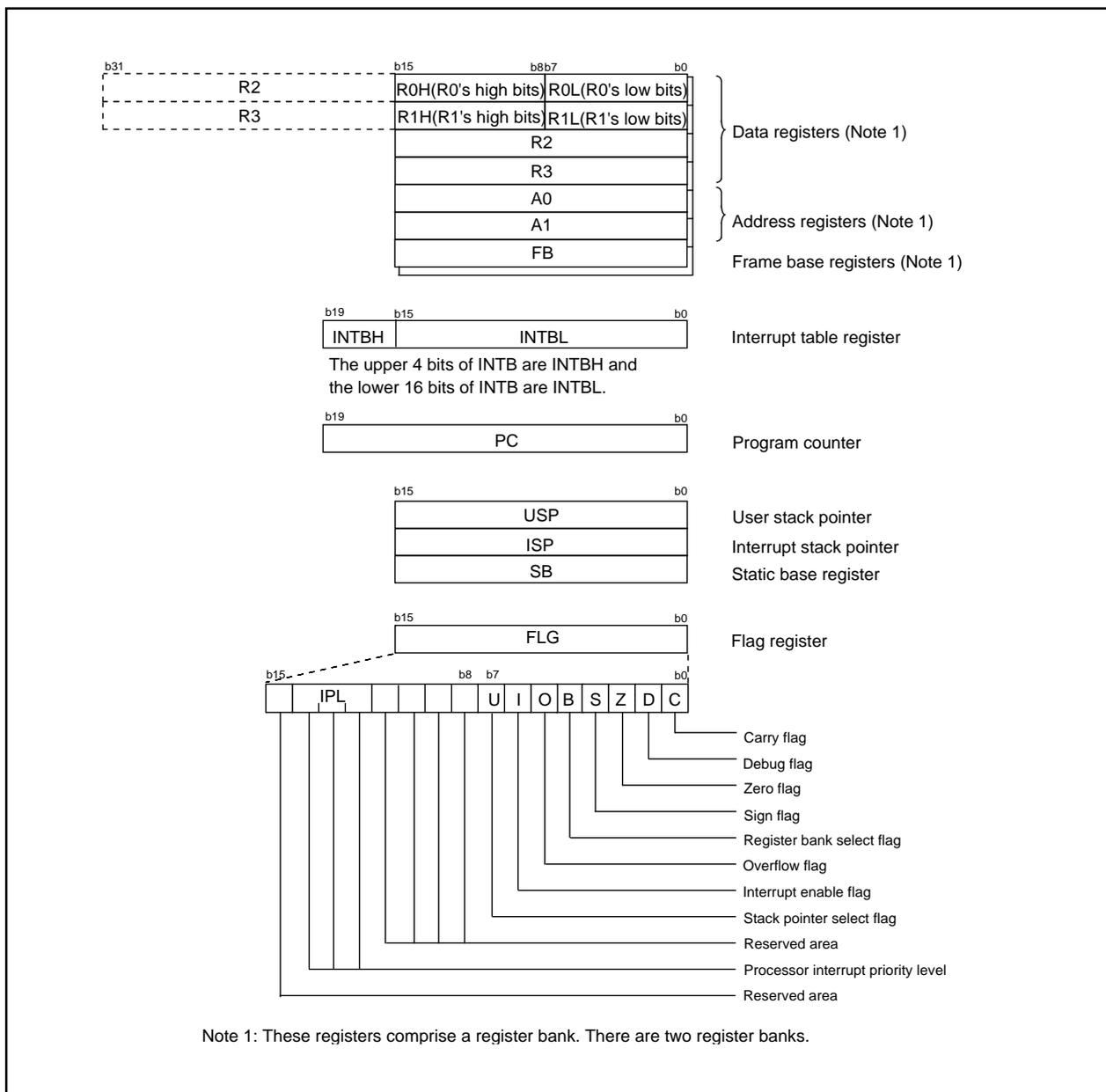

Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

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R8C/13 Group   2. Central Processing Unit (CPU)

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0" ; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

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R8C/13 Group   3. Memory

3. Memory

Figure 3.1 is a memory map of this MCU. The address space extends the 1M bytes from address 00000_{16} to $FFFFF_{16}$.

The internal ROM (program area) is allocated in a lower address direction beginning with address $0FFFF_{16}$. For example, a 16-Kbyte internal ROM is allocated to the addresses from $0C000_{16}$ to $0FFFF_{16}$.

The fixed interrupt vector table is allocated to the addresses from $0FFDC_{16}$ to $0FFFF_{16}$. Therefore, store the start address of each interrupt routine here.

The internal ROM (data area) is allocated to the addresses from 02000_{16} to $02FFF_{16}$.

The internal RAM is allocated in an upper address direction beginning with address 00400_{16}. For example, a 1-Kbyte internal RAM is allocated to the addresses from 00400_{16} to $007FF_{16}$. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

Special function registers (SFR) are allocated to the addresses from 00000_{16} to $002FF_{16}$. Peripheral function control registers are located here. Of the SFR, any space which has no functions allocated is reserved for future use and cannot be used by users.

Note1 The data flash ROM block A (2K bytes) and block B (2K bytes) are shown.

Type name	Internal ROM		Internal RAM	
	Size	Address 0YYYY16	Size	Address 0XXXX16
R5F21134FP, R5F21134DFP	16K bytes	0C00016	1K bytes	007FF16
R5F21133FP, R5F21133DFP	12K bytes	0D00016	768 bytes	006FF16
R5F21132FP, R5F21132DFP	8K bytes	0E00016	512 bytes	005FF16

Figure 3.1 Memory Map

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R8C/13 Group   4. Special Function Register (SFR)

4. Special Function Register (SFR)

Address	Register	Symbol	After reset
0000_{16}			
0001_{16}			
0002_{16}			
0003_{16}			
0004_{16}	Processor mode register 0 [1]	PM0	00_{16}
0005_{16}	Processor mode register 1	PM1	00_{16}
0006_{16}	System clock control register 0	CM0	01101000_2
0007_{16}	System clock control register 1	CM1	00100000_2
0008_{16}	High-speed ring control register 0	HR0	00_{16}
0009_{16}	Address match interrupt enable register	AIER	$XXXXXX00_2$
$000A_{16}$	Protect register	PRCR	$00XXX000_2$
$000B_{16}$	High-speed ring control register 1	HR1	40_{16}
$000C_{16}$	Oscillation stop detection register	OCD	00000100_2
$000D_{16}$	Watchdog timer reset register	WDTR	XX_{16}
$000E_{16}$	Watchdog timer start register	WDTS	XX_{16}
$000F_{16}$	Watchdog timer control register	WDC	$000XXXXX_2$
0010_{16}	Address match interrupt register 0	RMAD0	00_{16}
0011_{16}			00_{16}
0012_{16}			$X0_{16}$
0013_{16}			
0014_{16}	Address match interrupt register 1	RMAD1	00_{16}
0015_{16}			00_{16}
0016_{16}			$X0_{16}$
0017_{16}			
0018_{16}			
0019_{16}	Voltage detection register 1 [2]	VCR1	00_{16}
$001A_{16}$	Voltage detection register 2 [2]	VCR2	10000000_{16}
$001B_{16}$			
$001C_{16}$			
$001D_{16}$			
$001E_{16}$	INT0 input filter select register	INT0F	$XXXXX000_2$
$001F_{16}$	Voltage detection interrupt register [2]	D4INT	00_{16} [3] 01000001_2 [4]
0020_{16}			
0021_{16}			
0022_{16}			
0023_{16}			
0024_{16}			
0025_{16}			
0026_{16}			
0027_{16}			
0028_{16}			
0029_{16}			
$002A_{16}$			
$002B_{16}$			
$002C_{16}$			
$002D_{16}$			
$002E_{16}$			
$002F_{16}$			
0030_{16}			
0031_{16}			
0032_{16}			
0033_{16}			
0034_{16}			
0035_{16}			
0036_{16}			
0037_{16}			
0038_{16}			
0039_{16}			
$003A_{16}$			
$003B_{16}$			
$003C_{16}$			
$003D_{16}$			
$003E_{16}$			
$003F_{16}$			

X : Undefined
NOTES:
1. Blank columns are all reserved space. No access is allowed.
2. Software reset or the watchdog timer reset does not affect this register.
3. Owing to Reset input.
4. In the case of RESET pin = H retaining.

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R8C/13 Group

4. Special Function Register (SFR)

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆			
0049₁₆			
004A₁₆			
004B₁₆			
004C₁₆			
004D₁₆	Key input interrupt control register	KUPIC	XXXXX0002
004E₁₆	A-D conversion interrupt control register	ADIC	XXXXX0002
004F₁₆			
0050₁₆	Compare 1 interrupt control register	CMP1IC	XXXXX0002
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055₁₆	INT2 interrupt control register	INT2IC	XXXXX0002
0056₁₆	Timer X interrupt control register	TXIC	XXXXX0002
0057₁₆	Timer Y interrupt control register	TYIC	XXXXX0002
0058₁₆	Timer Z interrupt control register	TZIC	XXXXX0002
0059₁₆	INT1 interrupt control register	INT1IC	XXXXX0002
005A₁₆	INT3 interrupt control register	INT3IC	XXXXX0002
005B₁₆	Timer C interrupt control register	TCIC	XXXXX0002
005C₁₆	Compare 0 interrupt control register	CMP0IC	XXXXX0002
005D₁₆	INT0 interrupt control register	INT0IC	XX00X0002
005E₁₆			
005F₁₆			
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

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R8C/13 Group
4. Special Function Register (SFR)

Address	Register	Symbol	After reset
0080_{16}	Timer Y, Z mode register	TYZMR	00_{16}
0081_{16}	Prescaler Y	PREY	FF_{16}
0082_{16}	Timer Y secondary	TYSC	FF_{16}
0083_{16}	Timer Y primary	TYPR	FF_{16}
0084_{16}	Timer Y, Z waveform output control register	PUM	00_{16}
0085_{16}	Prescaler Z	PREZ	FF_{16}
0086_{16}	Timer Z secondary	TZSC	FF_{16}
0087_{16}	Timer Z primary	TZPR	FF_{16}
0088_{16}			
0089_{16}			
$008A_{16}$	Timer Y, Z output control register	TYZOC	00_{16}
$008B_{16}$	Timer X mode register	TXMR	00_{16}
$008C_{16}$	Prescaler X	PREX	FF_{16}
$008D_{16}$	Timer X register	TX	FF_{16}
$008E_{16}$	Count source set register	TCSS	00_{16}
$008F_{16}$			
0090_{16}	Timer C register	TC	00_{16}
0091_{16}			00_{16}
0092_{16}			
0093_{16}			
0094_{16}			
0095_{16}			
0096_{16}	External input enable register	INTEN	00_{16}
0097_{16}			
0098_{16}	Key input enable register	KIEN	00_{16}
0099_{16}			
$009A_{16}$	Timer C control register 0	TCC0	00_{16}
$009B_{16}$	Timer C control register 1	TCC1	00_{16}
$009C_{16}$	Capture, compare 0 register	TM0	XX_{16}
$009D_{16}$			XX_{16}
$009E_{16}$	Compare 1 register	TM1	XX_{16}
$009F_{16}$			XX_{16}
$00A0_{16}$	UART0 transmit/receive mode register	U0MR	00_{16}
$00A1_{16}$	UART0 bit rate generator	U0BRG	XX_{16}
$00A2_{16}$	UART0 transmit buffer register	U0TB	XX_{16}
$00A3_{16}$			XX_{16}
$00A4_{16}$	UART0 transmit/receive control register 0	U0C0	00001000_2
$00A5_{16}$	UART0 transmit/receive control register 1	U0C1	00000010_2
$00A6_{16}$	UART0 receive buffer register	U0RB	XX_{16}
$00A7_{16}$			XX_{16}
$00A8_{16}$	UART1 transmit/receive mode register	U1MR	00_{16}
$00A9_{16}$	UART1 bit rate generator	U1BRG	XX_{16}
$00AA_{16}$	UART1 transmit buffer register	U1TB	XX_{16}
$00AB_{16}$			XX_{16}
$00AC_{16}$	UART1 transmit/receive control register 0	U1C0	00001000_2
$00AD_{16}$	UART1 transmit/receive control register 1	U1C1	00000010_2
$00AE_{16}$	UART1 receive buffer register	U1RB	XX_{16}
$00AF_{16}$			XX_{16}
$00B0_{16}$	UART transmit/receive control register 2	UCON	00_{16}
$00B1_{16}$			
$00B2_{16}$			
$00B3_{16}$			
$00B4_{16}$			
$00B5_{16}$			
$00B6_{16}$			
$00B7_{16}$			
$00B8_{16}$			
$00B9_{16}$			
$00BA_{16}$			
$00BB_{16}$			
$00BC_{16}$			
$00BD_{16}$			
$00BE_{16}$			
$00BF_{16}$			

X : Undefined
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R8C/13 Group   4. Special Function Register (SFR)

Address	Register	Symbol	After reset
$00C0_{16}$	A-D register	AD	XX_{16}
$00C1_{16}$			XX_{16}
$00C2_{16}$			
$00C3_{16}$			
$00C4_{16}$			
$00C5_{16}$			
$00C6_{16}$			
$00C7_{16}$			
$00C8_{16}$			
$00C9_{16}$			
$00CA_{16}$			
$00CB_{16}$			
$00CC_{16}$			
$00CD_{16}$			
$00CE_{16}$			
$00CF_{16}$			
$00D0_{16}$			
$00D1_{16}$			
$00D2_{16}$			
$00D3_{16}$			
$00D4_{16}$	A-D control register 2	ADCON2	00_{16}
$00D5_{16}$			
$00D6_{16}$	A-D control register 0	ADCON0	$00000XXX_2$
$00D7_{16}$	A-D control register 1	ADCON1	00_{16}
$00D8_{16}$			
$00D9_{16}$			
$00DA_{16}$			
$00DB_{16}$			
$00DC_{16}$			
$00DD_{16}$			
$00DE_{16}$			
$00DF_{16}$			
$00E0_{16}$	Port P0 register	P0	XX_{16}
$00E1_{16}$	Port P1 register	P1	XX_{16}
$00E2_{16}$	Port P0 direction register	PD0	00_{16}
$00E3_{16}$	Port P1 direction register	PD1	00_{16}
$00E4_{16}$			
$00E5_{16}$	Port P3 register	P3	XX_{16}
$00E6_{16}$			
$00E7_{16}$	Port P3 direction register	PD3	00_{16}
$00E8_{16}$	Port P4 register	P4	XX_{16}
$00E9_{16}$			
$00EA_{16}$	Port P4 direction register	PD4	00_{16}
$00EB_{16}$			
$00EC_{16}$			
$00ED_{16}$			
$00EE_{16}$			
$00EF_{16}$			
$00F0_{16}$			
$00F1_{16}$			
$00F2_{16}$			
$00F3_{16}$			
$00F4_{16}$			
$00F5_{16}$			
$00F6_{16}$			
$00F7_{16}$			
$00F8_{16}$			
$00F9_{16}$			
$03FA_{16}$			
$00FB_{16}$			
$00FC_{16}$	Pull-up control register 0	PUR0	$00XX0000_2$
$00FD_{16}$	Pull-up control register 1	PUR1	$XXXXXX0X_2$
$00FE_{16}$	Port P1 drivability control register	DRR	00_{16}
$00FF_{16}$	Timer C output control register	TCOUT	00_{16}
$01B3_{16}$	Flash memory control register 4	FMR4	$0100000X_2$
$01B4_{16}$			
$01B5_{16}$	Flash memory control register 1	FMR1	$1000000X_2$
$01B6_{16}$			
$01B7_{16}$	Flash memory control register 0	FMR0	$XX000001_2$

X : Undefined
Blank columns are all reserved space. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}	Supply voltage	$V_{CC}=AV_{CC}$	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage	$V_{CC}=AV_{CC}$	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_{opr}=25°C	300	mW
T_{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	$^\circ$C
T_{stg}	Storage temperature		-65 to 150	$^\circ$C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard Min.	Standard Typ.	Standard Max.	Unit
V_{CC}	Supply voltage			2.7	5.0	5.5	V
AV_{CC}	Analog supply voltage			——	V_{CC}	——	V
V_{ss}	Supply voltage			——	0	——	V
AV_{ss}	Analog supply voltage			——	0	——	V
V_{IH}	"H" input voltage			0.8V_{CC}	——	V_{CC}	V
V_{IL}	"L" input voltage			0	——	0.2V_{CC}	V
$I_{OH (sum)}$	"H" peak all output currents	Sum of all pins' IOH (peak)		——	——	-60.0	mA
$I_{OH (peak)}$	"H" peak output current			——	——	-10.0	mA
$I_{OH (avg)}$	"H" average output current			——	——	-5.0	mA
$I_{OL (sum)}$	"L" peak all output currents	Sum of all pins' IOL (peak)		——	——	60	mA
$I_{OL (peak)}$	"L" peak output current	Except P1$_0$ to P1$_7$		——	——	10	mA
		P1$_0$ to P1$_7$	Drive ability HIGH	——	——	30	mA
			Drive ability LOW	——	——	10	mA
$I_{OL (avg)}$	"L" average output current	Except P1$_0$ to P1$_7$		——	——	5	mA
		P1$_0$ to P1$_7$	Drive ability HIGH	——	——	15	mA
			Drive ability LOW	——	——	5	mA
f (X_{IN})	Main clock input oscillation frequency	3.0V $\le$ Vcc $\le$ 5.5V		0	——	20	MHz
		2.7V $\le$ Vcc < 3.0V		0	——	10	MHz

Note
 1: Referenced to V_{CC} = AV_{CC} = 2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
 2: The mean output current is the mean value within 100ms.

Table 5.3 A-D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		Vref =VCC			10	Bit
–	Absolute accuracy	10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V			±3	LSB
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V			±2	LSB
		10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=3.3V			±5	LSB
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=3.3V			±2	LSB
R_{LADDER}	Ladder resistance		VREF=VCC	10		40	kΩ
t_{CONV}	Conversion time	10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V	3.3			µs
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V	2.8			µs
V_{REF}	Reference voltage			2.0		Vcc	V
V_{IA}	Analog input voltage			0		Vref	V
–	A-D operation clock frequency[2]	Without sample & hold		0.25		10	MHz
		With sample & hold		1.0		10	MHz

Note

1: Referenced to VCC=AVCC=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.

2: When fAD is 10 MHz more, divide the fAD and make A-D operation clock frequency (ØAD) lower than 10 MHz.

3: When the Vcc is less than 4.2V, divide the fAD and make A-D operation clock frequency (ØAD) lower than fAD/2.
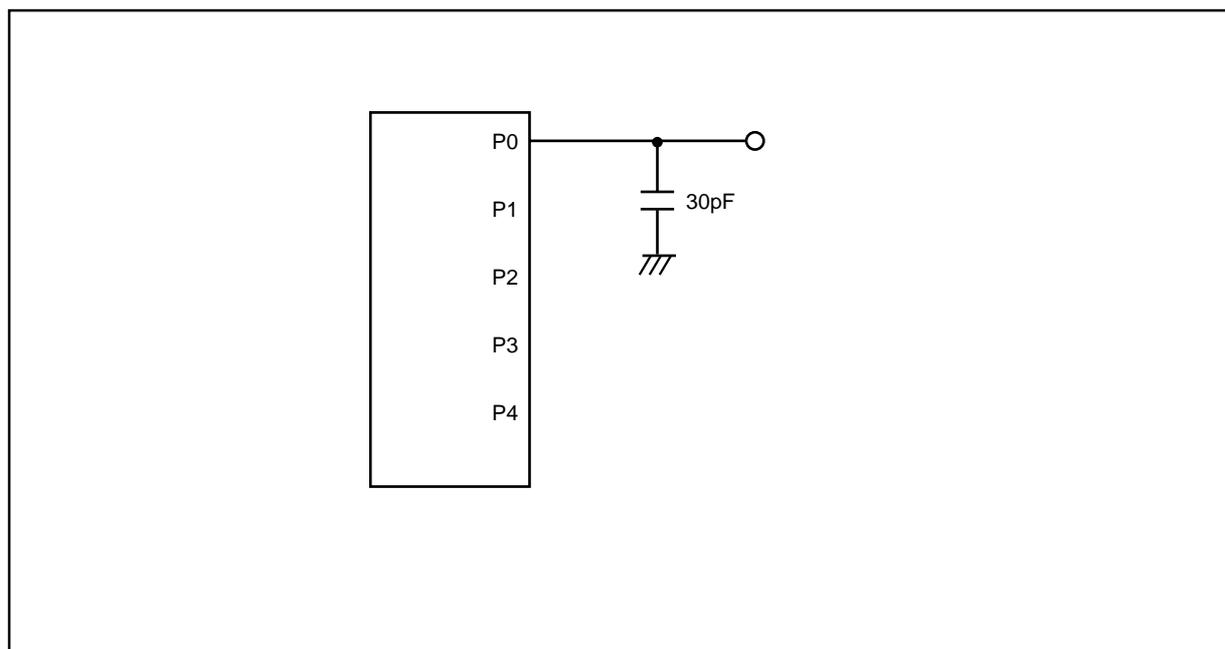
Figure 5.1 Port P0 to P4 measurement circuit

Table 5.4 Flash Memory (Program area) Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase cycle [2]		100 [3]	—	—	cycle
–	Byte program time	V_{CC} = 5.0 V at Topr = 25 °C	—	50	—	µs
–	Block erase time	V_{CC} = 5.0 V at Topr = 25 °C	—	0.4	—	s
td(SR-ES)	Time delay from Suspend Request until Erase Suspend		—	—	TBD	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program, Erase Temperature		0	—	60	°C
–	Data-retention duration	Topr = 55 °C	—	—	20	year

Table 5.5 Flash Memory (Data area Block A, Block B) Electrical Characteristics [4]

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase endurance[2]		10000 [3]	—	—	times
–	Byte program time(program/erase endurance ≤1000 times)	V_{CC} = 5.0 V at Topr = 25 °C	—	50	400	µs
–	Byte program time(program/erase endurance >1000 times)	V_{CC} = 5.0 V at Topr = 25 °C	—	65	—	µs
–	Block erase time(program/erase endurance ≤1000 times)	V_{CC} = 5.0 V at Topr = 25 °C	—	0.2	9	s
–	Block erase time(program/erase endurance >1000 times)	V_{CC} = 5.0 V at Topr = 25 °C	—	0.3	—	s
td(SR-ES)	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program/Erase Temperature		-20(-40)[8]	—	85	°C
–	Data-retention duration	Topr = 55 °C	—	—	20	year

Note
 1: Referenced to V_{CC}=AVcc=2.7 to 5.5V at Topr = 0 to 60 °C unless otherwise specified.
 2: Definition of Program/Erase
    The cycle of Program/Erase shows a cycle for each block.
    If the program/erase number is "n" (n = 100, 10000), "n" times erase can be performed for each block.
    For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.
    However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).
 3: Maximum numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.
 4: Table 5.5 applies for Block A or B when the Program/Erase cycles are more than 1000. The byte program time and block erase time up to 1000 cycles are the same as that of the program area (see Table 5.4).
 5: To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.
 6: If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.
 7: Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
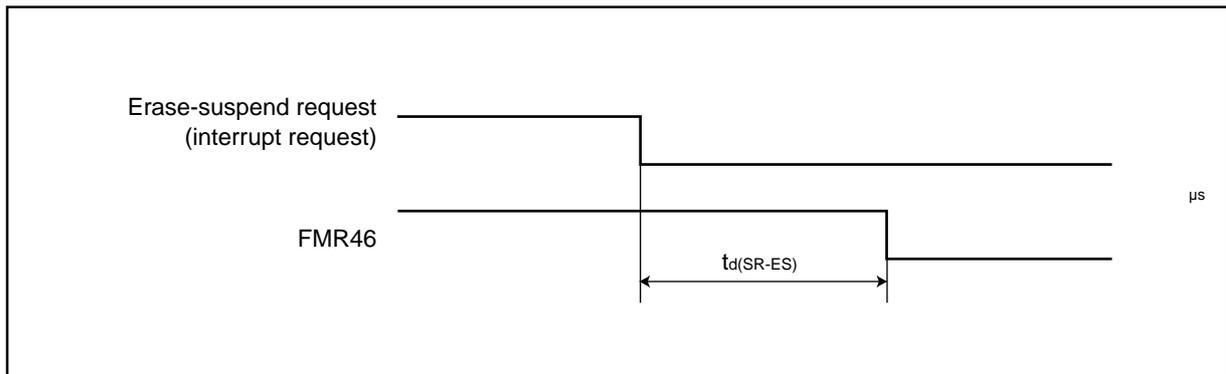 8: -40 °C for D version.

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Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Min.	Standard Typ.	Max.	Unit
Vdet4	Voltage detection level		3.3	3.8	4.3	V
	Voltage detection interrupt request generating time[2]			40		µs
	Voltage detection circuit self consumption current	VC27=1, VCC=5.0V		600		nA
td(E-A)	Waiting time till voltage detection circuit operation starts[3]				20	µs

NOTES:
1. The measureing condition is Vcc=AVcc=5.0 V and Topr=25 °C.
2. This shows the time till the voltage detection interrupt request is generated since the voltage passes Vdet.
3. This shows the required time till the voltage detection circuit operates when setting to "1" again after setting the VC27 bit in the VCR2 register to "0".

Table 5.7 Power-on Reset Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Min.	Standard Typ.	Max.	Unit
	Power-on reset start time[2]	Vcc<0.5V	TBD			ms
	Power-on reset cancel operation start voltage		3.3	3.8	4.3	V
	Hardware reset 2 cancel operation start voltage		3.3	3.8	4.3	V
	Supply start up condition when using power-on reset circuit	Intergradation time to 0V<2.7V			TBD	ms

Note
1: The measuring condition is Vcc=AVcc=5.0 V and Topr=25 °C.
2: Keep Vcc<0.5V for over regulated time to execute the reset operation.
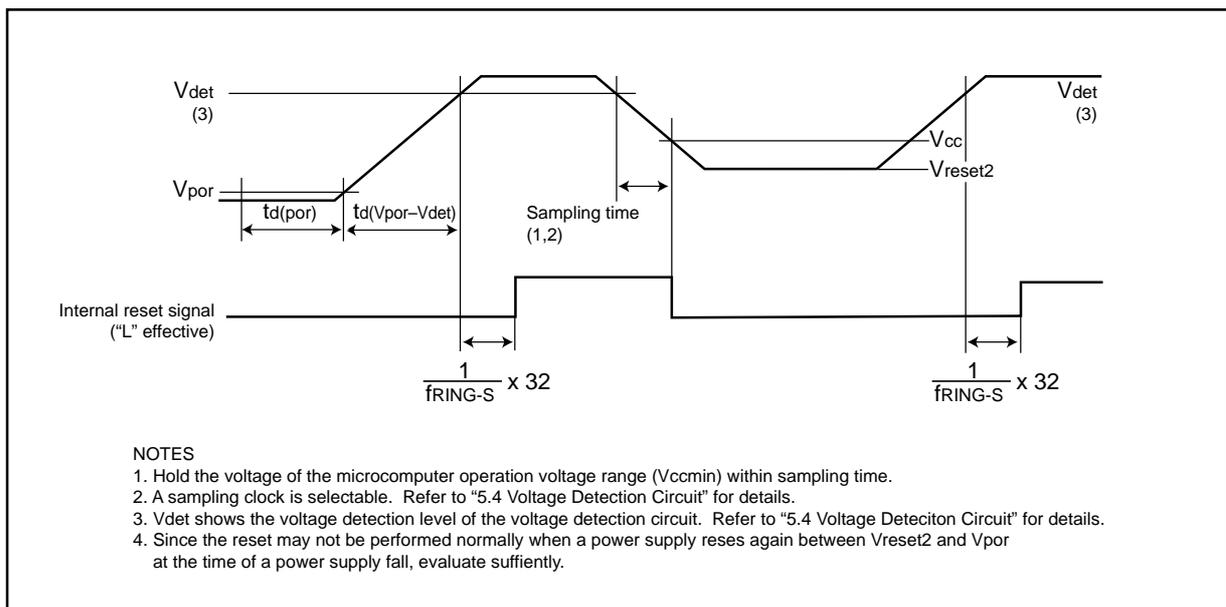
NOTES
1. Hold the voltage of the microcomputer operation voltage range (Vccmin) within sampling time.
2. A sampling clock is selectable. Refer to "5.4 Voltage Detection Circuit" for details.
3. Vdet shows the voltage detection level of the voltage detection circuit. Refer to "5.4 Voltage Deteciton Circuit" for details.
4. Since the reset may not be performed normally when a power supply reses again between Vreset2 and Vpor at the time of a power supply fall, evaluate suffiently.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.8 High-speed Ring Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Min.	Standard Typ.	Max.	Unit
	High-speed ring oscillator frequency 1 / {td(HRoffset)+td(HR)} when the reset is released	VCC=5.0V, Topr=25 °C Set "40_{16}" in the HR1 register		8		MHz
td(HRoffset)	Settable high-speed ring oscillator minimum period	VCC=5.0V, Topr=25 °C Set "00_{16}" in the HR1 register		61		ns
td(HR)	High-speed ring oscillator adjusted unit	Differences when setting "01_{16}" and "00_{16}" in the HR register		1		ns
	High-speed ring oscillator temperature dependence(1)	Frequency fluctuation in temperature range of -10 °C to 50 °C		±5		%
	High-speed ring oscillator temperature dependence(2)	Frequency fluctuation in temperature range of -40 °C to 80 °C		±10		%

NOTES:
1. The measuring condition is Vcc=AVcc=5.0 V and Topr=25 °C.

Table 5.9 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Min.	Standard Typ.	Max.	Unit
Vdet4	Voltage detection level		3.3	3.8	4.3	V
	Voltage detection interrupt request generating time[2]			40		V
	Voltage detection circuit self consumption current	VC27="1"		TBD		V
td(E-A)	Waiting time till voltage detection circuit operation starts[3]				20	V

Note
1: The measureing condition is Vcc=AVcc=5.0 V and Topr=25 °C.
2: This shows the time till the voltage detection interrupt request is generated since the voltage passes Vdet.
3: This shows the required time till the voltage detection circuit operates when setting to "1" again.

Table 5.10 Electrical Characteristics (1)   [Vcc=5V]

Symbol	Parameter		Measuring condition		Min.	Standard Typ.	Max.	Unit
VOH	"H" output voltage	Except XOUT	IOH=-5mA		Vcc-2.0		Vcc	V
			IOH=-200µA		Vcc-0.3		Vcc	V
		XOUT	Drive ability HIGH	IOH=-1 mA	Vcc-2.0		Vcc	V
			Drive ability LOW	IOL=-500µA	Vcc-2.0		Vcc	V
VOL	"L" output voltage	P10 to P17 Except XOUT	IOH= 5 mA				2.0	V
			IOH= 200 µA				0.45	V
		P10 to P17	Drive ability HIGH	IOH= 10 mA			2.0	V
			Drive ability LOW	IOL= 5 mA			2.0	V
		XOUT	Drive ability HIGH	IOH= 1 mA			2.0	V
			Drive ability LOW	IOL=500µA			2.0	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1			0.2		1.0	V
		RESET			0.2		2.2	V
IIH	"H" input current		VI=5V				5.0	µA
IIL	"L" input current		VI=0V				-5.0	µA
RPULLUP	Pull-up resistance		VI=0V		30	50	167	kΩ
RfXIN	Feedback resistance	XIN				1.0		MΩ
fRING-S	Low-speed ring oscillator frequency				40	125	250	kHz
VRAM	RAM retention voltage		At stop mode		2.0			V

NOTES:
1. Referenced to VCC=AVCC=4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=20MHz unless otherwise specified.

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Table 5.11 Electrical Characteristics (2)   [Vcc=5V]

Symbol	Parameter	Measuring condition		Min.	Standard Typ.	Max.	Unit
Icc	Power supply current (Vcc=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are Vss	High-speed mode	X_{IN}=20 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		9	15	mA
			X_{IN}=16 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		8	14	mA
			X_{IN}=10 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		5		mA
		Medium-speed mode	X_{IN}=20 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		4		mA
			X_{IN}=16 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		3		mA
			X_{IN}=10 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		2		mA
		High-speed ring oscillator mode	Main clock off High-speed ring oscillator on=8 MHz Low-speed ring oscillator on=125 kHz No division		4	8	mA
			Main clock off High-speed ring oscillator on=8 MHz Low-speed ring oscillator on=125 kHz Division by 8		1.5		mA
		Low-speed ring oscillator mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		0.4	2.0	mA
		Wait mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation		TBD	TBD	μA
		Wait mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off		TBD	TBD	μA
		Stop mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator off CM10="1" Peripheral clock off VC27="0"		0.8	3.0	μA

Note
1: The power supply current measuring is executed using the measuring program on frash memory.
2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: V$_{CC}$ = 5V, V$_{SS}$ = 0V at Ta = 25 °C) [V$_{CC}$=5V]

Table 5.12 X$_{IN}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(X$_{IN}$)	X$_{IN}$ input cycle time	62.5		ns
tWH(X$_{IN}$)	X$_{IN}$ input HIGH pulse width	30		ns
tWL(X$_{IN}$)	X$_{IN}$ input LOW pulse width	30		ns

Table 5.13 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	100		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	40		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	40		ns

Table 5.14 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	400 [1]		ns
tWH(TCIN)	TCIN input HIGH pulse width	200 [2]		ns
tWL(TCIN)	TCIN input LOW pulse width	200 [2]		ns

Note
1 : Use the greater value,either (1/ digital filter clock frequency x 6) or min. value.
2 : Use the greater value,either (1/ digital filter clock frequency x 3) or min. value.

Table 5.15 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	200		ns
tW(CKH)	CLKi input HIGH pulse width	100		ns
tW(CKL)	CLKi input LOW pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	35		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.16 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	$\overline{INT0}$ input HIGH pulse width	250 [1]		ns
tW(INL)	$\overline{INT0}$ input LOW pulse width	250 [2]		ns

Note
1 : When the $\overline{INT0}$ input filter select bit selects the digital filter, use the $\overline{INT0}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or min. value.
2 : When the $\overline{INT0}$ input filter select bit selects the digital filter, use the $\overline{INT0}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or min. value.
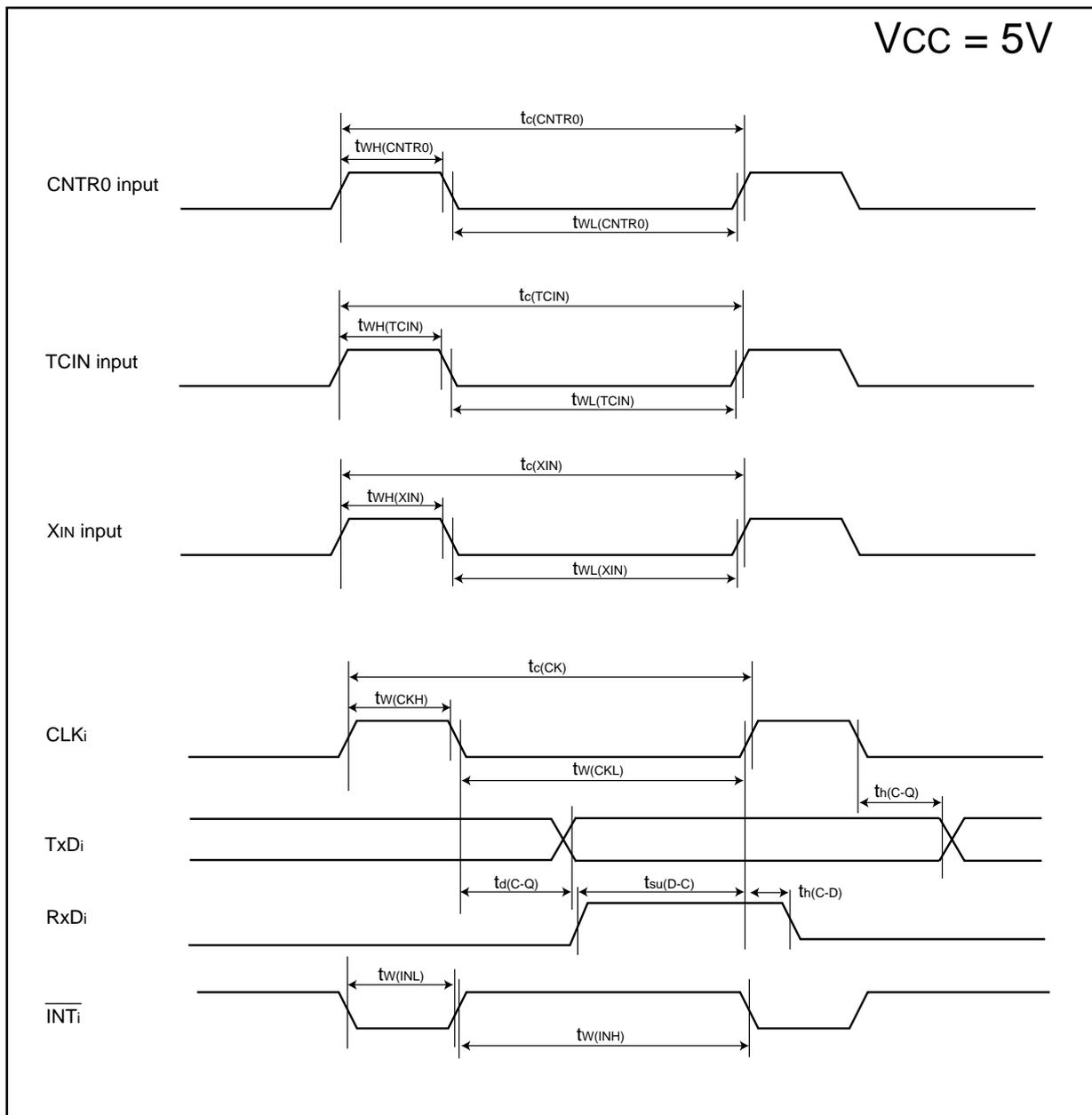
Figure 5.4 Vcc=5V timing diagram

Table 5.17 Electrical Characteristics (3)   [Vcc=3V]

Symbol	Parameter		Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-1mA		Vcc-0.5		Vcc	V
		X_{OUT}	Drive ability HIGH	I_{OH}=-0.1 mA	Vcc-0.5		Vcc	V
			Drive ability LOW	I_{OL}=-50 μA	Vcc-0.5		Vcc	V
V_{OL}	"L" output voltage	P10 to P17 Except X_{OUT}	I_{OH}= 1 mA				0.5	V
		P10 to P17	Drive ability HIGH	I_{OH}= 2 mA			0.5	V
			Drive ability LOW	I_{OL}= 1 mA			0.5	V
		X_{OUT}	Drive ability HIGH	I_{OH}= 0.1 mA			0.5	V
			Drive ability LOW	I_{OL}=50 μA			0.5	V
V_{T+}-V_{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1			0.2		0.8	V
		RESET			0.2		1.8	V
I_{IH}	"H" input current		V_I=3V				4.0	μA
I_{IL}	"L" input current		V_I=0V				-4.0	μA
R_{PULLUP}	Pull-up resistance		V_I=0V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	X_{IN}				3.0		MΩ
f_{RING-S}	Low-speed ring oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0			V

Note

1 : Referenced to Vcc=AVcc=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.

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Table 5.18 Electrical Characteristics (4)   [Vcc=3V]

Symbol	Parameter	Measuring condition		Min.	Standard Typ.	Max.	Unit
Icc	Power supply current (Vcc=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are Vss	High-speed mode	X_{IN}=20 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		8	13	mA
			X_{IN}=16 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		7	12	mA
			X_{IN}=10 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		5		mA
		Medium-speed mode	X_{IN}=20 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		3		mA
			X_{IN}=16 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		2.5		mA
			X_{IN}=10 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		1.6		mA
		High-speed ring oscillator mode	Main clock off High-speed ring oscillator on=8 MHz Low-speed ring oscillator on=125 kHz No division		3.5	7.5	mA
			Main clock off High-speed ring oscillator on=8 MHz Low-speed ring oscillator on=125 kHz Division by 8		1.5		mA
		Low-speed ring oscillator mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		0.4	2.0	mA
		Wait mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation		TBD	TBD	µA
		Wait mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off		TBD	TBD	µA
		Stop mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator off CM10="1" Peripheral clock off VC27="0"		0.7	3.0	µA

Note

1: The power supply current measuring is executed using the measuring program on frash memory.

2: Timer Y is operated with timer mode.

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Timing requirements (Unless otherwise noted: Vcc = 3V, Vss = 0V at Ta = 25 °C) [Vcc=3V]

Table 5.19 Xɪɴ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	143		ns
tWH(XIN)	XIN input HIGH pulse width	70		ns
tWL(XIN)	XIN input LOW pulse width	70		ns

Table 5.20 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	300		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	120		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	120		ns

Table 5.21 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	1200 [1]		ns
tWH(TCIN)	TCIN input HIGH pulse width	600 [2]		ns
tWL(TCIN)	TCIN input LOW pulse width	600 [2]		ns

Note
1 : Use the greater value,either (1/ digital filter clock frequency x 6) or min. value.
2 : Use the greater value,either (1/ digital filter clock frequency x 3) or min. value.

Table 5.22 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	300		ns
tW(CKH)	CLKi input HIGH pulse width	150		ns
tW(CKL)	CLKi input LOW pulse width	150		ns
td(C-Q)	TxDi output delay time		160	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	55		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.23 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	$\overline{INT0}$ input HIGH pulse width	380 [1]		ns
tW(INL)	$\overline{INT0}$ input LOW pulse width	380 [2]		ns

Note
1 : When the $\overline{INT0}$ input filter select bit selects the digital filter, use the $\overline{INT0}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or min. value.
2 : When the $\overline{INT0}$ input filter select bit selects the digital filter, use the $\overline{INT0}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or min. value.
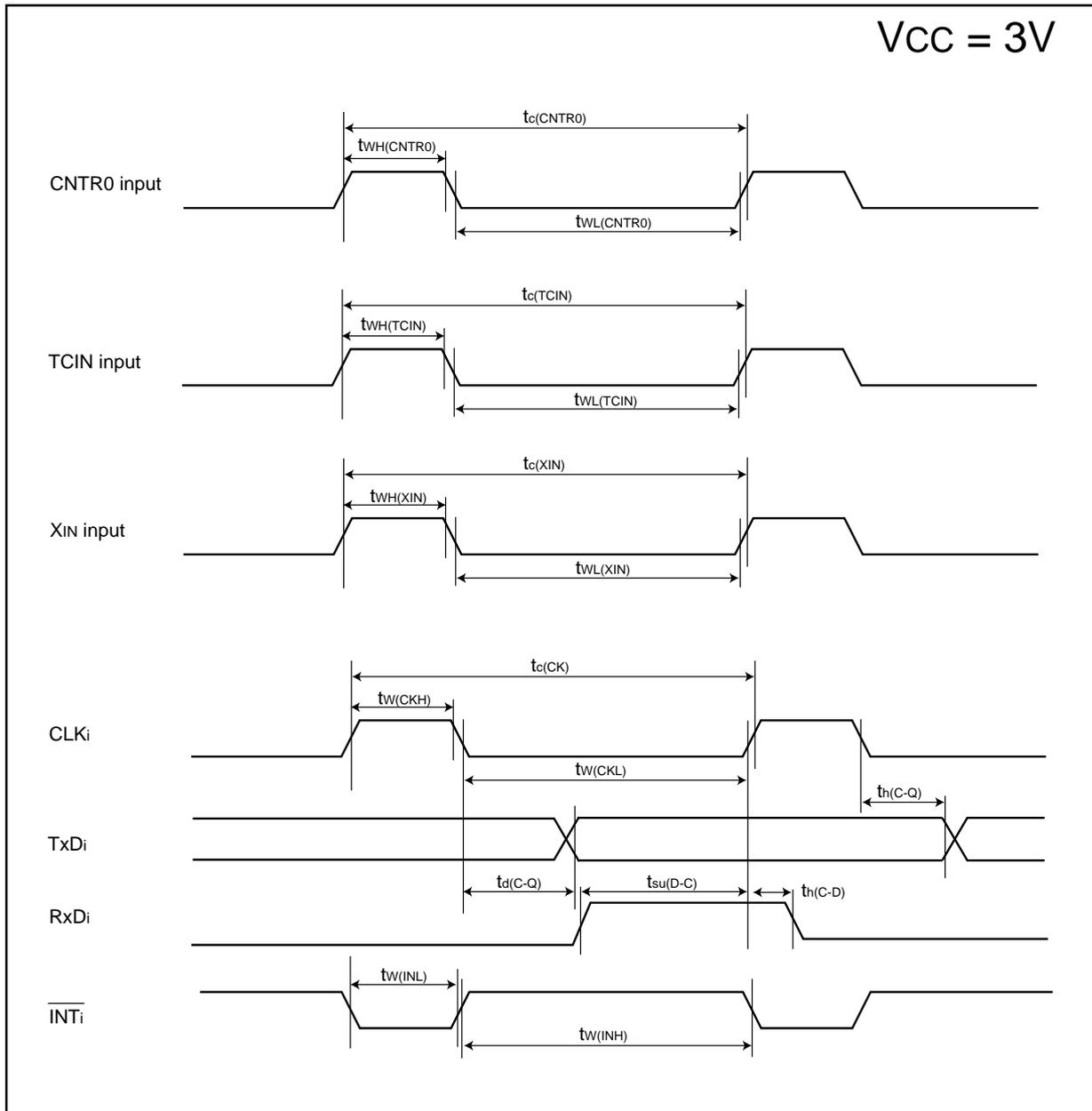
Figure 5.5 Vcc=3V timing diagram

Package Dimensions

32P6U-A   (MMP)   **Plastic 32pin 7×7mm body LQFP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP32-P-0707-0.80	–		Cu Alloy
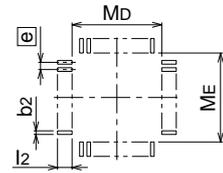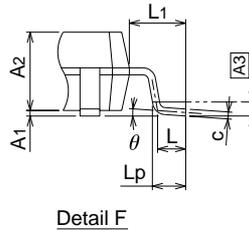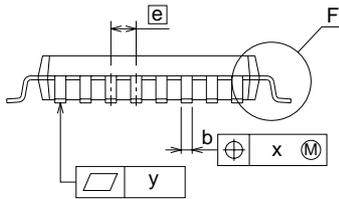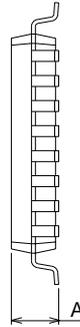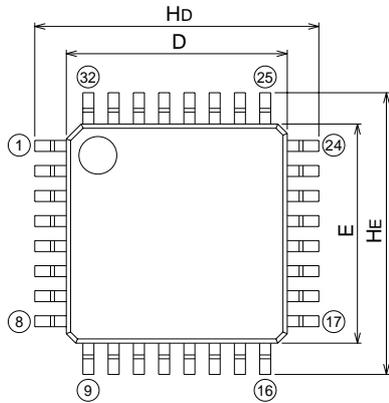
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.8	–
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
L	0.3	0.5	0.7
L_1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.2
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.5	–
I_2	1.0	–	–
M_D	–	7.4	–
M_E	–	7.4	–

Detail F

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REVISION HISTORY			R8C/13 Group Data Sheet	
Rev.	Date		Description	
		Page	Summary	
0.10	Oct 28, 2003		First edition issued	
0.20	Dec05, 2003	5	Figure 1.3 revised	
		10	Chapter 4, NOTES revised	
		16	Table 5.4 revised Table 5.5 revised	
		17	Table 5.6 revised Figure 5.3 added	
		18	Table 5.8 revised Table 5.10 revised	
		21	Figure 5.3 revised to Figure 5.4	
		22	Table 5.17 revised	
		25	Figure 5.4 revised to Figure 5.5	

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