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M16C/26A Group (M16C/26A, M16C/26T)

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

1. Overview

The M16C/26A group (M16C/26A, M16C/26T) of single-chip microcomputers is built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and is packaged in a 42-pin and 48pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and a DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations. There is a Normal-ver. for M16C/26A and T-ver. and v-ver. for M16C/26T.

1.1 Applications

Audio, cameras, office equipment, communications equipment, portable equipment,

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.



1.2 Performance Outline

Table 1.1 lists performance outline of M16C/26A group (M16C/26A, M16C/26T) 48-pin device. Table 1.2 lists performance outline of M16C/26A 42-pin device.

Table 1.1.	Performance outline of M16C/26A	group (48-pin device)(M16C/26A,	M16C/26T)
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	Item	Performance		
CPU	Number of basic instructions	91 instructions		
	Shortest instruction	50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V) (M16C/26A, M16C/26T(T-ver.))		
		100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V) (M16C/26A)		
		50 ns (f(BCLK)= 20MHz, Vcc= 4.2V to 5.5V -40 to 105°C) (M16C/26T(V-ver.))		
		62.5 ns (f(BCLK)= 16MHz, VCC= 4.2V to 5.5V -40 to 125°C) (M16C/26T(V-ver.))		
	Operation mode	Single chip mode		
	Address space	1M byte		
	Memory capacity	ROM/RAM : See the product list		
Peripheral	Port	Input/Output : 39 lines		
function	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels		
		Three-phase Motor Control Timer		
	Serial I/O	2 channels (UART, clock synchronous serial I/O)		
		1 channel (UART, clock synchronous, I ² C bus ¹ , or IEBus ²)		
	A/D converter	10 bit A/D Converter : 1 circuit, 12 channels		
	DMAC	2 channels		
	CRC calcuration circuit	2 polynomial (CRC-CCITT and CRC-16) with MSB/LSB selectable		
	Watchdog timer	15 bits x 1 channel (with prescaler)		
	Interrupt	20 internal and 8 external sources, 4 software sources, 7 levels		
	Clock generation circuit	4 circuits		
		Main clock(*), Sub-clock(*)		
		On-chip oscillator, PLL frequency synthesizer		
		(*)These circuit contain a built-in feedback resister.		
	Oscillation stop detection	Main clock oscillation stop, re-oscillation detection function		
	Low voltage detection circuit	Available (M16C/26A) Not available (M16C/26T)		
Electrical	Power supply voltage	Vcc=3.0V to 5.5V (f(BCLK)=20MHz) (M16C/26A)		
Characteristics		Vcc=2.7V to 5.5V (f(BCLK)=10MHz)		
		Vcc=3.0V to 5.5V (M16C/26T(T-ver.))		
		Vcc=4.2V to 5.5V (M16C/26T(V-ver.))		
	Power consumption	16mA (Vcc=5V, f(BCLK)=20MHz)		
		25 μA (Vcc=3V, f(BCLK)=f(Xcin)=32KHz on RAM)		
		1.8 μA (Vcc=3V, f(BCLK)=f(Xcin)=32KHz, in wait mode)		
		0.7 μA (Vcc=3V, when stop mode)		
Flash memory	Program/erase voltage	2.7V to 5.5V (M16C/26A)		
		3.0V to 5.5V (M16C/26T(T-ver.)) 4.2V to 5.5V (M16C/26T(V-ver.))		
	Number of program/erase	100 times (Block A ,Block B : 10,000 times (option ³))		
Operating am	bient temperature	-20 to 85°C / -40 to 85°C ⁴ (M16C/26A)		
-	-	-40 to 85°C (M16C/26T(T-ver.))		
		-40 to 105°C / -40 to 125°C (M16C/26T(V-ver.))		
Package		48-pin plastic molded QFP		

Notes:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.

2. IEBus is a trademark of NEC Electronics Corporation.

3. If you desire this option, please so specify.

4. See Table 1.6 for the operating ambient temperature.

Item		Performance	
CPU	Number of basic instructions	91 instructions	
	Shortest instruction	50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V)	
		100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V)	
	Operation mode	Single chip mode	
	Address space	1M byte	
	Memory capacity	ROM/RAM : See the product list	
Peripheral	Port	Input/Output : 33 lines	
function	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels	
		Three-phase Motor Control Timer	
	Serial I/O	1 channel (UART, clock synchronous serial I/O)	
		1 channel (UART, clock synchronous, I ² C bus ¹ , or IEBus ²)	
	A/D converter	10 bit A/D Converter : 1 circuit, 10 channels	
	DMAC	2 channels	
	CRC calcuration circuit	2 polynomial (CRC-CCITT and CRC-16) with MSB/LSB selectable	
	Watchdog timer	15 bits x 1 channel (with prescaler)	
	Interrupt	18 internal and 8 external sources, 4 software sources, 7 levels	
	Clock generation circuit	4 circuits	
		Main clock(*), Sub-clock(*)	
		On-chip oscillator, PLL frequency synthesizer	
		(*)These circuit contain a built-in feedback resister.	
	Oscillation stop detection	Main clock oscillation stop, re-oscillation detection function	
	Low voltage detection circuit	Available	
Electrical	Power supply voltage	Vcc=3.0V to 5.5V (f(BCLK)=20MHz)	
Characteristics		Vcc=2.7V to 5.5V (f(BCLK)=10MHz)	
	Power consumption	16mA (Vcc=5V, f(BCLK)=20MHz)	
		25 μ A (Vcc=3V, f(BCLK)=f(X _{CIN})=32KHz on RAM)	
		1.8 μA (Vcc=3V, f(BCLK)=f(Xcin)=32KHz, in wait mode)	
		0.7 μA (Vcc=3V, when stop mode)	
Flash memory	Program/erase voltage	2.7V to 5.5V	
	Number of program/erase	100 times(all area) or 1,000 times(program ara)/10,000 times(data area) ³	
Operating ambient temperature		-20 to 85°C / -40 to 85°C ³	
Package		42-pin plastic molded SSOP	

Table 1.2. Performance outline of M16C/26A group (42-pin device) (M16C/26A)

Notes:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.

2. IEBus is a trademark of NEC Electronics Corporation.

3. See Table 1.6 for the number of program/erase and the operating ambient temperature.

1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/26A group, 48-pin device.



Figure 1.1. M16C/26A Group, 48-pin Block Diagram

Figure 1.2 is a block diagram of the M16C/26A group, 42-pin device.



Figure 1.2. M16C/26A Group, 42-pin Block Diagram

As of Jun 2004

1.4 Product List

Tables 1.3 to 1.5 list the M16C/28 group products and Figure 1.3 shows the type numbers, memory sizes and packages.

Table 1.3.	Product List	(1) -M16C/26A
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	-				Describe
Type No.		ROM capacity	RAM capacity	Package type	Remarks
M30260M3A-XXXGP	(D)	24K byte	1K byte		
M30260M4A-XXXGP	(D)	32K byte	1K byte	48P60	
M30260M6A-XXXGP	(D)	48K byte	2K byte		
M30260M8A-XXXGP	(D)	64K byte	2K byte	7	Maak DOM Varaian
M30263M3A-XXXFP	(D)	24K byte	1K byte		Wask ROW Version
M30263M4A-XXXFP	(D)	32K byte	1K byte		
M30263M6A-XXXFP	M30263M6A-XXXFP (D)		2K byte	- 42F2K	
M30263M8A-XXXFP	(D)	64K byte	2K byte		
M30260F3AGP	(D)	24K + 4K byte	1K byte		
M30260F4AGP	(D)	32K + 4K byte	1K byte	40000	
M30260F6AGP	(D)	48K + 4K byte	2K byte	48P6Q	
M30260F8AGP	(D)	64K + 4K byte	2K byte	7	Flash ROM Version
M30263F3AFP	(D)	24K + 4K byte	1K byte		
M30263F4AFP	(D)	32K + 4K byte	1K byte		
M30263F6AFP	(D)	48K + 4K byte	2K byte	- 42F2K	
M30263F8AFP	(D)	64K + 4K byte	2K byte		
	-	(D)	la mana a mat		

(P) : under planning (D) : under development

Table 1.4. Product List (2) -M16C/26T T-ver.

As of Jun 2004 Type No. ROM capacity RAM capacity Package type Remarks M30260M3T-XXXGP (P) 24K byte 1K byte M30260M4T-XXXGP (P) 32K byte 1K byte Mask ROM Version 48P6Q M30260M6T-XXXGP (P) 48K byte 2K byte M30260M8T-XXXGP (P) 64K byte 2K byte M30260F3TGP 24K + 4K byte 1K byte (D) M30260F4TGP (D) 32K + 4K byte 1K byte Flash ROM Version 48P6Q M30260F6TGP 48K + 4K byte 2K byte (D) M30260F8TGP (D) 64K + 4K byte 2K byte

(P) : under planning (D) : under development

NOTES: Specification of M16C/26T partly varies from the one of M16C/26A

Table 1 5	Product List	(3)	-M16C/26T	V-ver
Table 1.J.	FIOUUCI LIST	5		A-AGI

As of Jun 2004

Type No.		ROM capacity	RAM capacity	Package type	Remarks
M30260M3V-XXXGP	(P)	24K byte	1K byte		
M30260M4V-XXXGP	(P)	32K byte	1K byte	48P60	Mask ROM Version
M30260M6V-XXXGP	(P)	48K byte	2K byte		
M30260M8V-XXXGP	(P)	64K byte	2K byte		
M30260F3VGP	(D)	24K + 4K byte	1K byte		
M30260F4VGP	(D)	32K + 4K byte	1K byte	48P60	Flash ROM Version
M30260F6VGP	(D)	48K + 4K byte	2K byte		
M30260F8VGP	(D)	64K + 4K byte	2K byte		

(P) : under planning (D) : under development

NOTES: Specification of M16C/26T partly varies from the one of M16C/26A





Figure 1.3. Type No., Memory Size, and Package

Table 1.6. Product code	(Flash memor	y version, M16C/26A)
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		Internal (Program	ROM n area)	Internal ROM (Data area)			
Product Code	Package	Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	Operating Ambient Temperature	
D3				100	0°C to 60°C	-40°C to 85°C	
D5		100		100	0 0 10 60 0	-20°C to 85°C	
D7		4.000	0°C to 60°C	10.000	-40°C to 85°C	-40°C to 85°C	
D9		1,000		10,000	-20°C to 85°C	-20°C to 85°C	
U3		100		0 0 10 60 0	100	0°C to 60°C	-40°C to 85°C
U5	Lead-free			100	0.010.00.0	-20°C to 85°C	
U7		4.000	1	10.000	-40°C to 85°C	-40°C to 85°C	
U9		1,000		10,000	-20°C to 85°C	-20°C to 85°C	

(MASK ROM version, M16C/26A)

Product Code	Package	Operating Ambient Temperature
D3	Lood included	-40°C to 85°C
D5	Lead-Included	-20°C to 85°C
U3		-40°C to 85°C
U5	Lead-free	-20°C to 85°C

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1.5 Pin Configuration

Figures 1.5 and 1.6 show the pin configurations (top view).



Figure 1.5. Pin Configuration (Top View) of M16C/26A Group, 48-pin Package

Figure 1.6. Pin Configuration (Top View) of M16C/26A Group, 42-pin Package

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Table 1.6 and 1.7 describes the available pins.

Table 1.6. Pin Description(1)

Pin name	Signal name	I/O type	Function
Vcc,Vss	Power supply		Apply 0V to the Vss pin, and the following voltage to the Vcc pin.
	input		2.7 to 5.5V (M16C/26A)
			3.0 to 5.5V (M16C/26T T-ver.)
			4.2 to 5.5V (M16C/26T V-ver.)
CNVss	CNVss	Input	Connect this pin to Vss.
RESET	Reset input	Input	"L" on this input resets the microcomputer.
Xin	Clock input	Input	These pins are provided for the main clock generating circuit input/output.
Xout	Clock output	Output	Connect a ceramic resonator or crystal between the XIN and the XOUT pins.
			To use an externally derived clock, input it to the XIN pin and leave the XOUT
			pin open. If X _{IN} is not used (for external oscillator or external clock)
			connect XIN pin to Vcc and leave Xout pin open.
AVcc	Analog power		This pin is a power supply input for the A/D converter. Connect this
	supply input		pin to Vcc.
AVss	Analog power		This pin is a power supply input for the A/D converter. Connect this
	supply input		pin to Vss.
Vref	Reference	Input	This pin is a reference voltage input for the A/D converter.
	Voltage input		
P1₅~P17	I/O port P1	Input/	This is an 3-bit CMOS I/O port. It has an input/output port direction
		output	register that allows the user to set each pin for input or output individually.
			When used for input, a pull-up resister option can be selected for the
			entire group of three pins. Additional software selectable secondary
			functions are: 1) P1₅ to P17 can be configured as external INT interrupt
			pins; 2) P1₅ to P17 can be configured as position-data-retain function
			input pins,and; 3) P1₅ can input a trigger for the A/D converter.
P60~P67	I/O port P6	Input/	This is an 8-bit CMOS I/O port. It has an input/output port direction
		output	register that allows the user to set each pin for input or output individually.
			When used for input, a pull-up resister option can be selected for the
			entire group of four pins. Pins in this port also function as UART0 and
			UART1 I/O, as selected by software.P60 to P63 are not available in the 42
			pin version.
P70~P77	I/O port P7	Input/	This is an 8-bit I/O port equivalent to P6. P7 can also function as I/O for
		output	timer A0 to A3, as selected by software. Additional programming options
			are: P7o to P73 can assume UART1 I/O or UART2 I/O capabilities, and
			P72 to P75 can function as output pins for the three-phase motor control
			timer.

Table 1.7. Pin Description(2)

Pin name	Signal name	I/O type	Function
P80~P87	I/O port P8	Input/	This is an 8-bit I/O port equivalent to P6. Additional software-selectable
		output	secondary functions are: 1) $P8_0$ and $P8_1$ can act as either I/O for Timer
			A4, or as output pins for the three-phase motor control timer; 2) P82 to
			P8₄ can be configured as external INT interrupt pins. P8₄ can be used for
			Timer A Zphase function; 3) P8₅ can be used as NMI/SD. P8₅ can not be
			used as I/O port while the three-phase motor control is enabled. Apply a
			stable "H" to P8 $_5$ after setting the direction register for P8 $_5$ to "0" when
			the three-phase motor control is enabled, and; 4) P86 and P87 can serve
			as I/O pins for the sub-clock generation circuit. In this latter case, a quartz
			oscillator must be connented between P86 (XCOUT pin) and P87 (XCIN pin).
P90~P93	I/O port P9	Input/	This is an 4-bit I/O port equivalent to P6. Additional software-selectable
		output	secondary functions are: 1) $P9_0$ to $P9_2$ can act as Timer B0~B2 input
			pins, and; 2) P9 $_0$ to P9 $_3$ can act as A/D converter input pins.
			P9o outputs a no-divide, divide-by-8 or divide-by-32 clock of XIN or a
			clock of the same frequency as XCIN as selected by program. P9 $_2$ to P9 $_3$
			are not available in the 42 pin version.
P100~P107	I/O port P10	Input/	This is an 8-bit I/O port equivalent to P6. This port can also function as
		output	A/D converter input pins, as selected by software. Furthermore, P104 to
			P107 can also function as input pins for the key input interrupt function.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map. The linear address space of 1M bytes extends from address 0000016 to FFFF16. The internal ROM is allocated in a lower address direction beginning with address FFFF16. For example, a 64-Kbyte internal ROM is allocated to the address from F000016 to FFFF16.

The fixed interrupt vector table is allocated to the address from FFFDC16 to FFFFF16. Therefore store the start address of each interrupt routine here. For details, refer to the "Interrupt".

These devices also contain two blocks of Flash ROM as Data Flash memory to store data. These two blocks of 2K bytes are located from 0F00016 to 0FFFF16 on all versions.

The internal RAM is allocated in an upper address direction beginning with address 0040016. For example, a 1-Kbyte internal RAM is allocated to the address from 0040016 to 007FF16. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SFR is allocated to the address from 0000016 to 003FF16. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from FFE0016 to FFFDB16. This vector is used by the JMPS or JSRS instruction. For details, refer to the "M16C/60 and M16C/20 Series Software Manual".

Figure 3.1. Memory Map

4. Special Function Register (SFR) Map

Address	Register	S	Symbol	After reset
000016	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~			
000116				
000216				
000316				
000416	Processor mode register 0			0016
000516	Processor mode register 1			000010002
000016	System clock control register 1			010010002
000816	System clock control register 1			001000002
000916	Address match interrupt enable register	A		XXXXXX002
000A16	Protect register	F	PBCR	XX000002
000B16				
000C16	Oscillation stop detection register	(Note 2) (CM2	0X0000102
000D16				
000E16	Watchdog timer start register	<u>\</u>		<u>??16</u>
000F16	Watchdog timer control register	\		00??????2(Note3)
001016	Address match interrupt register 0	r	RIMADU	0016
001116				0016 X016
001216				7010
001416	Address match interrupt register 1	F		0016
001516	· · · · · · · · · · · · · · · · · · ·			0016
001616				X016
001716				
001816				
001916	Voltage detection register 1 (Note 4,5)	/CR1	000010002
001A16	Voltage detection register 2	Note 4,5)	/CR2	0016
001B16	PLL control register 0			0001 \0100
001C16	PLL control register 0	r		0001X0102
001E16	Processor mode register 2	F	PM2	XXX000002
001E16	Power supply down detection interrupt register	(Note 5)	D4INT	0016
002016	DMA0 source pointer		SAR0	??16
002116				??16
002216				X?16
002316				
002416	DMA0 destination pointer	[DAR0	??16
002516				??16 X2:-
002016				Χ./16
002816	DMA0 transfer counter		ICB0	2216
002916				?? ₁₆
002A16				
002B16				
002C16	DMA0 control register		DM0CON	00000?002
002D16				
002E16				
002016				00
003016	DMA1 source pointer		SAR1	??16
003116				??16 X210
003316				V ; 10
003416	DMA1 destination pointer		DAR1	??16
003516		-		??16
003616				X?16
003716				
003816	DMA1 transfer counter	7	TCR1	??16
003916				??16
003A16				
003C16	DMA4 control conjeter			00000000
003016	DIVIA1 control register	[00000?002
003E16				
003F16				

Note 1: The blank areas are reserved and cannot be used by users.

Note 2: The CM20, CM21 and CM27 bits do not change at oscillation stop detection reset.

Note 3: The WDC5 bit is "0" (cold start) immediately after power-on. It can only be set to "1" in a program.

It is set to "0" when the input voltage at the VCC pin drops to Vdet2 or less while the VC25 bit in the VCR2 register is set to "1" (2V detection circuit enable).

Note 4: This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.

Note 5: This register can not use for M16C/26T

X : Nothing is mapped to this bit ? : Undefined

Address	Register	Symbol	After reset
004016			
004116			
004216			
004316			
004416	INT3 interrupt control register	INT3IC	XX00?0002
004516	······································		
004616			
004716			
004816	INT5 interrupt control register	INT5IC	XX00?0002
004916	INT4 interrupt control register	INT4IC	XX0020002
004A16	UART2 Bus collision detection interrupt control register	BCNIC	XXXX20002
004B16	DMA0 interrupt control register	DMOIC	XXXX20002
004C16	DMA1 interrupt control register	DM1IC	XXXX20002
004D16	Key input interrupt control register	KUPIC	XXXX20002
004F16	A/D conversion interrupt control register	ADIC	XXXX20002
004E16	LIART2 transmit interrupt control register	S2TIC	XXXX20002
005016	LIART2 receive interrunt control register	S2RIC	XXXX20002
005116	LIARTO transmit interrupt control register	SOTIC	XXXX20002
005216	LIARTO receive interrupt control register	SORIC	XXXX20002
005316	LIART1 transmit interrupt control register	SITIC	XXXX20002
005/14	UART1 receive interrunt control register	S1RIC	XXXX?0002
005516	TimerA0 interrupt control register		XXXX?0002
005616	TimerA0 Interrupt control register		XXXX20002
005016	TimerA1 Interrupt control register		XXX20002
005846	TimerA2 interrupt control register	TA2IC	XXXX20002
005016	TimerA3 Interrupt control register		XXX20002
005916	TimerA4 Interrupt control register		XXX20002
005A16	TimerB0 Interrupt control register		XXX20002
005016	TimerD1 Interrupt control register		
005016			XX020002
005D16	INTO Interrupt control register		XX00?0002
005E16	INTO Interrupt control register	INTIC	XX00?0002
003F16			XX00?0002
006016			
006116			
006216			
006316			
006416			
006516			
006616			
006716			
006816			
006916			
006A16			
006B16			
006C16			
006D16			
006E16			
006F16			
007016			
007116			
007216			
007316			
007416			
007516			
007616			
007716			
007816			
007916			
007A16			
007B16			
007C16			
007D16			
007E16			
007F16			

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit ? : Undefined

Address	Register		Symbol	After reset	
008016			,		
008116					
008216					
008316					
008416					
008516					_
008016					
≈					~
01B016					
01B116					_
01B216	Floch momony control register 4	(Noto 2)		01000000	_
01B316	Flash memory control register 4	(NOLE 2)		01000002	
01B516	Flash memory control register 1	(Note 2)	FMR1	000???0?2	-
01B616		(11010 2)		0000.2	
01B716	Flash memory control register 0	(Note 2)	FMR0	0116	
01B816					
01B916					
01BA16					
01BB16					
01BC16					
01BD16					
01BE16					-
010110					_
7					~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
025016					
025116					
025216					
025316					
025416					
025616					
025716					
025816					
025916					
025A16	Three phase protect control register		TPRC	0016	
025B16					
025C16	On-chip oscillator control register		ROCR	000001012	
025D16	Pin assignment control register		PACR	0016	
025E16	Peripheral clock select register		PCLKR	00000112	
2					~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
033016					
033116					
033216					
033316					-+
033546					-+
033616					
033716					-
033816					
033916					
033A16					
033B16					
033C16					
033D16					
033E16	NMI digital debounce register		NDDR	FF16	
U33F16	Port17 digital debounce register		P17DDR	FF16	

Note 1: The blank areas are reserved and cannot be used by users. Note 2: This register is included in the flash memory version.

X :Nothing is mapped to this bit ? : Undefined

RENESAS

Address	Register	Symbol	After reset
034016			
034116			
034216	Timer A1-1 register	TA11	??16
034316		??16	
034416	Timer A2-1 register	TA21	??16
034516	Timer A 4 4 merciator	??16	
034616	limer A4-1 register	??16 2240	
034816	Three phase PW/M control register 0	INIVCO	0016
034916	Three phase PWM control register 0	INVC1	0016
034A16	Three phase output buffer register 0	IDB0	0016
034B16	Three phase output buffer register 1	IDB1	0016
034C16	Dead time timer	DTT	??16
034D16	Timer B2 Interrupt occurrence frequency set counter	ICTB2	X?16
034E16	Position-data-retain function control register	PDRF	XXXX00002
034F16			
035016			
035716			
035316			
035416			
035516			
035616			
035716			
035816	Port function control register	PFCR	001111112
035916			
035A16			
035B16			
035C16			
035E46	Interrupt request source coloct register 2	IESDOV	
035E16	Interrupt request cause select register 2	IFSR	0016
036016			0010
036116			
036216			
036316			
036416			
036516			
036616			
036716			
036016			
036A16			
036B16			
036C16			
036D16			
036E16			
036F16			
037016			
037116			
03/216			
037316	LIART2 special mode register 4		0016
037516	UART2 special mode register 3	112SMR3	
037616	UART2 special mode register 2	U2SMR2	X00000002
037716	UART2 special mode register	U2SMR	X0000002
037816	UART2 transmit/receive mode register	U2MR	0016
037916	UART2 bit rate register	U2BRG	??16
037A16	UART2 transmit buffer register	U2TB	???????2
037B16			XXXXXXX?2
037C16	UART2 transmit/receive control register 0	U2C0	000010002
037D16	UART2 transmit/receive control register 1	<u>U2C1</u>	000000102
037E16	UART2 receive buffer register	U2RB	???????2
037F16			<u>????</u> XX?2

Note 1 :The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit ? : Undefined

Address	Register	Symbol	After reset
038016	Count start flag	TABSR	0016
038116	Clock prescaler reset flag	CPSRF	0XXXXXXX2
038216	One-shot start flag	ONSF	0016
038316	Trigger select register	TRGSR	0016
038416	Up-dowm flag	UDF	0016
038516			
038616	Timer A0 register	TA0	??16
038716			??16
038816	Timer A1 register	TA1	??16
038916	-		??16
038A16	Timer A2 register	TA2	??16
038B16	Timer A2 register	ТАр	2210
038D16	Timer AS register	TAS	224c
038E16	Timer A4 register	ТА4	2216
038F16		1777	?? ₁₆
039016	Timer B0 register	TB0	?? ₁₆
039116			??16
039216	Timer B1 register	TB1	??16
039316	Ŭ		??16
039416	Timer B2 register	TB2	??16
039516	-		??16
039616	Timer A0 mode register	TA0MR	0016
039716	Timer A1 mode register	TA1MR	0016
039816	Timer A2 mode register	TA2MR	0016
039916	Timer A3 mode register	TA3MR	0016
039A16	Timer A4 mode register	TA4MR	0016
039B16	Timer B0 mode register	TBOMR	00??00002
039C16	Timer B1 mode register	TB1MR	00?X00002
039D16	Timer B2 mode register		<u>00?X00002</u> X0000000
039E16		10230	X0000002
03A016	LIARTO transmit/receive mode register	LIOMP	0016
03A116	UARTO hit rate register	UOBRG	?? ₁₆
03A216	UART0 transmit buffer register	UOTB	222222 22222222222
03A316			XXXXXXX?2
03A416	UART0 transmit/receive control register 0	U0C0	000010002
03A516	UART0 transmit/receive control register 1	U0C1	00000102
03A616	UART0 receive buffer register	UORB	???????2
03A716			?????XX?2
03A816	UART1 transmit/receive mode register	U1MR	0016
03A916	UART1 bit rate register	U1BRG	??16
03AA16	UART1 transmit buffer register	U1TB	????????
03AB16		114.00	XXXXXXX?2
034016	UARTI I ITANSMIT/receive control register U		0000010002
034546			222222222
03AF16	OANT TECEIVE DUILETTEUISIET	UIRD	22222222222222222222222222222222222222
03B016	UART transmit/receive control register 2	UCON	X0000002
03B116			,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
03B216			
03B316			
03B416	CRC snoop address register	CRCSAR	??16
03B516	· •		00XXXX??2
03B616	CRC mode register	CRCMR	0XXXXXX02
03B716			
03B816	DMA0 request cause select register	DM0SL	0016
03B916	211		
03BA16	DMA1 request cause select register	DM1SL	0016
03BB16		0000	00
030016	UKU data register	CRCD	??16 2240
03BE16		CRCIN	2216
03BF16			: : 10

Note 1 :The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit ? : Undefined

Address	Register	Symbol	After reset
03C016	A/D register 0	AD0	???????2
03C116			XXXXXX??2
03C216	A/D register 1	AD1	???????2
03C316	A/D register 2	۵D2	2222222222
03C416 03C516		ADZ	XXXXXX??2
03C616	A/D register 3	AD3	???????2
03C716	-		XXXXXX??2
03C816	A/D register 4	AD4	????????
03C916	A/D register 5	AD5	XXXXXX??2
03CA16 03CB16		705	XXXXXX??2
03CC16	A/D register 6	AD6	???????2
03CD16			XXXXXX??2
03CE16	A/D register 7	AD7	???????2
03CF16			XXXXXX??2
03D016			
03D216	A/D trigger control register	ADTRGCON	XXXX00002
03D316	A/D status register 0	ADSTAT0	00000X002
03D416	A/D control register 2	ADCON2	0016
03D516	A/D control register 0		000002220
03D616 03D716	A/D control register 0	ADCON0	00000???2
03D816		71200111	0010
03D916			
03DA16			
03DB16			
03DC16			
03DE16			
03DF16			
03E016			
03E116	Port P1 register	P1	??16
03E216	Port P1 direction register	PD1	0016
03E416			0018
03E516			
03E616			
03E716			
03E816			
03E916 03EA16			
03EB16			
03EC16	Port P6 register	P6	??16
03ED16	Port P7 register	P7	??16
03EE16	Port P6 direction register	PD6	0016
03E016	Port P8 register	P8	?? ₁₆
03F116	Port P9 register	P9	???X????2
03F216	Port P8 direction register	PD8	0016
03F316	Port P9 direction register	PD9	000X00002
03F416	Port P10 register	P10	??16
03F616	Port P10 direction register	PD10	0016
03F716		1210	0010
03F816			
03F916			
03FA16			
03FC16	Pull-up control register 0	PLIRO	0016
03FD16	Pull-up control register 1	PUR1	0016
03FE16	Pull-up control register 2	PUR2	0016
03FF16	Port control register	PCR	0016

Note 1 :The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit

? : Undefined

5. Package

Recommended Mount Pad Dimension in Millimeters Max А 1.7 0 0.1 0.2 A1 A2 1.4 b 0.17 0.22 0.27 0.125 С 0.105 0.175 D 6.9 7.0 7.1 Е 6.9 7.0 7.1 е 0.5 _ _ 9.2 ΗD 8.8 9.0 ΗE 8.8 9.0 9.2 L 0.35 0.5 0.65 1.0 L1 Lp 0.45 0.6 0.75 A3 0.25 Х 0.08 0.1 y _ θ 0° 8° 0.225 b2 _ 12 1.0 _

Recommended

7.4 Plastic 42pin 450mil SSOP

7.4

_

MD

ME

Plastic 48pin 7×7mm body LQFP

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6. Functional differences

6.1 Functional differences between M16C/26A and M16C/26T

Item	M16C/26A	M16C/26T
Main Clock During	Oscillating	Not oscillating
and After Reset	(Initial value of CM05 bit is set to "0"	(Initial value of CM05 bit is set to "1"
	during and after reset)	during and after reset)
Voltage Detection	Available	Not available
Circuit	(Power supply detection register 1,	(Reserved register)
(Function of 001916,	Power supply detection register 2,	
001A16, 001F16)	Power supply down detection interrupt register)	
Package	48P6Q, 42P2R	48P6Q

Note. Since the emulator between the M16C/26A and M16C/29 group are same, all functions of M16C/29 are built in the emulator. When evaluating M16C/26A group, do not access to the SFR which is not built in M16C/26A group.

Refer to Hardware Manual about detail and electrical characteristics.

6.2 Functional differences between M16C/26A and M16C/26

Item	M16C/26A	M16C/26
Clock Generation	4 circuits (Main clock oscillation circuit.	3 circuits (Main clock oscillation circuit.
Circuit	Sub clock oscillation circuit,	Sub clock oscillation circuit,
	On-chip oscillator,	On-chip oscillator)
	PLL frequency synthesizer)	
System Clock	On-chip oscillator	Main clock
Source After Reset	(Initial value "1" of CM21 bit)	(Initial value "0" of CM21 bit)
(Initial value of the CM21		
bit in the CM2 register)	Available	Not available
limit Detection Circuit	(VC25 bit)	(Reserved bit)
(The b5 bit in the VCR2 register)		
On-chip Oscillator Clock	Selectable (8MHz/1MHz/500KHz)	Fixed (1MHz)
PACR2 to PACR0 in	Necessary to set after reset	No PACR register
the PACR Register	48pin:"1002", 42pin:"0012"	
IFSR20 Bit in the	Necessary to set to "1" after reset	No IFSR2A register
IFSR2A Register	·····	
External Interrupt	8 causes (INT2 added)	7 causes
13 pin (48-pin version)		IVcc
Function		
P70 P71	N-ch open drain output and CMOS	N-ch open drain output
	output are selectable by S/W	
A/D Input Pin	12 channels	8 channels
(48-pin version)		
A/D Operation Mode	8 modes (single repeat single sweep	5 modes (single repeat single sweep
	repeat sweep mode 0, repeat sweep,	repeat sweep mode 0 repeat sweep
	mode 1. simultaneous sampling.	mode 1)
	delayed trigger mode 0, delayed	,
	trigger mode 1)	
	1 shunt current measurement function	
	is available	
Timer B Operation	5 modes (timer, event counter, pulse	4 modes (timer, event counter, pulse
Mode	periods measurement, pulse width	periods measurement, pulse width
	measurment, A/D trigger)	measurment)
	1 shunt current measurement function	
CRC Calculation	Available (compatible to CRC-CCITI	Not available
	and CRC-16 methods)	
Three-Phase Motor	•Waveform output/Switching port output	•Waveform output/Switching port output
Control	by software is enabled	by software is disabled
	•Position-data-retain function	•No position-data-retain function
Digital Debounce	This function is in the NMI/SD pin and	Not available
Function		
3 pin (48-pin version)	P90/CLKOUT/TB0IN/AN30	P90/180IN
Function	(CLKOUT: f1, f8, f32, and fC output)	
UART1 Compatible	Switching to P64 to P67 or P70 to P73	P64 to P67
Pin	is enabled	
Flash Memory	Protection to blocks 0, 1 by FMR02 bit	Protection to blocks 0,1 by FMR02 bit
Protect Function	Protection to the blocks 0 to 3 by	
	FMR16 bit	
Package	48P6Q, 42P2R	48P6Q

Note. Since the emulator between the M16C/26A and M16C/29 group are same, all functions of M16C/29 are built in the emulator. When evaluating M16C/26A group, do not access to the SFR which is not built in M16C/26A group.

Refer to Hardware Manual about detail and electrical characteristics.

REVISION HISTORY

M16C/26A Group (M16C/26A, M16C/26T) Short Sheet

Rev.	Date		Description	
		Page	Summary	
0.20	Dec/ 01/ 03		First edition	
0.30	Jun/15/04	All	Descriptions about M16C/26A and M16C/26AT are added.	
		1	The section "1. Overview" is partly revised.	
		2,3	Table 1.1 and 1.2 are partly revised. Note 2 in Table 1.1 and 1.2 are revised.	
		4,5	Figure 1.1 and 1.2 integrate descriptions.	
		6	The section "1.4 Product List" is partly revised.	
		7	Table 1.6 "Porduct code" is added.	
		8	Figure 1.4 "Marking Diagram of Flash Memory versionfor M16C/26A (Top View) " is added	
		9,10	Figure 1.5 to 1.6 are partly revised.	
		11	Table 1.6 is revised.	
		12	Table 1.7 is partly revised.	
		15	The Chapter "3. Memory" is partly revised. Note 2 in Figure 3.1 is added.	
		16	The Chapter "4. Special Function Register" is partly revised.	
		23, 24	The ChapIte "6. Functional differences" is added.	
0.40	Sep/30/04	All	M16C/26AT is changed to M16C/26T.	

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