3803/3804 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0073-0401Z
Rev.4.01
Nov 14, 2003

DESCRIPTION

The 3803/3804 group is the 8-bit microcomputer based on the 740 family core technology.

The 3803/3804 group is designed for household products, office automation equipment, and controlling systems that require analog signal processing, including the A-D converter and D-A converters.

The 3804 group is the version of the 3803 group to which an I^2C-BUS control function has been added.

FEATURES

- Basic machine-language instructions 71
- Minimum instruction execution time ..... 0.24 µs
  (at 16.8 MHz oscillation frequency)
- Memory size
  - ROM ..... 16 K to 60 K bytes
  - RAM ..... 640 to 2048 bytes
- Programmable input/output ports 56
- Software pull-up resistors ..... Built-in
- Interrupts
  - 21 sources, 16 vectors ..... 3803 group
    (external 8, internal 12, software 1)
  - 23 sources, 16 vectors ..... 3804 group
    (external 9, internal 13, software 1)
- Timers ..... 16-bit × 1
  8-bit × 4
  (with 8-bit prescaler)
- Watchdog timer ..... 16-bit × 1
- Serial I/O ..... 8-bit × 2 (UART or Clock-synchronized)
  8-bit × 1 (Clock-synchronized)
- PWM ..... 8-bit × 1 (with 8-bit prescaler)
- I^2C-BUS interface (3804 group only) ..... 1 channel
- A-D converter ..... 10-bit × 16 channels
  (8-bit reading enabled)
- D-A converter ..... 8-bit × 2 channels
- LED direct drive port 8
- Clock generating circuit ..... Built-in 2 circuits
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  - In high-, middle-speed mode
  - At 16.8 MHz oscillation frequency ..... 4.5 to 5.5 V
  - At 12.5 MHz oscillation frequency ..... 4.0 to 5.5 V
  - At 8.38 MHz oscillation frequency) ..... 2.7 to 5.5 V *
  - In low-speed mode
  - At 32 kHz oscillation frequency ..... 2.7 to 5.5 V *
  (* This value of flash memory version is 4.0 to 5.5 V.)
- Power dissipation
  - In high-speed mode ..... 60 mW (typ.)
  (at 16.8 MHz oscillation frequency, at 5 V power source voltage)
  - In low-speed mode ..... 60 µW (typ.)
  (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ..... –20 to 85°C
- Packages
  - SP ..... 64P4B (64-pin 750 mil SDIP)
  - FP ..... 64P6N-A (64-pin 14 × 14 mm QFP)
  - HP ..... 64P6Q-A (64-pin 10 × 10 mm LQFP)

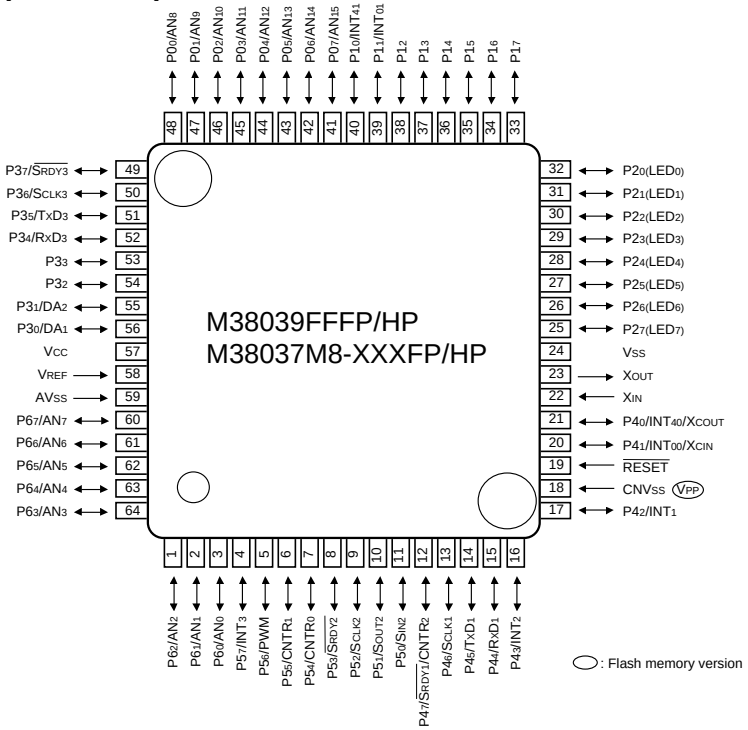
<Flash memory mode>

- Supply voltage ..... V_{CC} = 5 V ± 10 %
- Program/Erase voltage ..... V_{PP} = 11.7 V to 12.6 V
- Programming method ..... Programming in unit of byte
- Erasing method
  - Batch erasing ..... Parallel/Serial I/O mode
  - Block erasing ..... CPU reprogramming mode
- Program/Erase control by software command
- Number of times for programming/erasing 100
- Operating temperature range (at programming/erasing) .....
  ..... Room temperature

■Notes

1. The flash memory version cannot be used for application embedded in the MCU card.
2. Supply voltage Vcc of the flash memory version is 4.0 to 5.5 V.

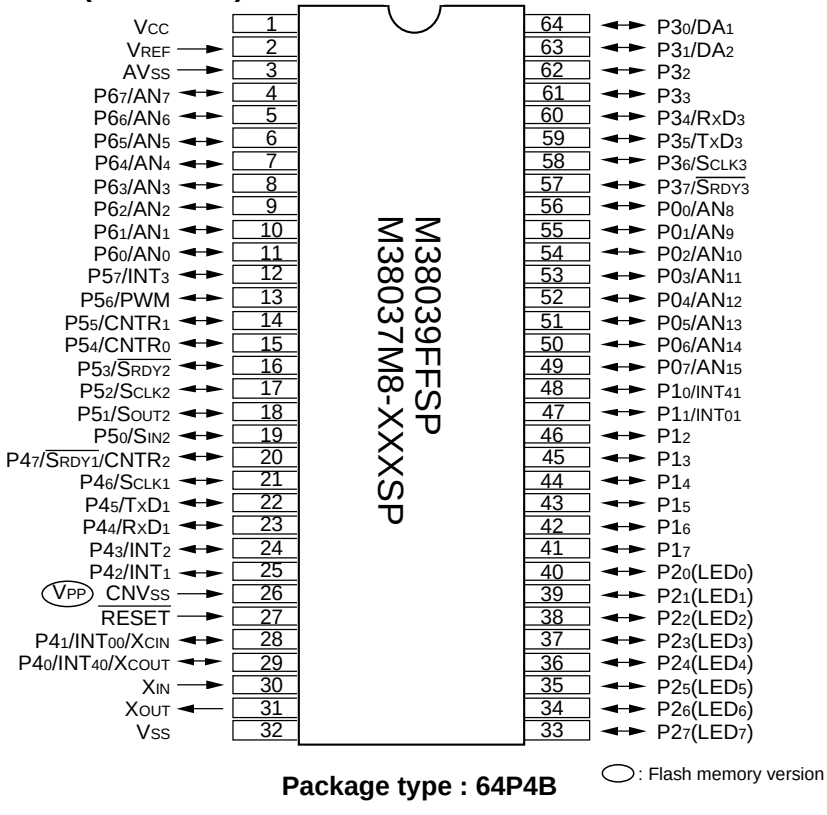
PIN CONFIGURATION (TOP VIEW)



Package type : 64P6N-A/64P6Q-A

Fig. 1 3803 group pin configuration

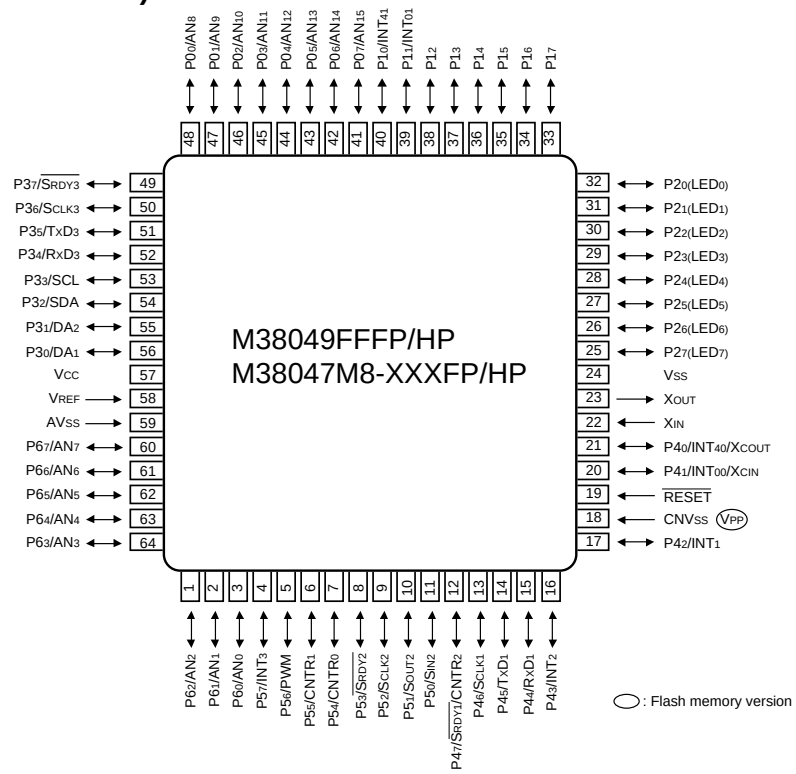
PIN CONFIGURATION (TOP VIEW)



Package type : 64P4B

Fig. 2 3803 group pin configuration

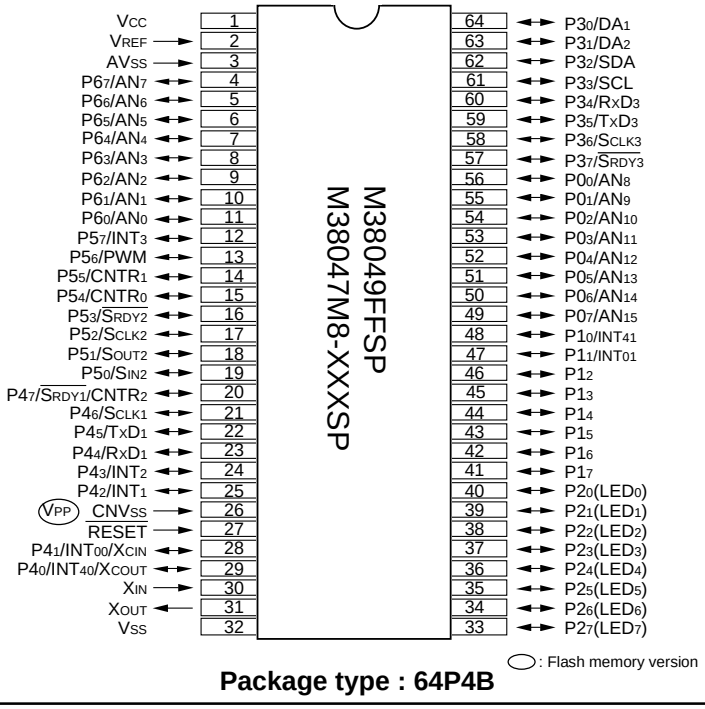
PIN CONFIGURATION (TOP VIEW)



Package type : 64P6N-A/64P6Q-A

Fig. 3 3804 group pin configuration

PIN CONFIGURATION (TOP VIEW)



Package type : 64P4B

Fig. 4 3804 group pin configuration

FUNCTIONAL BLOCK

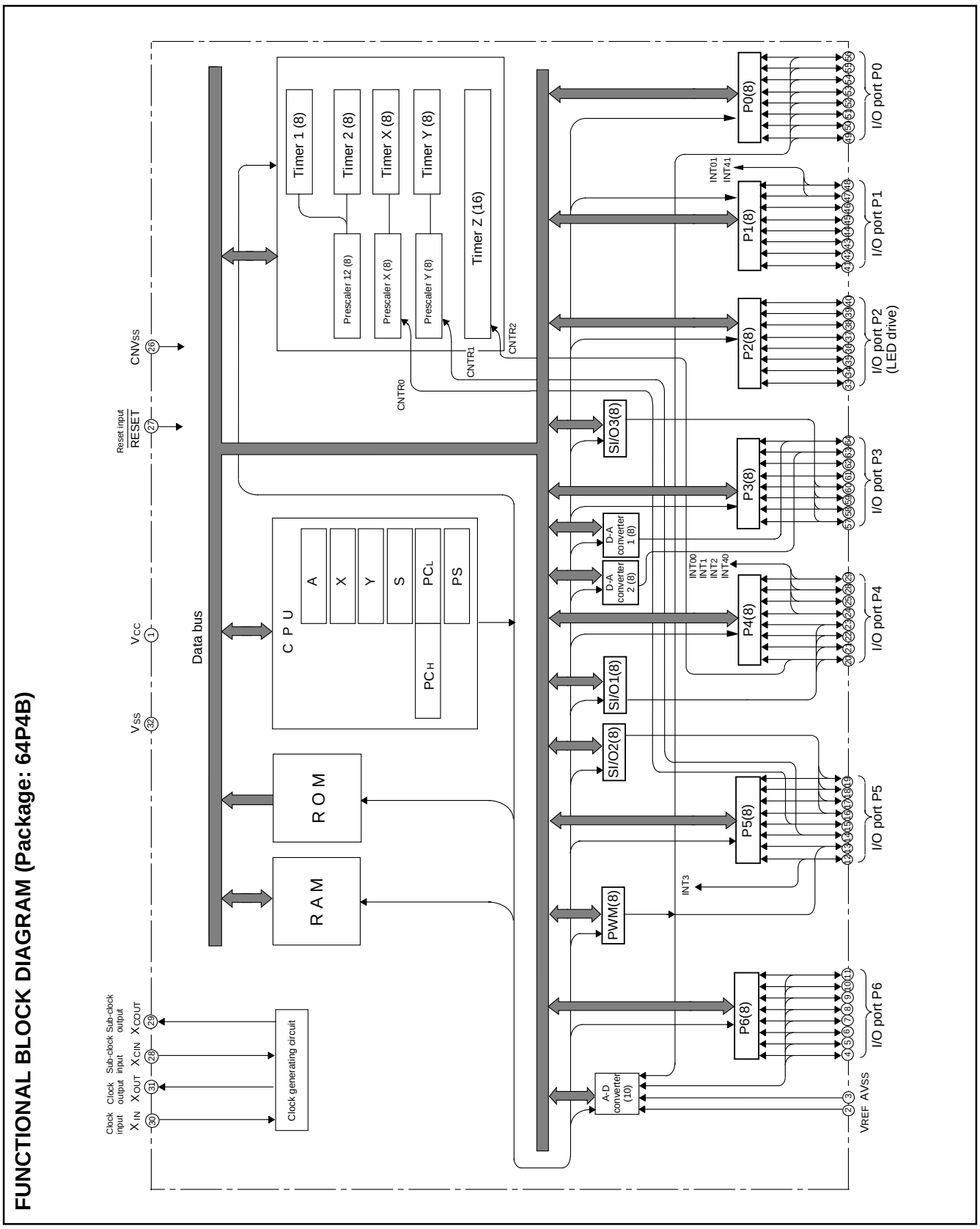


Fig. 5 3803 group functional block diagram

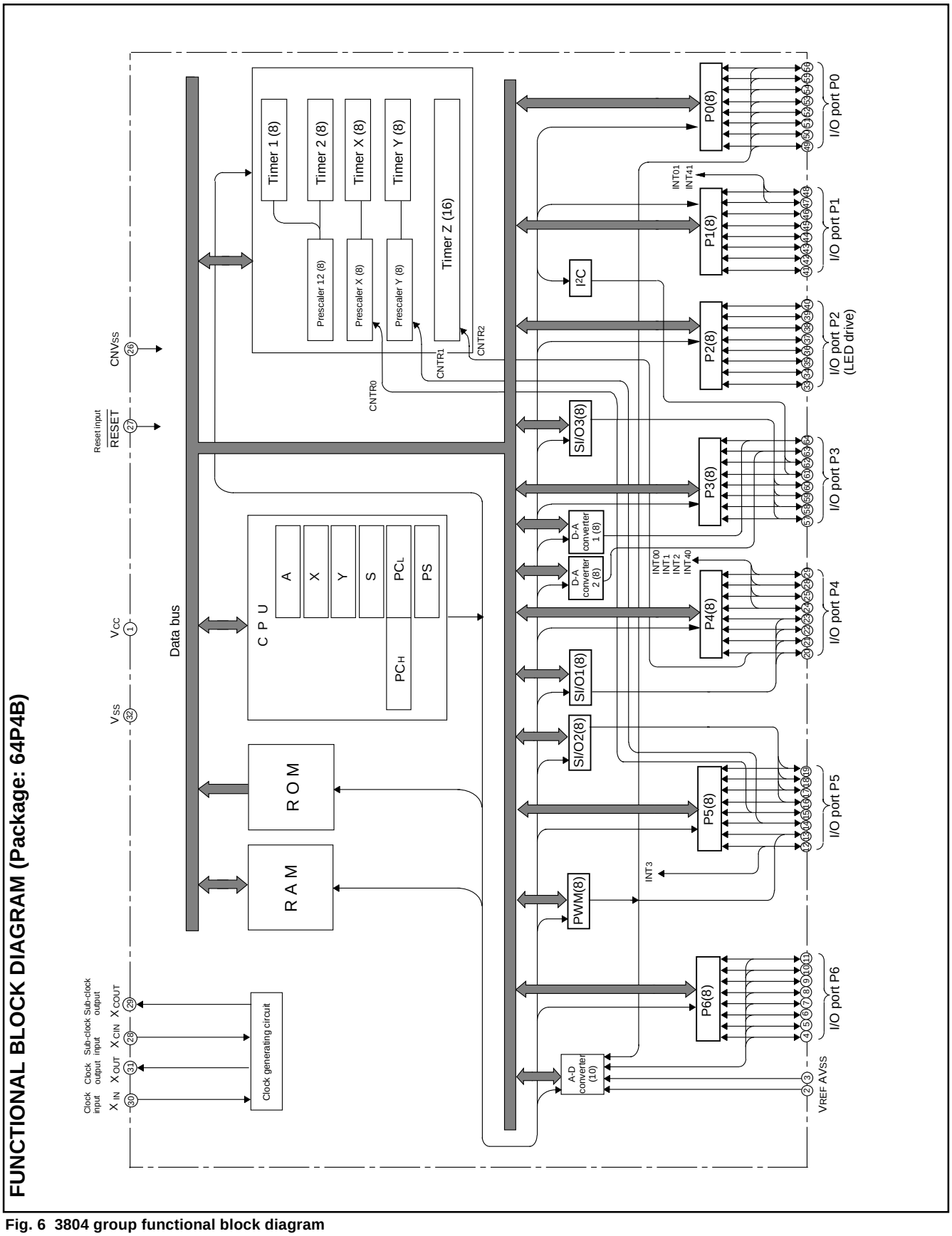


Fig. 6 3804 group functional block diagram

PIN DESCRIPTION

Table 1 Pin description (3803 group)

Pin	Name	Functions	Function except a port function
VCC, VSS	Power source	•Apply voltage of 2.7 V – 5.5 V to Vcc, and 0 V to Vss. •In the flash memory version, apply voltage of 4.0 V – 5.5 V to Vcc, and 0 V to Vss	
CNVSS	CNVSS input	•This pin controls the operation mode of the chip. •Normally connected to VSS. •In the flash memory version, this becomes VPP power source input pin.	
VREF	Reference voltage	•Reference voltage input pin for A-D and D-A converters.	
AVSS	Analog power source	•Analog power source input pin for A-D and D-A converters. •Connect to VSS.	
$\overline{\text{RESET}}$	Reset input	•Reset input pin for active “L”.	
XIN	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. •When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
XOUT	Clock output		
P00/AN8–P07/AN15	I/O port P0	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled in a bit unit. •P20–P27 are enabled to output large current for LED drive.	•A-D converter input pin
P10/INT41 P11/INT01	I/O port P1		•Interrupt input pin
P12–P17			
P20–P27	I/O port P2		
P30/DA1 P31/DA2	I/O port P3	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •P30, P31, P34–P37 are CMOS 3-state output structure. •P32, P33 are N-channel open-drain output structure. •Pull-up control of P30, P31, P34–P37 is enabled in a bit unit.	•D-A converter input pin
P32, P33			
P34/RxD3 P35/TxD3 P36/SCLK3 P37/$\overline{\text{SRDY3}}$			•Serial I/O3 function pin
P40/INT40/XCOUT P41/INT00/XCIN	I/O port P4	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled in a bit unit.	•Interrupt input pin •Sub-clock generating I/O pin (resonator connected)
P42/INT1 P43/INT2			•Interrupt input pin
P44/RxD1 P45/TxD1 P46/SCLK1			•Serial I/O1 function pin
P47/$\overline{\text{SRDY1}}$/CNTR2			•Serial I/O1, timer Z function pin
P50/SIN2 P51/SOUT2 P52/SCLK2 P53/$\overline{\text{SRDY2}}$	I/O port P5	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled in a bit unit.	•Serial I/O2 function pin
P54/CNTR0			•Timer X function pin
P55/CNTR1			•Timer Y function pin
P56/PWM			•PWM output pin
P57/INT3			•Interrupt input pin
P60/AN0–P67/AN7	I/O port P6		•A-D converter input pin

Table 2 Pin description (3804 group)

Pin	Name	Functions	Function except a port function
V_{CC}, V_{SS}	Power source	•Apply voltage of 2.7 V – 5.5 V to Vcc, and 0 V to Vss. •In the flash memory version, apply voltage of 4.0 V – 5.5 V to Vcc, and 0 V to Vss	
CNVSS	CNVSS input	•This pin controls the operation mode of the chip. •Normally connected to V_{SS}. •In the flash memory version, this becomes V_{PP} power source input pin.	
V_{REF}	Reference voltage	•Reference voltage input pin for A-D and D-A converters.	
AVSS	Analog power source	•Analog power source input pin for A-D and D-A converters. •Connect to V_{SS}.	
$\overline{RESET}$	Reset input	•Reset input pin for active “L”.	
X_{IN}	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. •When an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
P0$_0$/AN$_8$–P0$_7$/AN$_{15}$	I/O port P0	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled in a bit unit. •P2$_0$–P2$_7$ are enabled to output large current for LED drive.	•A-D converter input pin
P1$_0$/INT$_{41}$ P1$_1$/INT$_{01}$	I/O port P1		•Interrupt input pin
P1$_2$–P1$_7$			
P2$_0$–P2$_7$	I/O port P2		
P3$_0$/DA$_1$ P3$_1$/DA$_2$	I/O port P3	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •P3$_2$ to P3$_3$ can be switched between CMOS compatible input level or SMBUS input level in the I^2C-BUS interface function. •P3$_0$, P3$_1$, P3$_4$–P3$_7$ are CMOS 3-state output structure. •P3$_2$, P3$_3$ are N-channel open-drain output structure. •Pull-up control of P3$_0$, P3$_1$, P3$_4$–P3$_7$ is enabled in a bit unit.	•D-A converter input pin
P3$_2$/SDA P3$_3$/SCL			•I^2C-BUS interface function pins
P3$_4$/RxD$_3$ P3$_5$/TxD$_3$ P3$_6$/SCLK$_3$ P3$_7$/$\overline{SRDY3}$			•Serial I/O3 function pin
P4$_0$/INT$_{40}$/XCOUT P4$_1$/INT$_{00}$/XCIN	I/O port P4	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled in a bit unit.	•Interrupt input pin •Sub-clock generating I/O pin (resonator connected)
P4$_2$/INT$_1$ P4$_3$/INT$_2$			•Interrupt input pin
P4$_4$/RxD$_1$ P4$_5$/TxD$_1$ P4$_6$/SCLK$_1$			•Serial I/O1 function pin
P4$_7$/$\overline{SRDY1}$/CNTR$_2$			•Serial I/O1, timer Z function pin
P5$_0$/SIN$_2$ P5$_1$/SOUT$_2$ P5$_2$/SCLK$_2$ P5$_3$/$\overline{SRDY2}$	I/O port P5	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled in a bit unit.	•Serial I/O2 function pin
P5$_4$/CNTR$_0$			•Timer X function pin
P5$_5$/CNTR$_1$			•Timer Y function pin
P5$_6$/PWM			•PWM output pin
P5$_7$/INT$_3$			•Interrupt input pin
P6$_0$/AN$_0$–P6$_7$/AN$_7$	I/O port P6		•A-D converter input pin

PART NUMBERING

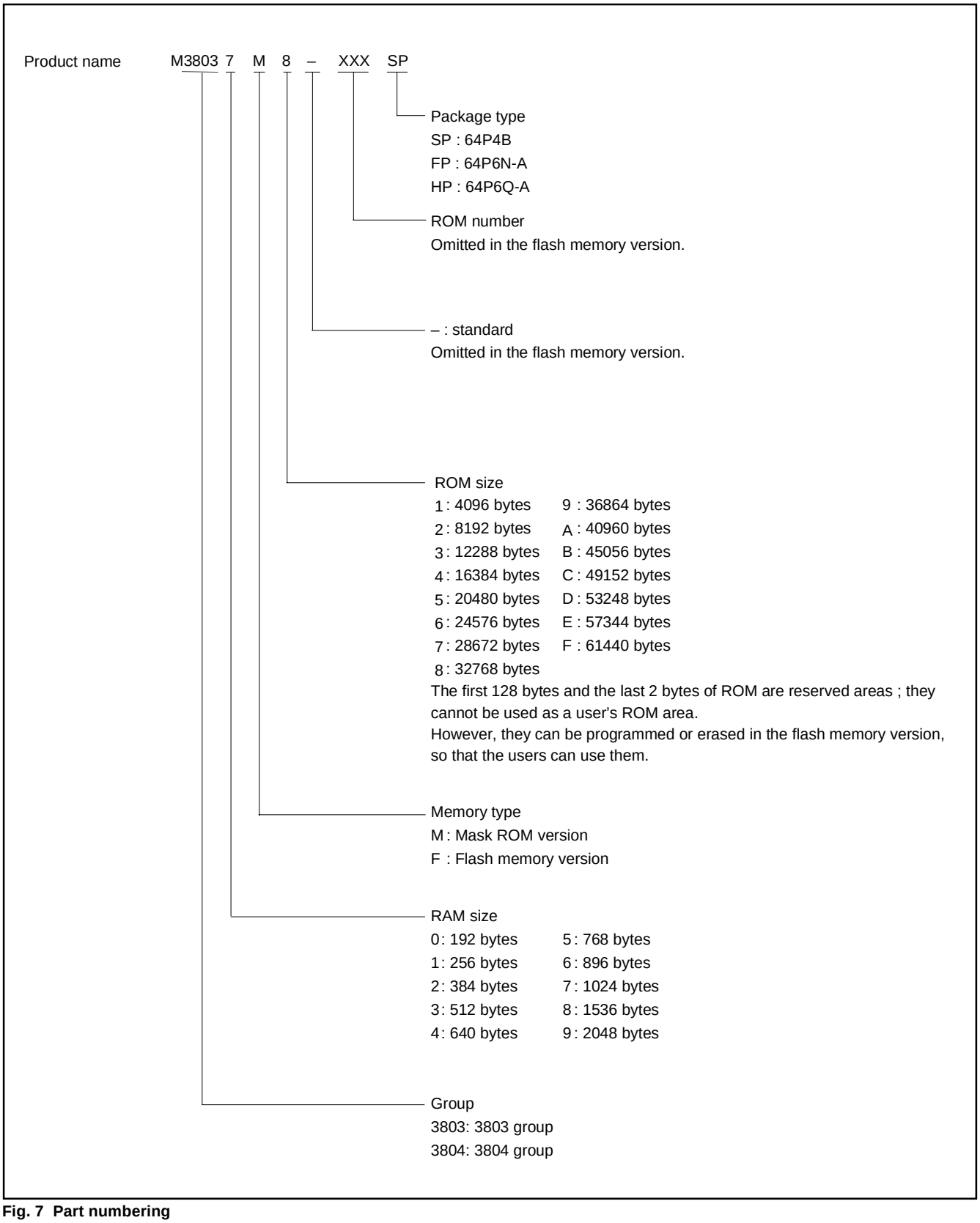


Fig. 7 Part numbering

GROUP EXPANSION

GROUP EXPANSION

Renesas plans to expand the 3803/3804 group as follows.

Memory Type

Support for mask ROM and flash memory versions.

Memory Size

Flash memory size ..... 60 K bytes
Mask ROM size ..... 16 K to 60 K bytes
RAM size ..... 640 to 2048 bytes

Packages

64P4B ..... 64-pin shrink plastic-molded DIP
64P6N-A ..... 0.8 mm-pitch plastic molded QFP
64P6Q-A ..... 0.5 mm-pitch plastic molded LQFP

Memory Expansion Plan

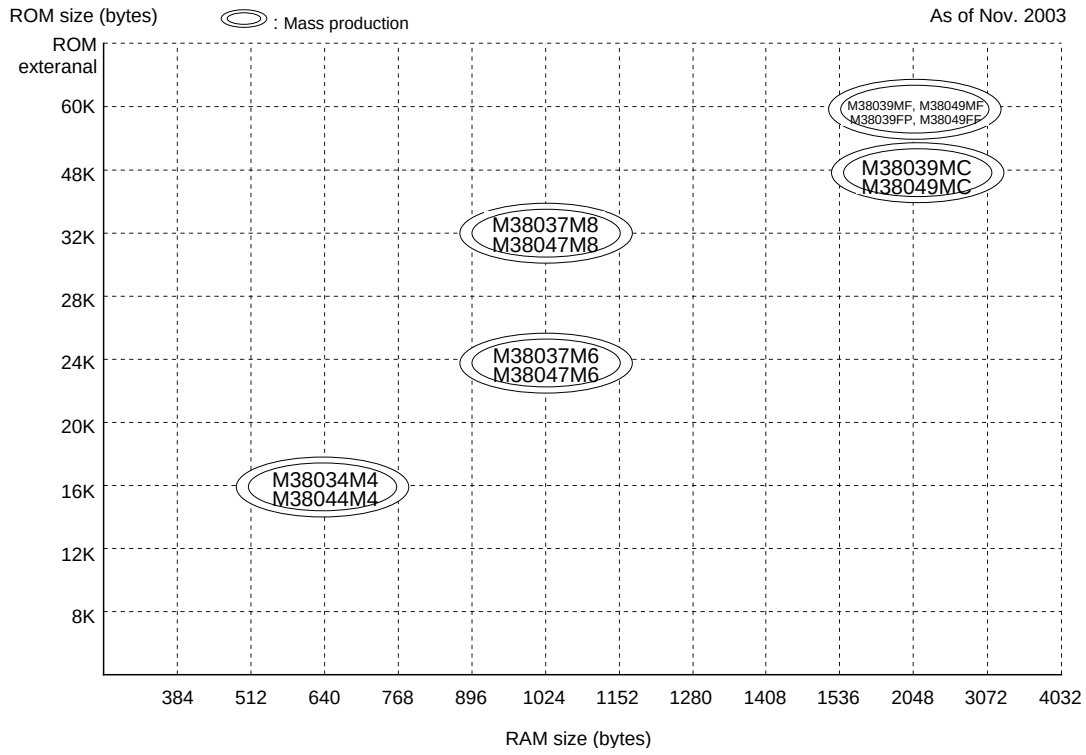


Fig. 8 Memory expansion plan

Currently planning products are listed below.

Table 3 Support products **As of Nov. 2003**

Product name	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38034M4-XXXSP	16384 (16254)	640	64P4B	Mask ROM version
M38034M4-XXXFP			64P6N-A	
M38034M4-XXXHP			64P6Q-A	
M38044M4-XXXSP			64P4B	
M38044M4-XXXFP			64P6N-A	
M38044M4-XXXHP			64P6Q-A	
M38037M6-XXXSP	24576 (24446)	1024	64P4B	Mask ROM version
M38037M6-XXXFP			64P6N-A	
M38037M6-XXXHP			64P6Q-A	
M38047M6-XXXSP			64P4B	
M38047M6-XXXFP			64P6N-A	
M38047M6-XXXHP			64P6Q-A	
M38037M8-XXXSP	32768 (32638)	1024	64P4B	Mask ROM version
M38037M8-XXXFP			64P6N-A	
M38037M8-XXXHP			64P6Q-A	
M38047M8-XXXSP			64P4B	
M38047M8-XXXFP			64P6N-A	
M38047M8-XXXHP			64P6Q-A	
M38039MC-XXXSP	49152 (49022)	2048	64P4B	Mask ROM version
M38039MC-XXXFP			64P6N-A	
M38039MC-XXXHP			64P6Q-A	
M38049MC-XXXSP			64P4B	
M38049MC-XXXFP			64P6N-A	
M38049MC-XXXHP			64P6Q-A	
M38039MF-XXXSP	61440 (61310)	2048	64P4B	Mask ROM version
M38039MF-XXXFP			64P6N-A	
M38039MF-XXXHP			64P6Q-A	
M38049MF-XXXSP			64P4B	
M38049MF-XXXFP			64P6N-A	
M38049MF-XXXHP			64P6Q-A	
M38039FFSP	61440	2048	64P4B	Flash memory version
M38039FFFP			64P6N-A	
M38039FFHP			64P6Q-A	
M38049FFSP			64P4B	
M38049FFFP			64P6N-A	
M38049FFHP			64P6Q-A	

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 3803/3804 group uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 10.

Store registers other than those described in Figure 10 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

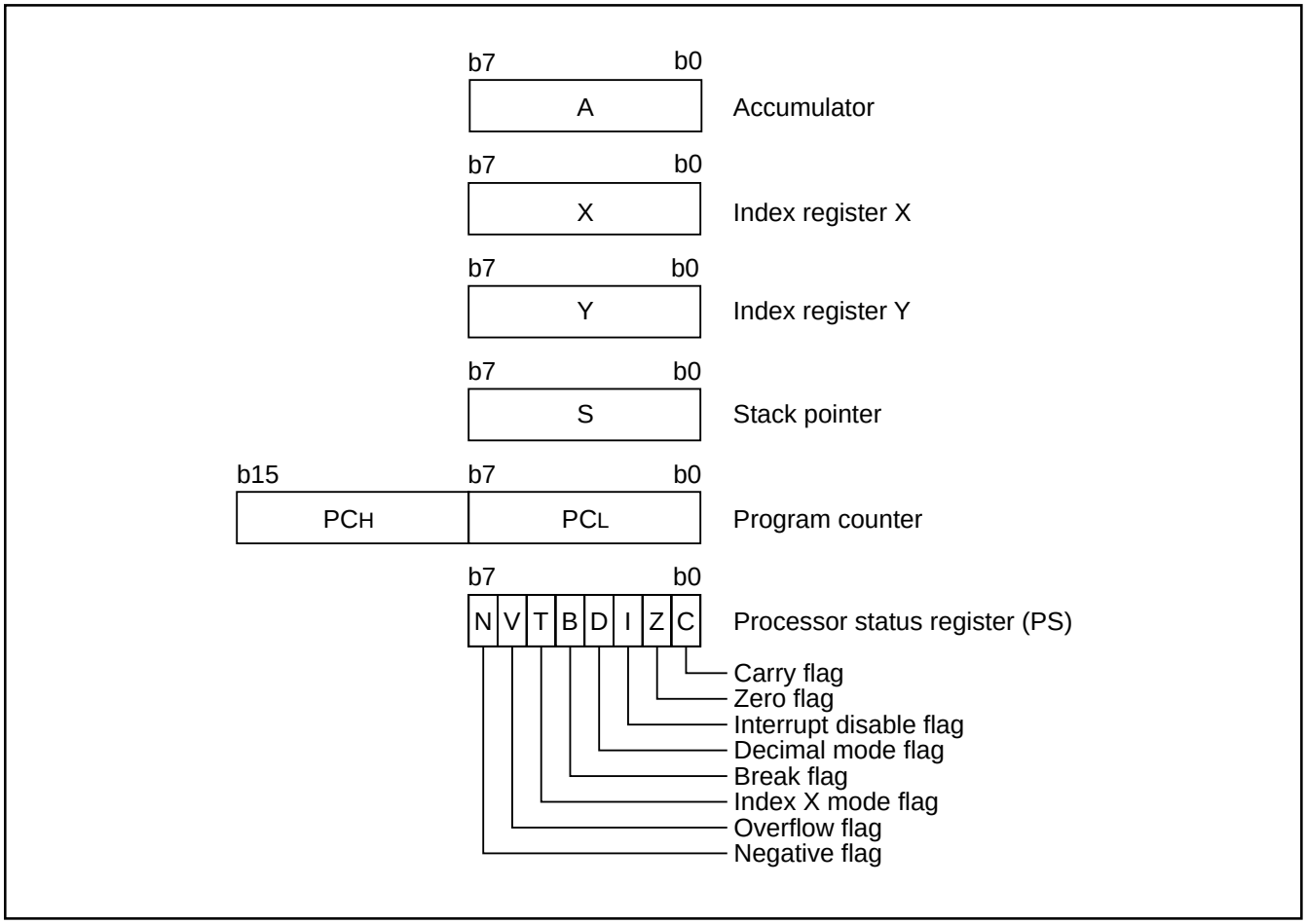


Fig.9 740 Family CPU register structure

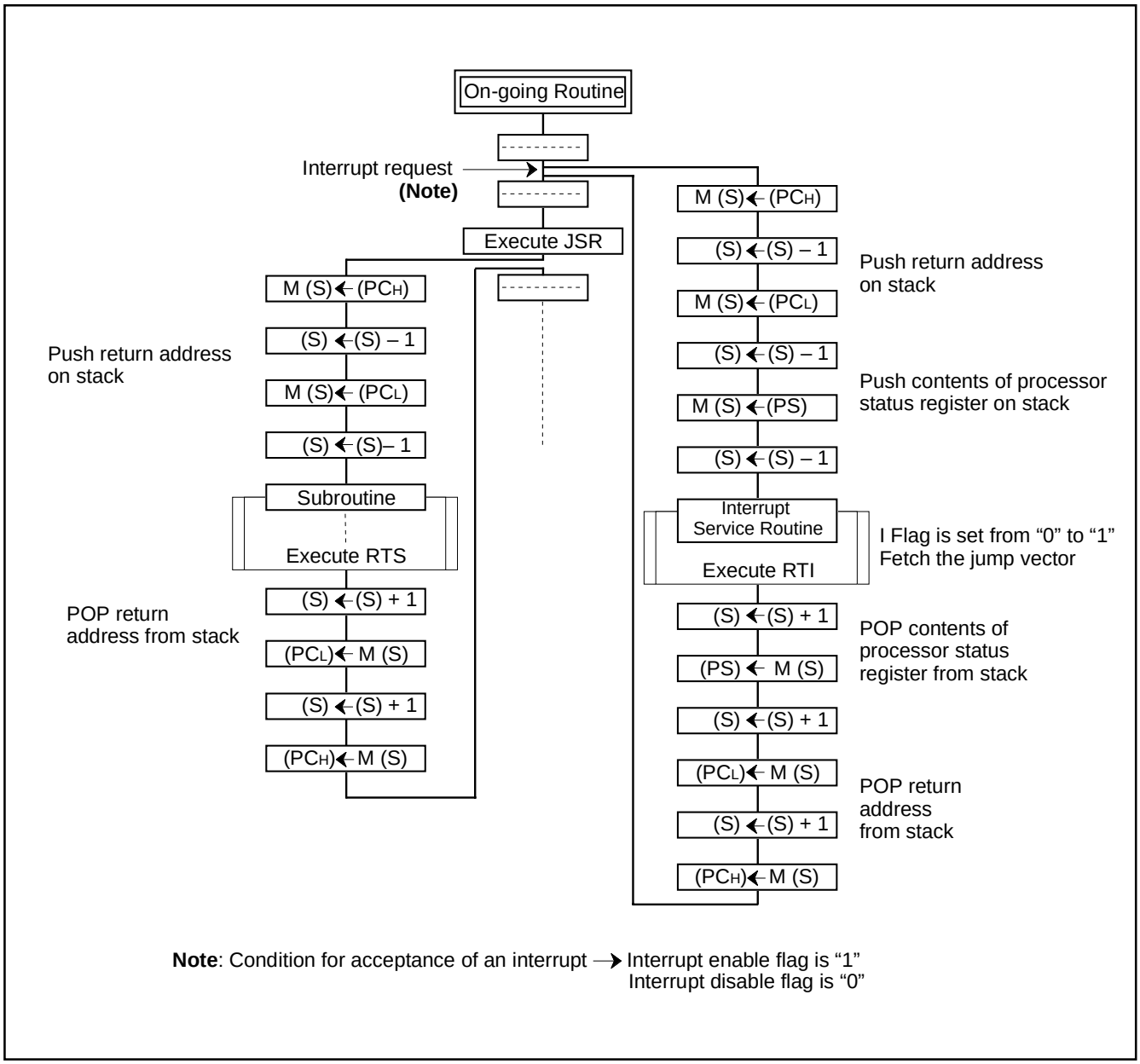


Fig. 10 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

•Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is “1”.

•Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”. Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

•Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.

•Bit 5: Index X mode flag (T)

When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, etc.

The CPU mode register is allocated at address 003B16.

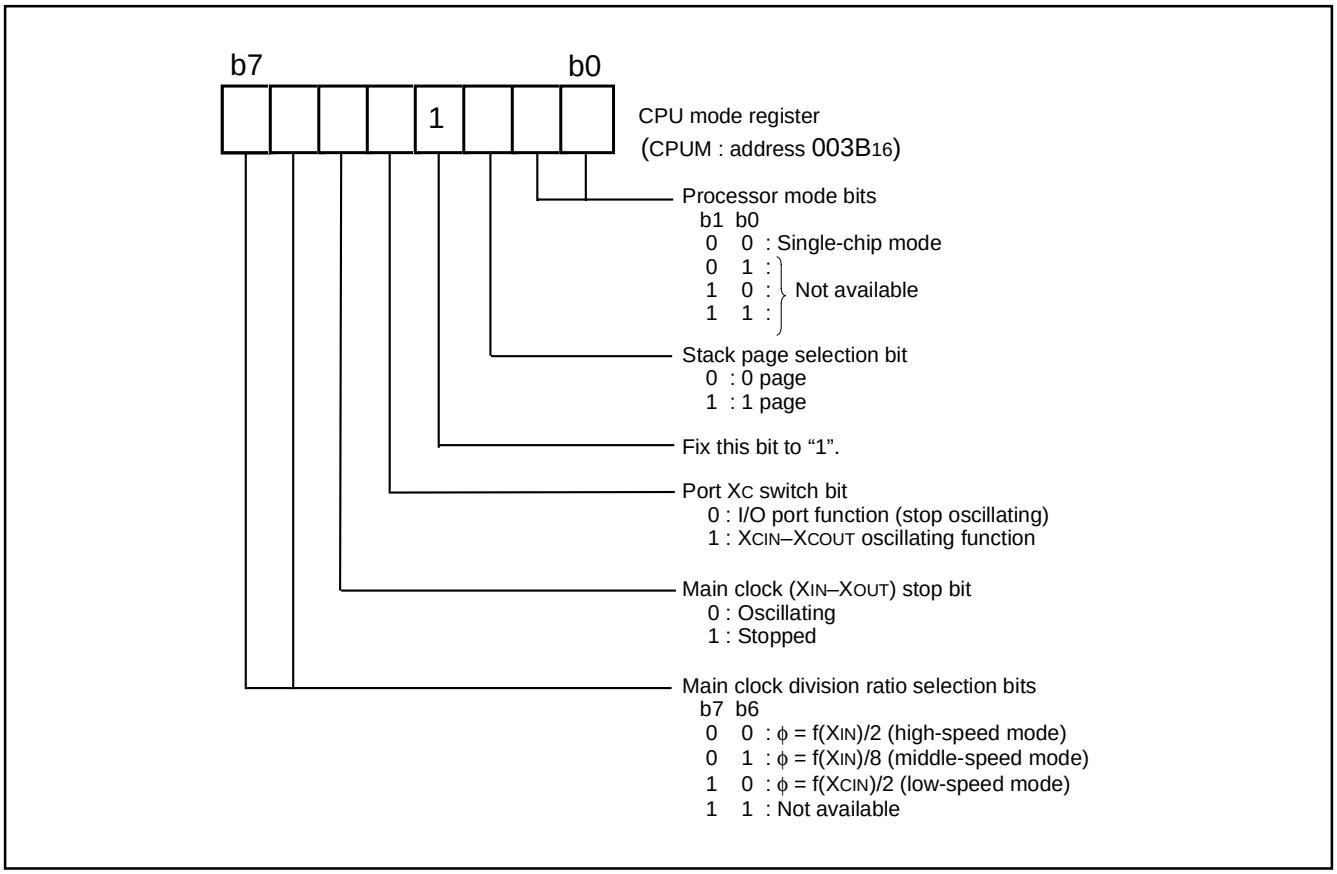


Fig.11 Structure of CPU mode register

MISRG

(1) Bit 0 of address 0010_{16}: Oscillation stabilizing time set after STP instruction released bit

When the MCU stops the clock oscillation by the STP instruction and the STP instruction has been released by an external interrupt source, usually, the fixed values of Timer 1 and Prescaler 12 (Timer 1 = 01_{16}, Prescaler 12 = FF_{16}) are automatically reloaded in order for the oscillation to stabilize. The user can inhibit the automatic setting by setting "1" to bit 0 of MISRG (address 0010_{16}). However, by setting this bit to "1", the previous values, set just before the STP instruction was executed, will remain in Timer 1 and Prescaler 12. Therefore, you will need to set an appropriate value to each register, in accordance with the oscillation stabilizing time, before executing the STP instruction.
Figure 12 shows the structure of MISRG.

(2) Bits 1, 2, 3 of address 0010_{16}: Middle-speed Mode Automatic Switch Function

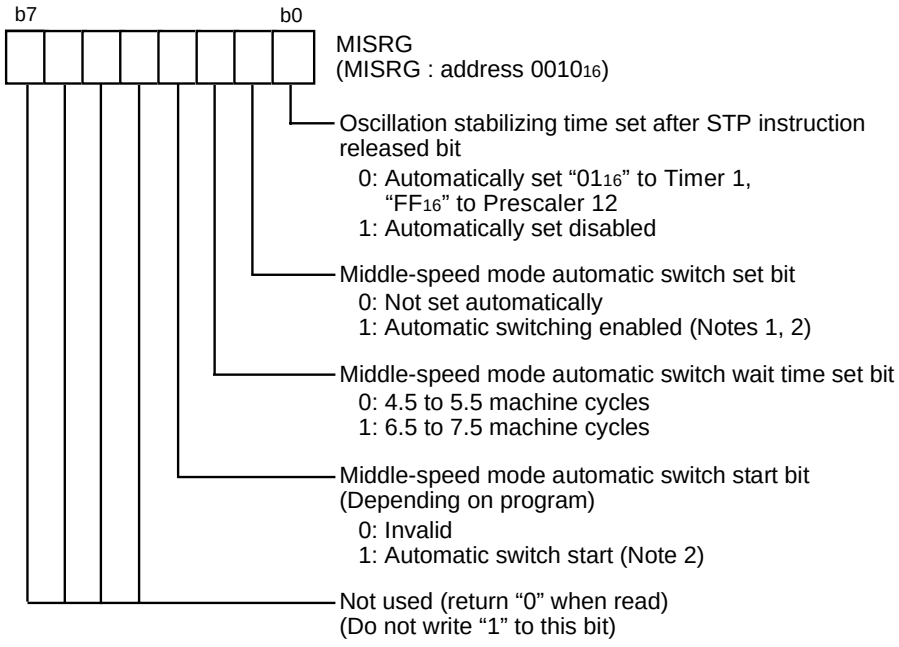
In order to switch the clock mode of an MCU which has a sub-clock, the following procedure is necessary:
set CPU mode register ($003B_{16}$) --> start main clock oscillation --> wait for oscillation stabilization --> switch to middle-speed mode (or high-speed mode).
However, the 3803/3804 group has the built-in function which automatically switches from low to middle-speed mode either by the SCL/SDA interrupt (only for the 3804 group) or by program.

●Middle-speed mode automatic switch by SCL/SDA Interrupt (only for 3804 group)

The SCL/SDA interrupt source enables an automatic switch when the middle-speed mode automatic switch set bit (bit 1) of MISRG (address 0010_{16}) is set to "1". The conditions for an automatic switch execution depend on the settings of bits 5 and 6 of the I^2C start/stop condition control register (address 0016_{16}). Bit 5 is the SCL/SDA interrupt pin polarity selection bit and bit 6 is the SCL/SDA interrupt pin selection bit. The main clock oscillation stabilizing time can also be selected by middle-speed mode automatic switch wait time set bit (bit 2) of the MISRG.

●Middle-speed mode automatic switch by program

The middle-speed mode can also be automatically switched by program while operating in low-speed mode. By setting the middle-speed automatic switch start bit (bit 3) of MISRG (address 0010_{16}) to "1" in the condition that the middle-speed mode automatic switch set bit is "1" while operating in low-speed mode, the MCU will automatically switch to middle-speed mode. In this case, the oscillation stabilizing time of the main clock can be selected by the middle-speed automatic switch wait time set bit (bit 2) of MISRG (address 0010_{16}).



Notes 1: During operation in low-speed mode, it is possible automatically to switch to middle-speed mode owing to SCL/SDA interrupt. This is valid only for the 3804 group.
2: When automatic switch to middle-speed mode from low-speed mode occurs, the values of CPU mode register ($3B_{16}$) change.

Fig.12 Structure of MISRG

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address XXXX16
192	00FF16
256	013F16
384	01BF16
512	023F16
640	02BF16
768	033F16
896	03BF16
1024	043F16
1536	063F16
2048	083F16

ROM area

ROM size (bytes)	Address YYYY16	Address ZZZZ16
4096	F00016	F08016
8192	E00016	E08016
12288	D00016	D08016
16384	C00016	C08016
20480	B00016	B08016
24576	A00016	A08016
28672	900016	908016
32768	800016	808016
36864	700016	708016
40960	600016	608016
45056	500016	508016
49152	400016	408016
53248	300016	308016
57344	200016	208016
61440	100016	108016

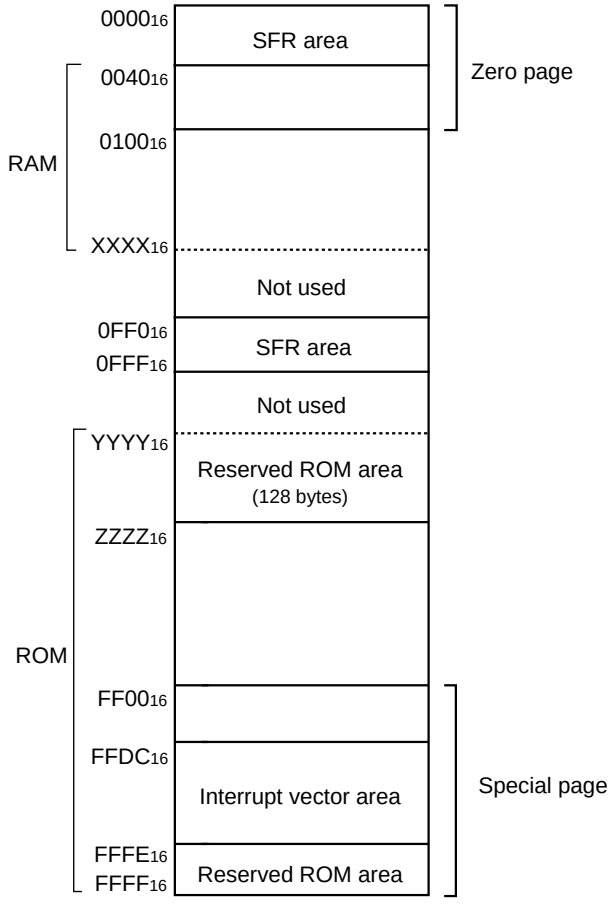


Fig. 13 Memory map diagram

0000₁₆	Port P0 (P0)
0001₁₆	Port P0 direction register (P0D)
0002₁₆	Port P1 (P1)
0003₁₆	Port P1 direction register (P1D)
0004₁₆	Port P2 (P2)
0005₁₆	Port P2 direction register (P2D)
0006₁₆	Port P3 (P3)
0007₁₆	Port P3 direction register (P3D)
0008₁₆	Port P4 (P4)
0009₁₆	Port P4 direction register (P4D)
000A₁₆	Port P5 (P5)
000B₁₆	Port P5 direction register (P5D)
000C₁₆	Port P6 (P6)
000D₁₆	Port P6 direction register (P6D)
000E₁₆	Timer 12, X count source selection register (T12XCSS)
000F₁₆	Timer Y, Z count source selection register (TYZCSS)
0010₁₆	MISRG
0011₁₆	Reserved ✻
0012₁₆	Reserved ✻
0013₁₆	Reserved ✻
0014₁₆	Reserved ✻
0015₁₆	Reserved ✻
0016₁₆	Reserved ✻
0017₁₆	Reserved ✻
0018₁₆	Transmit/Receive buffer register 1 (TB1/RB1)
0019₁₆	Serial I/O1 status register (SIO1STS)
001A₁₆	Serial I/O1 control register (SIO1CON)
001B₁₆	UART1 control register (UART1CON)
001C₁₆	Baud rate generator (BRG1)
001D₁₆	Serial I/O2 control register (SIO2CON)
001E₁₆	Watchdog timer control register (WDTCON)
001F₁₆	Serial I/O2 register (SIO2)

0020₁₆	Prescaler 12 (PRE12)
0021₁₆	Timer 1 (T1)
0022₁₆	Timer 2 (T2)
0023₁₆	Timer XY mode register (TM)
0024₁₆	Prescaler X (PREX)
0025₁₆	Timer X (TX)
0026₁₆	Prescaler Y (PREY)
0027₁₆	Timer Y (TY)
0028₁₆	Timer Z low-order (TZL)
0029₁₆	Timer Z high-order (TZH)
002A₁₆	Timer Z mode register (TZM)
002B₁₆	PWM control register (PWMCON)
002C₁₆	PWM prescaler (PREPWM)
002D₁₆	PWM register (PWM)
002E₁₆	
002F₁₆	Baud rate generator 3 (BRG3)
0030₁₆	Transmit/Receive buffer register 3 (TB3/RB3)
0031₁₆	Serial I/O3 status register (SIO3STS)
0032₁₆	Serial I/O3 control register (SIO3CON)
0033₁₆	UART3 control register (UART3CON)
0034₁₆	AD/DA control register (ADCON)
0035₁₆	A-D conversion register 1 (AD1)
0036₁₆	D-A1 conversion register (DA1)
0037₁₆	D-A2 conversion register (DA2)
0038₁₆	A-D conversion register 2 (AD2)
0039₁₆	Interrupt source selection register (INTSEL)
003A₁₆	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1 (IREQ1)
003D₁₆	Interrupt request register 2 (IREQ2)
003E₁₆	Interrupt control register 1 (ICON1)
003F₁₆	Interrupt control register 2 (ICON2)

0FF0₁₆	Port P0 pull-up control register (PULL0)
0FF1₁₆	Port P1 pull-up control register (PULL1)
0FF2₁₆	Port P2 pull-up control register (PULL2)
0FF3₁₆	Port P3 pull-up control register (PULL3)
0FF4₁₆	Port P4 pull-up control register (PULL4)
0FF5₁₆	Port P5 pull-up control register (PULL5)
0FF6₁₆	Port P6 pull-up control register (PULL6)

0FFE₁₆	Flash memory control register (FCON)
0FFF₁₆	Flash command register (FCMD)

✻ Reserved area: Do not write any data to this addresses, because these areas are reserved.

Fig. 14 Memory map of 3803 group's special function register (SFR)

0000_{16}	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)
0008_{16}	Port P4 (P4)
0009_{16}	Port P4 direction register (P4D)
$000A_{16}$	Port P5 (P5)
$000B_{16}$	Port P5 direction register (P5D)
$000C_{16}$	Port P6 (P6)
$000D_{16}$	Port P6 direction register (P6D)
$000E_{16}$	Timer 12, X count source selection register (T12XCSS)
$000F_{16}$	Timer Y, Z count source selection register (TYZCSS)
0010_{16}	MISRG
0011_{16}	I^2C data shift register (S0)
0012_{16}	I^2C special mode status register (S3)
0013_{16}	I^2C status register (S1)
0014_{16}	I^2C control register (S1D)
0015_{16}	I^2C clock control register (S2)
0016_{16}	I^2C START/STOP condition control register (S2D)
0017_{16}	I^2C special mode control register (S3D)
0018_{16}	Transmit/Receive buffer register 1 (TB1/RB1)
0019_{16}	Serial I/O1 status register (SIO1STS)
$001A_{16}$	Serial I/O1 control register (SIO1CON)
$001B_{16}$	UART1 control register (UART1CON)
$001C_{16}$	Baud rate generator (BRG1)
$001D_{16}$	Serial I/O2 control register (SIO2CON)
$001E_{16}$	Watchdog timer control register (WDTCON)
$001F_{16}$	Serial I/O2 register (SIO2)

0020_{16}	Prescaler 12 (PRE12)
0021_{16}	Timer 1 (T1)
0022_{16}	Timer 2 (T2)
0023_{16}	Timer XY mode register (TM)
0024_{16}	Prescaler X (PREX)
0025_{16}	Timer X (TX)
0026_{16}	Prescaler Y (PREY)
0027_{16}	Timer Y (TY)
0028_{16}	Timer Z low-order (TZL)
0029_{16}	Timer Z high-order (TZH)
$002A_{16}$	Timer Z mode register (TZM)
$002B_{16}$	PWM control register (PWMCON)
$002C_{16}$	PWM prescaler (PREPWM)
$002D_{16}$	PWM register (PWM)
$002E_{16}$	
$002F_{16}$	Baud rate generator 3 (BRG3)
0030_{16}	Transmit/Receive buffer register 3 (TB3/RB3)
0031_{16}	Serial I/O3 status register (SIO3STS)
0032_{16}	Serial I/O3 control register (SIO3CON)
0033_{16}	UART3 control register (UART3CON)
0034_{16}	AD/DA control register (ADCON)
0035_{16}	A-D conversion register 1 (AD1)
0036_{16}	D-A1 conversion register (DA1)
0037_{16}	D-A2 conversion register (DA2)
0038_{16}	A-D conversion register 2 (AD2)
0039_{16}	Interrupt source selection register (INTSEL)
$003A_{16}$	Interrupt edge selection register (INTEDGE)
$003B_{16}$	CPU mode register (CPUM)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003D_{16}$	Interrupt request register 2 (IREQ2)
$003E_{16}$	Interrupt control register 1 (ICON1)
$003F_{16}$	Interrupt control register 2 (ICON2)

$0FF0_{16}$	Port P0 pull-up control register (PULL0)
$0FF1_{16}$	Port P1 pull-up control register (PULL1)
$0FF2_{16}$	Port P2 pull-up control register (PULL2)
$0FF3_{16}$	Port P3 pull-up control register (PULL3)
$0FF4_{16}$	Port P4 pull-up control register (PULL4)
$0FF5_{16}$	Port P5 pull-up control register (PULL5)
$0FF6_{16}$	Port P6 pull-up control register (PULL6)
$0FF7_{16}$	I^2C slave address register 0 (S0D0)
$0FF8_{16}$	I^2C slave address register 1 (S0D1)
$0FF9_{16}$	I^2C slave address register 2 (S0D2)

$0FFE_{16}$	Flash memory control register (FCON)
$0FFF_{16}$	Flash command register (FCMD)

Fig. 15 Memory map of 3804 group's special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Table 6 I/O port function of 3803 group

Pin	Name	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
P0$_0$/AN$_8$–P0$_7$/AN$_{15}$	Port P0	CMOS compatible input level	A-D converter input	AD/DA control register	(1)
P1$_0$/INT$_{41}$	Port P1	CMOS 3-state output	External interrupt input	Interrupt edge selection register	(2)
P1$_1$/INT$_{01}$					
P1$_2$–P1$_7$					(3)
P2$_0$/LED$_0$–P2$_7$/LED$_7$	Port P2				
P3$_0$/DA$_1$	Port P3	CMOS compatible input level	D-A converter output	AD/DA control register	(4)
P3$_1$/DA$_2$		CMOS 3-state output			
P3$_2$		CMOS compatible input level			(5)
P3$_3$		N-channel open-drain output			
P3$_4$/RxD$_3$		CMOS compatible input level	Serial I/O3 function I/O	Serial I/O3 control register	(6)
P3$_5$/TxD$_3$		CMOS 3-state output		UART3 control register	(7)
P3$_6$/SCLK$_3$					(8)
P3$_7$/SRDY$_3$					(9)
P4$_0$/INT$_{40}$/XCIN	Port P4	CMOS compatible input level	External interrupt input	Interrupt edge selection register	(10)
P4$_1$/INT$_{00}$/XCOUT		CMOS 3-state output	Sub-clock generating circuit	CPU mode register	(11)
P4$_2$/INT$_1$			External interrupt input	Interrupt edge selection register	(2)
P4$_3$/INT$_2$					
P4$_4$/RxD$_1$			Serial I/O1 function I/O	Serial I/O1 control register	(6)
P4$_5$/TxD$_1$					(7)
P4$_6$/SCLK$_1$				UART1 control register	(8)
P4$_7$/SRDY$_1$/CNTR$_2$			Serial I/O1 function I/O Timer Z function I/O	Serial I/O1 control register Timer Z mode register	(12)
P5$_0$/SIN$_2$	Port P5	CMOS compatible input level	Serial I/O2 function I/O	Serial I/O2 control register	(13)
P5$_1$/SOUT$_2$		CMOS 3-state output			(14)
P5$_2$/SCLK$_2$					(15)
P5$_3$/SRDY$_2$					(16)
P5$_4$/CNTR$_0$			Timer X, Y function I/O	Timer XY mode register	(17)
P5$_5$/CNTR$_1$					
P5$_6$/PWM			PWM output	PWM control register	(18)
P5$_7$/INT$_3$			External interrupt input	Interrupt edge selection register	(2)
P6$_0$/AN$_0$–P6$_7$/AN$_7$	Port P6	CMOS compatible input level	A-D converter input	AD/DA control register	(1)
		CMOS 3-state output			

Notes 1: Refer to the applicable sections how to use double-function ports as function I/O ports.

2: Make sure that the input level at each pin is either 0 V or V_{CC} during execution of the STP instruction.
When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.

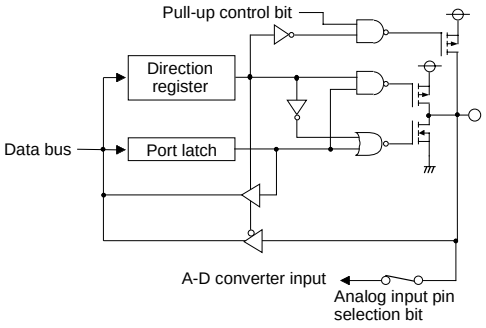
Table 7 I/O port function of 3804 group

Pin	Name	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
P0$_0$/AN$_8$–P0$_7$/AN$_{15}$	Port P0	CMOS compatible input level	A-D converter input	AD/DA control register	(1)
P1$_0$/INT$_{41}$ P1$_1$/INT$_{01}$	Port P1	CMOS 3-state output	External interrupt input	Interrupt edge selection register	(2)
P1$_2$–P1$_7$					(3)
P2$_0$/LED$_0$– P2$_7$/LED$_7$	Port P2				
P3$_0$/DA$_1$ P3$_1$/DA$_2$	Port P3	CMOS compatible input level CMOS 3-state output	D-A converter output	AD/DA control register	(4)
P3$_2$/SDA P3$_3$/SCL		CMOS compatible input level N-channel open-drain output CMOS/SMBUS input level (when selecting I^{2}C-BUS interface function)	I^{2}C-BUS interface function I/O	I^{2}C control register	(5)
P3$_4$/RxD$_3$ P3$_5$/TxD$_3$ P3$_6$/SCLK$_3$ P3$_7$/$\overline{\text{SRDY}}_3$		CMOS compatible input level CMOS 3-state output	Serial I/O3 function I/O	Serial I/O3 control register UART3 control register	(6) (7) (8) (9)
P4$_0$/INT$_{00}$/XCIN P4$_1$/INT$_{40}$/XCOUT	Port P4	CMOS compatible input level CMOS 3-state output	External interrupt input Sub-clock generating circuit	Interrupt edge selection register CPU mode register	(10) (11)
P4$_2$/INT$_1$ P4$_3$/INT$_2$			External interrupt input	Interrupt edge selection register	(2)
P4$_4$/RxD$_1$ P4$_5$/TxD$_1$ P4$_6$/SCLK$_1$			Serial I/O1 function I/O	Serial I/O1 control register UART1 control register	(6) (7) (8)
P4$_7$/$\overline{\text{SRDY}}_1$/CNTR$_2$			Serial I/O1 function I/O Timer Z function I/O	Serial I/O1 control register Timer Z mode register	(12)
P5$_0$/SIN$_2$ P5$_1$/SOUT$_2$ P5$_2$/SCLK$_2$ P5$_3$/$\overline{\text{SRDY}}_2$	Port P5	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O	Serial I/O2 control register	(13) (14) (15) (16)
P5$_4$/CNTR$_0$ P5$_5$/CNTR$_1$			Timer X, Y function I/O	Timer XY mode register	(17)
P5$_6$/PWM			PWM output	PWM control register	(18)
P5$_7$/INT$_3$			External interrupt input	Interrupt edge selection register	(2)
P6$_0$/AN$_0$–P6$_7$/AN$_7$	Port P6	CMOS compatible input level CMOS 3-state output	A-D converter input	AD/DA control register	(1)

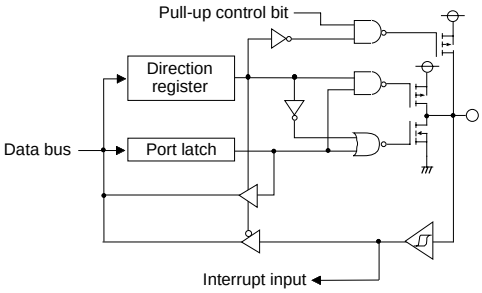
Notes 1: Refer to the applicable sections how to use double-function ports as function I/O ports.

2: Make sure that the input level at each pin is either 0 V or V_{CC} during execution of the STP instruction.
When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.

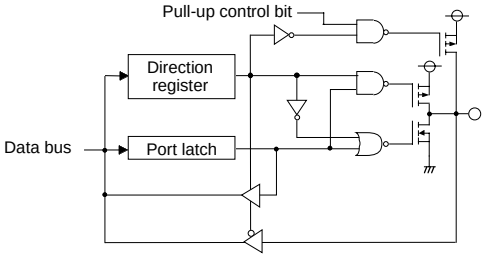
(1) Ports P0, P6



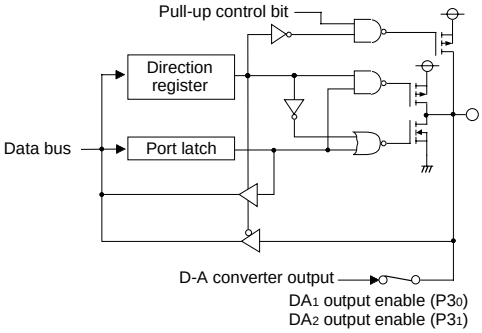
(2) Ports P10, P11, P42, P43, P57



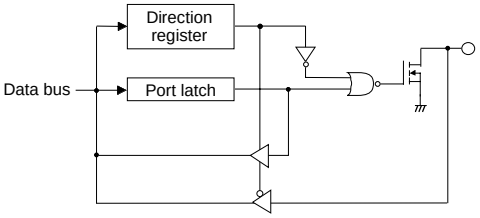
(3) Ports P12 to P17, P2



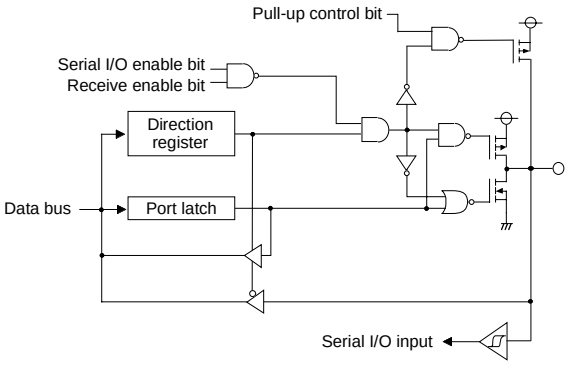
(4) Ports P30, P31



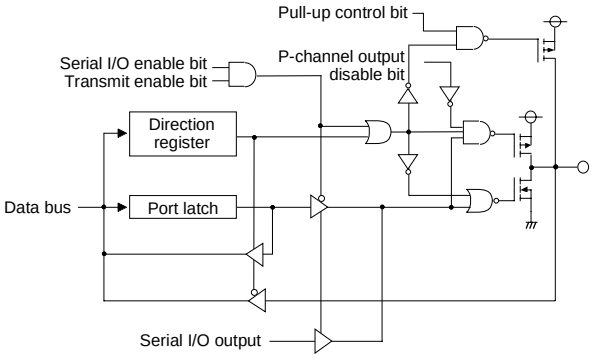
(5) Ports P32, P33



(6) Ports P34, P44



(7) Ports P35, P45



(8) Ports P36, P46

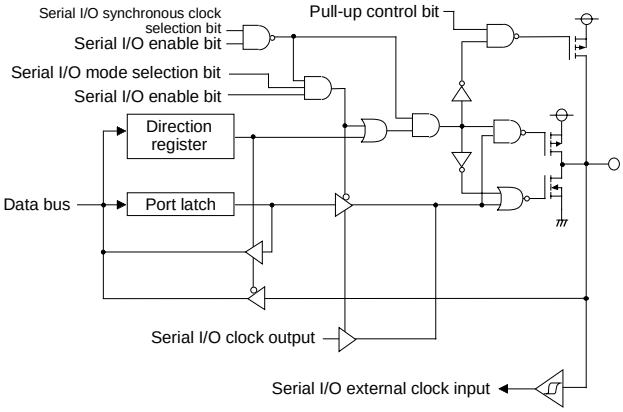
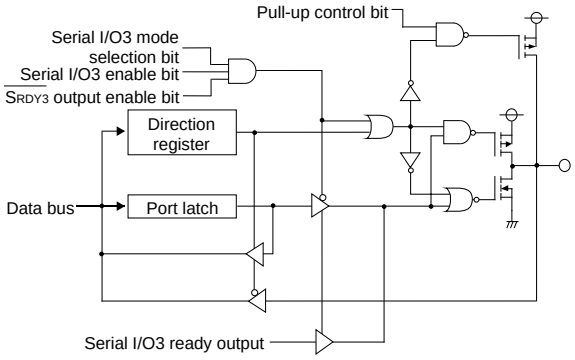
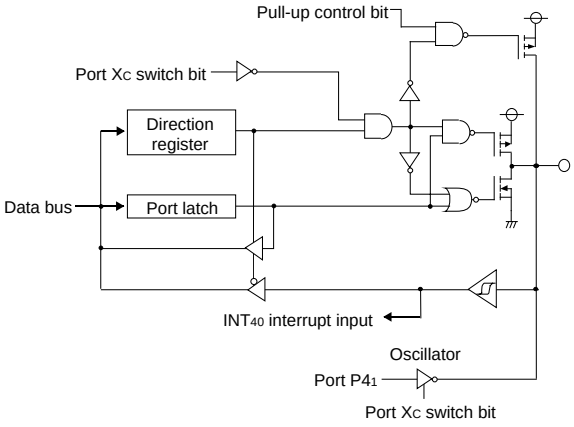


Fig. 16 Port block diagram of 3803 group (1)

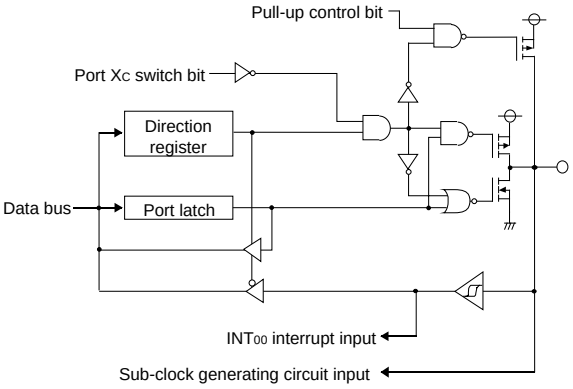
(9) Port P3$_7$



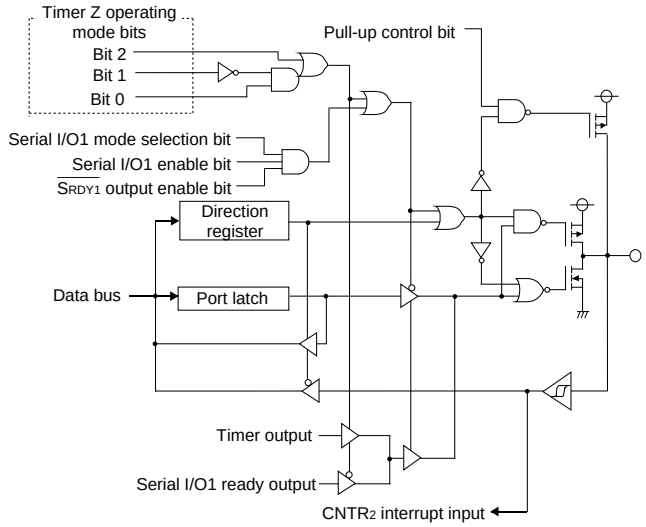
(10) Port P4$_0$



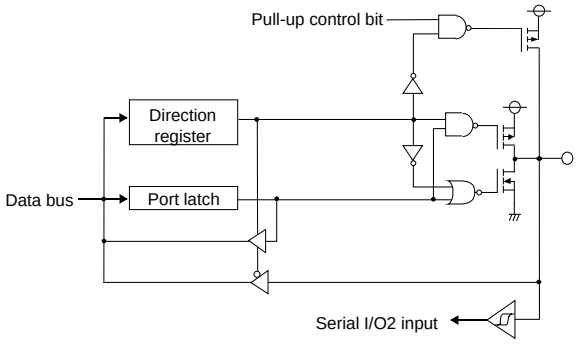
(11) Port P4$_1$



(12) Port P4$_7$



(13) Port P5$_0$



(14) Port P5$_1$

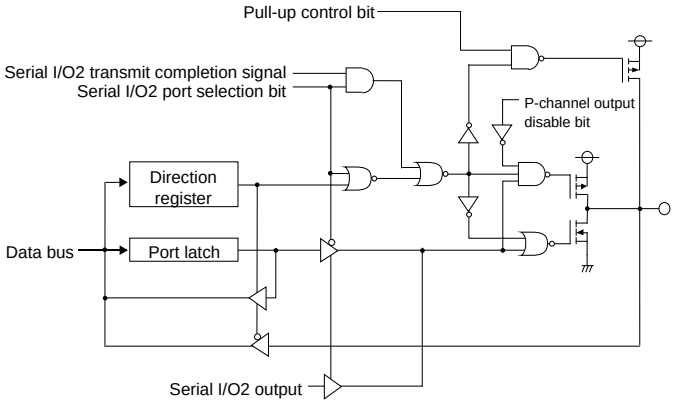
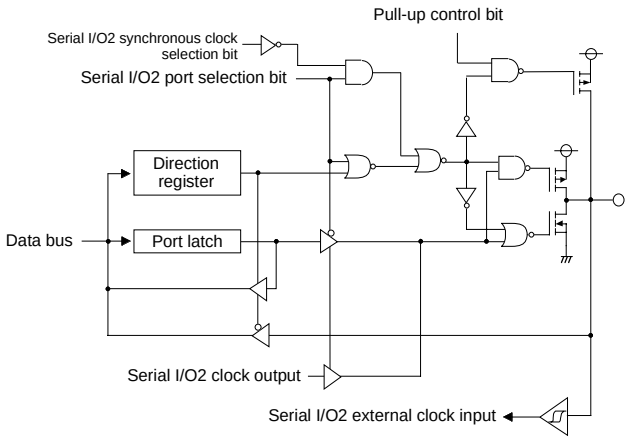
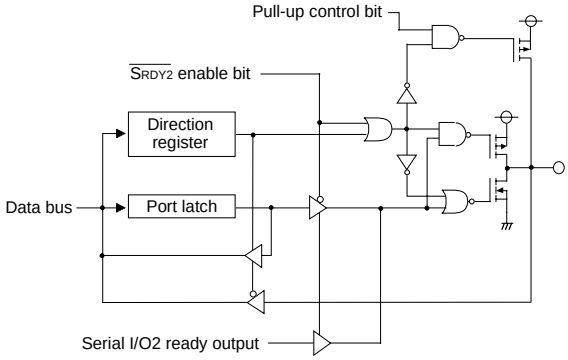


Fig. 17 Port block diagram of 3803 group (2)

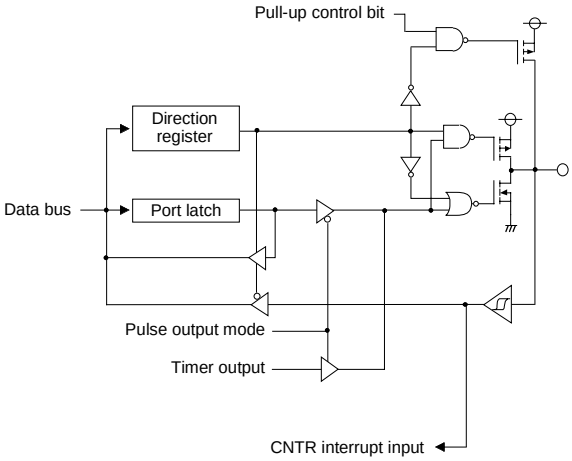
(15) Port P5$_2$



(16) Port P5$_3$



(17) Ports P5$_4$, P5$_5$



(18) Port P5$_6$

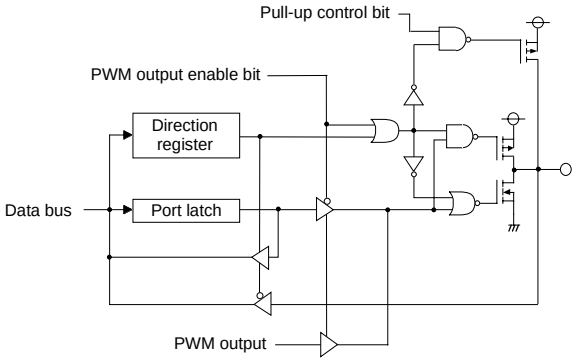
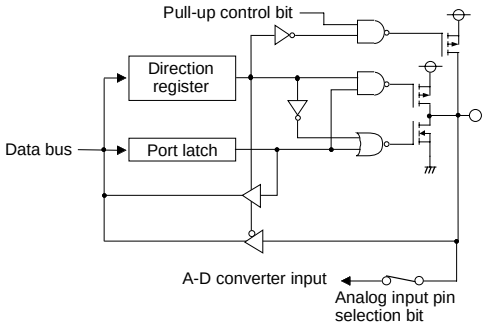
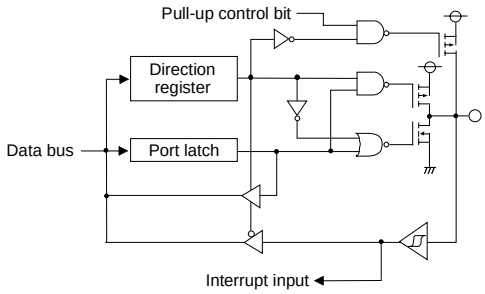


Fig. 18 Port block diagram of 3803 group (3)

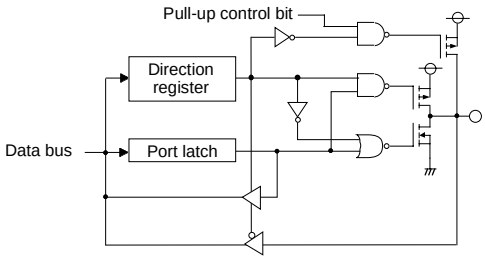
(1) Ports P0, P6



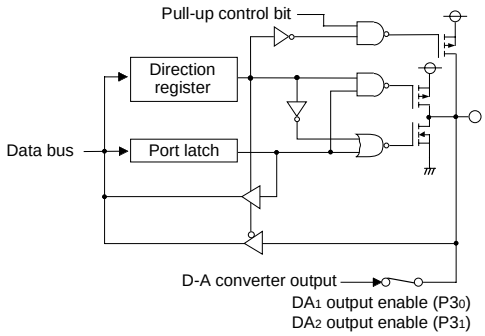
(2) Ports P10, P11, P42, P43, P57



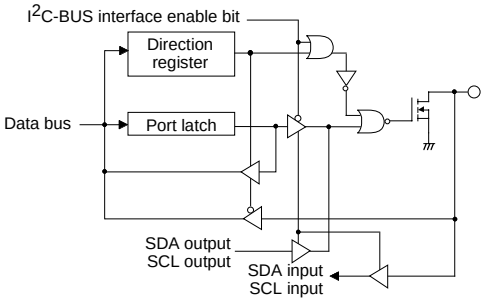
(3) Ports P12 to P17, P2



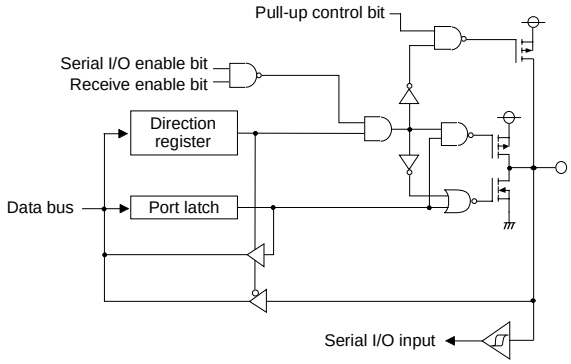
(4) Ports P30, P31



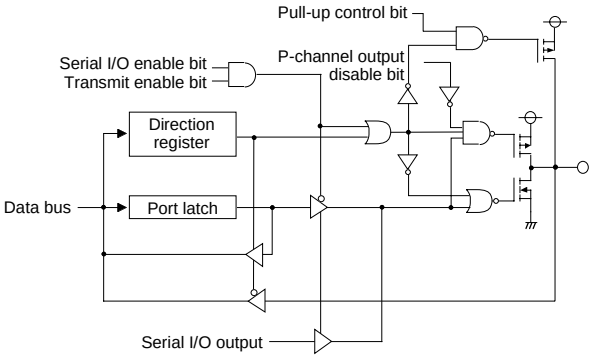
(5) Ports P32, P33



(6) Ports P34, P44



(7) Ports P35, P45



(8) Ports P36, P46

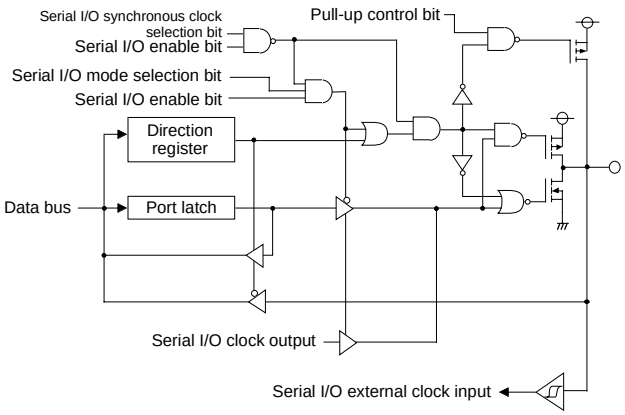
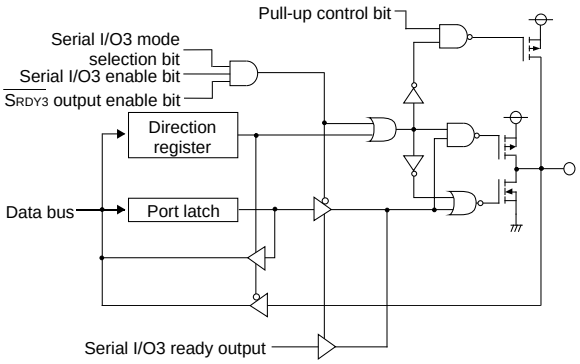
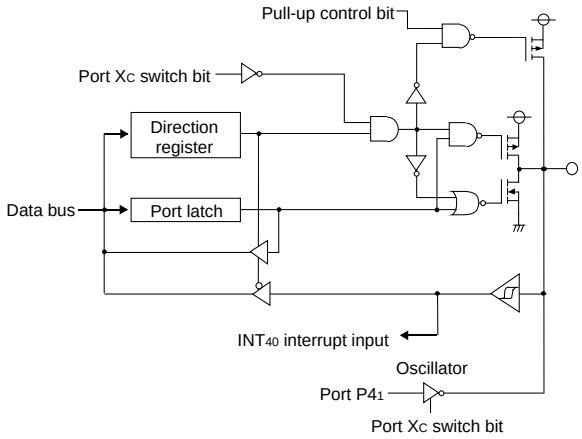


Fig. 19 Port block diagram of 3804 group (1)

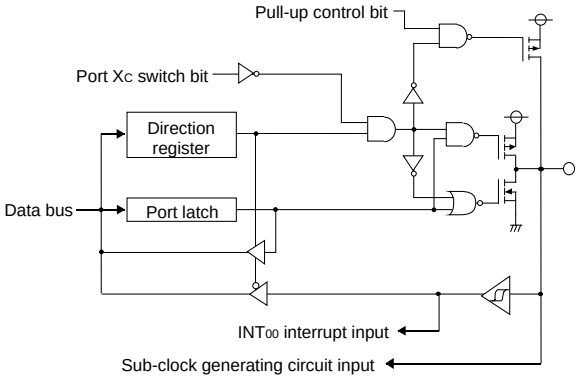
(9) Port P3$_7$



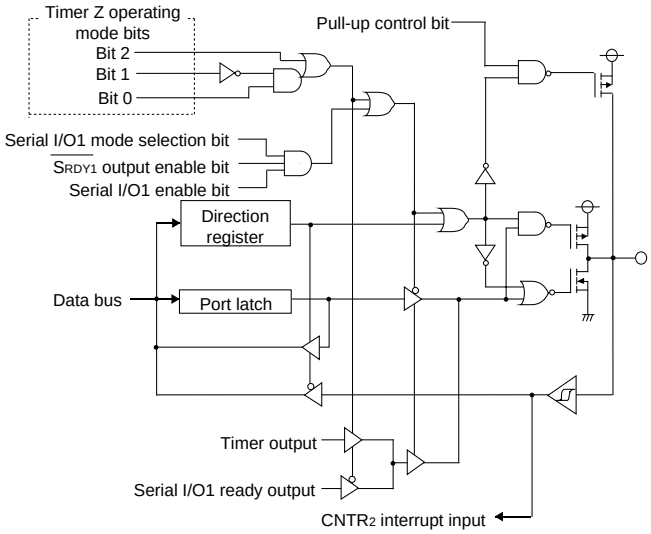
(10) Port P4$_0$



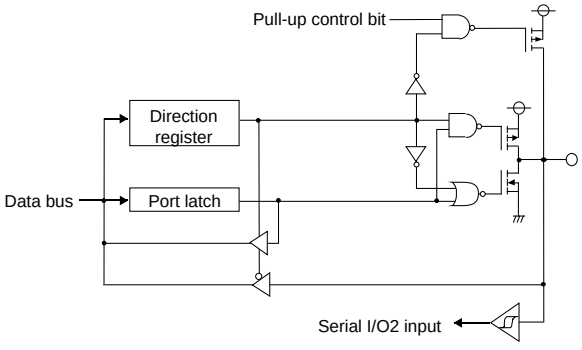
(11) Port P4$_1$



(12) Port P4$_7$



(13) Port P5$_0$



(14) Port P5$_1$

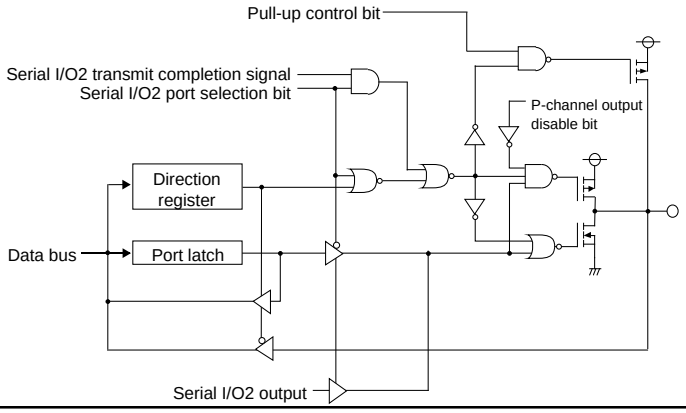
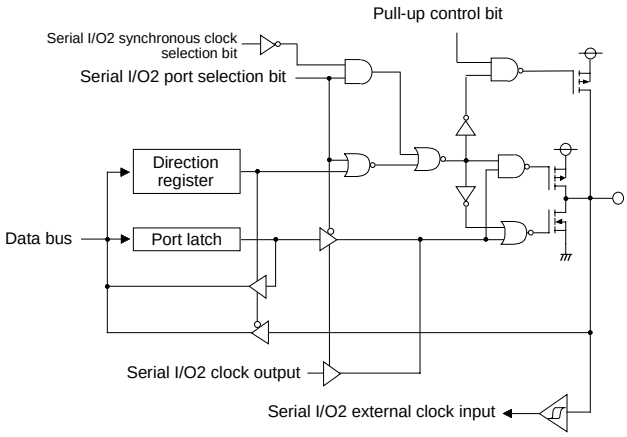
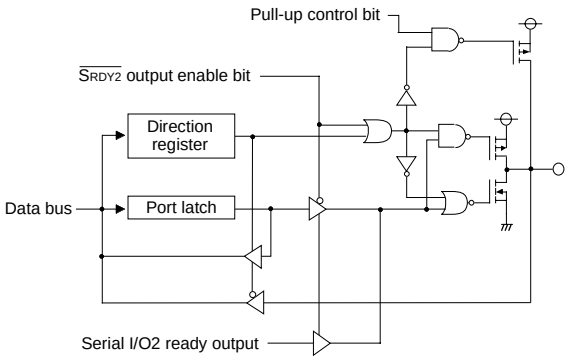


Fig. 20 Port block diagram of 3804 group (2)

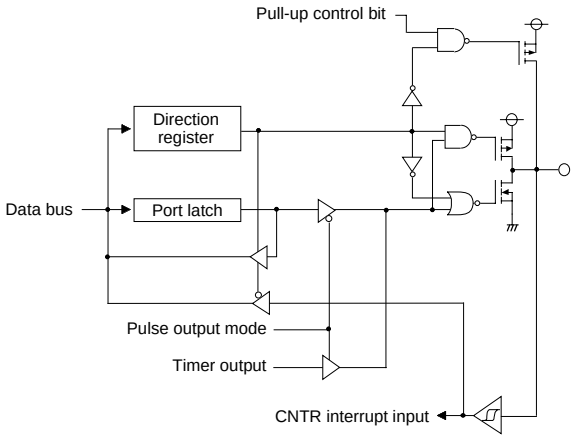
(15) Port P5$_2$



(16) Port P5$_3$



(17) Ports P5$_4$, P5$_5$



(18) Port P5$_6$

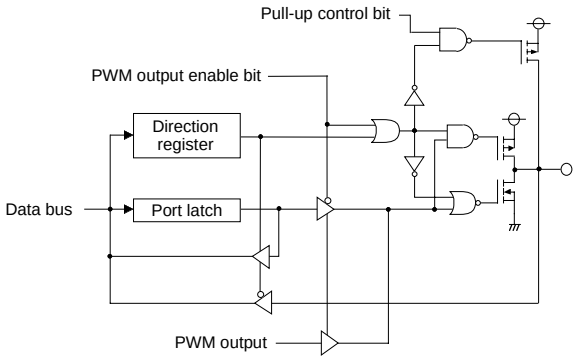
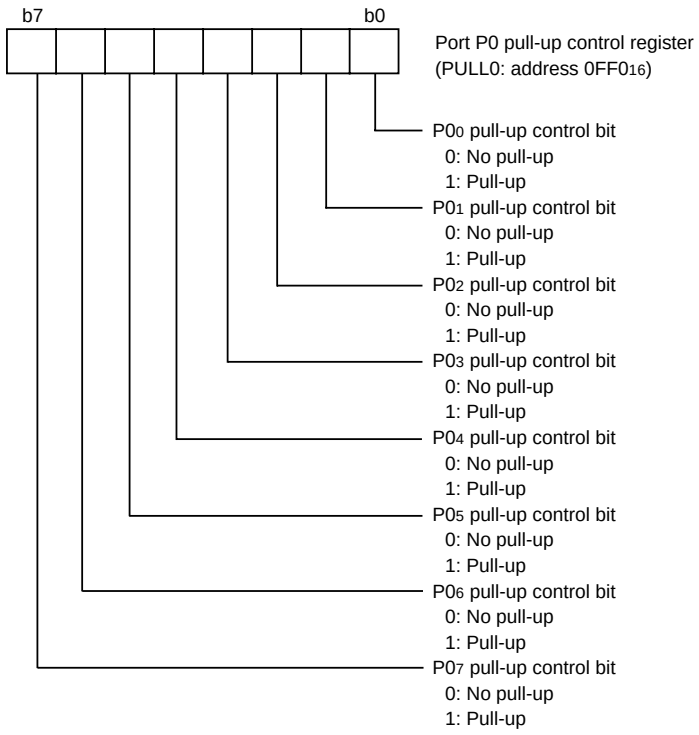
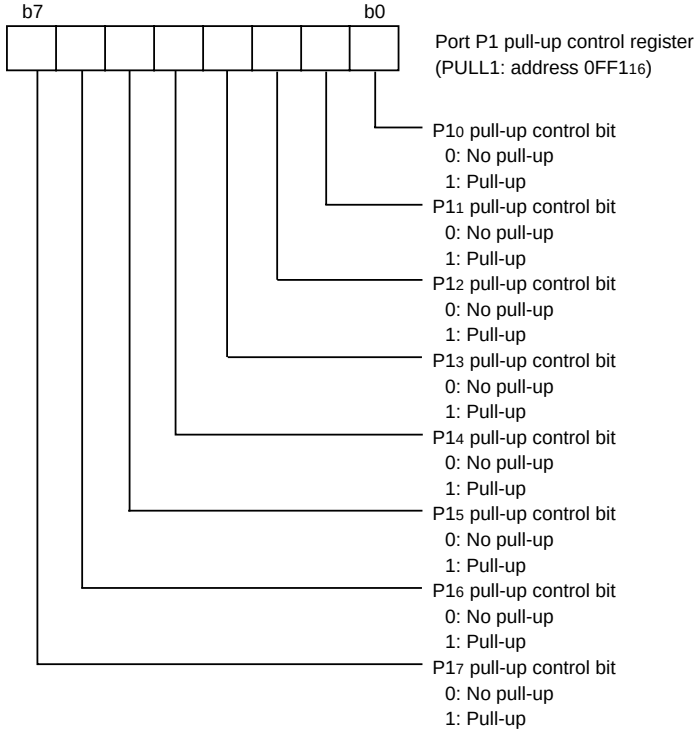


Fig. 21 Port block diagram of 3804 group (3)

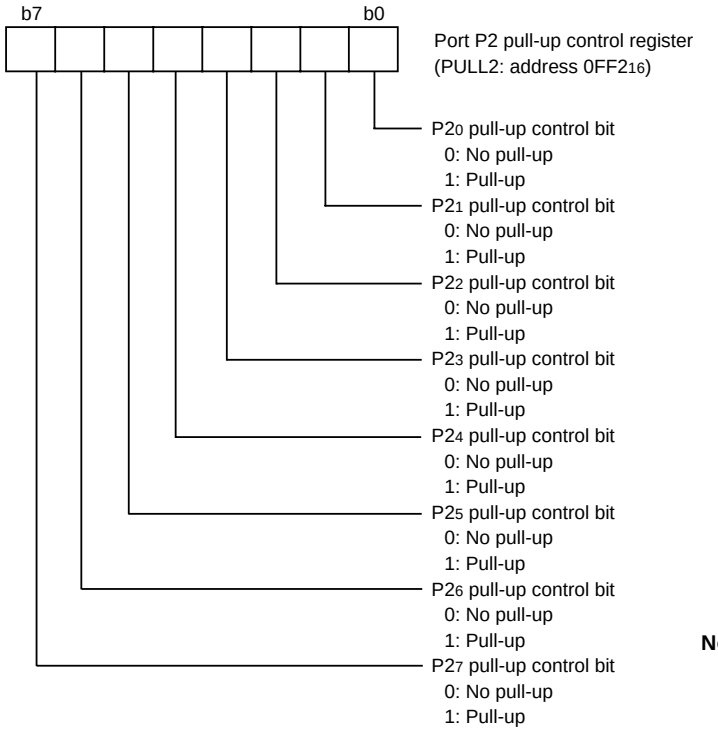


Note: Pull-up control is valid when the corresponding bit of the port direction register is “0” (input).
When that bit is “1” (output), pull-up cannot be set to the port of which pull-up is selected.

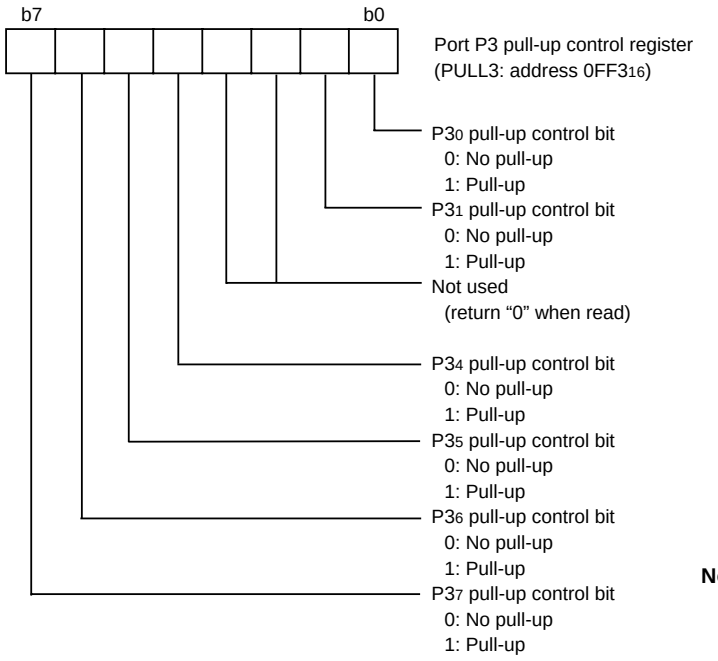


Note: Pull-up control is valid when the corresponding bit of the port direction register is “0” (input).
When that bit is “1” (output), pull-up cannot be set to the port of which pull-up is selected.

Fig. 22 Structure of port pull-up control register (1)

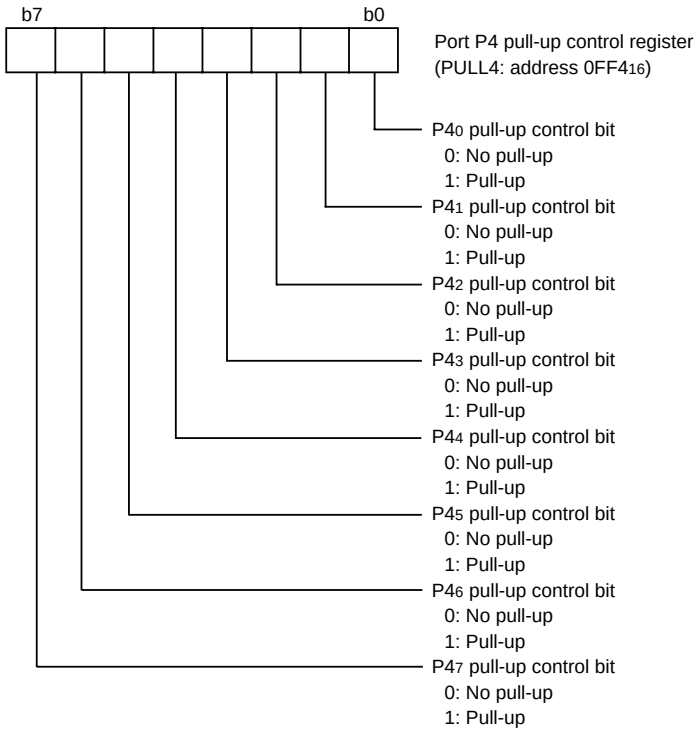


Note: Pull-up control is valid when the corresponding bit of the port direction register is “0” (input).
When that bit is “1” (output), pull-up cannot be set to the port of which pull-up is selected.

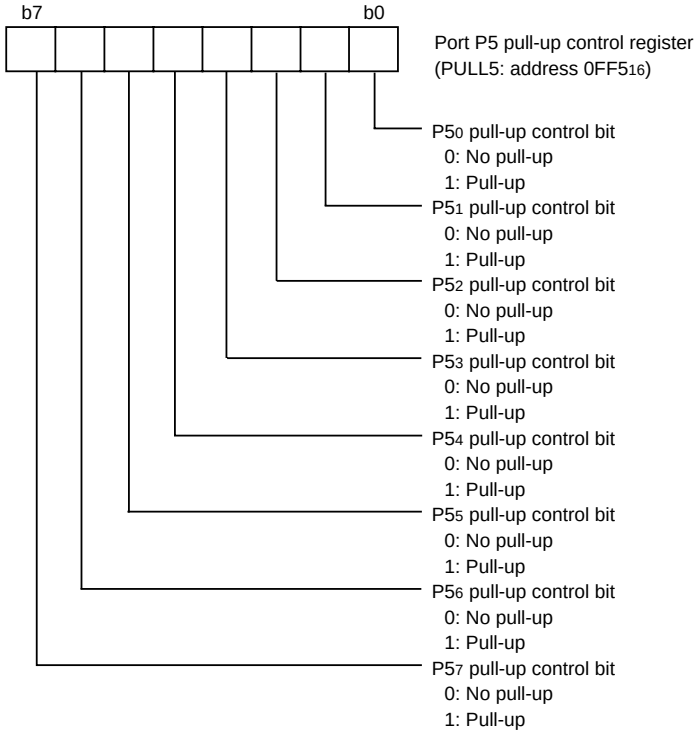


Note: Pull-up control is valid when the corresponding bit of the port direction register is “0” (input).
When that bit is “1” (output), pull-up cannot be set to the port of which pull-up is selected.

Fig. 23 Structure of port pull-up control register (2)



Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input). When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.



Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input). When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.

Fig. 24 Structure of port pull-up control register (3)

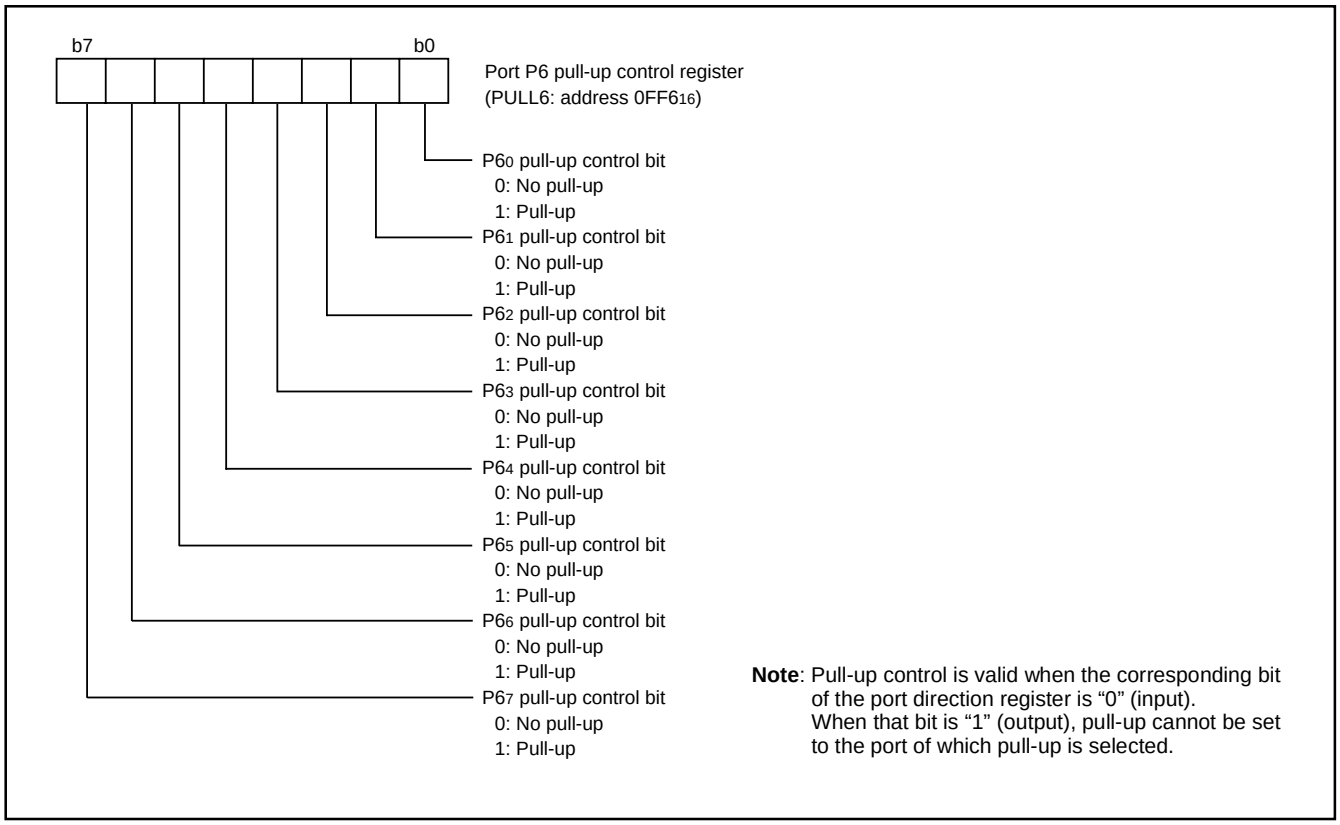


Fig. 25 Structure of port pull-up control register (4)

INTERRUPTS

The 3803 group's interrupts are a type of vector and occur by 16 sources among 21 sources: eight external, twelve internal, and one software.

The 3804 group's interrupts occur by 16 sources among 23 sources: nine external, thirteen internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The reset and the BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the reset and the BRK instruction interrupt.

When several interrupt requests occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

Interrupt Source Selection

Which of each combination of the following interrupt sources can be selected by the interrupt source selection register (address 0039_{16}).

1. INT_0 or Timer Z
2. Serial I/O1 transmission or SCL, SDA (for 3804 group)
3. $CNTR_0$ or SCL, SDA (for 3804 group)
4. $CNTR_1$ or Serial I/O3 reception
5. Serial I/O2 or Timer Z
6. INT_2 or I^2C (for 3804 group)
7. INT_4 or $CNTR_2$
8. A-D converter or serial I/O3 transmission

External Interrupt Pin Selection

The occurrence sources of the external interrupt INT_0 and INT_4 can be selected from either input from INT_{00} and INT_{40} pin, or input from INT_{01} and INT_{41} pin by the INT_0, INT_4 interrupt switch bit of interrupt edge selection register (bit 6 of address $003A_{16}$).

■ Notes

When setting the followings, the interrupt request bit may be set to "1".

•When switching external interrupt active edge
Related register: Interrupt edge selection register (address $3A_{16}$)
Timer XY mode register (address 23_{16})
Timer Z mode register (address $2A_{16}$)
I^2C start/stop condition control register (address 16_{16}) (3804 group only)

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
Related register: Interrupt source selection register (address 39_{16})

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

①Set the corresponding interrupt enable bit to "0" (disabled).
②Set the interrupt edge select bit or the interrupt source select bit.
③Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
④Set the corresponding interrupt enable bit to "1" (enabled).

Table 8 Interrupt vector addresses and priority of 3803 group

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
Timer Z				At timer Z underflow	
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Serial I/O1 reception	4	$FFF7_{16}$	$FFF6_{16}$	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	5	$FFF5_{16}$	$FFF4_{16}$	At completion of serial I/O1 transmission shift or when transmission buffer is empty	Valid when serial I/O1 is selected
Timer X	6	$FFF3_{16}$	$FFF2_{16}$	At timer X underflow	
Timer Y	7	$FFF1_{16}$	$FFF0_{16}$	At timer Y underflow	
Timer 1	8	$FFEF_{16}$	$FFEE_{16}$	At timer 1 underflow	STP release timer underflow
Timer 2	9	$FFED_{16}$	$FFEC_{16}$	At timer 2 underflow	
$CNTR_0$	10	$FFEB_{16}$	$FFEA_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	11	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
Serial I/O3 reception				At completion of serial I/O3 data reception	Valid when serial I/O3 is selected
Serial I/O2	12	$FFE7_{16}$	$FFE6_{16}$	At completion of serial I/O2 data transmission or reception	Valid when serial I/O2 is selected
Timer Z				At timer Z underflow	
INT_2	13	$FFE5_{16}$	$FFE4_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
INT_3	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of INT_3 input	External interrupt (active edge selectable)
INT_4	15	$FFE1_{16}$	$FFE0_{16}$	At detection of either rising or falling edge of INT_4 input	External interrupt (active edge selectable)
$CNTR_2$				At detection of either rising or falling edge of $CNTR_2$ input	External interrupt (active edge selectable)
A-D converter	16	$FFDF_{16}$	$FFDE_{16}$	At completion of A-D conversion	
Serial I/O3 transmission				At completion of serial I/O3 transmission shift or when transmission buffer is empty	Valid when serial I/O3 is selected
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

Table 9 Interrupt vector addresses and priority of 3804 group

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
Timer Z				At timer Z underflow	
INT1	3	FFF916	FFF816	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
Serial I/O1 reception	4	FFF716	FFF616	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	5	FFF516	FFF416	At completion of serial I/O1 transmission shift or when transmission buffer is empty	Valid when serial I/O1 is selected
SCL, SDA				At detection of either rising or falling edge of SCL or SDA	External interrupt (active edge selectable)
Timer X	6	FFF316	FFF216	At timer X underflow	
Timer Y	7	FFF116	FFF016	At timer Y underflow	
Timer 1	8	FFEF16	FFEE16	At timer 1 underflow	STP release timer underflow
Timer 2	9	FFED16	FFEC16	At timer 2 underflow	
CNTR0	10	FFEB16	FFEA16	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
SCL, SDA				At detection of either rising or falling edge of SCL or SDA	External interrupt (active edge selectable)
CNTR1	11	FFE916	FFE816	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
Serial I/O3 reception				At completion of serial I/O3 data reception	Valid when serial I/O3 is selected
Serial I/O2	12	FFE716	FFE616	At completion of serial I/O2 data transmission or reception	Valid when serial I/O2 is selected
Timer Z				At timer Z underflow	
INT2	13	FFE516	FFE416	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
I^2C				At completion of data transfer	
INT3	14	FFE316	FFE216	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
INT4	15	FFE116	FFE016	At detection of either rising or falling edge of INT4 input	External interrupt (active edge selectable)
CNTR2				At detection of either rising or falling edge of CNTR2 input	External interrupt (active edge selectable)
A-D converter	16	FFDF16	FFDE16	At completion of A-D conversion	
Serial I/O3 transmission				At completion of serial I/O3 transmission shift or when transmission buffer is empty	Valid when serial I/O3 is selected
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

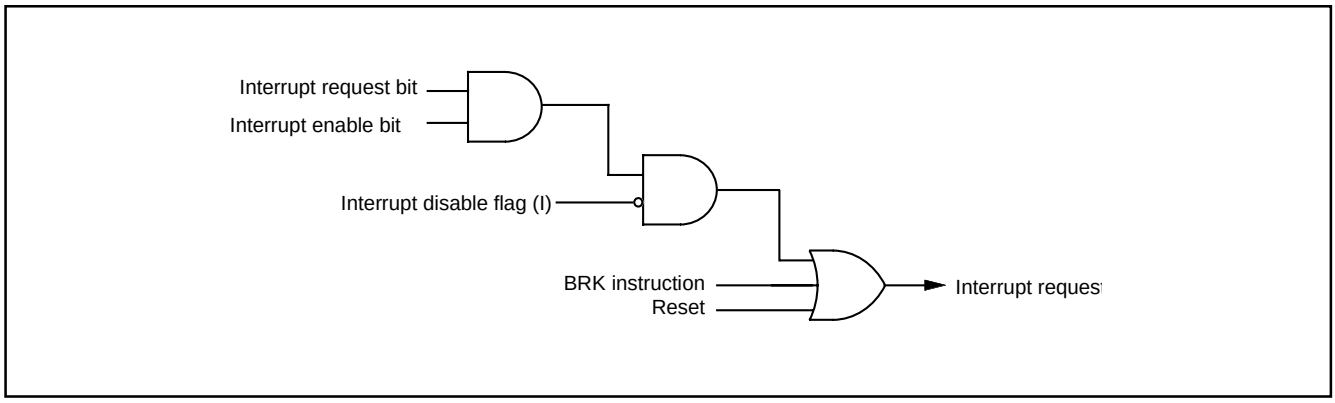


Fig. 26 Interrupt control

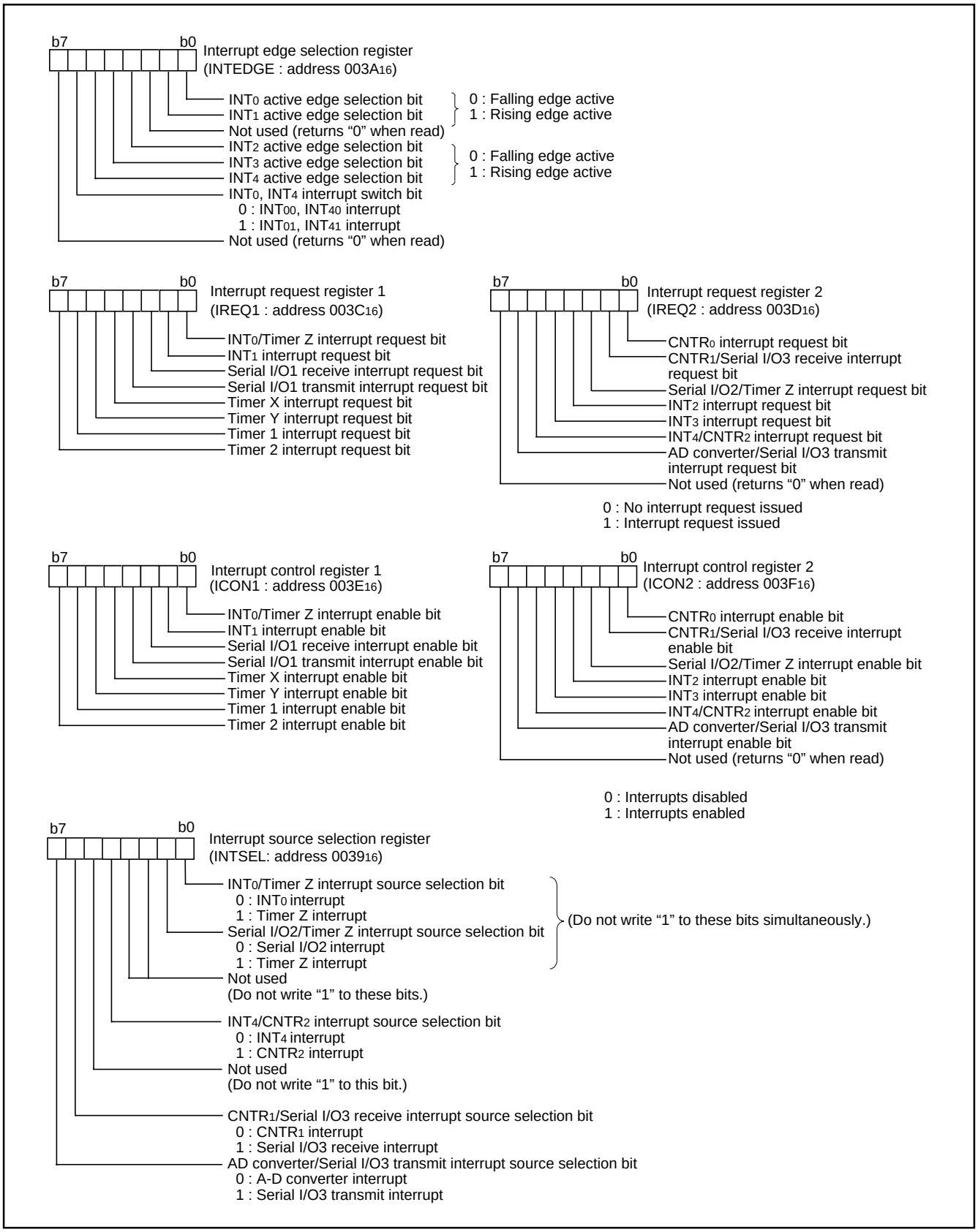


Fig. 27 Structure of interrupt-related registers of 3803 group

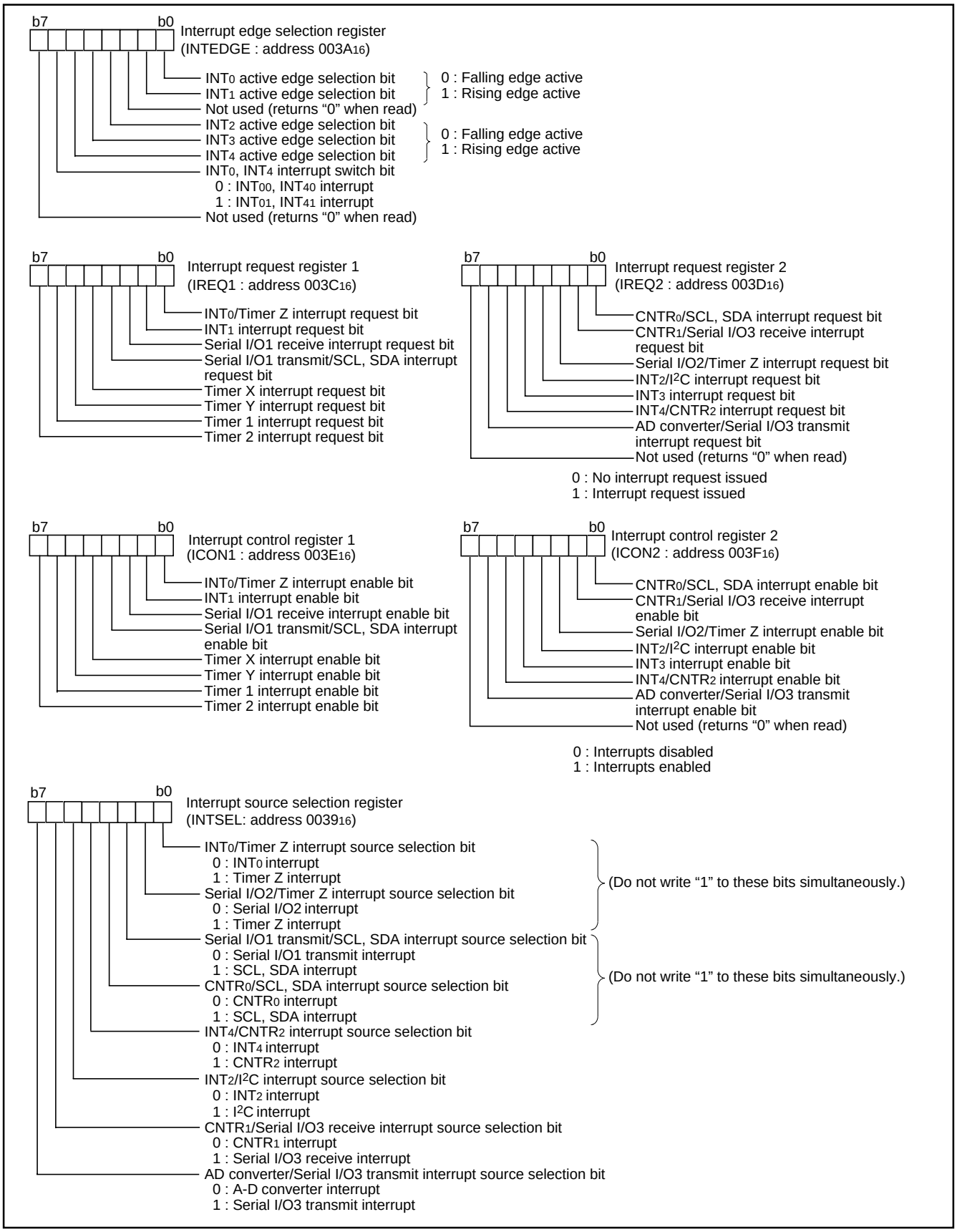


Fig. 28 Structure of interrupt-related registers of 3804 group

TIMERS

●8-bit Timers

The 3803/3804 group has four 8-bit timers: timer 1, timer 2, timer X, and timer Y.

The timer 1 and timer 2 use one prescaler in common, and the timer X and timer Y use each prescaler. Those are 8-bit prescalers. Each of the timers and prescalers has a timer latch or a prescaler latch.

The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch.

All timers are down-counters. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the contents of the corresponding timer latch are reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to that timer is set to "1".

●Timer divider

The divider count source is switched by the main clock division ratio selection bits of CPU mode register (bits 7 and 6 at address $003B_{16}$). When these bits are "00" (high-speed mode) or "01" (middle-speed mode), X_{IN} is selected. When these bits are"10" (low-speed mode), X_{CIN} is selected.

●Prescaler 12

The prescaler 12 counts the output of the timer divider. The count source is selected by the timer 12, X count source selection register among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024 of f(X_{IN}) or f(X_{CIN}).

Timer 1 and Timer 2

The timer 1 and timer 2 counts the output of prescaler 12 and periodically set the interrupt request bit.

●Prescaler X and prescaler Y

The prescaler X and prescaler Y count the output of the timer divider or f(X_{CIN}). The count source is selected by the timer 12, X count source selection register (address $000E_{16}$) and the timer Y, Z count source selection register (address $000F_{16}$) among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, and 1/1024 of f(X_{IN}) or f(X_{CIN}); and f(X_{CIN}).

Timer X and Timer Y

The timer X and timer Y can each select one of four operating modes by setting the timer XY mode register (address 0023_{16}).

(1) Timer mode

●Mode selection

This mode can be selected by setting "00" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023_{16}).

●Explanation of operation

The timer count operation is started by setting "0" to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 0023_{16}).

When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the contents of timer latch are reloaded into the timer and the count is continued.

(2) Pulse output mode

●Mode selection

This mode can be selected by setting "01" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023_{16}).

●Explanation of operation

The operation is the same as the timer mode's. Moreover the pulse which is inverted each time the timer underflows is output from $CNTR_0$/$CNTR_1$ pin. When the $CNTR_0$ active edge switch bit (bit 2) and the $CNTR_1$ active edge switch bit (bit 6) of the timer XY mode register (address 0023_{16}) is "0", the output starts with "H" level. When it is "1", the output starts with "L" level.

When the value of the $CNTR_0$/$CNTR_1$ active edge switch bit is changed during pulse output, the output level of the $CNTR_0$/$CNTR_1$ pin is inverted.

■Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin and port $P5_4$/$P5_5$ to output in this mode.

(3) Event counter mode

●Mode selection

This mode can be selected by setting “10” to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023_{16}).

●Explanation of operation

The operation is the same as the timer mode’s except that the timer counts signals input from the $CNTR_0$ or $CNTR_1$ pin. The valid edge for the count operation depends on the $CNTR_0$ active edge switch bit (bit 2) or the $CNTR_1$ active edge switch bit (bit 6) of the timer XY mode register (address 0023_{16}). When it is “0”, the rising edge is valid. When it is “1”, the falling edge is valid.

■Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin and port $P5_4$/$P5_5$ to input in this mode.

(4) Pulse width measurement mode

●Mode selection

This mode can be selected by setting “11” to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023_{16}).

●Explanation of operation

When the $CNTR_0$ active edge switch bit (bit 2) or the $CNTR_1$ active edge switch bit (bit 6) of the timer XY mode register (address 0023_{16}) is “1”, the timer counts during the term of one falling edge of $CNTR_0$/$CNTR_1$ pin input until the next rising edge of input (“L” term). When it is “0”, the timer counts during the term of one rising edge input until the next falling edge input (“H” term).

■Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin and port $P5_4$/$P5_5$ to input in this mode.

The count operation can be stopped by setting “1” to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 0023_{16}). The interrupt request bit is set to “1” each time the timer underflows.

•Precautions when switching count source

When switching the count source by the timer 12, X and Y count source selection bits, the value of timer count is altered in inconsiderable amount owing to generating of thin pulses on the count input signals.

Therefore, select the timer count source before setting the value to the prescaler and the timer.

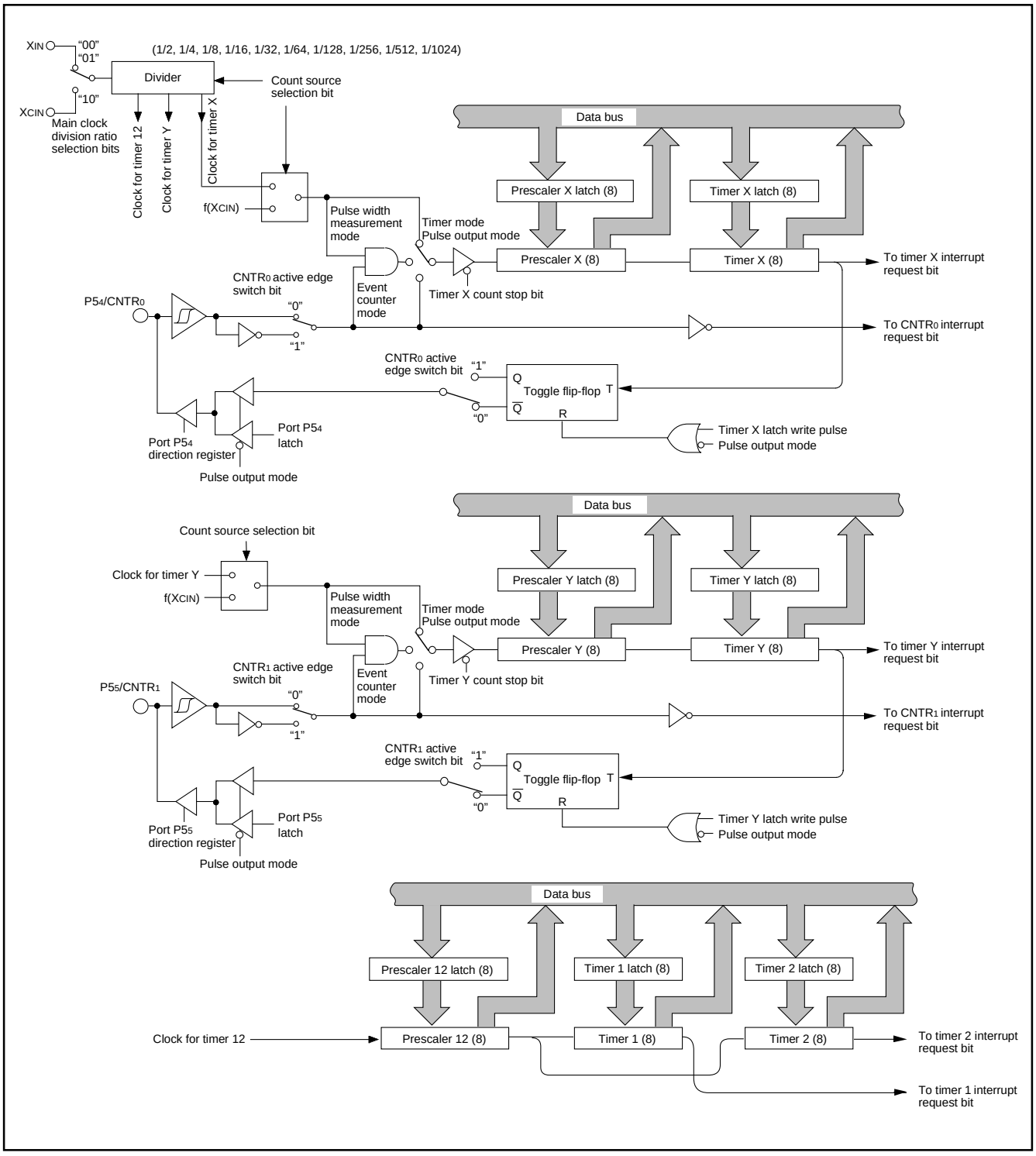


Fig. 29 Block diagram of timer X, timer Y, timer 1, and timer 2

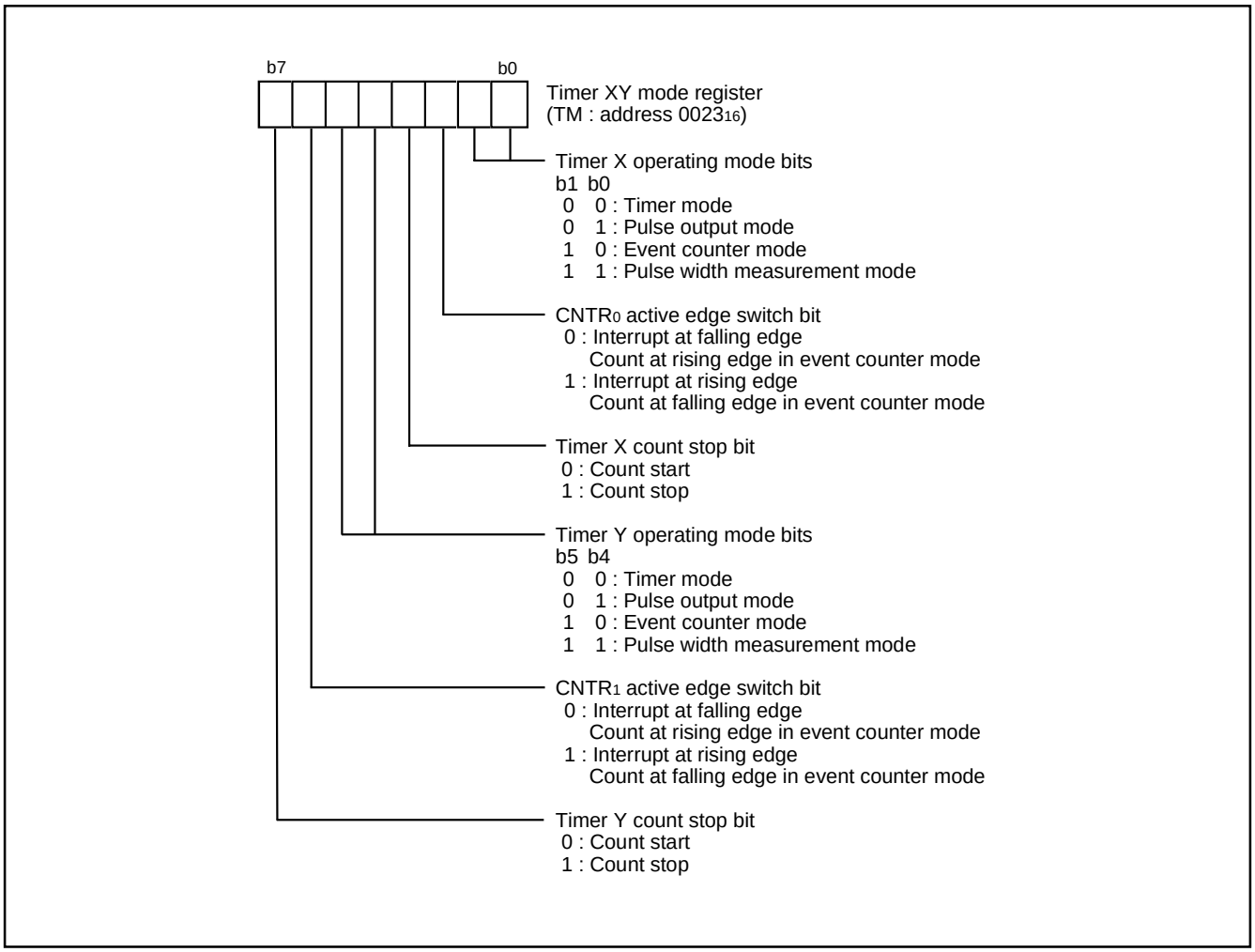


Fig. 30 Structure of timer XY mode register

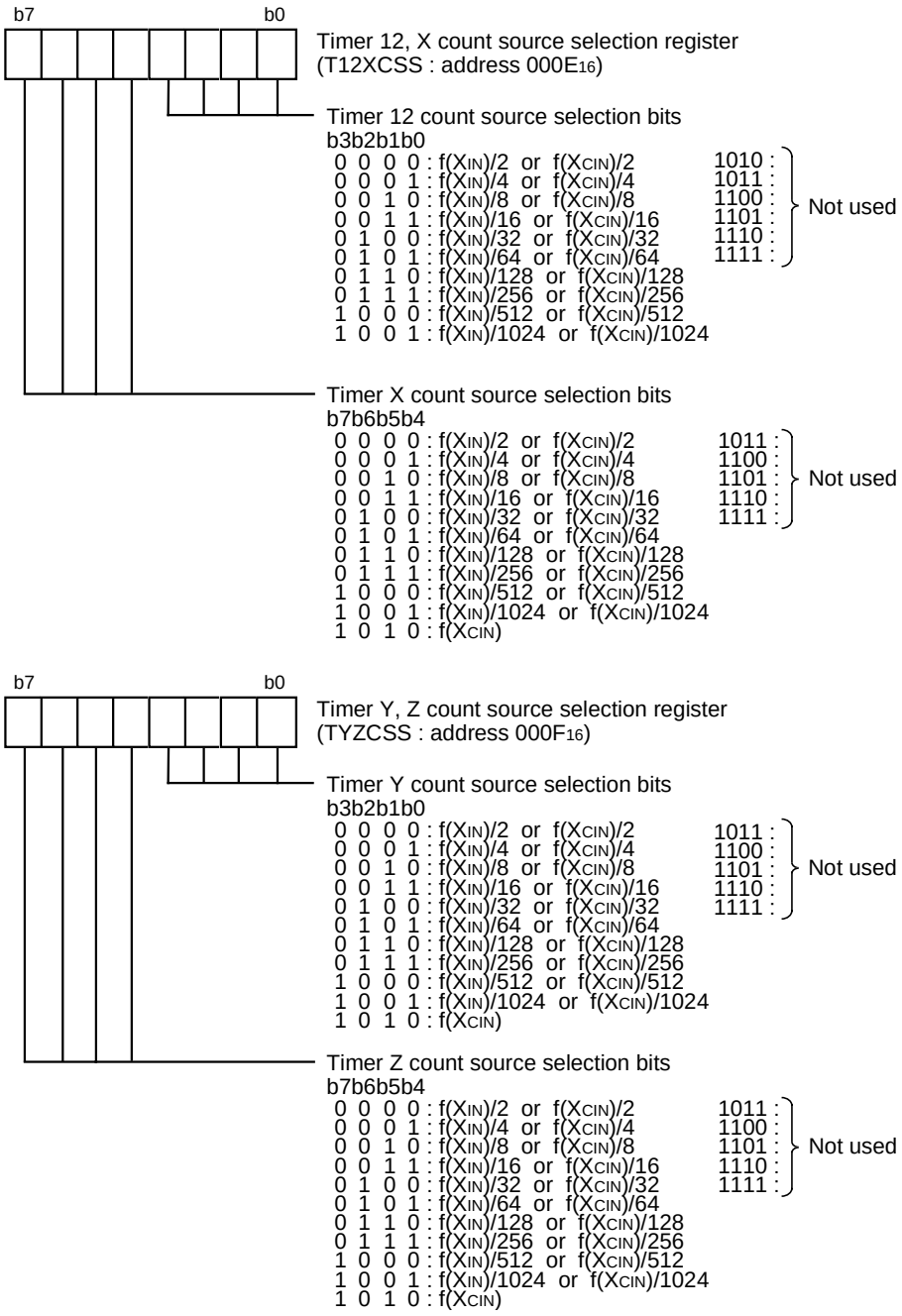


Fig. 31 Structure of timer 12, X and timer Y, Z count source selection registers

●16-bit Timers

The timer Z is a 16-bit timer. When the timer reaches "0000_{16}", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to the timer Z is set to "1".

When reading/writing to the timer Z, perform reading/writing to both the high-order byte and the low-order byte. When reading the timer Z, read from the high-order byte first, followed by the low-order byte. Do not perform the writing to the timer Z between read operation of the high-order byte and read operation of the low-order byte. When writing to the timer Z, write to the low-order byte first, followed by the high-order byte. Do not perform the reading to the timer Z between write operation of the low-order byte and write operation of the high-order byte.

The timer Z can select the count source by the timer Z count source selection bits of timer Y, Z count source selection register (bits 7 to 4 at address $000F_{16}$).

Timer Z can select one of seven operating modes by setting the timer Z mode register (address $002A_{16}$).

(1) Timer mode

●Mode selection

This mode can be selected by setting "000" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address $002A_{16}$).

●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X_{IN}); or f(X_{CIN}) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X_{CIN}); or f(X_{CIN}) can be selected as the count source.

●Interrupt

When an underflow occurs, the INT_0/timer Z interrupt request bit (bit 0) of the interrupt request register 1 (address $003C_{16}$) is set to "1".

●Explanation of operation

During timer stop, usually write data to a latch and a timer at the same time to set the timer value.

The timer count operation is started by setting "0" to the timer Z count stop bit (bit 6) of the timer Z mode register (address $002A_{16}$).

When the timer reaches "0000_{16}", an underflow occurs at the next count pulse and the contents of timer latch are reloaded into the timer and the count is continued.

When writing data to the timer during operation, the data is written only into the latch. Then the new latch value is reloaded into the timer at the next underflow.

(2) Event counter mode

●Mode selection

This mode can be selected by setting "000" to the timer Z operating mode bits (bits 2 to 0) and setting "1" to the timer/event counter mode switch bit (bit 7) of the timer Z mode register (address $002A_{16}$).

The valid edge for the count operation depends on the $CNTR_2$ active edge switch bit (bit 5) of the timer Z mode register (address $002A_{16}$). When it is "0", the rising edge is valid. When it is "1", the falling edge is valid.

●Interrupt

The interrupt at an underflow is the same as the timer mode's.

●Explanation of operation

The operation is the same as the timer mode's.

Set the double-function port of $CNTR_2$ pin and port $P4_7$ to input in this mode.

Figure 34 shows the timing chart of the timer/event counter mode.

(3) Pulse output mode

●Mode selection

This mode can be selected by setting "001" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address $002A_{16}$).

●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X_{IN}); or f(X_{CIN}) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X_{CIN}); or f(X_{CIN}) can be selected as the count source.

●Interrupt

The interrupt at an underflow is the same as the timer mode's.

●Explanation of operation

The operation is the same as the timer mode's. Moreover the pulse which is inverted each time the timer underflows is output from $CNTR_2$ pin. When the $CNTR_2$ active edge switch bit (bit 5) of the timer Z mode register (address $002A_{16}$) is "0", the output starts with "H" level. When it is "1", the output starts with "L" level.

■Precautions

Set the double-function port of $CNTR_2$ pin and port $P4_7$ to output in this mode.

[During timer operation stop]

The output from $CNTR_2$ pin is initialized to the level depending on $CNTR_2$ active edge switch bit by writing to the timer.

[During timer operation enabled]

When the value of the $CNTR_2$ active edge switch bit is changed, the output level of $CNTR_2$ pin is inverted.

Figure 35 shows the timing chart of the pulse output mode.

(4) Pulse period measurement mode

●Mode selection

This mode can be selected by setting “010” to the timer Z operating mode bits (bits 2 to 0) and setting “0” to the timer/event counter mode switch bit (b7) of the timer Z mode register (address $002A_{16}$).

●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X_{IN}); or f(X_{CIN}) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X_{CIN}); or f(X_{CIN}) can be selected as the count source.

●Interrupt

The interrupt at an underflow is the same as the timer mode’s. When the pulse period measurement is completed, the INT_4/$CNTR_2$ interrupt request bit (bit 5) of the interrupt request register 2 (address $003D_{16}$) is set to “1”.

●Explanation of operation

The cycle of the pulse which is input from the $CNTR_2$ pin is measured. When the $CNTR_2$ active edge switch bit (bit 5) of the timer Z mode register (address $002A_{16}$) is “0”, the timer counts during the term from one falling edge of $CNTR_2$ pin input to the next falling edge. When it is “1”, the timer counts during the term from one rising edge input to the next rising edge input.

When the valid edge of measurement completion/start is detected, the 1’s complement of the timer value is written to the timer latch and “$FFFF_{16}$” is set to the timer.

Furthermore when the timer underflows, the timer Z interrupt request occurs and “$FFFF_{16}$” is set to the timer. When reading the timer Z, the value of the timer latch (measured value) is read. The measured value is retained until the next measurement completion.

■Precautions

Set the double-function port of $CNTR_2$ pin and port $P4_7$ to input in this mode.

A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse period).

Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.

“$FFFF_{16}$” is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected. Consequently, the timer value at start of pulse period measurement depends on the timer value just before measurement start.

Figure 36 shows the timing chart of the pulse period measurement mode.

(5) Pulse width measurement mode

●Mode selection

This mode can be selected by setting “011” to the timer Z operating mode bits (bits 2 to 0) and setting “0” to the timer/event counter mode switch bit (b7) of the timer Z mode register (address $002A_{16}$).

●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X_{IN}); or f(X_{CIN}) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X_{CIN}); or f(X_{CIN}) can be selected as the count source.

●Interrupt

The interrupt at an underflow is the same as the timer mode’s. When the pulse widths measurement is completed, the INT_4/$CNTR_2$ interrupt request bit (bit 5) of the interrupt request register 2 (address $003D_{16}$) is set to “1”.

●Explanation of operation

The pulse width which is input from the $CNTR_2$ pin is measured. When the $CNTR_2$ active edge switch bit (bit 5) of the timer Z mode register (address $002A_{16}$) is “0”, the timer counts during the term from one rising edge input to the next falling edge input (“H” term). When it is “1”, the timer counts during the term from one falling edge of $CNTR_2$ pin input to the next rising edge of input (“L” term).

When the valid edge of measurement completion is detected, the 1’s complement of the timer value is written to the timer latch and “$FFFF_{16}$” is set to the timer.

When the timer Z underflows, the timer Z interrupt occurs and “$FFFF_{16}$” is set to the timer Z. When reading the timer Z, the value of the timer latch (measured value) is read. The measured value is retained until the next measurement completion.

■Precautions

Set the double-function port of $CNTR_2$ pin and port $P4_7$ to input in this mode.

A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse widths).

Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.

“$FFFF_{16}$” is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected. Consequently, the timer value at start of pulse width measurement depends on the timer value just before measurement start.

Figure 37 shows the timing chart of the pulse width measurement mode.

(6) Programmable waveform generating mode

●Mode selection

This mode can be selected by setting "100" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address $002A_{16}$).

●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X_{IN}); or f(X_{CIN}) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X_{CIN}); or f(X_{CIN}) can be selected as the count source.

●Interrupt

The interrupt at an underflow is the same as the timer mode's.

●Explanation of operation

The operation is the same as the timer mode's. Moreover the timer outputs the data set in the output level latch (bit 4) of the timer Z mode register (address $002A_{16}$) from the $CNTR_2$ pin each time the timer underflows.

Changing the value of the output level latch and the timer latch after an underflow makes it possible to output an optional waveform from the $CNTR_2$ pin.

■Precautions

Set the double-function port of $CNTR_2$ pin and port $P4_7$ to output in this mode.

Figure 38 shows the timing chart of the programmable waveform generating mode.

(7) Programmable one-shot generating mode

●Mode selection

This mode can be selected by setting "101" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address $002A_{16}$).

●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X_{IN}); or f(X_{CIN}) can be selected as the count source.

●Interrupt

The interrupt at an underflow is the same as the timer mode's.

The trigger to generate one-shot pulse can be selected by the INT_1 active edge selection bit (bit 1) of the interrupt edge selection register (address $003A_{16}$). When it is "0", the falling edge active is selected; when it is "1", the rising edge active is selected.

When the valid edge of the INT_1 pin is detected, the INT_1 interrupt request bit (bit 1) of the interrupt request register 1 (address $003C_{16}$) is set to "1".

●Explanation of operation

•"H" one-shot pulse; Bit 5 of timer Z mode register = "0"

The output level of the $CNTR_2$ pin is initialized to "L" at mode selection. When trigger generation (input signal to INT_1 pin) is detected, "H" is output from the $CNTR_2$ pin. When an underflow occurs, "L" is output. The "H" one-shot pulse width is set by the setting value to the timer Z register low-order and high-order. When trigger generating is detected during timer count stop, although "H" is output from the $CNTR_2$ pin, "H" output state continues because an underflow does not occur.

•"L" one-shot pulse; Bit 5 of timer Z mode register = "1"

The output level of the $CNTR_2$ pin is initialized to "H" at mode selection. When trigger generation (input signal to INT_1 pin) is detected, "L" is output from the $CNTR_2$ pin. When an underflow occurs, "H" is output. The "L" one-shot pulse width is set by the setting value to the timer Z low-order and high-order. When trigger generating is detected during timer count stop, although "L" is output from the $CNTR_2$ pin, "L" output state continues because an underflow does not occur.

■Precautions

Set the double-function port of $CNTR_2$ pin and port $P4_7$ to output, and of INT_1 pin and port $P4_2$ to input in this mode.

This mode cannot be used in low-speed mode.

If the value of the $CNTR_2$ active edge switch bit is changed during one-shot generating enabled or generating one-shot pulse, then the output level from $CNTR_2$ pin changes.

Figure 39 shows the timing chart of the programmable one-shot generating mode.

■Notes regarding all modes

●Timer Z write control

Which write control can be selected by the timer Z write control bit (bit 3) of the timer Z mode register (address $002A_{16}$), writing data to both the latch and the timer at the same time or writing data only to the latch.

When the operation "writing data only to the latch" is selected, the value is set to the timer latch by writing data to the address of timer Z and the timer is updated at next underflow. After reset release, the operation "writing data to both the latch and the timer at the same time" is selected, and the value is set to both the latch and the timer at the same time by writing data to the address of timer Z.

In the case of writing data only to the latch, if writing data to the latch and an underflow are performed almost at the same time, the timer value may become undefined.

●Timer Z read control

A read-out of timer value is impossible in pulse period measurement mode and pulse width measurement mode. In the other modes, a read-out of timer value is possible regardless of count operating or stopped.

However, a read-out of timer latch value is impossible.

●Switch of interrupt active edge of $CNTR_2$ and INT_1

Each interrupt active edge depends on setting of the $CNTR_2$ active edge switch bit and the INT_1 active edge selection bit.

●Switch of count source

When switching the count source by the timer Z count source selection bits, the value of timer count is altered in inconsiderable amount owing to generating of thin pulses on the count input signals.

Therefore, select the timer count source before setting the value to the prescaler and the timer.

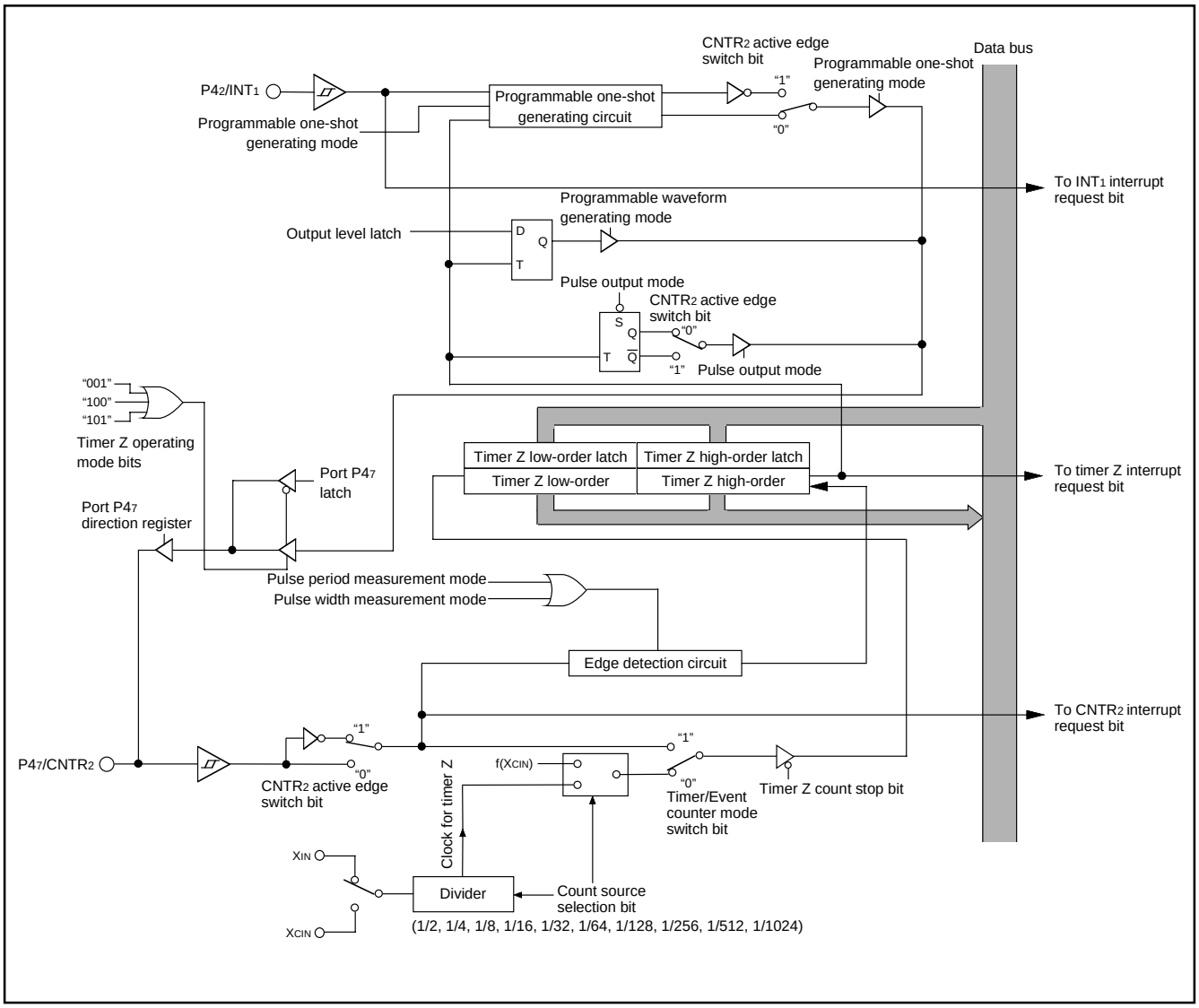


Fig. 32 Block diagram of timer Z

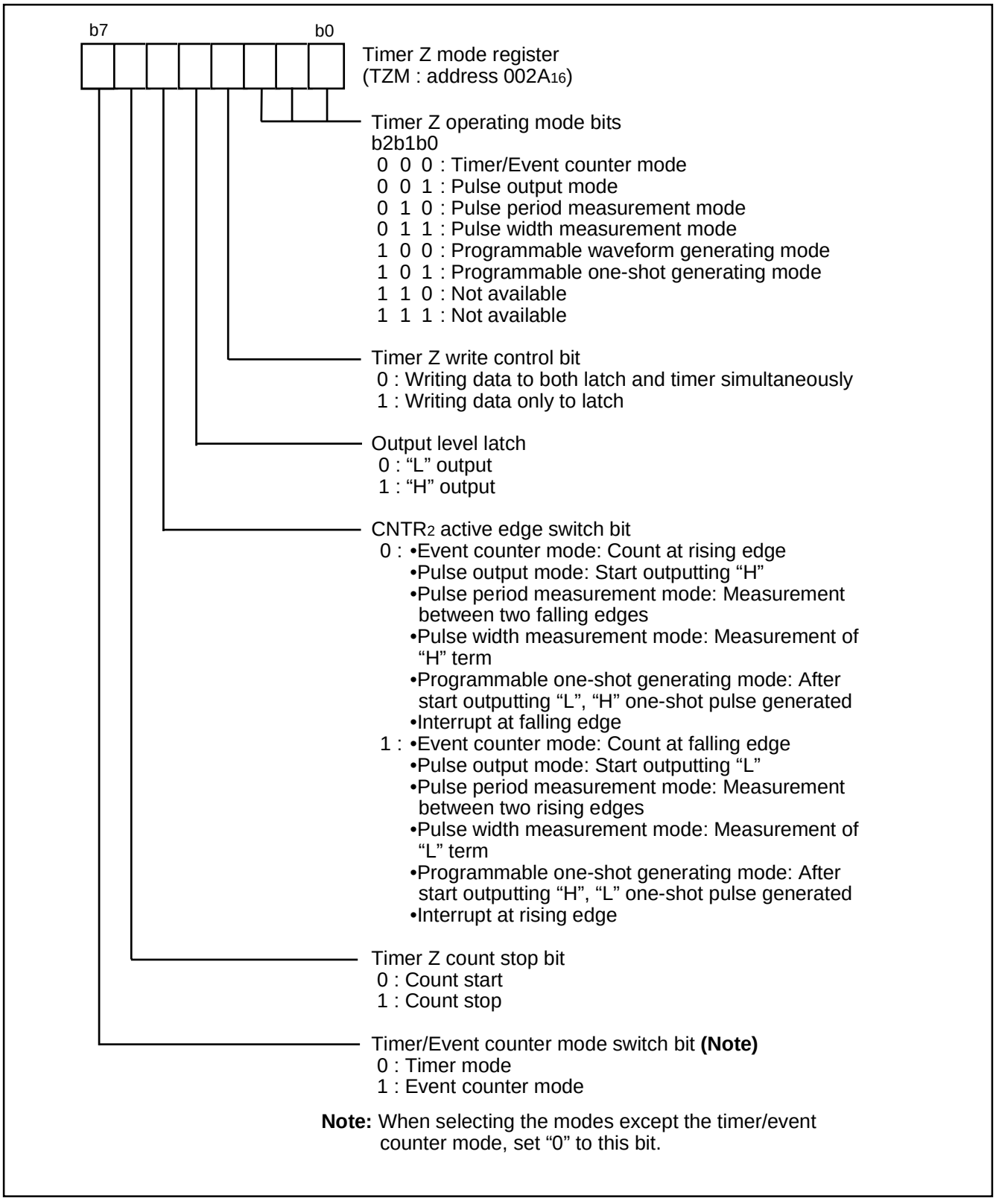
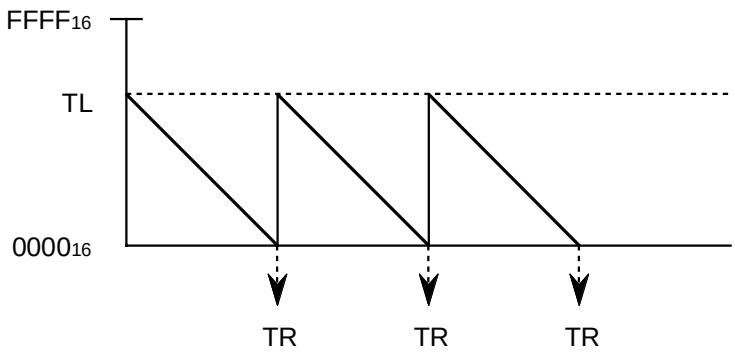
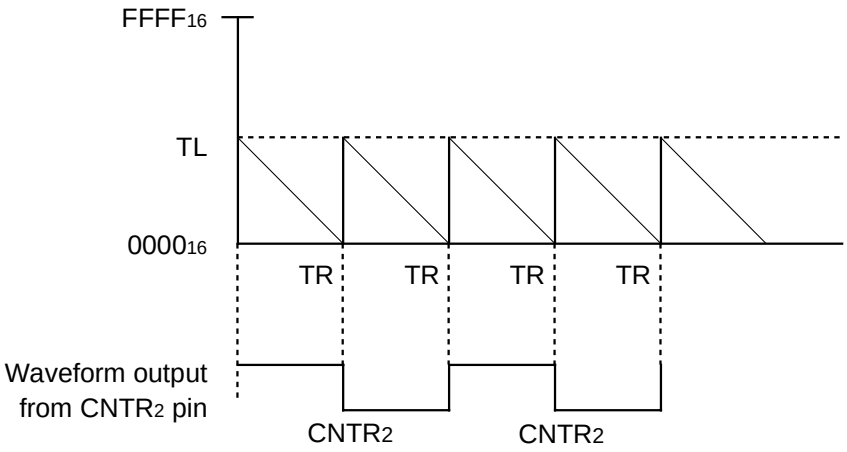


Fig. 33 Structure of timer Z mode register



TL : Value set to timer latch
TR : Timer interrupt request

Fig. 34 Timing chart of timer/event counter mode



TL : Value set to timer latch
TR : Timer interrupt request
CNTR2 : CNTR2 interrupt request
(CNTR2 active edge switch bit = “0”; Falling edge active)

Fig. 35 Timing chart of pulse output mode

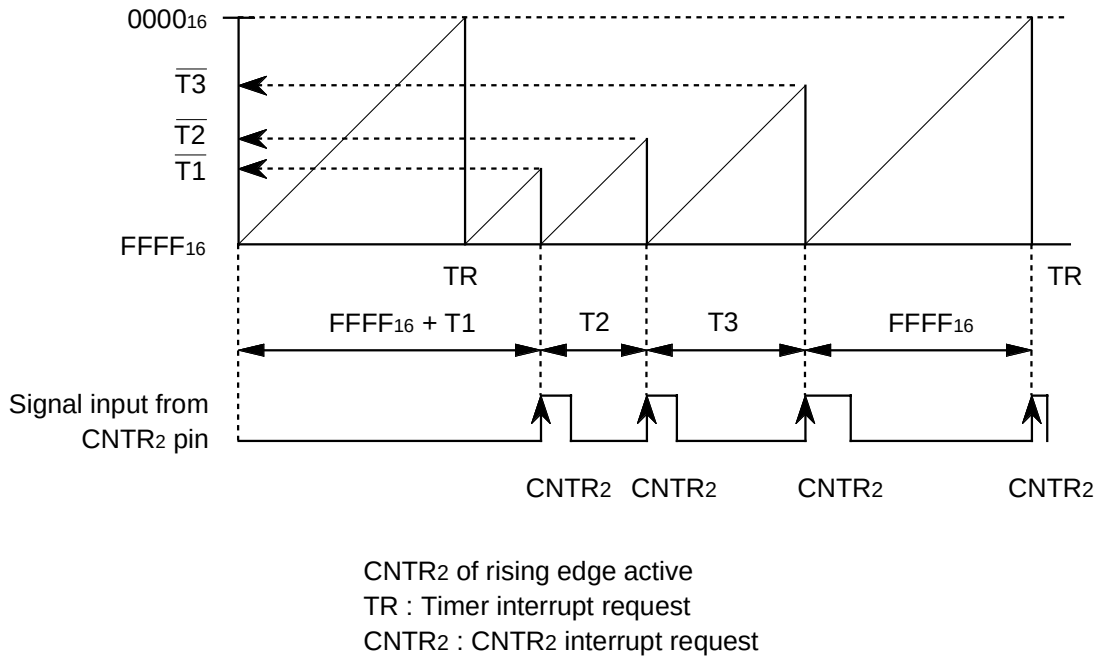


Fig. 36 Timing chart of pulse period measurement mode (Measuring term between two rising edges)

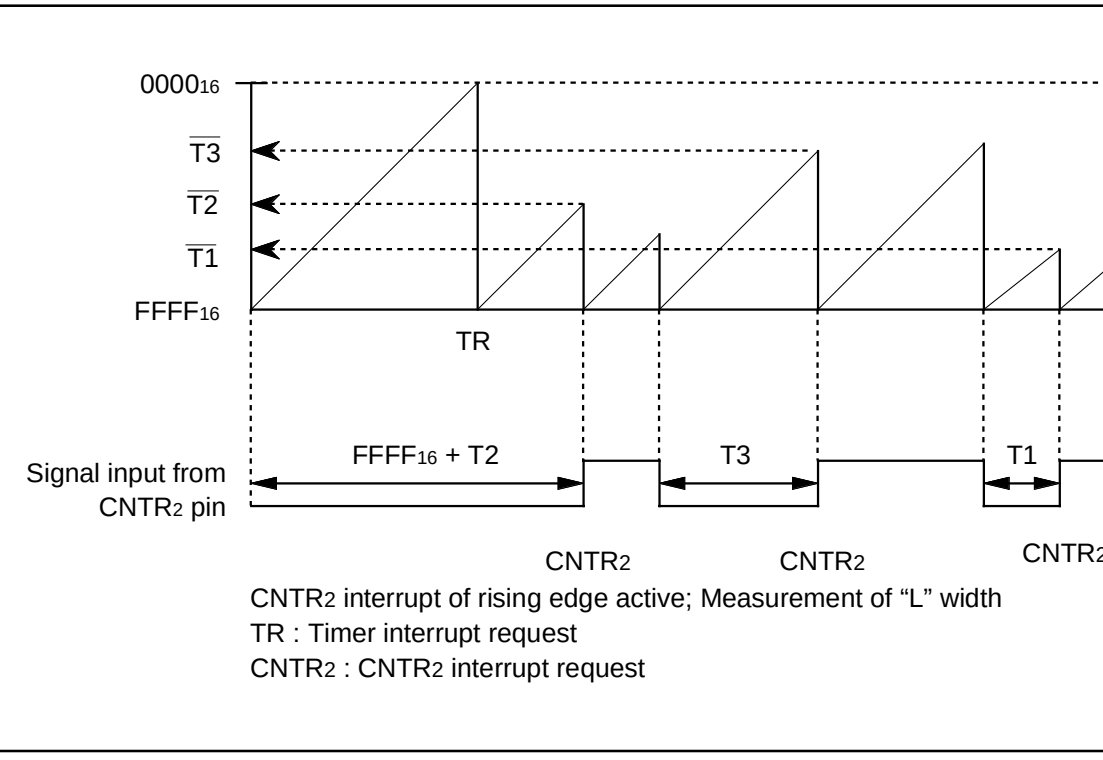
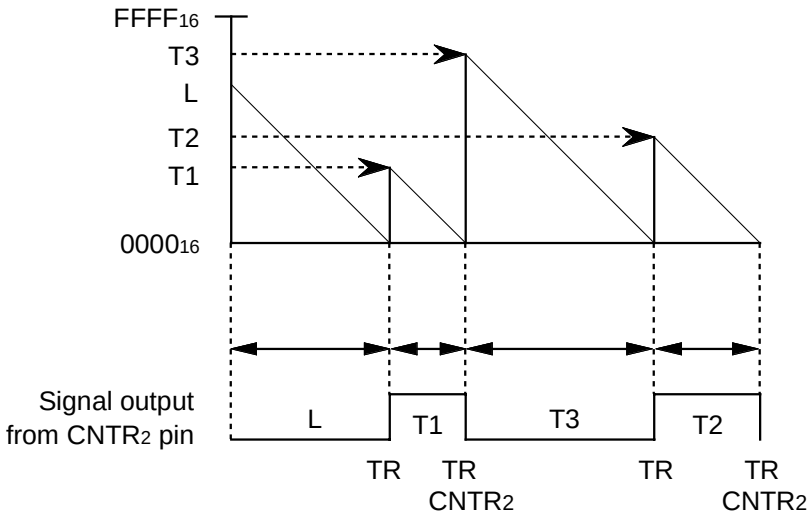
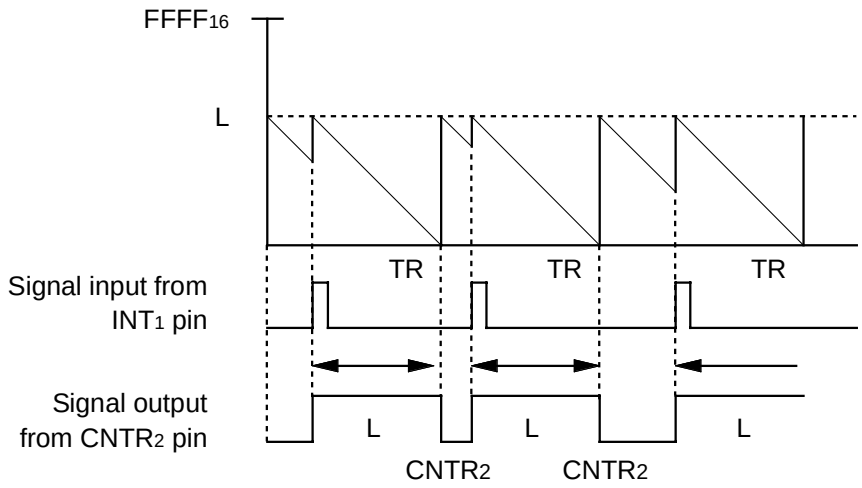


Fig. 37 Timing chart of pulse width measurement mode (Measuring “L” term)



L : Timer initial value
TR : Timer interrupt request
CNTR2 : CNTR2 interrupt request
(CNTR2 active edge switch bit = “0”; Falling edge active)

Fig. 38 Timing chart of programmable waveform generating mode



L : One-shot pulse width
TR : Timer interrupt request
CNTR2 : CNTR2 interrupt request
(CNTR2 active edge switch bit = “0”; Falling edge active)

Fig. 39 Timing chart of programmable one-shot generating mode (“H” one-shot pulse generating)

SERIAL I/O
Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6 of address 001A16) to “1”.

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer register.

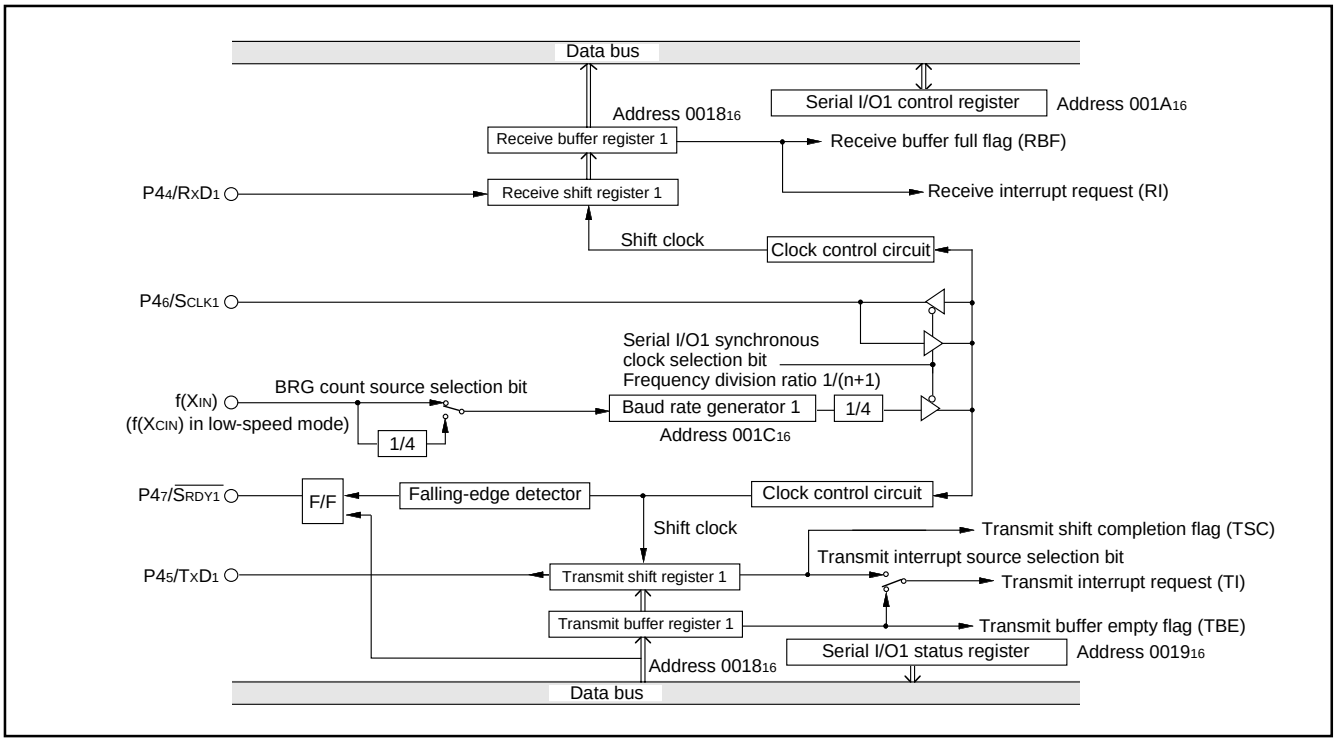
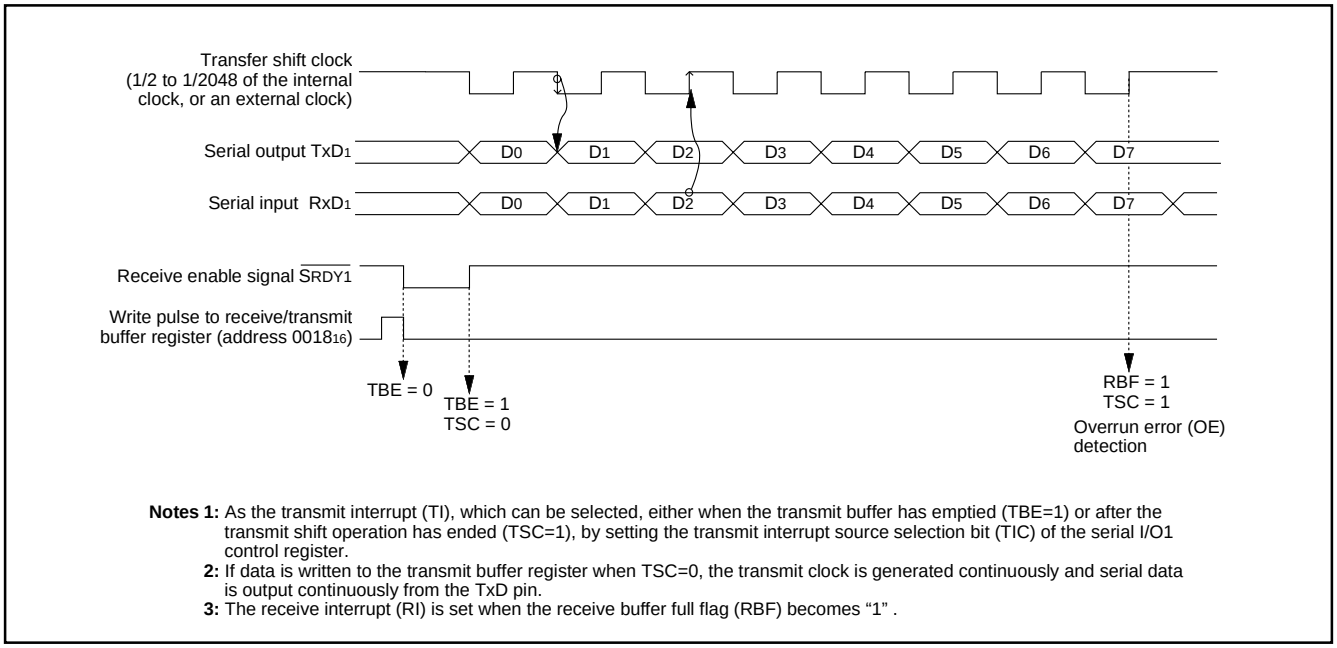


Fig. 40 Block diagram of clock synchronous serial I/O1



Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes “1” .

Fig. 41 Operation of clock synchronous serial I/O1

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit of the serial I/O1 control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in a memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

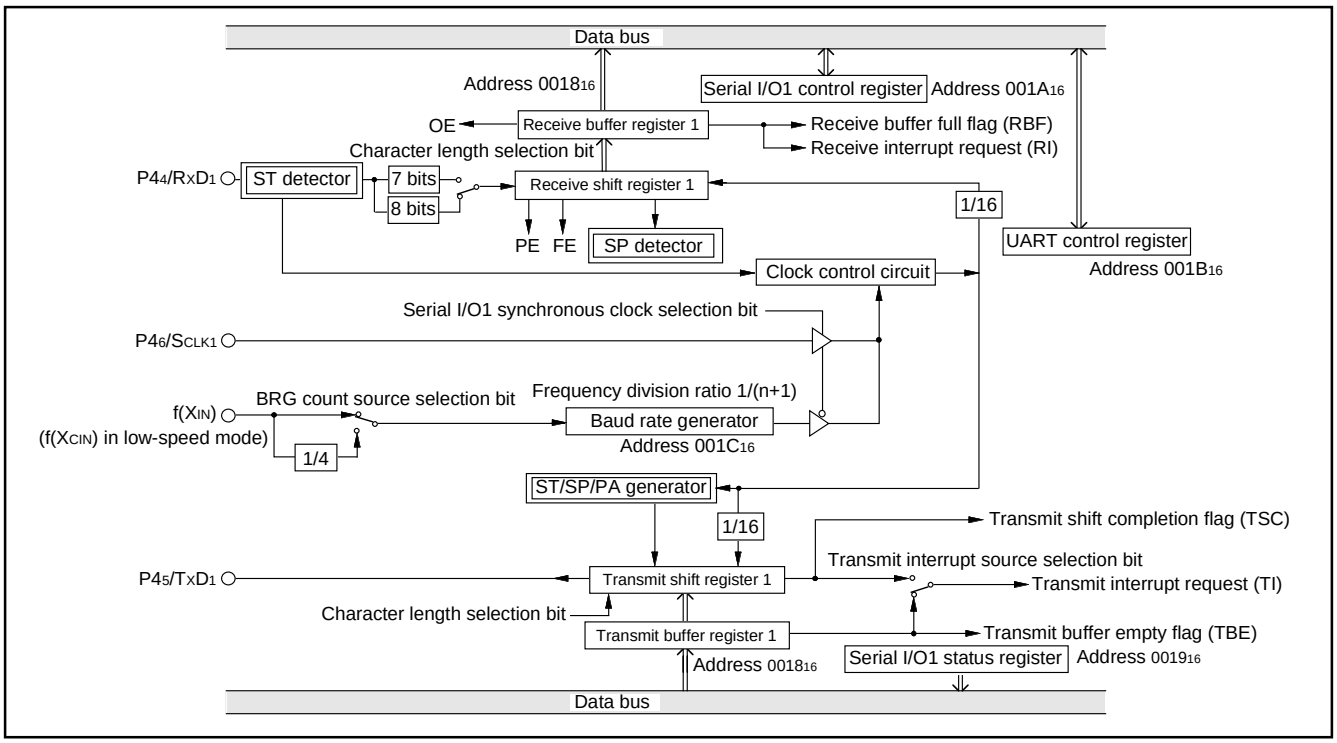
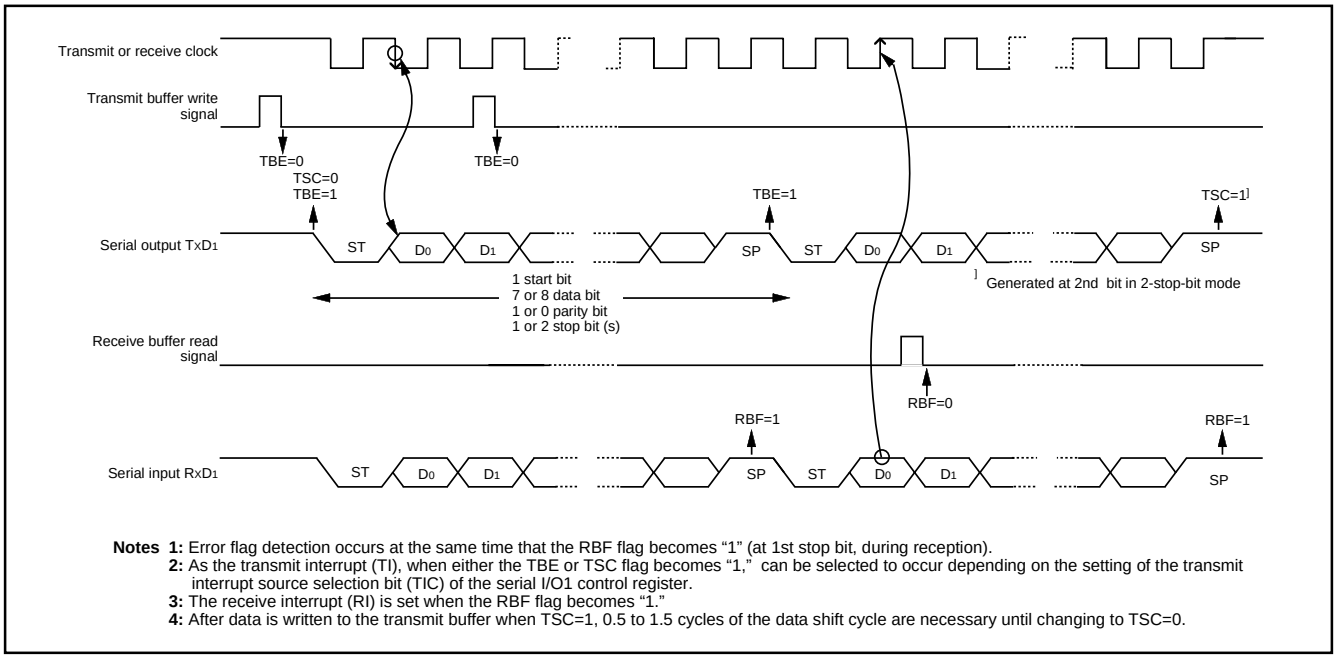


Fig. 42 Block diagram of UART serial I/O1



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1,” can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1.”
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle are necessary until changing to TSC=0.

Fig. 43 Operation of UART serial I/O1

[Serial I/O1 Control Register (SIO1CON)] 001A16

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART1 Control Register (UART1CON)] 001B16

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer, and one bit (bit 4) which is always valid and sets the output structure of the P45/TxD1 pin.

[Serial I/O1 Status Register (SIO1STS)] 001916

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing “0” to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O1 status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to “1”, the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Transmit Buffer Register 1/Receive Buffer Register 1 (TB1/RB1)] 001816

The transmit buffer register 1 and the receive buffer register 1 are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is “0”.

[Baud Rate Generator 1 (BRG1)] 001C16

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

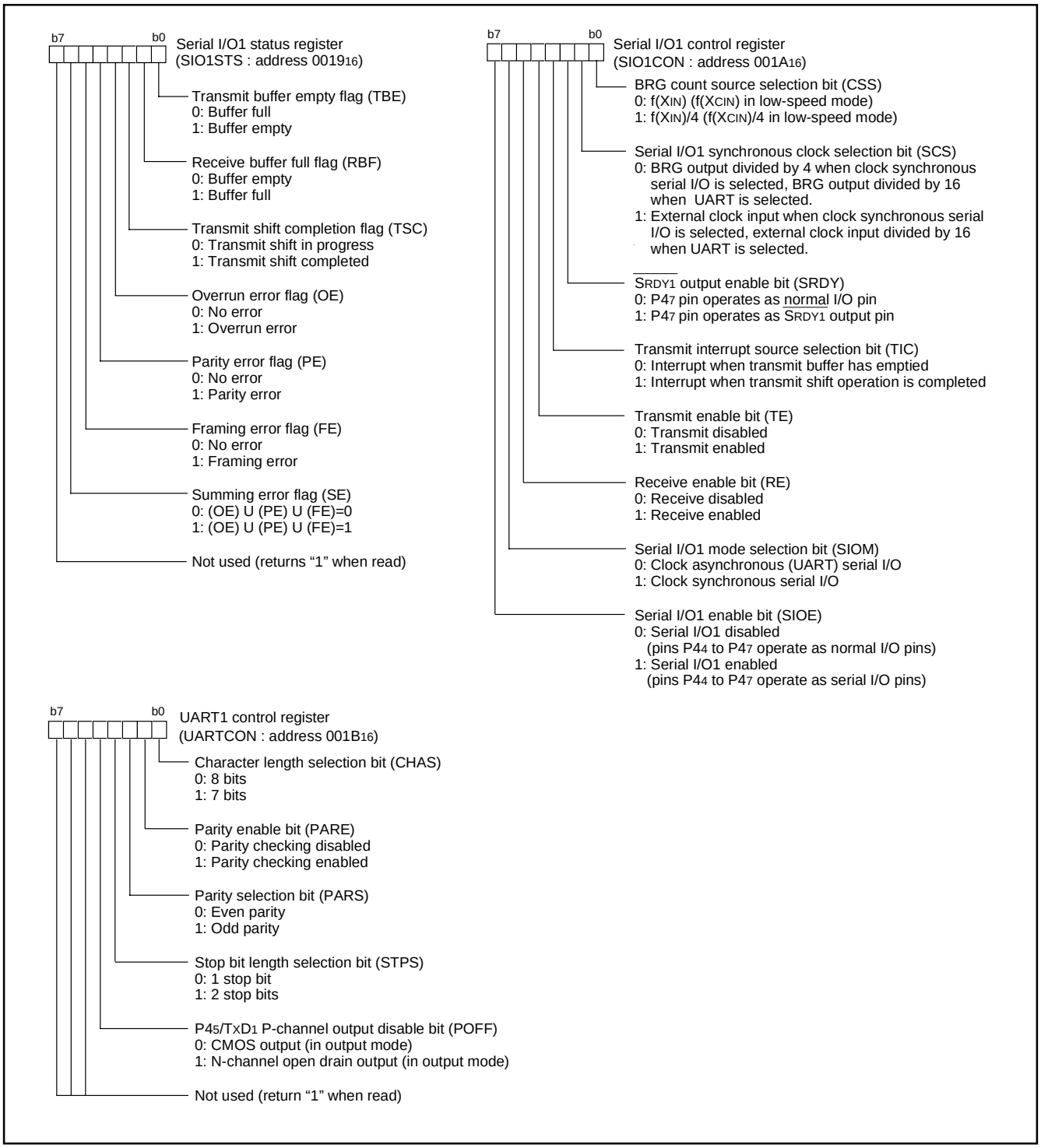


Fig. 44 Structure of serial I/O1 control registers

■ Notes concerning serial I/O1

1. Notes when selecting clock synchronous serial I/O

1.1 Stop of transmission operation

● **Note**

Clear the serial I/O1 enable bit and the transmit enable bit to “0” (serial I/O and transmit disabled).

● **Reason**

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to “0” (serial I/O disabled), the internal transmission is running (in this case, since pins TxD1, RxD1, SCLK1, and $\overline{\text{SRDY1}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to “1” at this time, the data during internally shifting is output to the TxD1 pin and an operation failure occurs.

1.2 Stop of receive operation

● **Note**

Clear the receive enable bit to “0” (receive disabled), or clear the serial I/O1 enable bit to “0” (serial I/O disabled).

1.3 Stop of transmit/receive operation

● **Note**

Clear both the transmit enable bit and receive enable bit to “0” (transmit and receive disabled).
(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

● **Reason**

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.
In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to “0” (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O1 enable bit to “0” (serial I/O disabled) (refer to **1.1**).

2. Notes when selecting clock asynchronous serial I/O

2.1 Stop of transmission operation

● **Note**

Clear the transmit enable bit to “0” (transmit disabled). The transmission operation does not stop by clearing the serial I/O1 enable bit to “0”.

● **Reason**

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to “0” (serial I/O disabled), the internal transmission is running (in this case, since pins TxD1, RxD1, SCLK1, and $\overline{\text{SRDY1}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to “1” at this time, the data during internally shifting is output to the TxD1 pin and an operation failure occurs.

2.2 Stop of receive operation

● **Note**

Clear the receive enable bit to “0” (receive disabled).

2.3 Stop of transmit/receive operation

● **Note 1 (only transmission operation is stopped)**

Clear the transmit enable bit to “0” (transmit disabled). The transmission operation does not stop by clearing the serial I/O1 enable bit to “0”.

● **Reason**

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to “0” (serial I/O disabled), the internal transmission is running (in this case, since pins TxD1, RxD1, SCLK1, and $\overline{\text{SRDY1}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to “1” at this time, the data during internally shifting is output to the TxD1 pin and an operation failure occurs.

● **Note 2 (only receive operation is stopped)**

Clear the receive enable bit to “0” (receive disabled).

3. $\overline{\text{SRDY1}}$ output of reception side

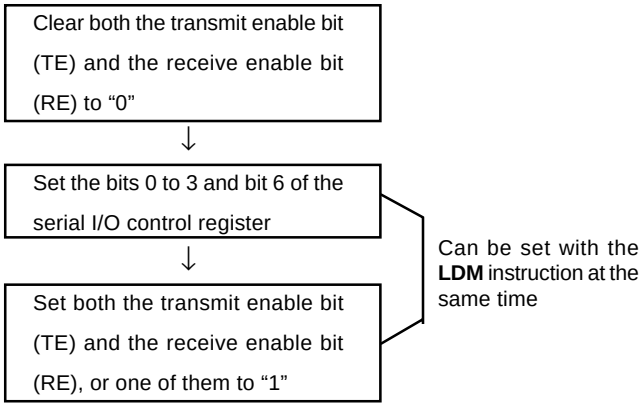
● **Note**

When signals are output from the $\overline{\text{SRDY1}}$ pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the $\overline{\text{SRDY1}}$ output enable bit, and the transmit enable bit to “1” (transmit enabled).

4. Setting serial I/O1 control register again

● **Note**

Set the serial I/O1 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to “0.”



5. Data transmission control with referring to transmit shift register completion flag

● **Note**

After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from “1” to “0” with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

6. Transmission control when external clock is selected

● **Note**

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to “1” at “H” of the SCLK1 input level. Also, write data to the transmit buffer register at “H” of the SCLK1 input level.

7. Transmit interrupt request when transmit enable bit is set

● **Note**

When using the transmit interrupt, take the following sequence.

① Set the serial I/O1 transmit interrupt enable bit to “0” (disabled).
② Set the transmit enable bit to “1”.
③ Set the serial I/O1 transmit interrupt request bit to “0” after 1 or more instruction has executed.
④ Set the serial I/O1 transmit interrupt enable bit to “1” (enabled).

● **Reason**

When the transmit enable bit is set to “1”, the transmit buffer empty flag and the transmit shift register shift completion flag are also set to “1”. Therefore, regardless of selecting which timing for the generating of transmit interrupts, the interrupt request is generated and the transmit interrupt request bit is set at this point.

Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O2, the transmitter and the receiver must use the same clock. If the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

[Serial I/O2 Control Register (SIO2CON)] 001D16

The serial I/O2 control register contains eight bits which control various serial I/O2 functions.

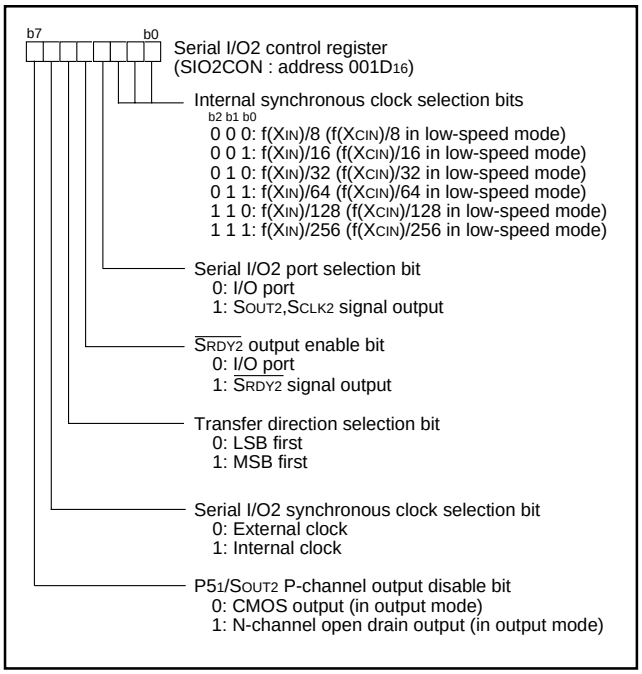


Fig. 45 Structure of serial I/O2 control register

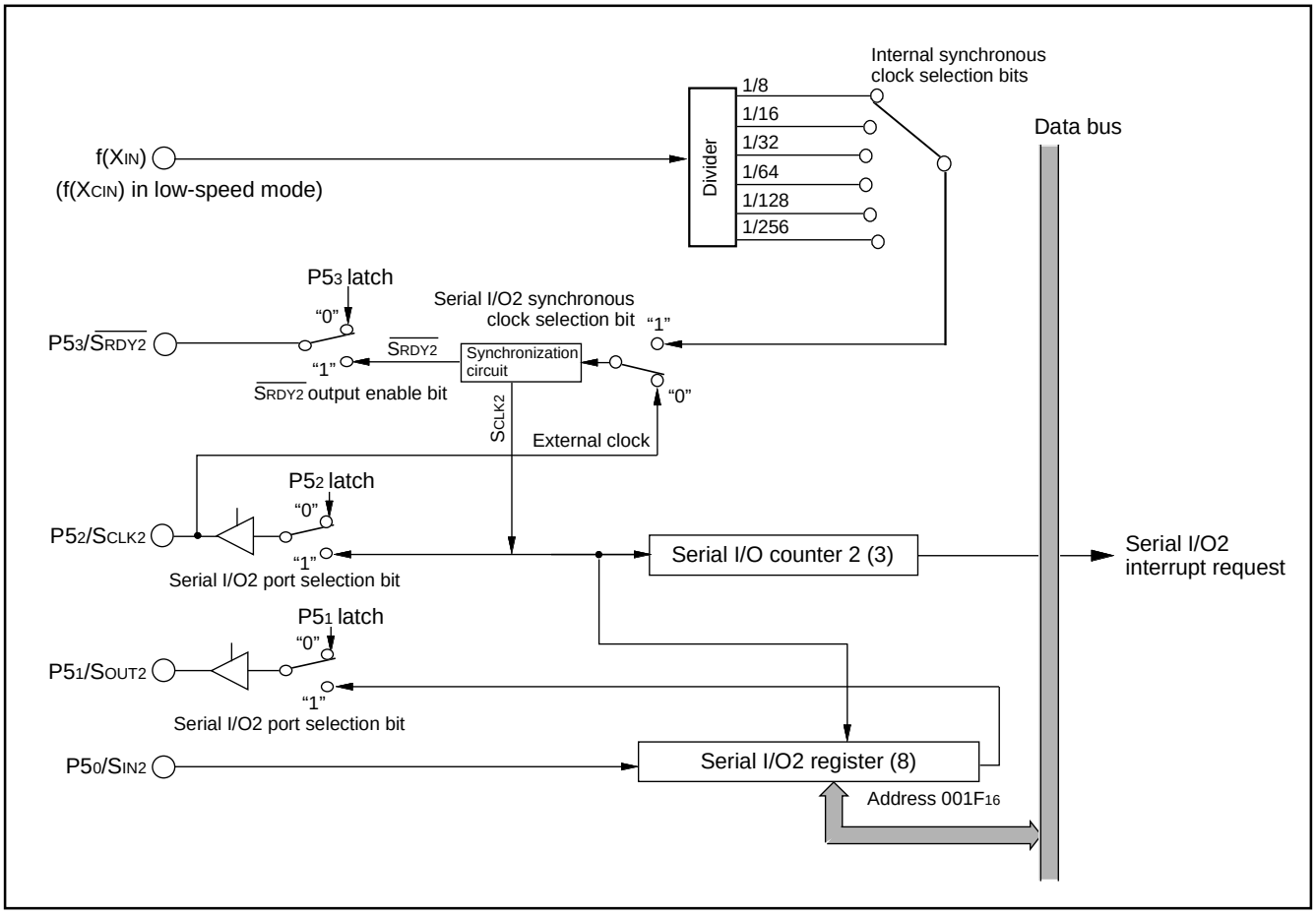
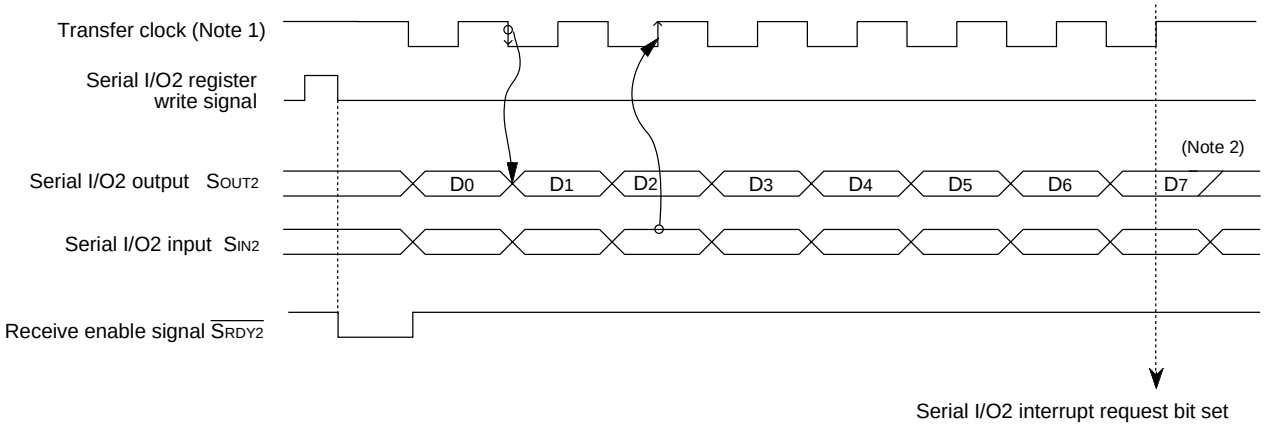


Fig. 46 Block diagram of serial I/O2



Notes 1: When the internal clock is selected as the transfer clock, the divide ratio of f(X_{IN}), or f(X_{CIN}) in low-speed mode, can be selected by setting bits 0 to 2 of the serial I/O2 control register.
2: When the internal clock is selected as the transfer clock, the S_{OUT2} pin goes to high impedance after transfer completion.

Fig. 47 Timing of serial I/O2

Serial I/O3

Serial I/O3 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O3 mode can be selected by setting the serial I/O3 mode selection bit of the serial I/O3 control register (bit 6 of address 0032_{16}) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer register.

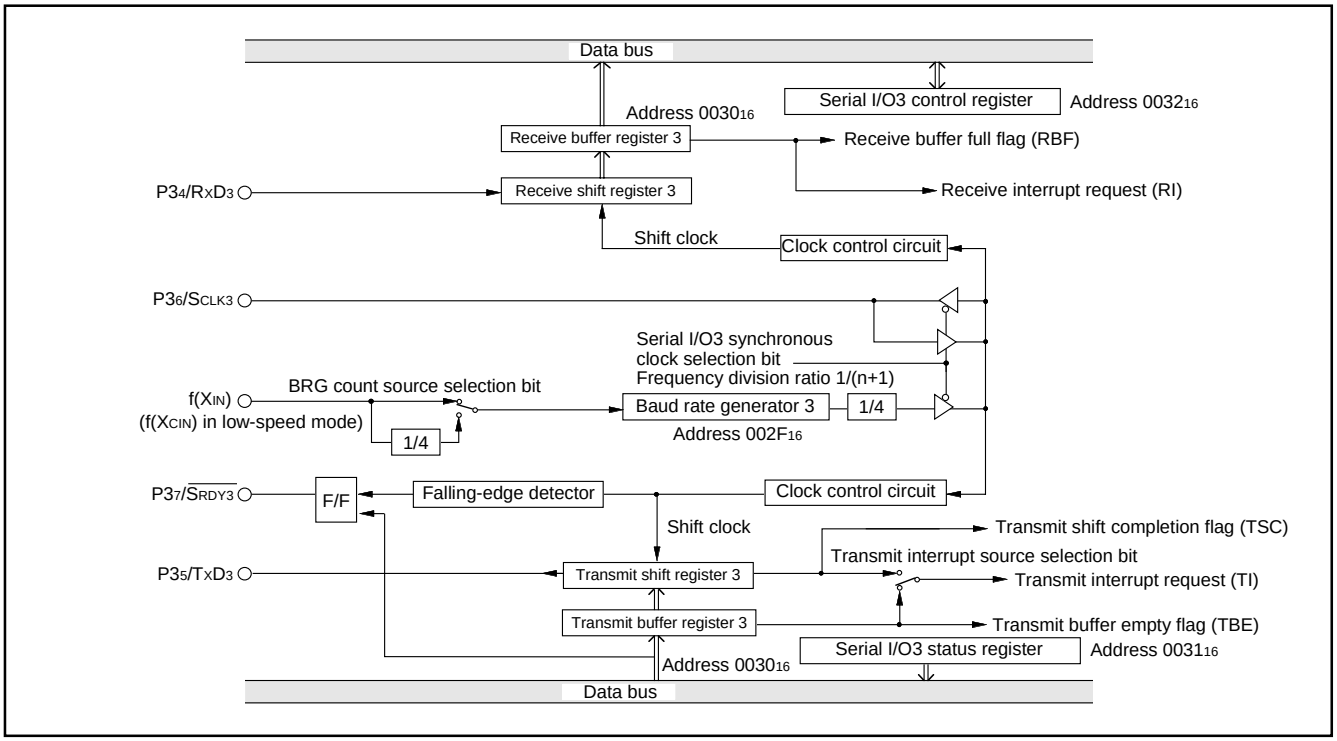
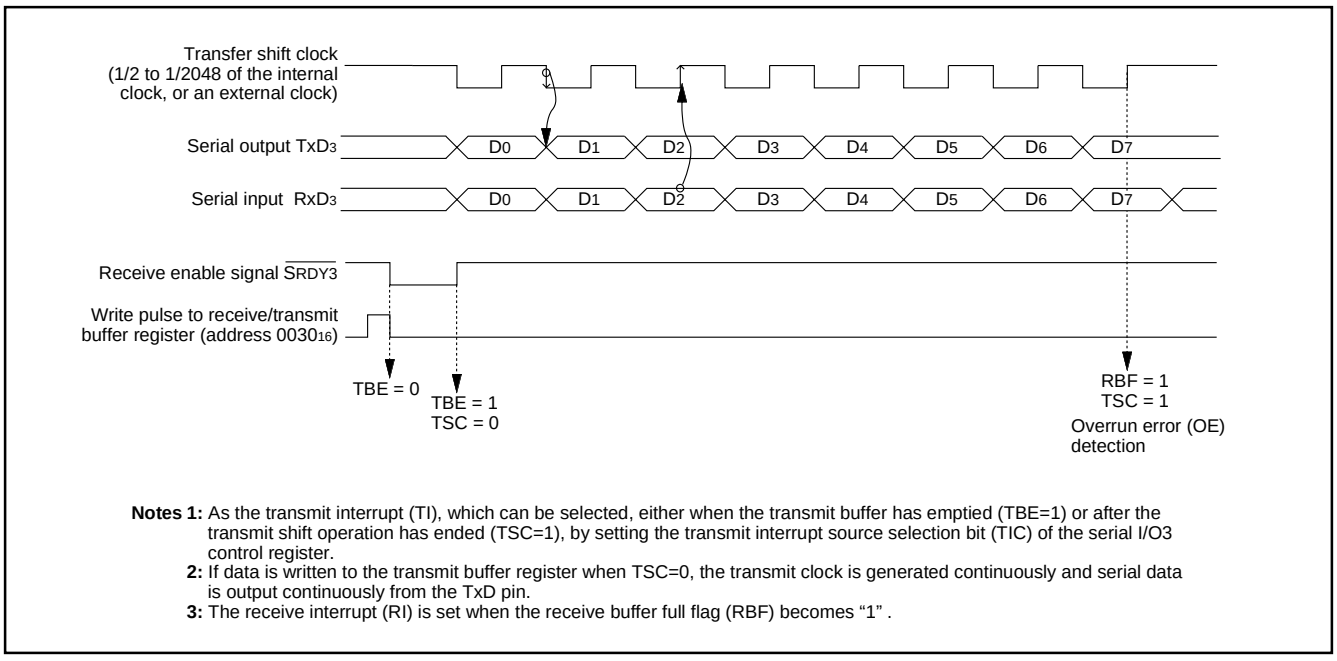


Fig. 48 Block diagram of clock synchronous serial I/O3



Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O3 control register.

2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.

3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig. 49 Operation of clock synchronous serial I/O3

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O3 mode selection bit of the serial I/O3 control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in a memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

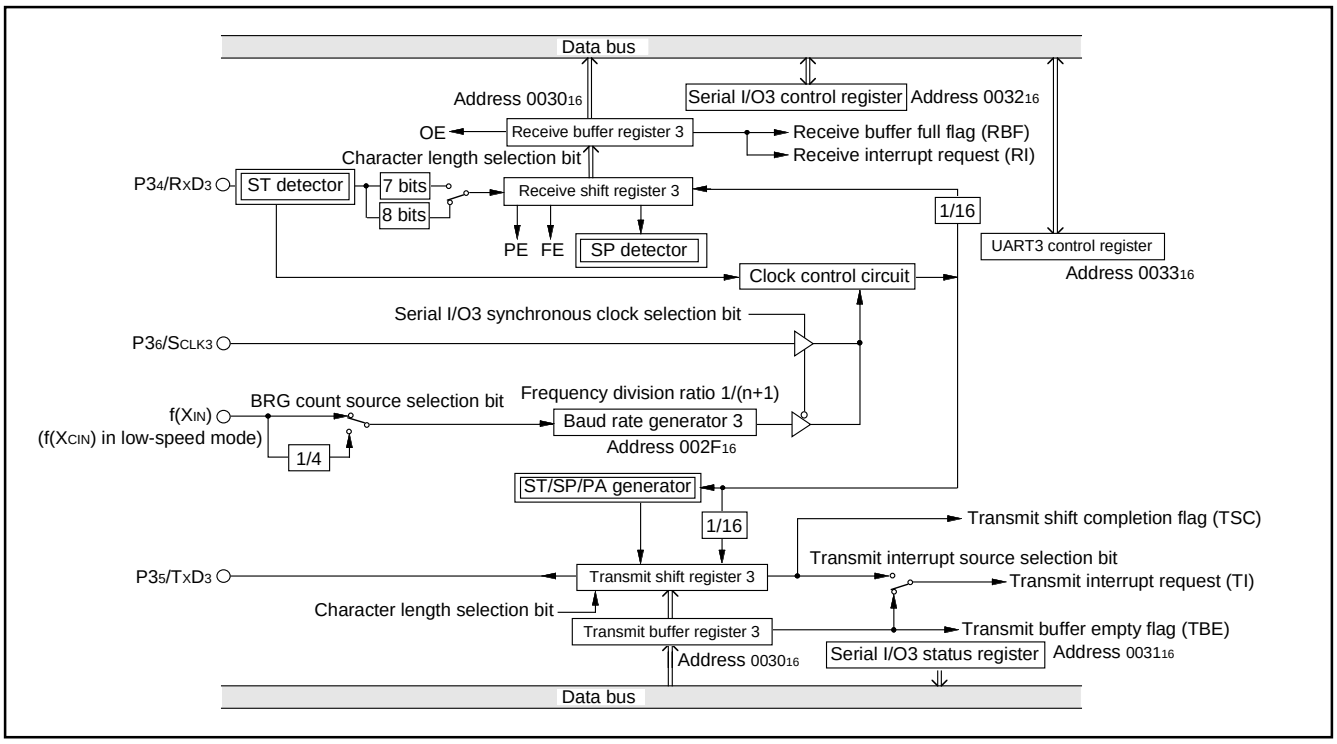
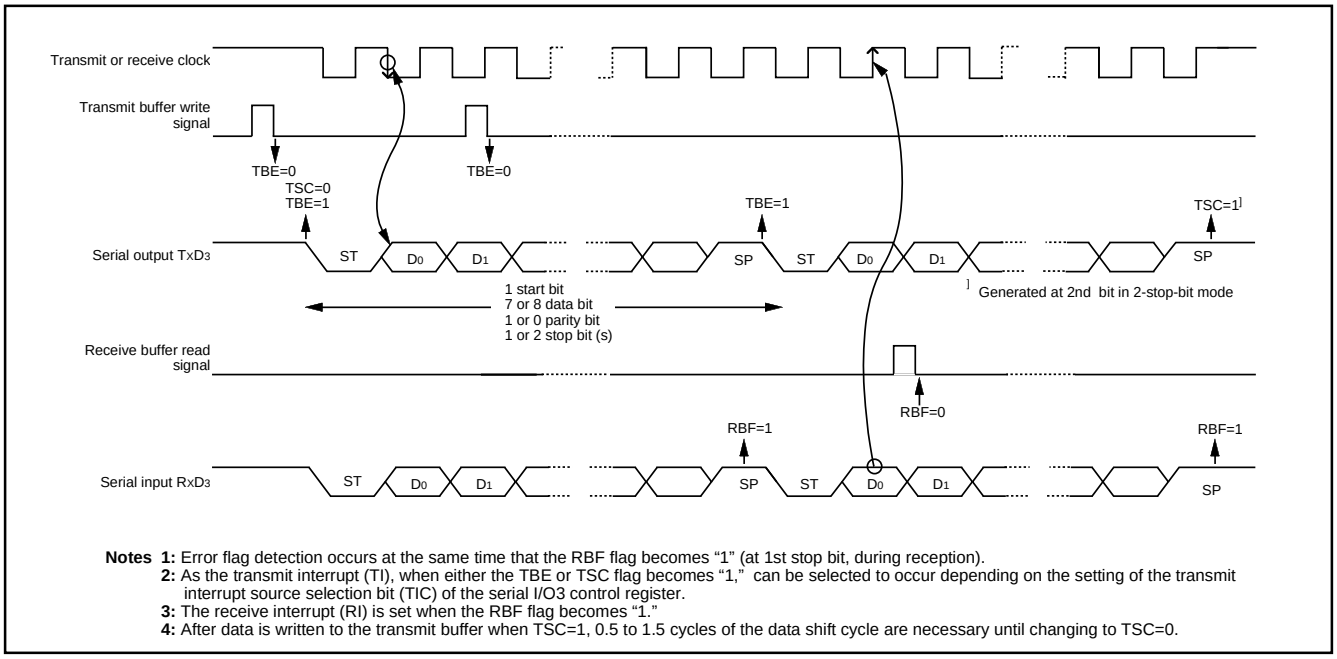


Fig. 50 Block diagram of UART serial I/O3



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1,” can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O3 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1.”
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle are necessary until changing to TSC=0.

Fig. 51 Operation of UART serial I/O3

[Serial I/O3 Control Register (SIO3CON)] 0032$_{16}$

The serial I/O3 control register consists of eight control bits for the serial I/O3 function.

[UART3 Control Register (UART3CON)] 0033$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer, and one bit (bit 4) which is always valid and sets the output structure of the P3$_5$/TxD$_3$ pin.

[Serial I/O3 Status Register (SIO3STS)] 0031$_{16}$

The read-only serial I/O3 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O3 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O3 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing “0” to the serial I/O3 enable bit SIOE (bit 7 of the serial I/O3 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O3 status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O3 control register has been set to “1”, the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Transmit Buffer Register 3/Receive Buffer Register 3 (TB3/RB3)] 0030$_{16}$

The transmit buffer register 3 and the receive buffer register 3 are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is “0”.

[Baud Rate Generator 3 (BRG3)] 002F$_{16}$

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

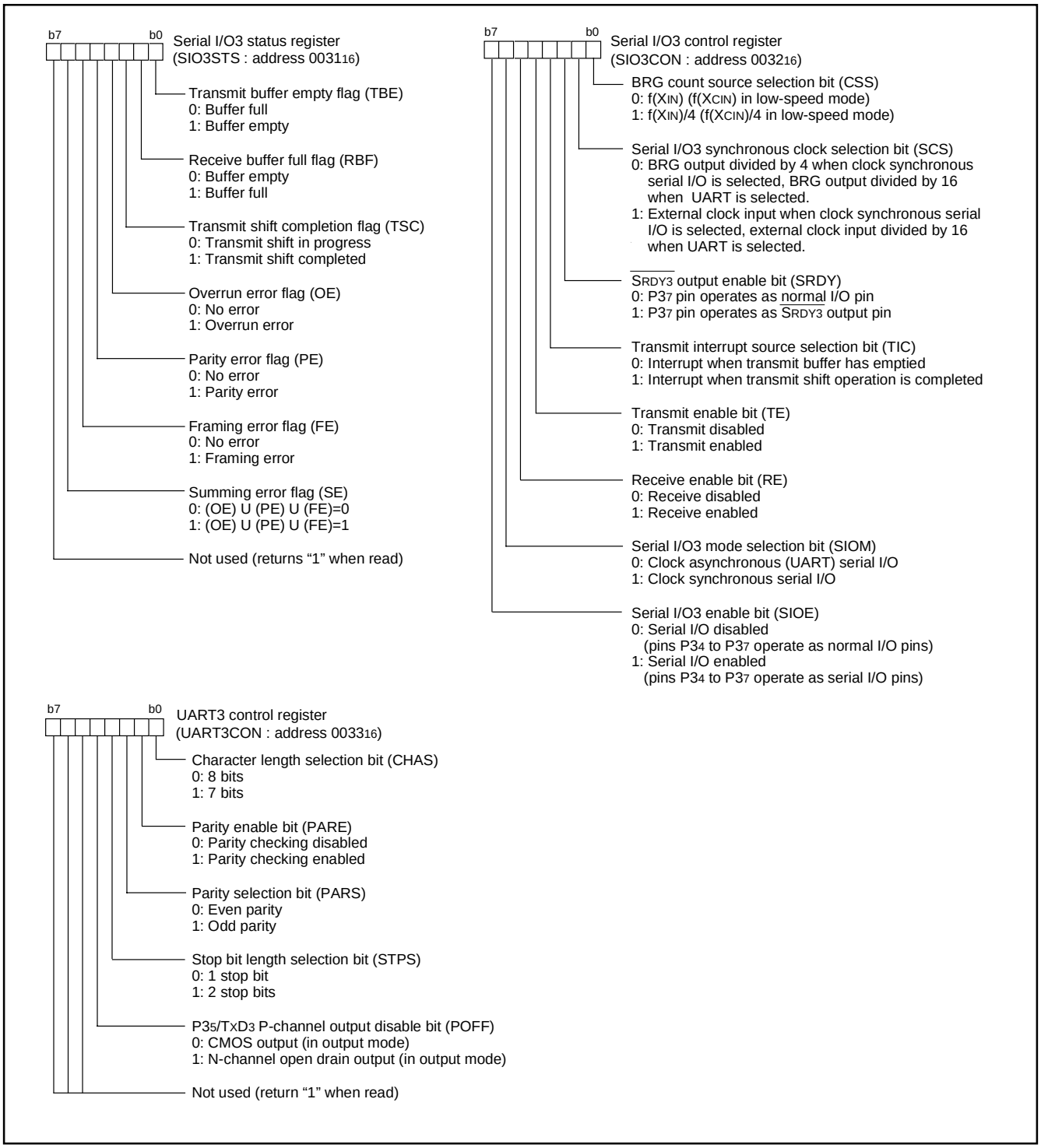


Fig. 52 Structure of serial I/O3 control registers

■ Notes concerning serial I/O3

1. Notes when selecting clock synchronous serial I/O

1.1 Stop of transmission operation

● **Note**

Clear the serial I/O3 enable bit and the transmit enable bit to “0” (serial I/O and transmit disabled).

● **Reason**

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to “0” (serial I/O disabled), the internal transmission is running (in this case, since pins TxD3, RxD3, SCLK3, and $\overline{\text{SRDY3}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O enable bit is set to “1” at this time, the data during internally shifting is output to the TxD3 pin and an operation failure occurs.

1.2 Stop of receive operation

● **Note**

Clear the receive enable bit to “0” (receive disabled), or clear the serial I/O3 enable bit to “0” (serial I/O disabled).

1.3 Stop of transmit/receive operation

● **Note**

Clear both the transmit enable bit and receive enable bit to “0” (transmit and receive disabled).
(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

● **Reason**

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.
In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to “0” (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O3 enable bit to “0” (serial I/O disabled) (refer to **1.1**).

2. Notes when selecting clock asynchronous serial I/O

2.1 Stop of transmission operation

● **Note**

Clear the transmit enable bit to “0” (transmit disabled). The transmission operation does not stop by clearing the serial I/O3 enable bit to “0”.

● **Reason**

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to “0” (serial I/O disabled), the internal transmission is running (in this case, since pins TxD3, RxD3, SCLK3, and $\overline{\text{SRDY3}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O3 enable bit is set to “1” at this time, the data during internally shifting is output to the TxD3 pin and an operation failure occurs.

2.2 Stop of receive operation

● **Note**

Clear the receive enable bit to “0” (receive disabled).

2.3 Stop of transmit/receive operation

● **Note 1 (only transmission operation is stopped)**

Clear the transmit enable bit to “0” (transmit disabled). The transmission operation does not stop by clearing the serial I/O3 enable bit to “0”.

● **Reason**

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to “0” (serial I/O disabled), the internal transmission is running (in this case, since pins TxD3, RxD3, SCLK3, and $\overline{\text{SRDY3}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O3 enable bit is set to “1” at this time, the data during internally shifting is output to the TxD3 pin and an operation failure occurs.

● **Note 2 (only receive operation is stopped)**

Clear the receive enable bit to “0” (receive disabled).

3. $\overline{\text{SRDY3}}$ output of reception side

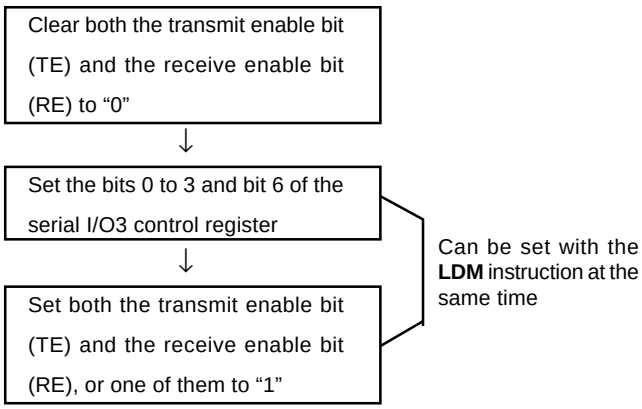
● **Note**

When signals are output from the $\overline{\text{SRDY3}}$ pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the $\overline{\text{SRDY3}}$ output enable bit, and the transmit enable bit to “1” (transmit enabled).

4. Setting serial I/O3 control register again

● **Note**

Set the serial I/O3 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to “0.”



5. Data transmission control with referring to transmit shift register completion flag

● **Note**

After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from “1” to “0” with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

6. Transmission control when external clock is selected

● **Note**

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to “1” at “H” of the SCLK3 input level. Also, write data to the transmit buffer register at “H” of the SCLK input level.

7. Transmit interrupt request when transmit enable bit is set

● **Note**

When using the transmit interrupt, take the following sequence.

① Set the serial I/O3 transmit interrupt enable bit to “0” (disabled).
② Set the transmit enable bit to “1”.
③ Set the serial I/O3 transmit interrupt request bit to “0” after 1 or more instruction has executed.
④ Set the serial I/O3 transmit interrupt enable bit to “1” (enabled).

● **Reason**

When the transmit enable bit is set to “1”, the transmit buffer empty flag and the transmit shift register shift completion flag are also set to “1”. Therefore, regardless of selecting which timing for the generating of transmit interrupts, the interrupt request is generated and the transmit interrupt request bit is set at this point.

PULSE WIDTH MODULATION (PWM)

The 3803/3804 group has PWM functions with an 8-bit resolution, based on a signal that is the clock input XIN or that clock input divided by 2 or the clock input XCIN or that clock input divided by 2 in low-speed mode.

Data Setting

The PWM output pin also functions as port P56. Set the PWM period by the PWM prescaler, and set the "H" term of output pulse by the PWM register.

If the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255) :

PWM period = 255 × (n+1) / f(XIN)

= 31.875 × (n+1) µs (when f(XIN) = 8 MHz)

Output pulse "H" term = PWM period × m / 255

= 0.125 × (n+1) × m µs

(when f(XIN) = 8 MHz)

PWM Operation

When bit 0 (PWM enable bit) of the PWM control register is set to "1", operation starts by initializing the PWM output circuit, and pulses are output starting at an "H".

If the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

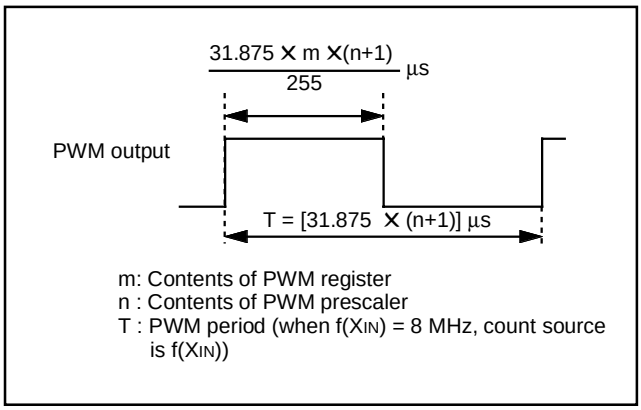


Fig. 53 Timing of PWM period

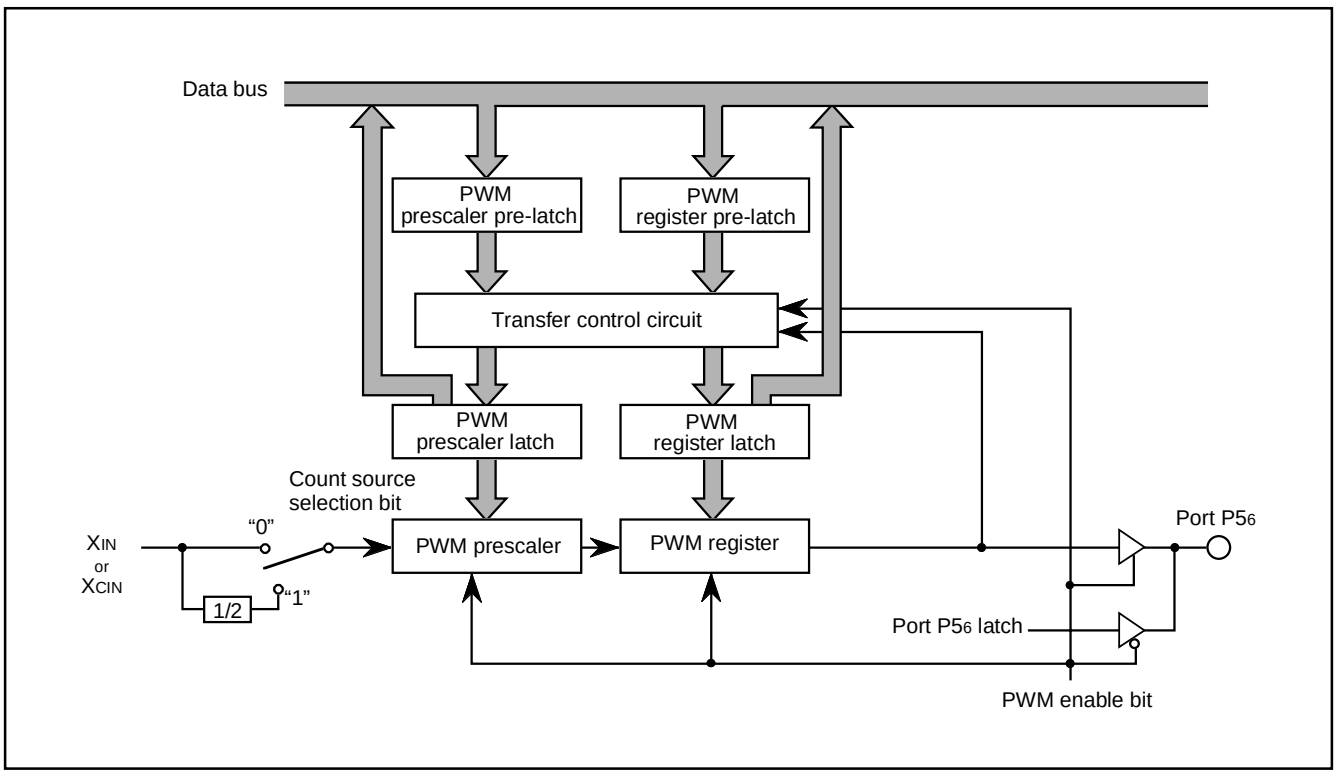


Fig. 54 Block diagram of PWM function

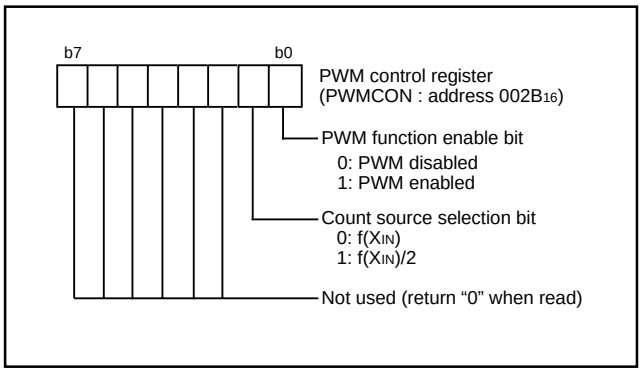


Fig. 55 Structure of PWM control register

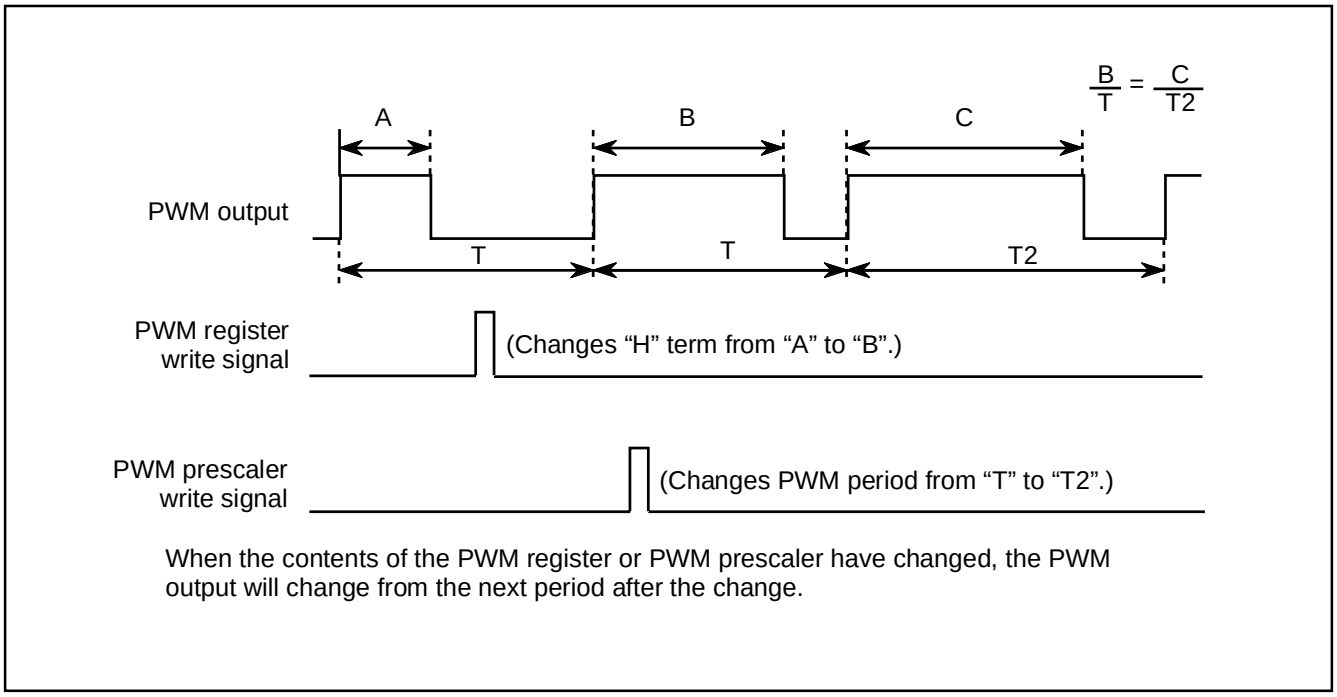


Fig. 56 PWM output timing when PWM register or PWM prescaler is changed

A-D CONVERTER
[A-D Conversion Register 1, 2 (AD1, AD2)] 003516, 003816

The A-D conversion register is a read-only register that stores the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

Bit 7 of the A-D conversion register 2 is the conversion mode selection bit. When this bit is set to "0," the A-D converter becomes the 10-bit A-D mode. When this bit is set to "1," that becomes the 8-bit A-D mode. The conversion result of the 8-bit A-D mode is stored in the A-D conversion register 1. As for 10-bit A-D mode, not only 10-bit reading but also only high-order 8-bit reading of conversion result can be performed by selecting the reading procedure of the A-D conversion registers 1, 2 after A-D conversion is completed (in Figure 58).

As for 10-bit A-D mode, the 8-bit reading inclined to MSB is performed when reading the A-D converter register 1 after A-D conversion is started; and when the A-D converter register 1 is read after reading the A-D converter register 2, the 8-bit reading inclined to LSB is performed.

[AD/DA Control Register (ADCON)] 003416

The AD/DA control register controls the A-D conversion process. Bits 0 to 2 and bit 4 select a specific analog input pin. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between V_{REF} and AV_{SS} into 1024, and that outputs the comparison voltage in the 10-bit A-D mode (256 division in 8-bit A-D mode).

The A-D converter successively compares the comparison voltage V_{ref} in each mode, dividing the V_{REF} voltage (see below), with the input voltage.

- 10-bit A-D mode (10-bit reading)

$$V_{ref} = \frac{V_{REF}}{1024} \times n \quad (n = 0–1023)$$

- 10-bit A-D mode (8-bit reading)

$$V_{ref} = \frac{V_{REF}}{256} \times n \quad (n = 0–255)$$

- 8-bit A-D mode

$$V_{ref} = \frac{V_{REF}}{256} \times (n–0.5) \quad (n = 1–255)$$
$$= 0 \qquad\qquad (n = 0)$$

Channel Selector

The channel selector selects one of ports $P6_7/AN_7$ to $P6_0/AN_0$ or $P0_7/AN_{15}$ to $P0_0/AN_8$, and inputs the voltage to the comparator.

Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage, and then stores the result in the A-D conversion registers 1, 2. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set $f(X_{IN})$ to 500 kHz or more during an A-D conversion.

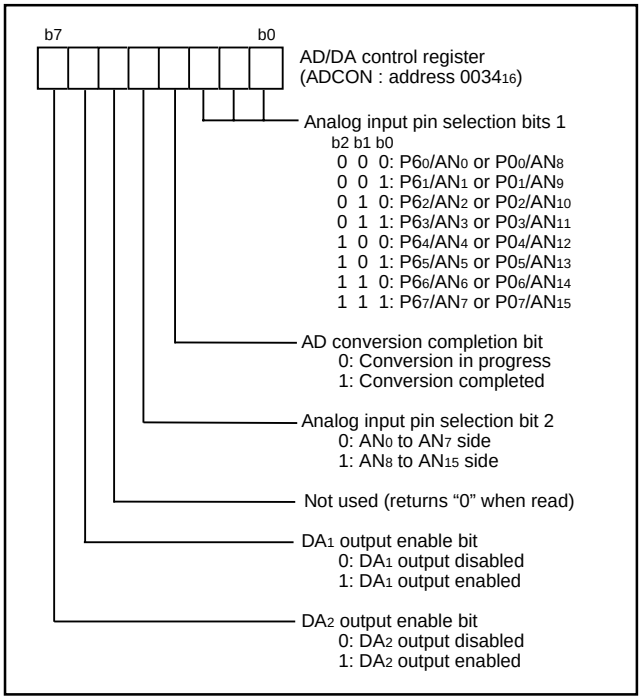


Fig. 57 Structure of AD/DA control register

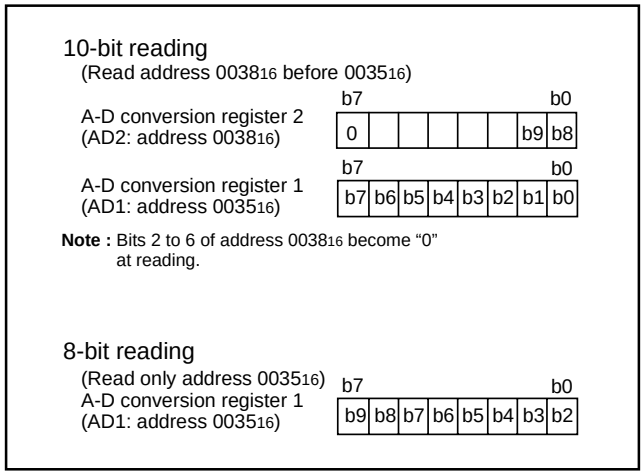


Fig. 58 Structure of 10-bit A-D mode reading

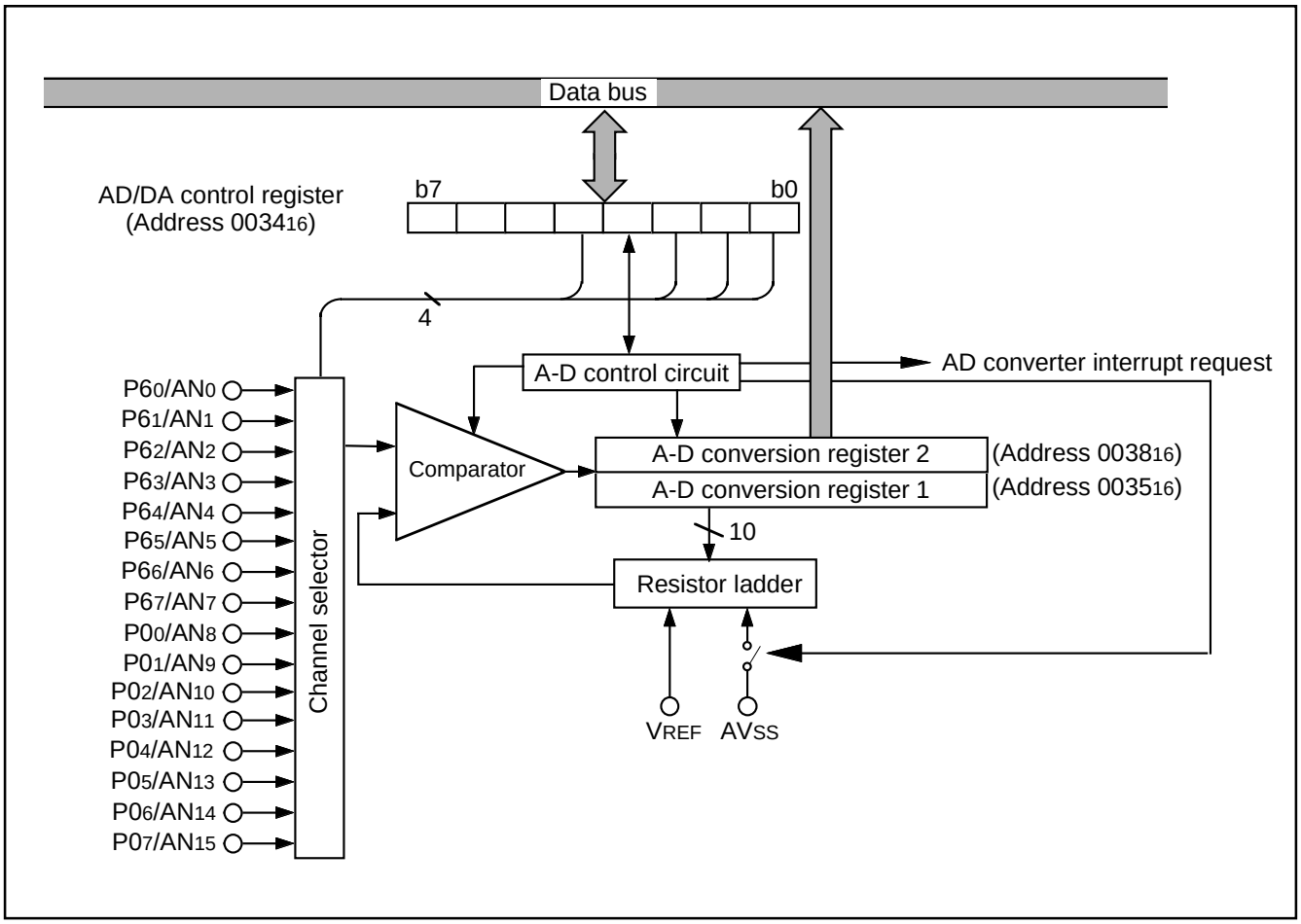


Fig. 59 Block diagram of A-D converter

D-A CONVERTER

The 3803/3804 group has two internal D-A converters (DA1 and DA2) with 8-bit resolution.

The D-A conversion is performed by setting the value in each D-A conversion register. The result of D-A conversion is output from the DA_1 or DA_2 pin by setting the DA output enable bit to "1".

When using the D-A converter, the corresponding port direction register bit ($P3_0/DA_1$ or $P3_1/DA_2$) must be set to "0" (input status).

The output analog voltage V is determined by the value n (decimal notation) in the D-A conversion register as follows:

$V = V_{REF} \times n/256$ (n = 0 to 255)

Where V_{REF} is the reference voltage.

At reset, the D-A conversion registers are cleared to "00_{16}", and the DA output enable bits are cleared to "0", and the $P3_0/DA_1$ and $P3_1/DA_2$ pins become high impedance.

The DA output does not have buffers. Accordingly, connect an external buffer when driving a low-impedance load.

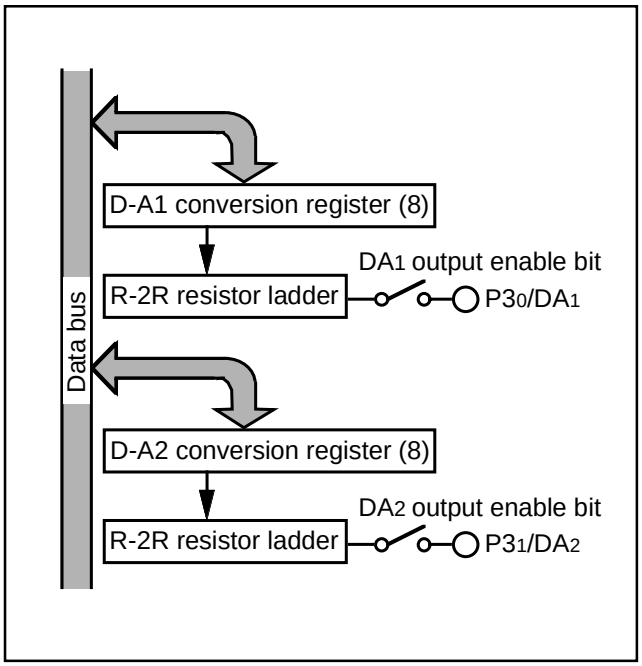


Fig. 60 Block diagram of D-A converter

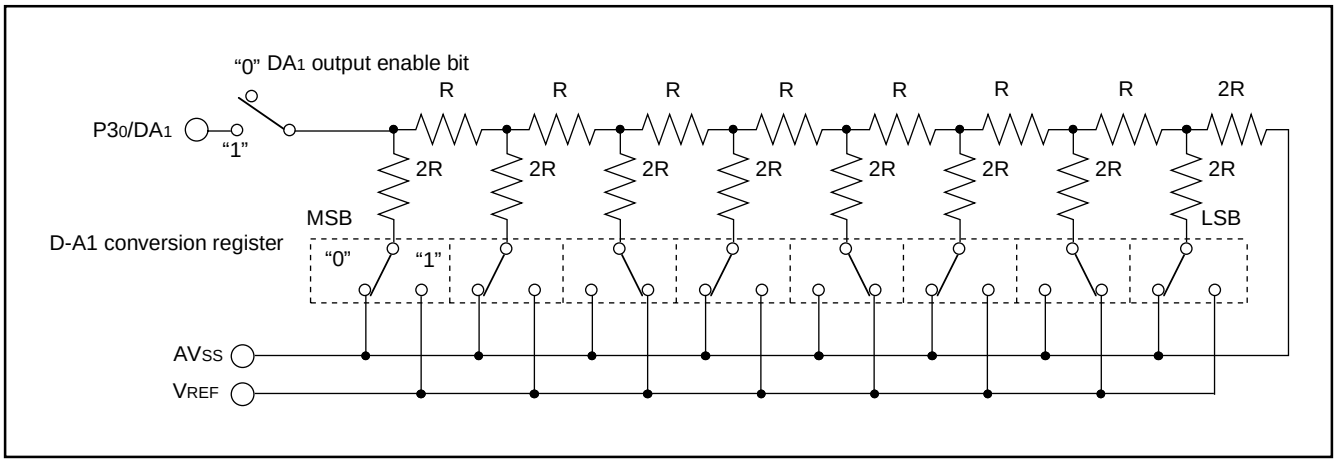


Fig. 61 Equivalent connection circuit of D-A converter (DA1)

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

Watchdog Timer Initial Value

Watchdog timer L is set to "FF16" and watchdog timer H is set to "FF16" by writing to the watchdog timer control register (address 001E16) or at a reset. Any write instruction that causes a write signal can be used, such as the STA, LDM, CLB, etc. Data can only be written to bits 6 and 7 of the watchdog timer control register. Regardless of the value written to bits 0 to 5, the above-mentioned value will be set to each timer.

Watchdog Timer Operations

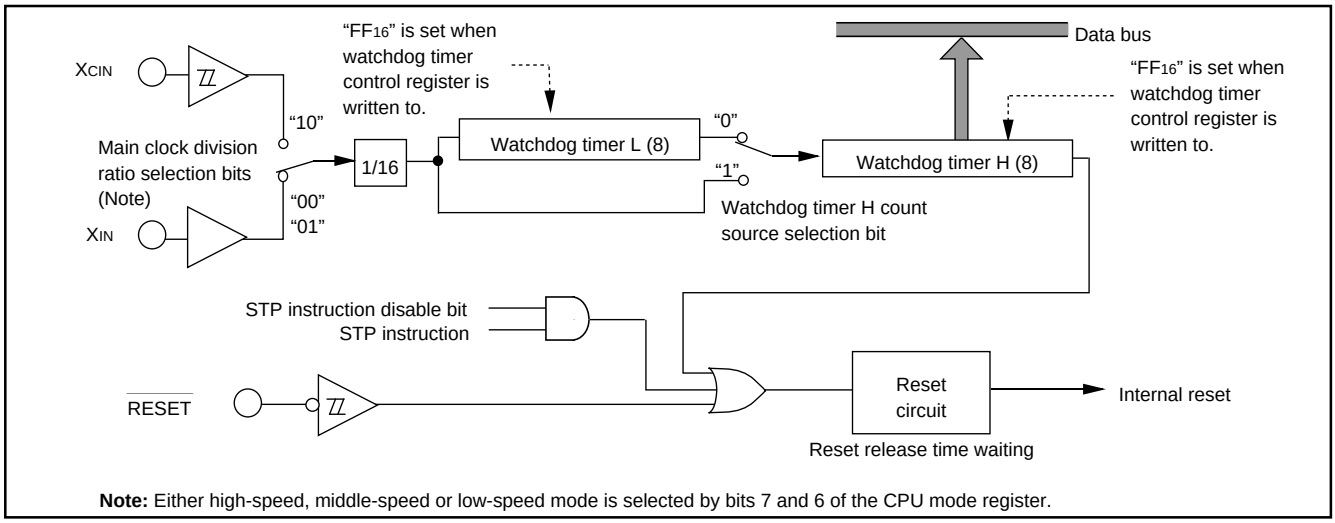
The watchdog timer stops at reset and a countdown is started by the writing to the watchdog timer control register. An internal reset occurs when watchdog timer H underflows. The reset is released after its release time. After the release, the program is restarted from the reset vector address. Usually, write to the watchdog timer control register by software before an underflow of the watchdog timer H. The watchdog timer does not function if the watchdog timer control register is not written to at least once.

When bit 6 of the watchdog timer control register is kept at "0", the STP instruction is enabled. When that is executed, both the clock and the watchdog timer stop. Count re-starts at the same time as the release of stop mode **(Note)**. The watchdog timer does not stop while a WIT instruction is executed. In addition, the STP instruction is disabled by writing "1" to this bit again. When the STP instruction is executed at this time, it is processed as an undefined instruction, and an internal reset occurs. Once a "1" is written to this bit, it cannot be programmed to "0" again.
The following shows the period between the write execution to the watchdog timer control register and the underflow of watchdog timer H.

Bit 7 of the watchdog timer control register is "0":
when XCIN = 32.768 kHz; 32 s
when XIN = 16 MHz; 65.536 ms

Bit 7 of the watchdog timer control register is "1":
when XCIN = 32.768 kHz; 125 ms
when XIN = 16 MHz; 256 µs

Note: The watchdog timer continues to count even while waiting for a stop release. Therefore, make sure that watchdog timer H does not underflow during this period.



Note: Either high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of the CPU mode register.

Fig. 62 Block diagram of Watchdog timer

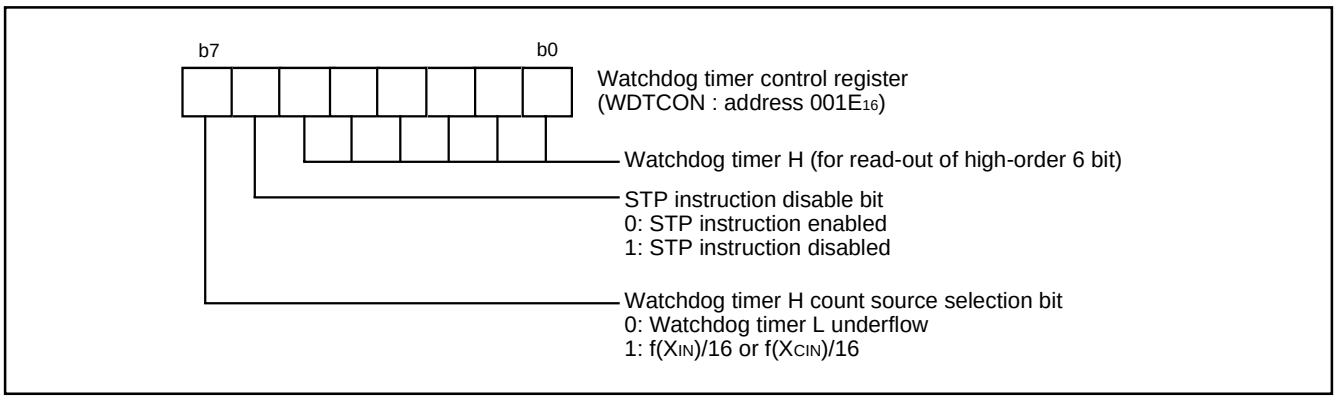


Fig. 63 Structure of Watchdog timer control register

MULTI-MASTER I²C-BUS INTERFACE

The 3804 group has the multi-master I²C-BUS interface.

The multi-master I²C-BUS interface is a serial communications circuit, conforming to the Philips I²C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications.

Figure 64 shows a block diagram of the multi-master I²C-BUS interface and Table 10 lists the multi-master I²C-BUS interface functions.

This multi-master I²C-BUS interface consists of the I²C slave address registers 0 to 2, the I²C data shift register, the I²C clock control register, the I²C control register, the I²C status register, the I²C START/STOP condition control register, the I²C special mode control register, the I²C special mode status register, and other control circuits.

When using the multi-master I²C-BUS interface, set 1 MHz or more to the internal clock ϕ.

Table 10 Multi-master I²C-BUS interface functions

Item	Function
Format	In conformity with Philips I²C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I²C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at ϕ= 4 MHz)

System clock ϕ = f(XIN)/2 (high-speed mode)
ϕ = f(XIN)/8 (middle-speed mode)

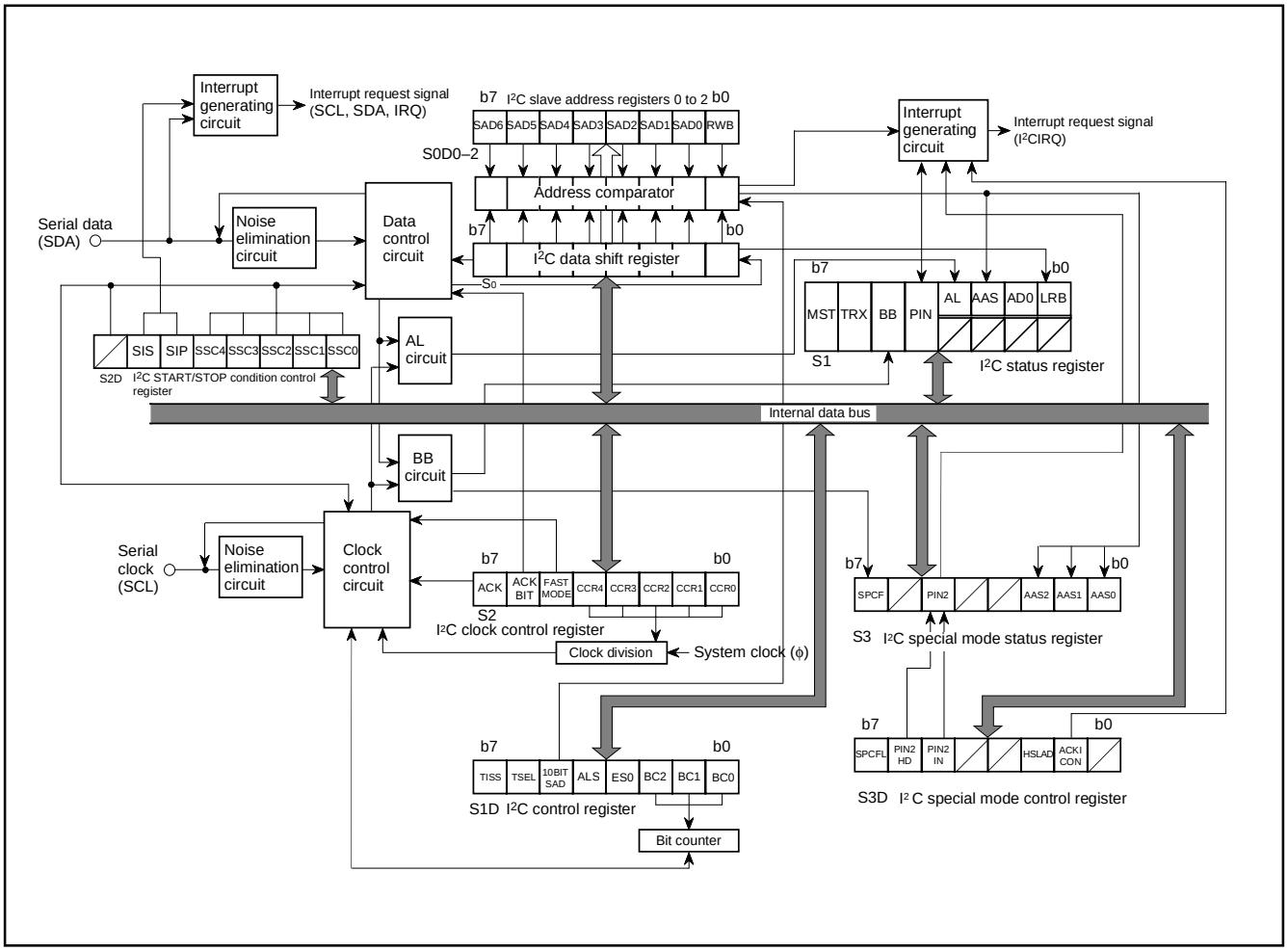


Fig. 64 Block diagram of multi-master I²C-BUS interface

✻ : Purchase of MITSUBISHI ELECTRIC CORPORATIONS I²C components conveys a license under the Philips I²C Patent Rights to use these components an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

[I²C Data Shift Register (S0)] 0011₁₆

The I²C data shift register (S0: address 0011₁₆) is an 8-bit shift register to store receive data and write transmit data.

When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL, and each time one-bit data is output, the data of this register are shifted by one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL, and each time one-bit data is input, the data of this register are shifted by one bit to the left. The minimum 2 cycles of the internal clock ϕ are required from the rising of the SCL until input to this register.

The I²C data shift register is in a write enable status only when the I²C-BUS interface enable bit (ES0 bit) of the I²C control register (S1D: address 0014₁₆) is "1". The bit counter is reset by a write instruction to the I²C data shift register. When both the ES0 bit and the MST bit of the I²C status register (S1: address 0013₁₆) are "1," the SCL is output by a write instruction to the I²C data shift register. Reading data from the I²C data shift register is always enabled regardless of the ES0 bit value.

[I²C Slave Address Registers 0 to 2 (S0D0 to S0D2)] 0FF7₁₆ to 0FF9₁₆

The I²C slave address registers 0 to 2 (S0D0 to S0D2: addresses 0FF7₁₆ to 0FF9₁₆) consists of a 7-bit slave address and a read/$\overline{\text{write}}$ bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition is detected.

•Bit 0: Read/$\overline{\text{write}}$ bit (RWB)

This is not used in the 7-bit addressing mode. In the 10-bit addressing mode, set RWB to "0" because the first address data to be received is compared with the contents (SAD6 to SAD0 + RWB) of the I²C slave address registers 0 to 2.

When 2-byte address data match slave address, a 7-bit slave address which is received after restart condition has detected and R/$\overline{\text{W}}$ data can be matched by setting "1" to RWB with software. The RWB is cleared to "0" automatically when the stop condition is detected.

•Bits 1 to 7: Slave address (SAD0–SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode or the 10-bit addressing mode, the address data transmitted from the master is compared with these bits' contents.

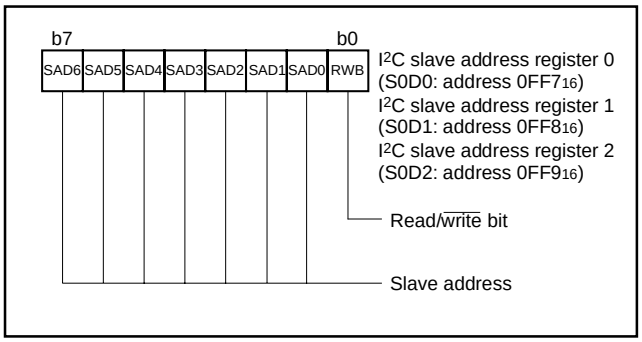


Fig. 65 Structure of I²C slave address registers 0 to 2

[I²C Clock Control Register (S2)] 0015₁₆

The I²C clock control register (S2: address 0015₁₆) is used to set ACK control, SCL mode and SCL frequency.

•Bits 0 to 4: SCL frequency control bits (CCR0–CCR4)

These bits control the SCL frequency. Refer to Table 11.

•Bit 5: SCL mode specification bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to "0," the standard clock mode is selected. When the bit is set to "1," the high-speed clock mode is selected.

When connecting the bus of the high-speed mode I²C bus standard (maximum 400 kbits/s), use 8 MHz or more oscillation frequency f(XIN) in the high-speed mode (2 division clock).

•Bit 6: ACK bit (ACK BIT)

This bit sets the SDA status when an ACK clock* is generated. When this bit is set to "0," the ACK return mode is selected and SDA goes to "L" at the occurrence of an ACK clock. When the bit is set to "1," the ACK non-return mode is selected. The SDA is held in the "H" status at the occurrence of an ACK clock.

However, when the slave address agree with the address data in the reception of address data at ACK BIT = "0," the SDA is automatically made "L" (ACK is returned). If there is a disagreement between the slave address and the address data, the SDA is automatically made "H" (ACK is not returned).

*ACK clock: Clock for acknowledgment

•Bit 7: ACK clock bit (ACK)

This bit specifies the mode of acknowledgment which is an acknowledgment response of data transfer. When this bit is set to "0," the no ACK clock mode is selected. In this case, no ACK clock occurs after data transmission. When the bit is set to "1," the ACK clock mode is selected and the master generates an ACK clock each completion of each 1-byte data transfer. The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (makes SDA "H") and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transfer. If data is written during transfer, the I²C clock generator is reset, so that data cannot be transferred normally.

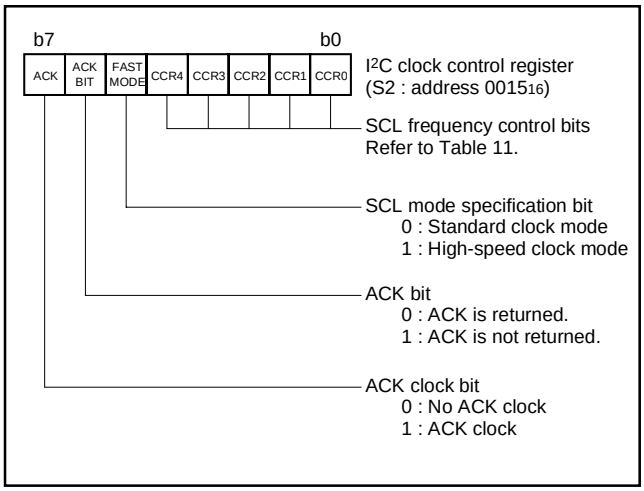


Fig. 66 Structure of I²C clock control register

Table 11 Set values of I²C clock control register and SCL frequency

Setting value of CCR4–CCR0					SCL frequency (at ϕ = 4 MHz, unit : kHz) **(Note 1)**	
CCR4	CCR3	CCR2	CCR1	CCR0	Standard clock mode	High-speed clock mode
0	0	0	0	0	Setting disabled	Setting disabled
0	0	0	0	1	Setting disabled	Setting disabled
0	0	0	1	0	Setting disabled	Setting disabled
0	0	0	1	1	– **(Note 2)**	333
0	0	1	0	0	– **(Note 2)**	250
0	0	1	0	1	100	400 **(Note 3)**
0	0	1	1	0	83.3	166
⋮	⋮	⋮	⋮	⋮	500/CCR value **(Note 3)**	1000/CCR value **(Note 3)**
1	1	1	0	1	17.2	34.5
1	1	1	1	0	16.6	33.3
1	1	1	1	1	16.1	32.3

Notes 1: Duty of SCL output is 50 %. The duty becomes 35 to 45 % only when the high-speed clock mode is selected and CCR value = 5 (400 kHz, at ϕ = 4 MHz). "H" duration of the clock fluctuates from –4 to +2 machine cycles in the standard clock mode, and fluctuates from –2 to +2 machine cycles in the high-speed clock mode. In the case of negative fluctuation, the frequency does not increase because "L" duration is extended instead of "H" duration reduction.
These are values when SCL synchronization by the synchronous function is not performed. CCR value is the decimal notation value of the SCL frequency control bits CCR4 to CCR0.

2: Each value of SCL frequency exceeds the limit at ϕ = 4 MHz or more. When using these setting value, use ϕ of 4 MHz or less.

3: The data formula of SCL frequency is described below:
ϕ/(8 × CCR value) Standard clock mode
ϕ/(4 × CCR value) High-speed clock mode (CCR value ≠ 5)
ϕ/(2 × CCR value) High-speed clock mode (CCR value = 5)
Do not set 0 to 2 as CCR value regardless of ϕ frequency.
Set 100 kHz (max.) in the standard clock mode and 400 kHz (max.) in the high-speed clock mode to the SCL frequency by setting the SCL frequency control bits CCR4 to CCR0.

[I²C Control Register (S1D)] 0014₁₆

The I²C control register (S1D: address 0014₁₆) controls data communication format.

•Bits 0 to 2: Bit counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. The I²C interrupt request signal occurs immediately after the number of count specified with these bits (ACK clock is added to the number of count when ACK clock is selected by ACK clock bit (bit 7 of S2, address 0015₁₆) have been transferred, and BC0 to BC2 are returned to "000₂".

Also when a START condition is received, these bits become "000₂" and the address data is always transmitted and received in 8 bits.

•Bit 3: I²C interface enable bit (ES0)

This bit enables to use the multi-master I²C-BUS interface. When this bit is set to "0," the use disable status is provided, so that the SDA and the SCL become high-impedance. When the bit is set to "1," use of the interface is enabled.

When ES0 = "0," the following is performed.

- PIN = "1," BB = "0" and AL = "0" are set (which are bits of the I²C status register, S1, at address 0013₁₆).
- Writing data to the I²C data shift register (S0: address 0011₁₆) is disabled.

•Bit 4: Data format selection bit (ALS)

This bit decides whether or not to recognize slave addresses. When this bit is set to "0," the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to "I²C Status Register," bit 1) is received, transfer processing can be performed. When this bit is set to "1," the free data format is selected, so that slave addresses are not recognized.

•Bit 5: Addressing format selection bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to "0," the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I²C slave address registers 0 to 2 are compared with address data. When this bit is set to "1," the 10-bit addressing format is selected, and all the bits of the I²C slave address registers 0 to 2 are compared with address data.

•Bit 7: I²C-BUS interface pin input level selection bit (TISS)

This bit selects the input level of the SCL and SDA pins of the multi-master I²C-BUS interface.

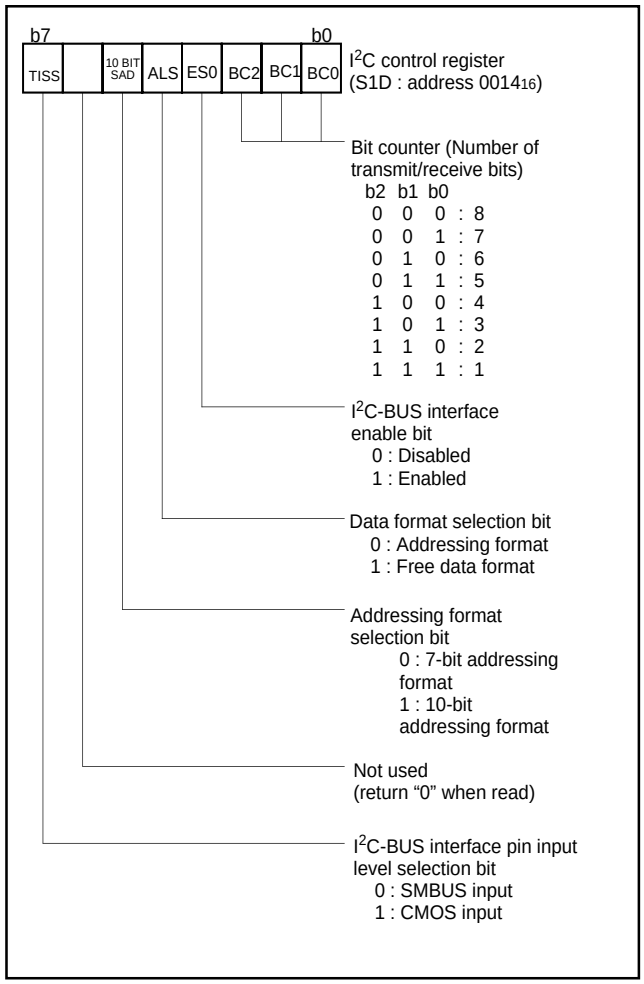


Fig. 67 Structure of I²C control register

[I²C Status Register (S1)] 0013₁₆

The I²C status register (S1: address 0013₁₆) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

Set "0000₂" to the low-order 4 bits, because these bits become the reserved bits at writing.

•Bit 0: Last receive bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0." If ACK is not returned, this bit is set to "1." Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (S0: address 0011₁₆).

•Bit 1: General call detecting flag (AD0)

When the ALS bit is "0", this bit is set to "1" when a general call* whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition, or reset.

*General call: The master transmits the general call address "00₁₆" to all slaves.

•Bit 2: Slave address comparison flag (AAS)

This flag indicates a comparison result of address data when the ALS bit is "0".

① In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions:
- The address data immediately after occurrence of a START condition agrees with the slave address stored in the high-order 7 bits of the I²C slave address register.
- A general call is received.

② In the slave receive mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition:
- When the address data is compared with the I²C slave address register (8 bits consisting of slave address and RWB bit), the first bytes agree.

③ This bit is set to "0" by executing a write instruction to the I²C data shift register (S0: address 0011₁₆) when ES0 is set to "1" or reset.

•Bit 3: Arbitration lost* detecting flag (AL)

In the master transmission mode, when the SDA is made "L" by any other device, arbitration is judged to have been lost, so that this bit is set to "1." At the same time, the TRX bit is set to "0," so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0." The arbitration lost can be detected only in the master transmission mode. When arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to detect the agreement of its own slave address and address data transmitted by another master device.

The AL bit is set to "0" in one of the following conditions:
- Executing a write instruction to the I²C data shift register (S0: address 0011₁₆)
- When the ES0 bit is "0"
- At reset

*Arbitration lost : The status in which communication as a master is disabled.

•Bit 4: SCL pin low hold bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the PIN bit changes from "1" to "0." At the same time, an interrupt request signal occurs to the CPU. The PIN bit is set to "0" in synchronization with a falling of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling of the PIN bit. When the PIN bit is "0," the SCL is kept in the "0" state and clock generation is disabled. Figure 69 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in one of the following conditions:
- Executing a write instruction to the I²C data shift register (S0: address 0011₁₆). (This is the only condition which the prohibition of the internal clock is released and data can be communicated except for the start condition detection.)
- When the ES0 bit is "0"
- At reset
- When writing "1" to the PIN bit by software

The PIN bit is set to "0" in one of the following conditions:
- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address agreement or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

•Bit 5: Bus busy flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0," this bus system is not busy and a START condition can be generated. The BB flag is set/reset by the SCL, SDA pins input signal regardless of master/slave. This flag is set to "1" by detecting the START condition, and is set to "0" by detecting the STOP condition. The condition of these detecting is set by the START/STOP condition setting bits (SSC4–SSC0) of the I²C START/STOP condition control register (S2D: address 0016₁₆). When the ES0 bit of the I²C control register (bit 3 of S1D, address 0014₁₆) is "0" or reset, the BB flag is set to "0."

For the writing function to the BB flag, refer to the sections "START Condition Generating Method" and "STOP Condition Generating Method" described later.

•Bit 6: Communication mode specification bit (transfer direction specification bit: TRX)

This bit decides a direction of transfer for data communication. When this bit is “0,” the reception mode is selected and the data of a transmitting device is received. When the bit is “1,” the transmission mode is selected and address data and control data are output onto the SDA in synchronization with the clock generated on the SCL.

This bit is set/reset by software and hardware. About set/reset by hardware is described below. This bit is set to “1” by hardware when all the following conditions are satisfied:

- When ALS is “0”
- In the slave reception mode or the slave transmission mode
- When the R/$\overline{W}$ bit reception is “1”

This bit is set to “0” in one of the following conditions:

- When arbitration lost is detected.
- When a STOP condition is detected.
- When writing “1” to this bit by software is invalid by the START condition duplication preventing function **(Note)**.
- With MST = “0” and when a START condition is detected.
- With MST = “0” and when ACK non-return is detected.
- At reset

•Bit 7: Communication mode specification bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is “0,” the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is “1,” the master is specified and a START condition and a STOP condition are generated. Additionally, the clocks required for data communication are generated on the SCL.

This bit is set to “0” in one of the following conditions.

- Immediately after completion of the byte which has lost arbitration when arbitration lost is detected
- When a STOP condition is detected.
- Writing “1” to this bit by software is invalid by the START condition duplication preventing function **(Note)**.
- At reset

Note: START condition duplication preventing function
The MST, TRX, and BB bits is set to “1” at the same time after confirming that the BB flag is “0” in the procedure of a START condition occurrence. However, when a START condition by another master device occurs and the BB flag is set to “1” immediately after the contents of the BB flag is confirmed, the START condition duplication preventing function makes the writing to the MST and TRX bits invalid. The duplication preventing function becomes valid from the rising of the BB flag to reception completion of slave address.

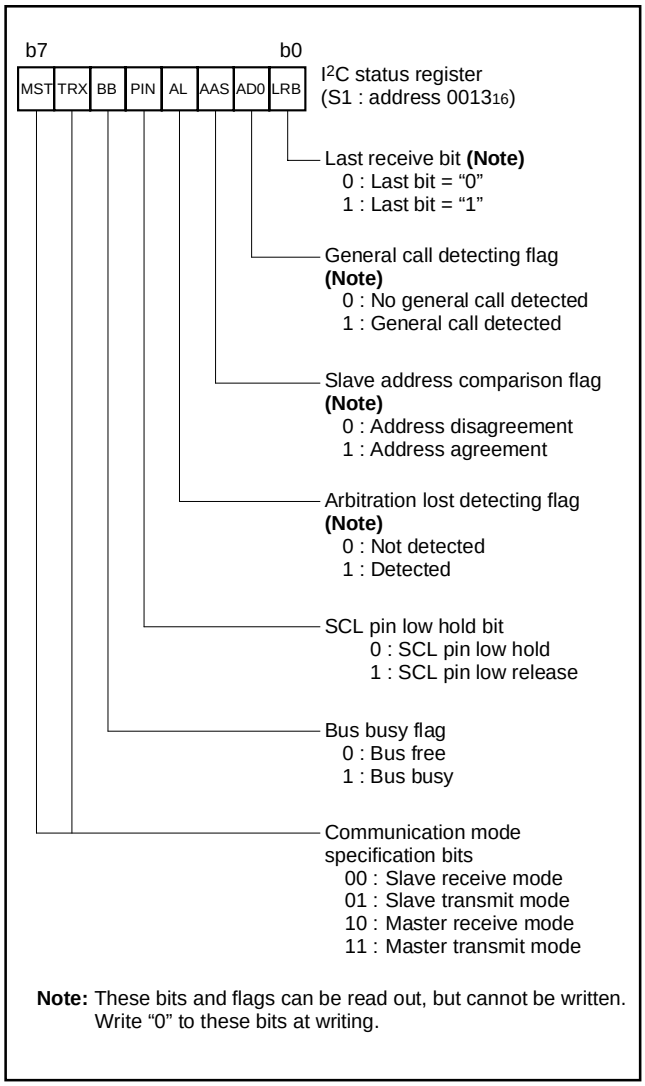


Fig. 68 Structure of I²C status register

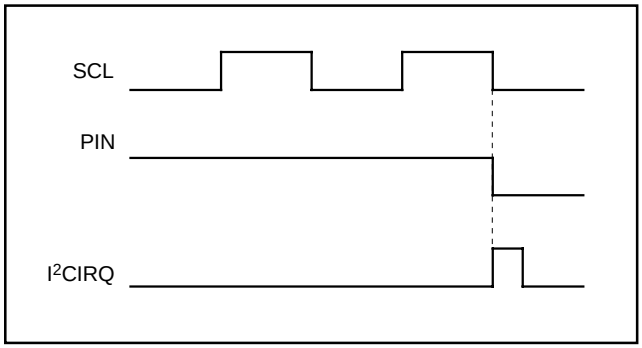


Fig. 69 Interrupt request signal generating timing

START Condition Generating Method

When writing “1” to the MST, TRX, and BB bits of the I²C status register (S1: address 001316) at the same time after writing the slave address to the I²C data shift register (S0: address 001116) with the condition in which the ES0 bit of the I²C control register (S1D: address 001416) is “1” and the BB flag is “0”, a START condition occurs. After that, the bit counter becomes “0002” and an SCL for 1 byte is output. The START condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 70, the START condition generating timing diagram, and Table 12, the START condition generating timing table.

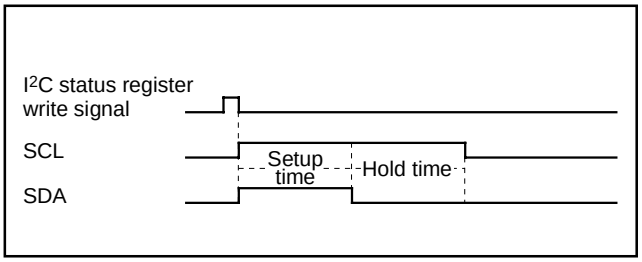


Fig. 70 START condition generating timing diagram

Table 12 START condition generating timing table

Item	Standard clock mode	High-speed clock mode
Setup time	5.0 µs (20 cycles)	2.5 µs (10 cycles)
Hold time	5.0 µs (20 cycles)	2.5 µs (10 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

STOP Condition Generating Method

When the ES0 bit of the I²C control register (S1D: address 001416) is “1,” write “1” to the MST and TRX bits, and write “0” to the BB bit of the I²C status register (S1: address 001316) simultaneously. Then a STOP condition occurs. The STOP condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 71, the STOP condition generating timing diagram, and Table 13, the STOP condition generating timing table.

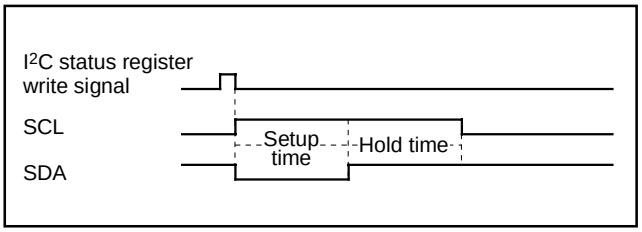


Fig. 71 STOP condition generating timing diagram

Table 13 STOP condition generating timing table

Item	Standard clock mode	High-speed clock mode
Setup time	5.0 µs (20 cycles)	3.0 µs (12 cycles)
Hold time	4.5 µs (18 cycles)	2.5 µs (10 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

START/STOP Condition Detecting Operation

The START/STOP condition detection operations are shown in Figures 72, 73, and Table 14. The START/STOP condition is set by the START/STOP condition set bit.

The START/STOP condition can be detected only when the input signal of the SCL and SDA pins satisfy three conditions: SCL release time, setup time, and hold time (see Table 14).

The BB flag is set to "1" by detecting the START condition and is reset to "0" by detecting the STOP condition.

The BB flag set/reset timing is different in the standard clock mode and the high-speed clock mode. Refer to Table 14, the BB flag set/reset time.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "I^2CIRQ" occurs to the CPU.

Table 14 START condition/STOP condition detecting conditions

	Standard clock mode	High-speed clock mode
SCL release time	SSC value + 1 cycle (6.25 µs)	4 cycles (1.0 µs)
Setup time	$\frac{\text{SSC value + 1}}{2}$ cycle < 4.0 µs (3.125 µs)	2 cycles (0.5 µs)
Hold time	$\frac{\text{SSC value + 1}}{2}$ cycle < 4.0 µs (3.125 µs)	2 cycles (0.5 µs)
BB flag set/ reset time	$\frac{\text{SSC value} - 1}{2}$ + 2 cycles (3.375 µs)	3.5 cycles (0.875 µs)

Note: Unit : Cycle number of internal clock ϕ
SSC value is the decimal notation value of the START/STOP condition set bits SSC4 to SSC0. Do not set "0" or an odd number to SSC value. The value in parentheses is an example when the I^2C START/STOP condition control register is set to "18_{16}" at ϕ = 4 MHz.

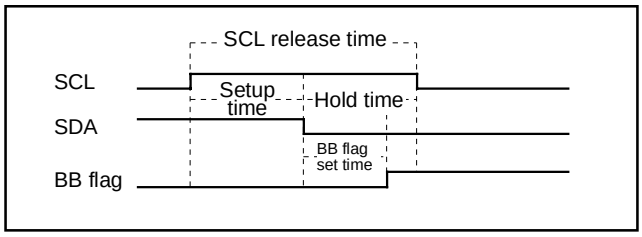


Fig. 72 START/STOP condition detecting timing diagram

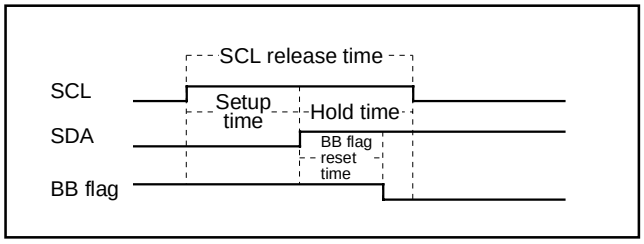


Fig. 73 STOP condition detecting timing diagram

[I²C START/STOP Condition Control Register (S2D)] 0016₁₆

The I²C START/STOP condition control register (S2D: address 0016₁₆) controls START/STOP condition detection.

•Bits 0 to 4: START/STOP condition set bits (SSC4–SSC0)

SCL release time, setup time, and hold time change the detection condition by value of the main clock divide ratio selection bit and the oscillation frequency f(XIN) because these time are measured by the internal system clock. Accordingly, set the proper value to the START/STOP condition set bits (SSC4 to SSC0) in considered of the system clock frequency. Refer to Table 14.

Do not set "00000₂" or an odd number to the START/STOP condition set bits (SSC4 to SSC0).

Refer to Table 15, the recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency.

•Bit 5: SCL/SDA interrupt pin polarity selection bit (SIP)

An interrupt can occur when detecting the falling or rising edge of the SCL or SDA pin. This bit selects the polarity of the SCL or SDA pin interrupt pin.

•Bit 6: SCL/SDA interrupt pin selection bit (SIS)

This bit selects the pin of which interrupt becomes valid between the SCL pin and the SDA pin.

Note: When changing the setting of the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I²C-BUS interface enable bit ES0, the SCL/SDA interrupt request bit may be set. When selecting the SCL/SDA interrupt source, disable the interrupt before the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I²C-BUS interface enable bit ES0 is set. Reset the request bit to "0" after setting these bits, and enable the interrupt.

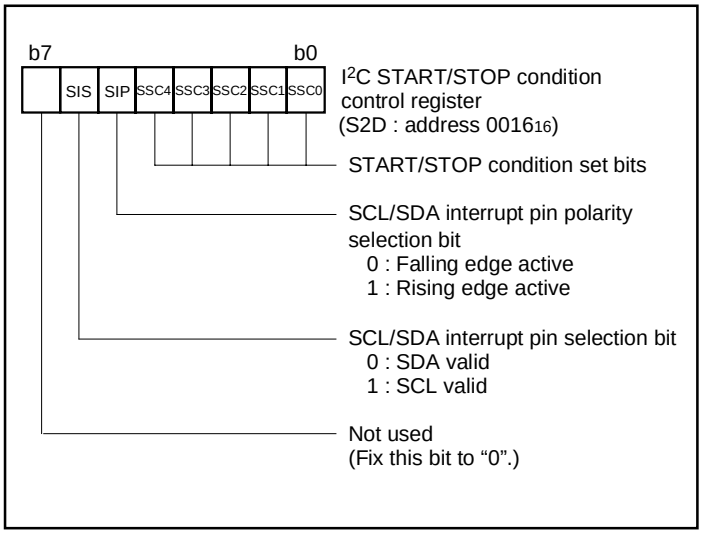


Fig. 74 Structure of I²C START/STOP condition control register

Table 15 Recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency

Oscillation frequency f(XIN) (MHz)	Main clock divide ratio	Internal clock ϕ (MHz)	START/STOP condition control register	SCL release time (µs)	Setup time (µs)	Hold time (µs)
8	2	4	XXX11010	6.75 µs (27 cycles)	3.5 µs (14 cycles)	3.25 µs (13 cycles)
			XXX11000	6.25 µs (25 cycles)	3.25 µs (13 cycles)	3.0 µs (12 cycles)
8	8	1	XXX00100	5.0 µs (5 cycles)	3.0 µs (3 cycles)	2.0 µs (2 cycles)
4	2	2	XXX01100	6.5 µs (13 cycles)	3.5 µs (7 cycles)	3.0 µs (6 cycles)
			XXX01010	5.5 µs (11 cycles)	3.0 µs (6 cycles)	2.5 µs (5 cycles)
2	2	1	XXX00100	5.0 µs (5 cycles)	3.0 µs (3 cycles)	2.0 µs (2 cycles)

Note: Do not set an odd number to the START/STOP condition set bits (SSC4 to SSC0) and "00000₂".

[I²C Special Mode Status Register (S3)] 0012₁₆

The I²C special mode status register (S3: address 0012₁₆) consists of the flags indicating I²C operating state in the I²C special mode, which is set by the I²C special mode control register (S3D: address 0017₁₆).

The stop condition flag is valid in all operating modes.

•Bit 0: Slave address 0 comparison flag (AAS0)
Bit 1: Slave address 1 comparison flag (AAS1)
Bit 2: Slave address 2 comparison flag (AAS2)

These flags indicate a comparison result of address data. These flags are valid only when the slave address control bit (MSLAD) is "1".

In the 7-bit addressing format of the slave reception mode, the respective slave address i (i = 0, 1, 2) comparison flags corresponding to the I²C slave address registers 0 to 2 are set to "1" when an address data immediately after an occurrence of a START condition agrees with the high-order 7-bit slave address stored in the I²C slave address registers 0 to 2 (addresses 0FF7₁₆ to 0FF9₁₆).

In the 10-bit addressing format of the slave mode, the respective slave address i (i = 0, 1, 2) comparison flags corresponding to the I²C slave address registers are set to "1" when an address data is compared with the 8 bits consisting of the slave address stored in the I²C slave address registers 0 to 2 and the RWB bit, and the first byte agrees.

These flags are initialized to "0" at reset, when the slave address control bit (MSLAD) is "0", or when writing data to the I²C data shift register (S0: address 0011₁₆).

•Bit 5: SCL pin low hold 2 flag (PIN2)

When the ACK interrupt control bit (ACKICON) and the ACK clock bit (ACK) are "1", this flag is set to "0" in synchronization with the falling of the data's last SCL clock, just before the ACK clock. The SCL pin is simultaneously held low, and the I²C interrupt request occurs.

This flag is initialized to "1" at reset, when the ACK interrupt control bit (ACKICON) is "0", or when writing "1" to the SCL pin low hold 2 flag set bit (PIN2IN).

The SCL pin is held low when either the SCL pin low hold bit (PIN) or the SCL pin low hold 2 flag (PIN2) becomes "0". The low hold state of the SCL pin is released when both the SCL pin low hold bit (PIN) and the SCL pin low hold 2 flag (PIN2) are "1".

•Bit 7: Stop condition flag (SPCF)

This flag is set to "1" when a STOP condition occurs.

This flag is initialized to "0" at reset, when the I²C-BUS interface enable bit (ES0) is "0", or when writing "1" to the STOP condition flag clear bit (SPFCL).

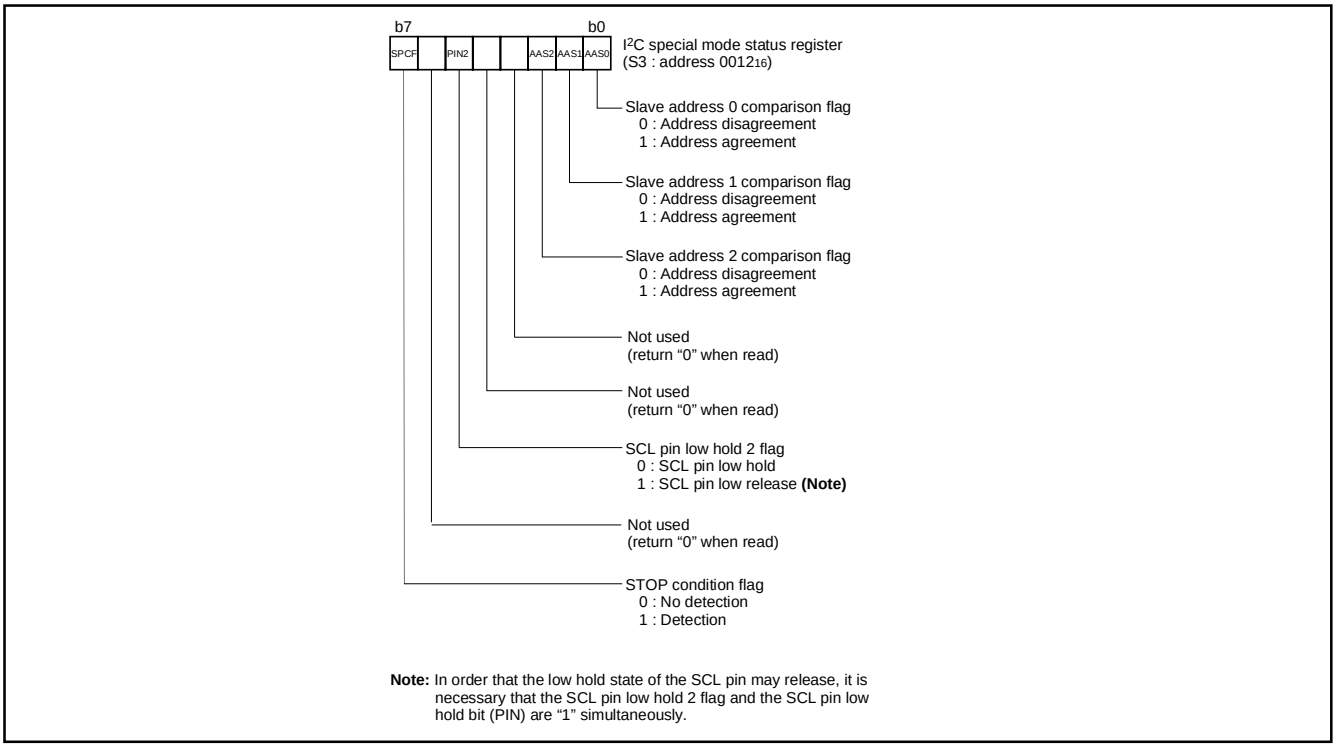


Fig. 75 Structure of I²C special mode status register

[I²C Special Mode Control Register (S3D)] 0017₁₆

The I²C special mode control register (S3D: address 0017₁₆) controls special functions such as occurrence timing of reception interrupt request and extending slave address comparison to 3 bytes.

•Bit 1: ACK interrupt control bit (ACKICON)

This bit controls the timing of I²C interrupt request occurrence at completion of data receiving due to master reception or slave reception.

When this bit is "0", the SCL pin low hold bit (PIN) is set to "0" in synchronization with the falling of the last SCL clock, including the ACK clock. The SCL pin is simultaneously held low, and the I²C interrupt request occurs.

When this bit is "1" and the ACK clock bit (ACK) is "1", the SCL pin low hold 2 flag (PIN2) is set to "0" in synchronization with the falling of the data's last SCL clock, just before the ACK clock. The SCL pin is simultaneously held low, and the I²C interrupt request occurs again. The ACK bit can be changed after the contents of data are confirmed by using this function.

•Bit 2: I²C slave address control bit (MSLAD)

This bit controls a slave address. When this bit is "0", only the I²C slave address register 0 (address 0FF7₁₆) becomes valid as a slave address and a read/write bit.

When this bit is "1", all of the I²C slave address registers 0 to 2 (addresses 0FF7₁₆ to 0FF9₁₆) become valid as a slave address and a read/write bit. In this case, when an address data agrees with any one of the I²C slave address registers 0 to 2, the slave address comparison flag (AAS) is set to "1" and the I²C slave address comparison flag corresponding to the agreed I²C slave address registers 0 to 2 is also set to "1".

•Bit 5: SCL pin low hold 2 flag set bit (PIN2IN)

Writing "1" to this bit initializes the SCL pin low hold 2 flag (PIN2) to "1".

When writing "0", nothing is generated.

•Bit 6: SCL pin low hold set bit (PIN2HD)

When the SCL pin low hold bit (PIN) becomes "0", the SCL pin is held low. However, the SCL pin low hold bit (PIN) cannot be set to "0" by software. The SCL pin low hold set bit (PIN2HD) is used to , hold the SCL pin in the low state by software. When writing "1" to this bit, the SCL pin low hold 2 flag (PIN2) becomes "0", and the SCL pin is held low. When writing "0", nothing occurs.

•Bit 7: STOP condition flag clear bit (SPFCL)

Writing "1" to this bit initializes the STOP condition flag (SPCF) to "0".

When writing "0", nothing is generated.

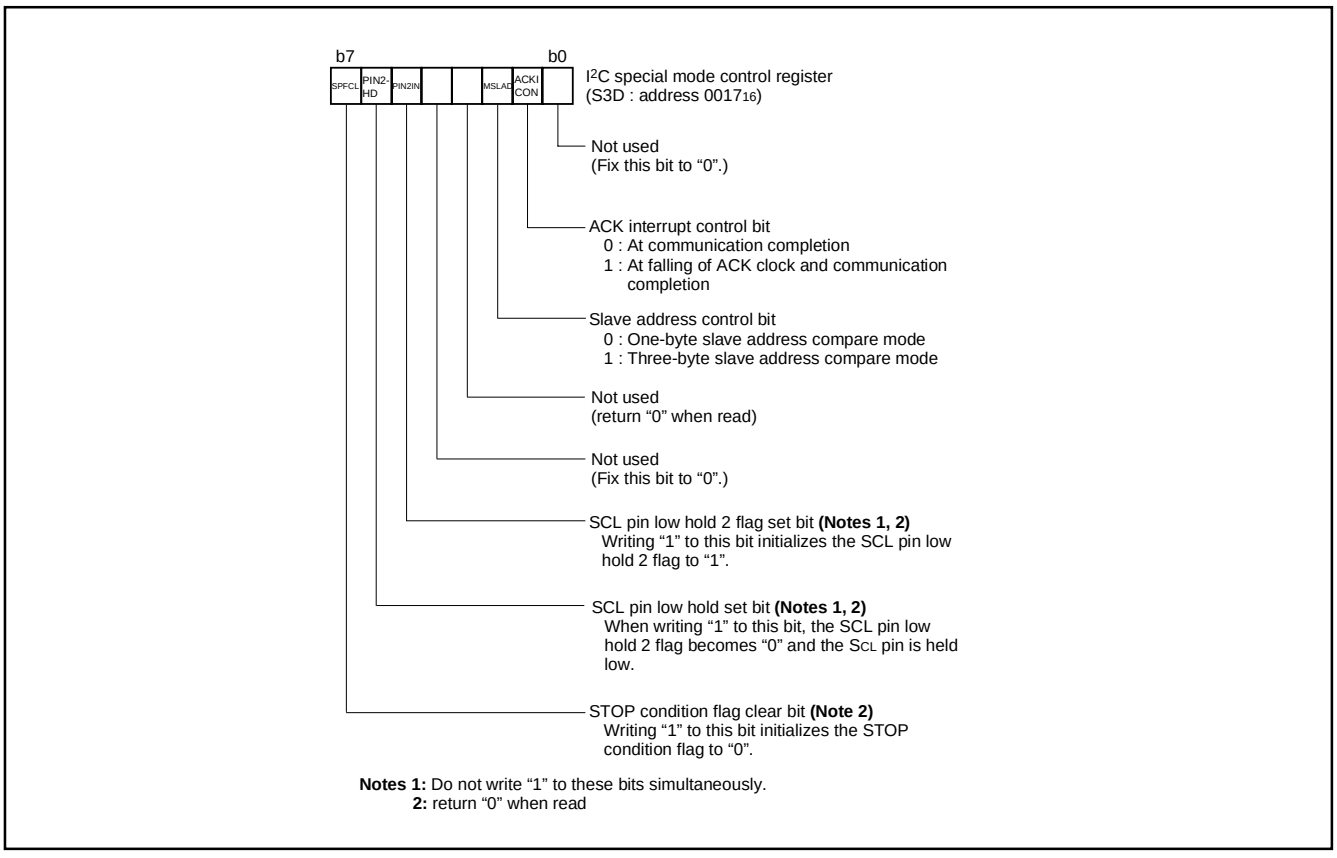


Fig. 76 Structure of I²C special mode control register

Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats are described below.

① 7-bit addressing format

To adapt the 7-bit addressing format, set the 10BIT SAD bit of the I²C control register (S1D: address 0014₁₆) to "0". The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I²C slave address register. At the time of this comparison, address comparison of the RWB bit of the I²C slave address register is not performed. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 77, (1) and (2).

② 10-bit addressing format

To adapt the 10-bit addressing format, set the 10BIT SAD bit of the I²C control register (S1D: address 0014₁₆) to "1." An address comparison is performed between the first-byte address data transmitted from the master and the 8-bit slave address stored in the I²C slave address register. At the time of this comparison, an address comparison between the RWB bit of the I²C slave address register and the R/$\overline{W}$ bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the RWB bit which is the last bit of the address data not only specifies the direction of communication for control data, but also is processed as an address data bit. When the first-byte address data agree with the slave address, the AAS bit of the I²C status register (S1: address 0013₁₆) is set to "1." After the second-byte address data is stored into the I²C data shift register (S0: address 0011₁₆), perform an address comparison between the second-byte data and the slave address by software. When the address data of the 2 bytes agree with the slave address, set the RWB bit of the I²C slave address register to "1" by software. This processing can make the 7-bit slave address and R/$\overline{W}$ data agree, which are received after a RESTART condition is detected, with the value of the I²C slave address register. For the data transmission format when the 10-bit addressing format is selected, refer to Figure 77, (3) and (4).

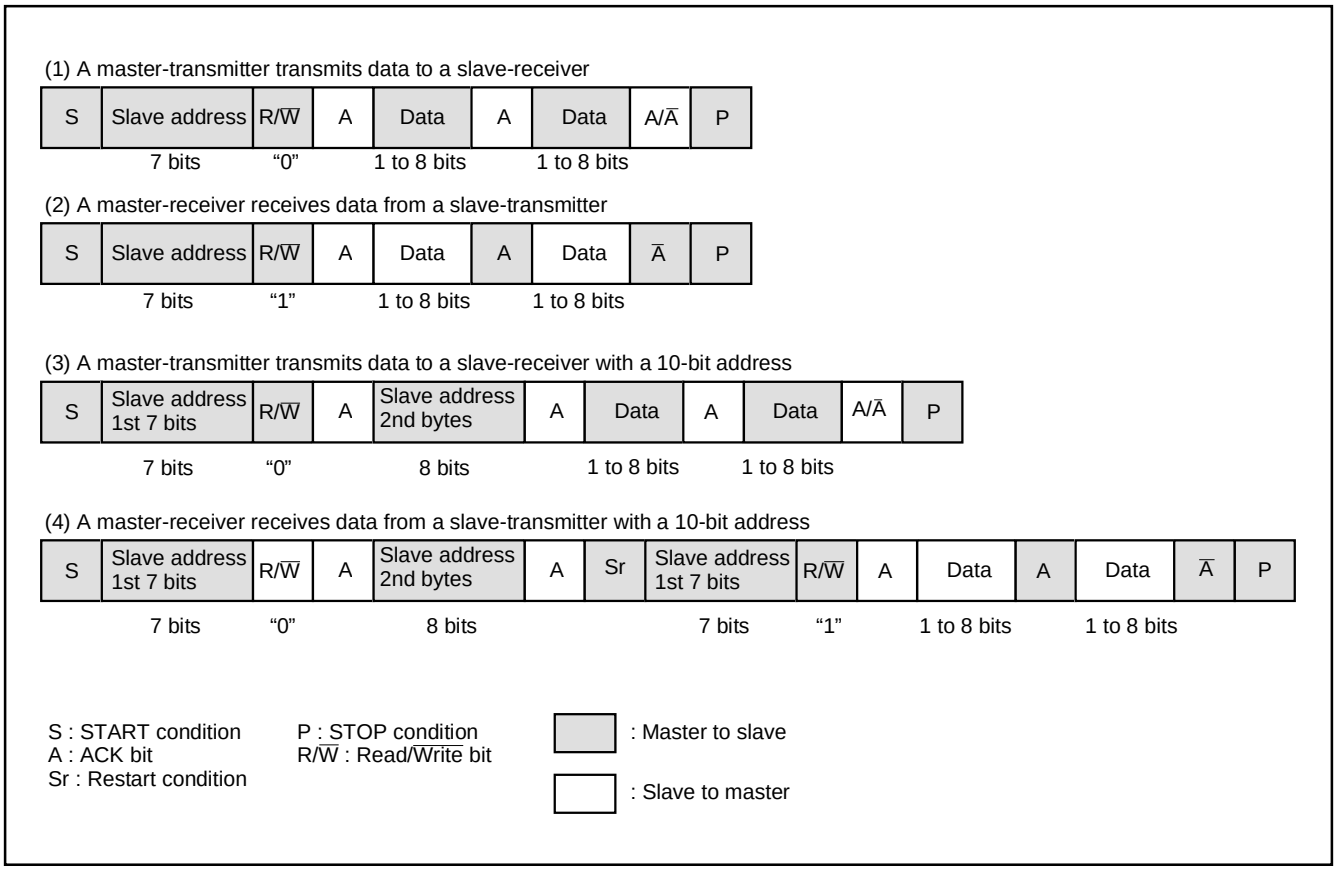


Fig. 77 Address data communication format

Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

① Set a slave address in the high-order 7 bits of the I^2C slave address register and "0" into the RWB bit.
② Set the ACK return mode and SCL = 100 kHz by setting "85_{16}" in the I^2C clock control register (S2: address 0015_{16}).
③ Set "00_{16}" in the I^2C status register (S1: address 0013_{16}) so that transmission/reception mode can become initializing condition.
④ Set a communication enable status by setting "08_{16}" in the I^2C control register (S1D: address 0014_{16}).
⑤ Confirm the bus free condition by the BB flag of the I^2C status register (S1: address 0013_{16}).
⑥ Set the address data of the destination of transmission in the high-order 7 bits of the I^2C data shift register (S0: address 0011_{16}) and set "0" in the least significant bit.
⑦ Set "$F0_{16}$" in the I^2C status register (S1: address 0013_{16}) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occur.
⑧ Set transmit data in the I^2C data shift register (S0: address 0011_{16}). At this time, an SCL and an ACK clock automatically occur.
⑨ When transmitting control data of more than 1 byte, repeat step ⑧.
⑩ Set "$D0_{16}$" in the I^2C status register (S1: address 0013_{16}) to generate a STOP condition if ACK is not returned from slave reception side or transmission ends.

Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode and using the addressing format is shown below.

① Set a slave address in the high-order 7 bits of the I^2C slave address register and "0" in the RWB bit.
② Set the no ACK clock mode and SCL = 400 kHz by setting "25_{16}" in the I^2C clock control register (S2: address 0015_{16}).
③ Set "00_{16}" in the I^2C status register (S1: address 0013_{16}) so that transmission/reception mode can become initializing condition.
④ Set a communication enable status by setting "08_{16}" in the I^2C control register (S1D: address 0014_{16}).
⑤ When a START condition is received, an address comparison is performed.
⑥ •When all transmitted addresses are "0" (general call):
AD0 of the I^2C status register (S1: address 0013_{16}) is set to "1" and an interrupt request signal occurs.
• When the transmitted addresses agree with the address set in ①:
AAS of the I^2C status register (S1: address 0013_{16}) is set to "1" and an interrupt request signal occurs.
• In the cases other than the above AD0 and AAS of the I^2C status register (S1: address 0013_{16}) are set to "0" and no interrupt request signal occurs.
⑦ Set dummy data in the I^2C data shift register (S0: address 0011_{16}).
⑧ When receiving control data of more than 1 byte, repeat step ⑦.
⑨ When a STOP condition is detected, the communication ends.

■Precautions when using multi-master I²C-BUS interface

(1) Read-modify-write instruction

The precautions when the read-modify-write instruction such as SEB, CLB etc. is executed for each register of the multi-master I²C-BUS interface are described below.

- I²C data shift register (S0: address 0011₁₆)
  When executing the read-modify-write instruction for this register during transfer, data may become a value not intended.
- I²C slave address registers 0 to 2 (S0D0 to S0D2: addresses 0FF7₁₆ to0FF9₁₆)
  When the read-modify-write instruction is executed for this register at detecting the STOP condition, data may become a value not intended. It is because H/W changes the read/write bit (RWB) at the above timing.
- I²C status register (S1: address 0013₁₆)
  Do not execute the read-modify-write instruction for this register because all bits of this register are changed by H/W.
- I²C control register (S1D: address 0014₁₆)
  When the read-modify-write instruction is executed for this register at detecting the START condition or at completing the byte transfer, data may become a value not intended. Because H/W changes the bit counter (BC0-BC2) at the above timing.
- I²C clock control register (S2: address 0015₁₆)
  The read-modify-write instruction can be executed for this register.
- I²C START/STOP condition control register (S2D: address 0016₁₆)
  The read-modify-write instruction can be executed for this register.

(2) START condition generating procedure using multi-master

1. Procedure example (The necessary conditions of the generating procedure are described as the following 2 to 5.

```
      ⋮
  LDA —                  (Taking out of slave address value)
  SEI                    (Interrupt disabled)
  BBS 5, S1, BUSBUSY     (BB flag confirming and branch process)
BUSFREE:
  STA S0                 (Writing of slave address value)
  LDM #$F0, S1           (Trigger of START condition generating)
  CLI                    (Interrupt enabled)
    ⋮
BUSBUSY:
  CLI                    (Interrupt enabled)
    ⋮
```

2. Use “Branch on Bit Set” of “BBS 5, S1, –” for the BB flag confirming and branch process.
3. Use “STA $12, STX $12” or “STY $12” of the zero page addressing instruction for writing the slave address value to the I²C data shift register.
4. Execute the branch instruction of above 2 and the store instruction of above 3 continuously shown the above procedure example.
5. Disable interrupts during the following three process steps:
   - BB flag confirming
   - Writing of slave address value
   - Trigger of START condition generating

   When the condition of the BB flag is bus busy, enable interrupts immediately.

(3) RESTART condition generating procedure

1. Procedure example (The necessary conditions of the generating procedure are described as the following 2 to 4.)
   Execute the following procedure when the PIN bit is “0.”

```
      ⋮
  LDM #$00, S1           (Select slave receive mode)
  LDA —                  (Taking out of slave address value)
  SEI                    (Interrupt disabled)
  STA S0                 (Writing of slave address value)
  LDM #$F0, S1           (Trigger of RESTART condition generating)
  CLI                    (Interrupt enabled)
    ⋮
```

2. Select the slave receive mode when the PIN bit is “0.” Do not write “1” to the PIN bit. Neither “0” nor “1” is specified for the writing to the BB bit.
   The TRX bit becomes “0” and the SDA pin is released.
3. The SCL pin is released by writing the slave address value to the I²C data shift register.
4. Disable interrupts during the following two process steps:
   - Writing of slave address value
   - Trigger of RESTART condition generating

(4) Writing to I²C status register

Do not execute an instruction to set the PIN bit to “1” from “0” and an instruction to set the MST and TRX bits to “0” from “1” simultaneously. It is because it may enter the state that the SCL pin is released and the SDA pin is released after about one machine cycle. Do not execute an instruction to set the MST and TRX bits to “0” from “1” simultaneously when the PIN bit is “1.” It is because it may become the same as above.

(5) Process of after STOP condition generating

Do not write data in the I²C data shift register S0 and the I²C status register S1 until the bus busy flag BB becomes “0” after generating the STOP condition in the master mode. It is because the STOP condition waveform might not be normally generated. Reading to the above registers does not have the problem.

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 16 cycles or more of X_{IN}. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between 2.7 V and 5.5 V, and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage is less than 0.54 V for V_{CC} of 2.7 V.

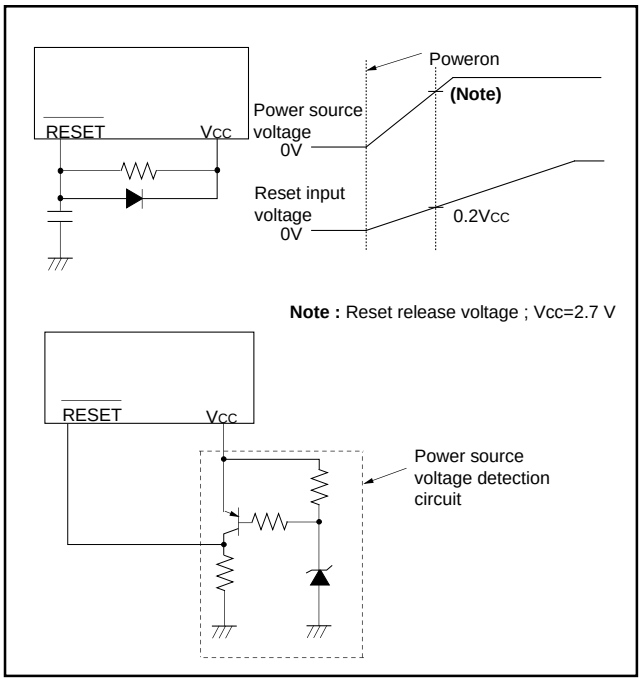


Fig. 78 Reset circuit example

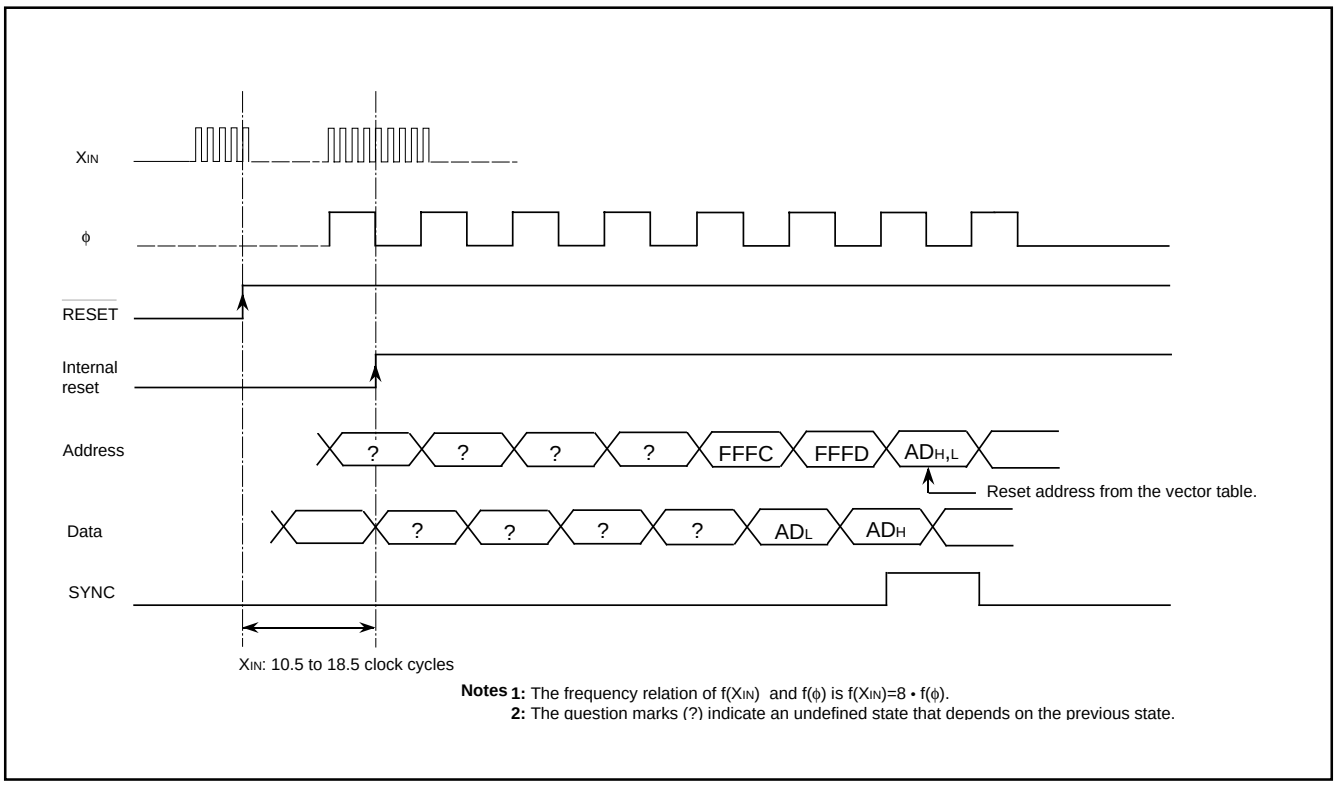


Fig. 79 Reset sequence

		Address	Register contents
(1)	Port P0 (P0)	0000_{16}	00_{16}
(2)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(3)	Port P1 (P1)	0002_{16}	00_{16}
(4)	Port P1 direction register (P1D)	0003_{16}	00_{16}
(5)	Port P2 (P2)	0004_{16}	00_{16}
(6)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(7)	Port P3 (P3)	0006_{16}	00_{16}
(8)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(9)	Port P4 (P4)	0008_{16}	00_{16}
(10)	Port P4 direction register (P4D)	0009_{16}	00_{16}
(11)	Port P5 (P5)	$000A_{16}$	00_{16}
(12)	Port P5 direction register (P5D)	$000B_{16}$	00_{16}
(13)	Port P6 (P6)	$000C_{16}$	00_{16}
(14)	Port P6 direction register (P6D)	$000D_{16}$	00_{16}
(15)	Timer 12, X count source selection register (T12XCSS)	$000E_{16}$	0 0 1 1 0 0 1 1
(16)	Timer Y, Z count source selection register (TYZCSS)	$000F_{16}$	0 0 1 1 0 0 1 1
(17)	MISRG	0010_{16}	00_{16}
(18)	Transmit/Receive buffer register 1 (TB1/RB1)	0018_{16}	X X X X X X X X
(19)	Serial I/O1 status register (SIO1STS)	0019_{16}	1 0 0 0 0 0 0 0
(20)	Serial I/O1 control register (SIO1CON)	$001A_{16}$	00_{16}
(21)	UART1 control register (UART1CON)	$001B_{16}$	1 1 1 0 0 0 0 0
(22)	Baud rate generator 1 (BRG1)	$001C_{16}$	X X X X X X X X
(23)	Serial I/O2 control register (SIO2CON)	$001D_{16}$	00_{16}
(24)	Watchdog timer control register (WDTCON)	$001E_{16}$	0 0 1 1 1 1 1 1
(25)	Serial I/O2 register (SIO2)	$001F_{16}$	X X X X X X X X
(26)	Prescaler 12 (PRE12)	0020_{16}	FF_{16}
(27)	Timer 1 (T1)	0021_{16}	01_{16}
(28)	Timer 2 (T2)	0022_{16}	FF_{16}
(29)	Timer XY mode register (TM)	0023_{16}	00_{16}
(30)	Prescaler X (PREX)	0024_{16}	FF_{16}
(31)	Timer X (TX)	0025_{16}	FF_{16}
(32)	Prescaler Y (PREY)	0026_{16}	FF_{16}
(33)	Timer Y (TY)	0027_{16}	FF_{16}

		Address	Register contents
(34)	Timer Z (low-order) (TZL)	0028_{16}	FF_{16}
(35)	Timer Z (high-order) (TZH)	0029_{16}	FF_{16}
(36)	Timer Z mode register (TZM)	$002A_{16}$	00_{16}
(37)	PWM control register (PWMCON)	$002B_{16}$	00_{16}
(38)	PWM prescaler (PREPWM)	$002C_{16}$	X X X X X X X X
(39)	PWM register (PWM)	$002D_{16}$	X X X X X X X X
(40)	Baud rate generator 3 (BRG3)	$002F_{16}$	X X X X X X X X
(41)	Transmit/Receive buffer register 3 (TB3/RB3)	0030_{16}	X X X X X X X X
(42)	Serial I/O3 status register (SIO3STS)	0031_{16}	1 0 0 0 0 0 0 0
(43)	Serial I/O3 control register (SIO3CON)	0032_{16}	00_{16}
(44)	UART3 control register (SIO3CON)	0033_{16}	1 1 1 0 0 0 0 0
(45)	AD/DA control register (ADCON)	0034_{16}	0 0 0 0 1 0 0 0
(46)	A-D conversion register 1 (AD1)	0035_{16}	X X X X X X X X
(47)	D-A1 conversion register (DA1)	0036_{16}	00_{16}
(48)	D-A2 conversion register (DA2)	0037_{16}	00_{16}
(49)	A-D conversion register 2 (AD2)	0038_{16}	0 0 0 0 0 0 X X
(50)	Interrupt source selection register (INTSEL)	0039_{16}	00_{16}
(51)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(52)	CPU mode register (CPUM)	$003B_{16}$	0 1 0 0 1 0 0 0
(53)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(54)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(55)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(56)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(57)	Port P0 pull-up control register (PULL0)	$0FF0_{16}$	00_{16}
(58)	Port P1 pull-up control register (PULL1)	$0FF1_{16}$	00_{16}
(59)	Port P2 pull-up control register (PULL2)	$0FF2_{16}$	00_{16}
(60)	Port P3 pull-up control register (PULL3)	$0FF3_{16}$	00_{16}
(61)	Port P4 pull-up control register (PULL4)	$0FF4_{16}$	00_{16}
(62)	Port P5 pull-up control register (PULL5)	$0FF5_{16}$	00_{16}
(63)	Port P6 pull-up control register (PULL6)	$0FF6_{16}$	00_{16}
(64)	Flash memory control register (FCON)	$0FFE_{16}$	00_{16}
(65)	Flash command register (FCMD)	$0FFF_{16}$	00_{16}
(66)	Processor status register	(PS)	X X X X X 1 X X
(67)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

Note : X : Not fixed
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 80 Internal status at reset (3803 group)

		Address	Register contents
(1)	Port P0 (P0)	0000_{16}	00_{16}
(2)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(3)	Port P1 (P1)	0002_{16}	00_{16}
(4)	Port P1 direction register (P1D)	0003_{16}	00_{16}
(5)	Port P2 (P2)	0004_{16}	00_{16}
(6)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(7)	Port P3 (P3)	0006_{16}	00_{16}
(8)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(9)	Port P4 (P4)	0008_{16}	00_{16}
(10)	Port P4 direction register (P4D)	0009_{16}	00_{16}
(11)	Port P5 (P5)	$000A_{16}$	00_{16}
(12)	Port P5 direction register (P5D)	$000B_{16}$	00_{16}
(13)	Port P6 (P6)	$000C_{16}$	00_{16}
(14)	Port P6 direction register (P6D)	$000D_{16}$	00_{16}
(15)	Timer 12, X count source selection register (T12XCSS)	$000E_{16}$	0 0 1 1 0 0 1 1
(16)	Timer Y, Z count source selection register (TYZCSS)	$000F_{16}$	0 0 1 1 0 0 1 1
(17)	MISRG	0010_{16}	00_{16}
(18)	I^2C data shift register (S0)	0011_{16}	X X X X X X X X
(19)	I^2C special mode status register (S3)	0012_{16}	0 0 1 0 0 0 0 0
(20)	I^2C status register (S1)	0013_{16}	0 0 0 1 0 0 0 X
(21)	I^2C control register (S1D)	0014_{16}	00_{16}
(22)	I^2C clock control register (S2)	0015_{16}	00_{16}
(23)	I^2C START/STOP condition control register (S2D)	0016_{16}	0 0 0 1 1 0 1 0
(24)	I^2C special mode control register (S3D)	0017_{16}	00_{16}
(25)	Transmit/Receive buffer register 1 (TB1/RB1)	0018_{16}	X X X X X X X X
(26)	Serial I/O1 status register (SIO1STS)	0019_{16}	1 0 0 0 0 0 0 0
(27)	Serial I/O1 control register (SIO1CON)	$001A_{16}$	00_{16}
(28)	UART1 control register (UART1CON)	$001B_{16}$	1 1 1 0 0 0 0 0
(29)	Baud rate generator 1 (BRG1)	$001C_{16}$	X X X X X X X X
(30)	Serial I/O2 control register (SIO2CON)	$001D_{16}$	00_{16}
(31)	Watchdog timer control register (WDTCON)	$001E_{16}$	0 0 1 1 1 1 1 1
(32)	Serial I/O2 register (SIO2)	$001F_{16}$	X X X X X X X X
(33)	Prescaler 12 (PRE12)	0020_{16}	FF_{16}
(34)	Timer 1 (T1)	0021_{16}	01_{16}
(35)	Timer 2 (T2)	0022_{16}	FF_{16}
(36)	Timer XY mode register (TM)	0023_{16}	00_{16}
(37)	Prescaler X (PREX)	0024_{16}	FF_{16}
(38)	Timer X (TX)	0025_{16}	FF_{16}
(39)	Prescaler Y (PREY)	0026_{16}	FF_{16}
(40)	Timer Y (TY)	0027_{16}	FF_{16}

		Address	Register contents
(41)	Timer Z (low-order) (TZL)	0028_{16}	FF_{16}
(42)	Timer Z (high-order) (TZH)	0029_{16}	FF_{16}
(43)	Timer Z mode register (TZM)	$002A_{16}$	00_{16}
(44)	PWM control register (PWMCON)	$002B_{16}$	00_{16}
(45)	PWM prescaler (PREPWM)	$002C_{16}$	X X X X X X X X
(46)	PWM register (PWM)	$002D_{16}$	X X X X X X X X
(47)	Baud rate generator 3 (BRG3)	$002F_{16}$	X X X X X X X X
(48)	Transmit/Receive buffer register 3 (TB3/RB3)	0030_{16}	X X X X X X X X
(49)	Serial I/O3 status register (SIO3STS)	0031_{16}	1 0 0 0 0 0 0 0
(50)	Serial I/O3 control register (SIO3CON)	0032_{16}	00_{16}
(51)	UART3 control register (SIO3CON)	0033_{16}	1 1 1 0 0 0 0 0
(52)	AD/DA control register (ADCON)	0034_{16}	0 0 0 0 1 0 0 0
(53)	A-D conversion register 1 (AD1)	0035_{16}	X X X X X X X X
(54)	D-A1 conversion register (DA1)	0036_{16}	00_{16}
(55)	D-A2 conversion register (DA2)	0037_{16}	00_{16}
(56)	A-D conversion register 2 (AD2)	0038_{16}	0 0 0 0 0 0 X X
(57)	Interrupt source selection register (INTSEL)	0039_{16}	00_{16}
(58)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(59)	CPU mode register (CPUM)	$003B_{16}$	0 1 0 0 1 0 0 0
(60)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(61)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(62)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(63)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(64)	Port P0 pull-up control register (PULL0)	$0FF0_{16}$	00_{16}
(65)	Port P1 pull-up control register (PULL1)	$0FF1_{16}$	00_{16}
(66)	Port P2 pull-up control register (PULL2)	$0FF2_{16}$	00_{16}
(67)	Port P3 pull-up control register (PULL3)	$0FF3_{16}$	00_{16}
(68)	Port P4 pull-up control register (PULL4)	$0FF4_{16}$	00_{16}
(69)	Port P5 pull-up control register (PULL5)	$0FF5_{16}$	00_{16}
(70)	Port P6 pull-up control register (PULL6)	$0FF6_{16}$	00_{16}
(71)	I^2C slave address register 0 (S0D0)	$0FF7_{16}$	00_{16}
(72)	I^2C slave address register 1 (S0D1)	$0FF8_{16}$	00_{16}
(73)	I^2C slave address register 2 (S0D3)	$0FF9_{16}$	00_{16}
(74)	Flash memory control register (FCON)	$0FFE_{16}$	00_{16}
(75)	Flash command register (FCMD)	$0FFF_{16}$	00_{16}
(76)	Processor status register	(PS)	X X X X X 1 X X
(77)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

Note : X : Not fixed
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 81 Internal status at reset (3804 group)

CLOCK GENERATING CIRCUIT

The 3803/3804 group has two built-in oscillation circuits: main clock XIN-XOUT oscillation circuit and sub clock XCIN-XCOUT oscillation circuit. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.
Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency Control
(1) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset is released, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

(4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1." When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.

Oscillation Control
(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. When the oscillation stabilizing time set after STP instruction released bit is "0," the prescaler 12 is set to "FF16" and timer 1 is set to "0116." When the oscillation stabilizing time set after STP instruction released bit is "1," set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.
After STP instruction is released, the input of the prescaler 12 is connected to count source which had set at executing the STP instruction, and the output of the prescaler 12 is connected to timer 1. Set the timer 1 interrupt enable bit to disabled ("0") before executing the STP instruction. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock ϕ is supplied for the first time, when timer 1 underflows. Therefore make sure not to set the timer 1 interrupt request bit to "1" before the STP instruction stops the oscillator. When the oscillator is restarted by reset, apply "L" level to the $\overline{\text{RESET}}$ pin until the oscillation is stable since a wait time will not be generated.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

■Note

- If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3f(XCIN).
- When using the quartz-crystal oscillator of high frequency, such as 16 MHz etc., it may be necessary to select a specific oscillator with the specification demanded.

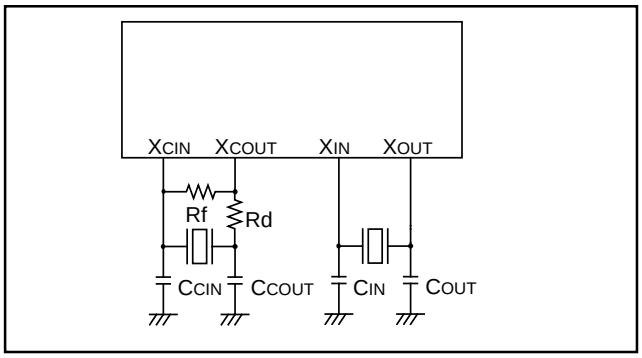


Fig. 82 Ceramic resonator circuit

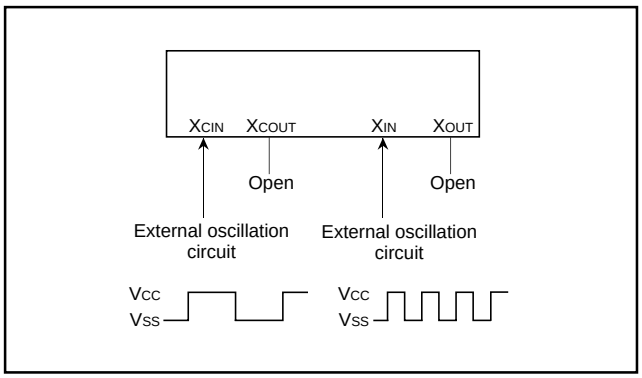
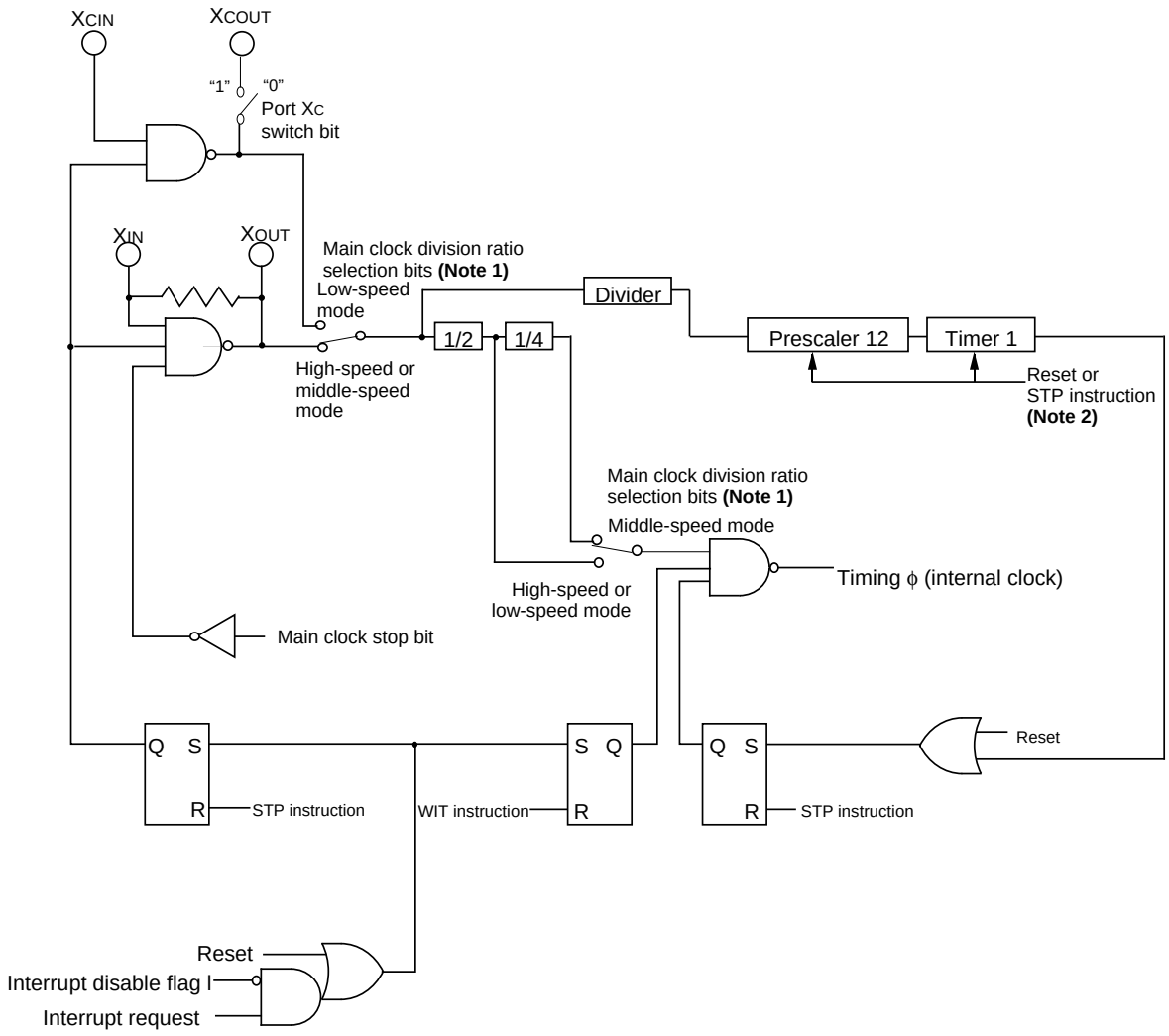


Fig. 83 External clock input circuit

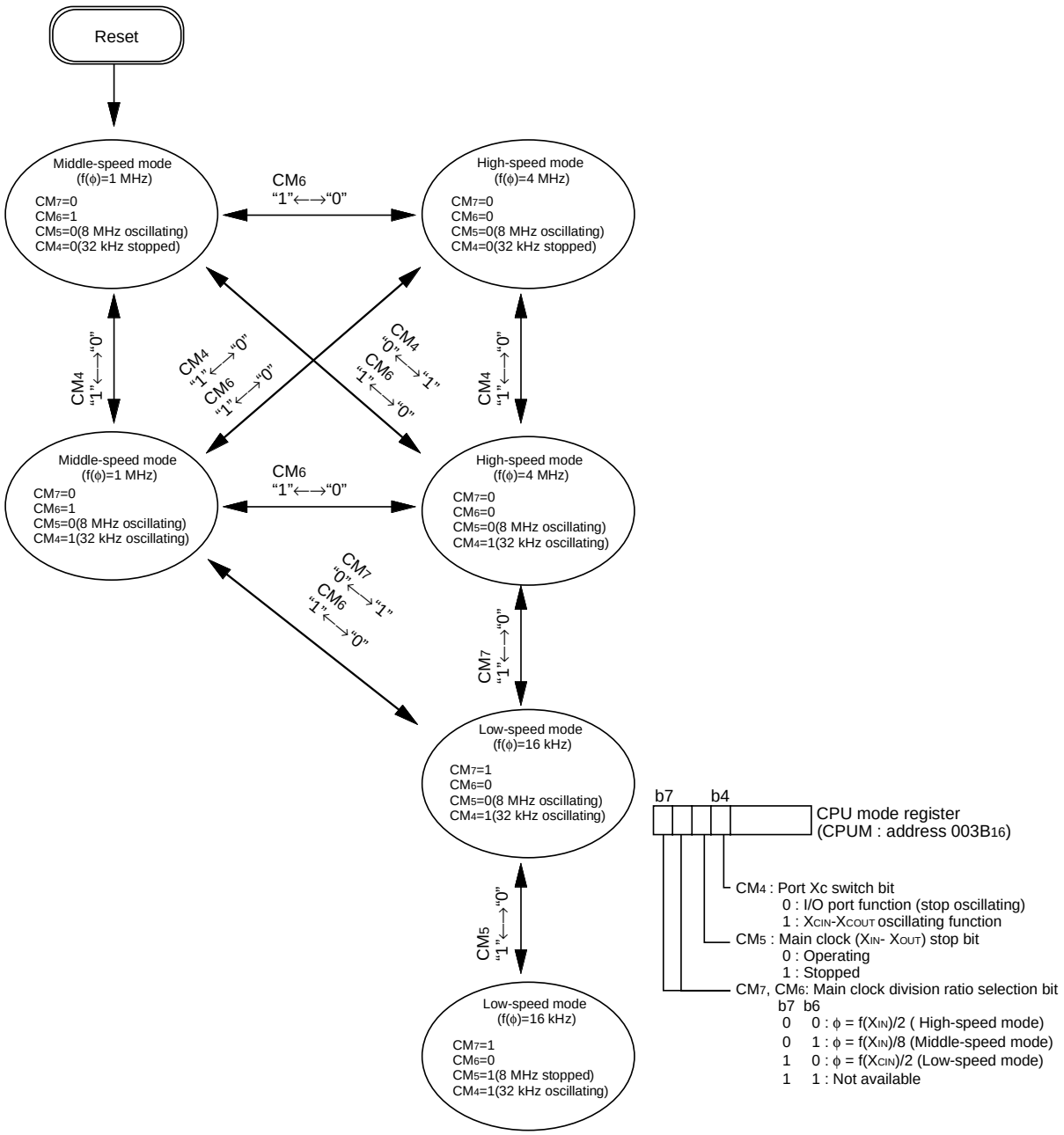


Notes 1: Either high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of the CPU mode register. When low-speed mode is selected, set port Xc switch bit (b4) to "1".

2: f(XIN)/16 is supplied as the count source to the prescaler 12 at reset. The count source before executing the STP instruction is supplied as the count source at executing STP instruction.

3: When bit 0 of MISRG is "0", timer 1 is set "01_{16}" and prescaler 12 is set "FF_{16}" automatically. When bit 0 of MISRG is "1", set the appropriate value to them in accordance with oscillation stabilizing time required by the using oscillator because nothing is automatically set into timer 1 and prescaler 12.

Fig. 84 System clock generating circuit block diagram (Single-chip mode)



Notes
1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the modes directly without an allow.)
2 : The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
3 : Timer operates in the wait mode.
4 : When the stop mode is ended, a delay of approximately 1 ms occurs by connecting prescaler 12 and Timer 1 in middle/high-speed mode.
5 : When the stop mode is ended, a delay of approximately 0.25 s occurs by Timer 1 and Timer 2 in low-speed mode.
6 : Wait until oscillation stabilizes after oscillating the main clock XIN before the switching from the low-speed mode to middle/high-speed mode.
7 : The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. ϕ indicates the internal clock.

Fig. 85 State transitions of system clock

FLASH MEMORY MODE

The 3803/3804 group has the flash memory mode in addition to the normal operation mode (microcomputer mode). The user can use this mode to perform read, program, and erase operations for the internal flash memory.

The 3803/3804 group has three modes the user can choose: the parallel input/output and serial input/output mode, where the flash memory is handled by using the external programmer, and the CPU reprogramming mode, where the flash memory is handled by the central processing unit (CPU). The following explains these modes.

(1) Flash memory mode 1 (parallel I/O mode)

The parallel I/O mode can be selected by connecting wires as shown in Figures 86, 87 and supplying power to the V_{CC} and V_{PP} pins. In this mode, the M38039FF/M38049FF operates as an equivalent of MITSUBISHI's CMOS flash memory M5M28F101. However, because the M38039FF/M38049FF's internal memory has a capacity of 60 Kbytes, programming is available for addresses 01000_{16} to $0FFFF_{16}$, and make sure that the data in addresses 00000_{16} to $00FFF_{16}$ and addresses 10000_{16} to $1FFFF_{16}$ are FF_{16}. Note also that the M38039FF/M38049FF does not contain a facility to read out a device identification code by applying a high voltage to address input (A9). Be careful not to erratically set program conditions when using a general-purpose PROM programmer.

Table 16 shows the pin assignments when operating in the parallel input/output mode.

Table 16 Pin assignments of M38039FF/M38049FF when operating in the parallel input/output mode

	M38039FF/M38049FF	M5M28F101
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV$_{SS}$	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, P1, P3$_1$	A_0–A_{16}
Data I/O	Port P2	D_0–D_7
$\overline{CE}$	P3$_6$	$\overline{CE}$
$\overline{OE}$	P3$_7$	$\overline{OE}$
$\overline{WE}$	P3$_3$	$\overline{WE}$

Functional Outline (parallel input/output mode)

In the parallel input/output mode, the 3803/3804 group allow the user to choose an operation mode between the read-only mode and the read/write mode (software command control mode) depending on the voltage applied to the V_{PP} pin. When $V_{PP} = V_{PP}L$, the read-only mode is selected, and the user can choose one of three states (e.g., read, output disable, or standby) depending on inputs to the $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ pins. When $V_{PP} = V_{PP}H$, the read/write mode is selected, and the user can choose one of four states (e.g., read, output disable, standby, or write) depending on inputs to the $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ pins. Table 17 shows assignment states of control input and each state.

● Read

The microcomputer enters the read state by driving the $\overline{CE}$, and $\overline{OE}$ pins low and the $\overline{WE}$ pin high; and the contents of memory corresponding to the address to be input to address input pins (A_0–A_{16}) are output to the data input/output pins (D_0–D_7).

● Output disable

The microcomputer enters the output disable state by driving the $\overline{CE}$ pin low and the $\overline{WE}$ and $\overline{OE}$ pins high; and the data input/output pins enter the floating state.

● Standby

The microcomputer enters the standby state by driving the $\overline{CE}$ pin high. the 3803/3804 group is placed in a power-down state consuming only a minimum supply current. At this time, the data input/output pins enter the floating state.

● Write

The microcomputer enters the write state by driving the V_{PP} pin high ($V_{PP} = V_{PP}H$) and then the $\overline{WE}$ pin low when the $\overline{CE}$ pin is low and the $\overline{OE}$ pin is high. In this state, software commands can be input from the data input/output pins, and the user can choose program or erase operation depending on the contents of this software command.

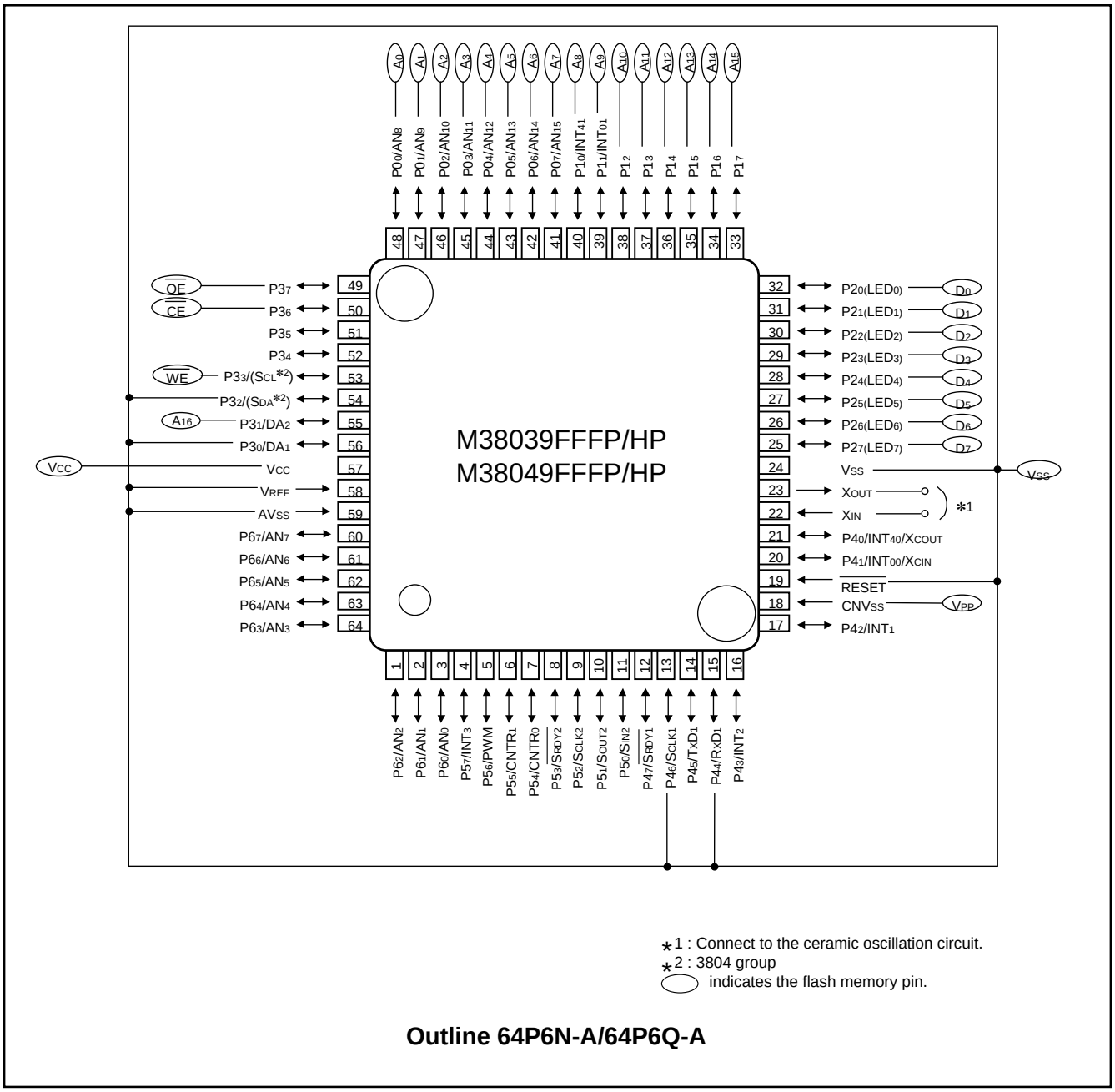
Table 17 Assignment states of control input and each state

Mode \ Pin / State		$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	Data I/O
Read-only	Read	V_{IL}	V_{IL}	V_{IH}	$V_{PP}L$	Output
	Output disable	V_{IL}	V_{IH}	V_{IH}	$V_{PP}L$	Floating
	Standby	V_{IH}	×	×	$V_{PP}L$	Floating
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	$V_{PP}H$	Output
	Output disable	V_{IL}	V_{IH}	V_{IH}	$V_{PP}H$	Floating
	Standby	V_{IH}	×	×	$V_{PP}H$	Floating
	Write	V_{IL}	V_{IH}	V_{IL}	$V_{PP}H$	Input

Note: × can be V_{IL} or V_{IH}.

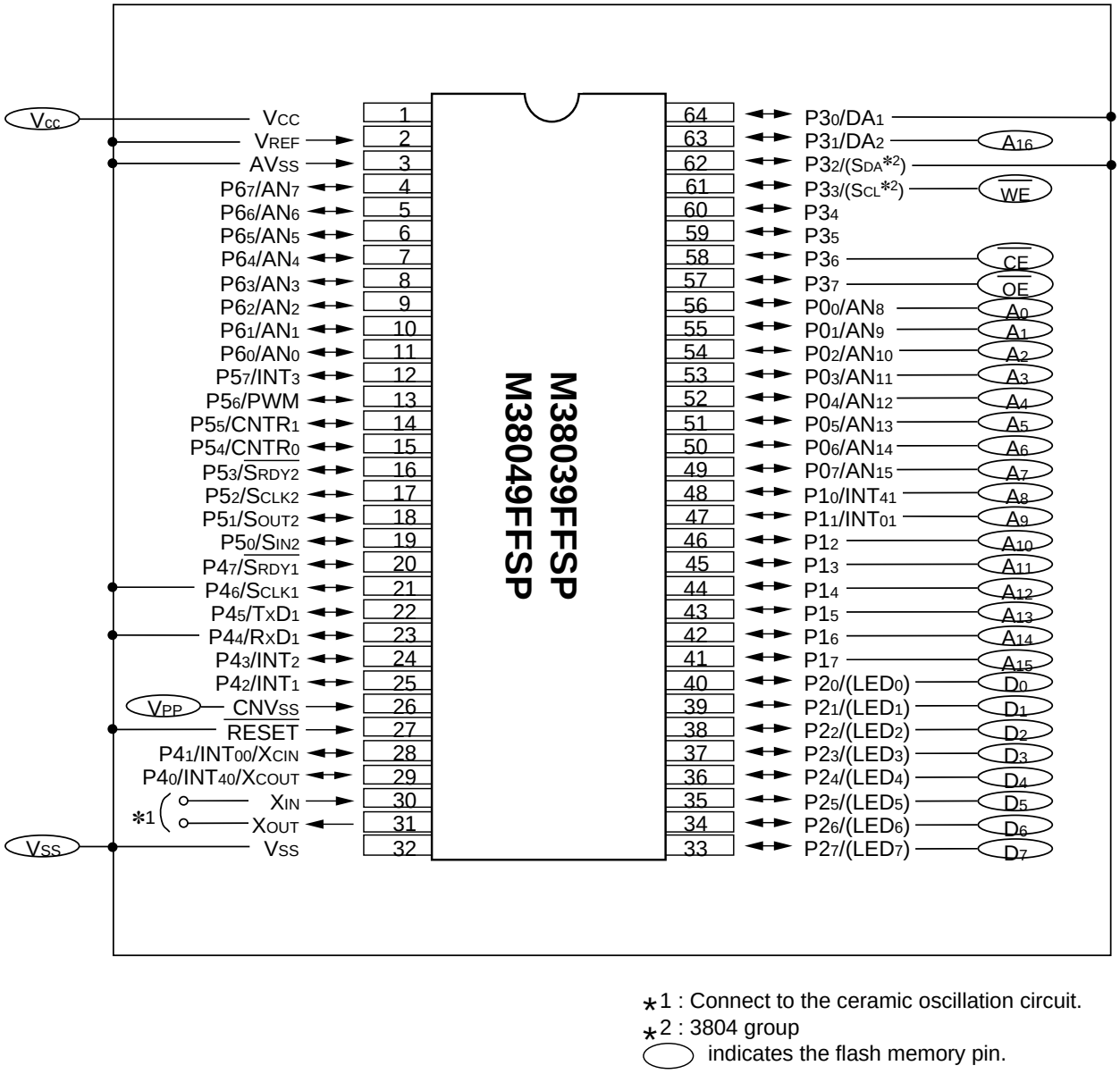
Table 18 Pin description (flash memory parallel I/O mode)

Pin	Name	Input /Output	Functions
V_{CC}, V_{SS}	Power supply	—	Supply 5 V ± 10 % to V_{CC} and 0 V to V_{SS}.
CNV$_{SS}$	V_{PP} input	Input	Supply 5 V ± 10 % in read-only mode, supply 11.7 V to 12.6 V in read/write mode.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}.
X_{IN}	Clock input	Input	Connect a ceramic resonator between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
AV$_{SS}$	Analog supply input	—	Connect to V_{SS}.
V_{REF}	Reference voltage input	Input	Connect to V_{SS}.
P0$_0$–P0$_7$	Address input (A$_0$–A$_7$)	Input	Port P0 functions as 8-bit address input (A$_0$–A$_7$).
P1$_0$–P1$_7$	Address input (A$_8$–A$_{15}$)	Input	Port P1 functions as 8-bit address input (A$_8$–A$_{15}$).
P2$_0$–P2$_7$	Data I/O (D$_0$–D$_7$)	I/O	Function as 8-bit data's I/O pins (D$_0$–D$_7$).
P3$_0$–P3$_7$	Control signal input	Input	P3$_7$, P3$_6$ and P3$_3$ function as the $\overline{OE}$, $\overline{CE}$ and $\overline{WE}$ input pins respectively. P3$_1$ functions as the A$_{16}$ input pin. Connect P3$_0$ and P3$_2$ to V_{SS}. Input "H" or "L" to P3$_4$, P3$_5$, or keep them open.
P4$_0$–P4$_7$	Input port P4	Input	Connect P4$_4$, P4$_6$ to V_{SS}. Input "H" or "L" to P4$_0$ - P4$_3$, P4$_5$, P4$_7$, or keep them open.
P5$_0$–P5$_7$	Input port P5	Input	Input "H" or "L", or keep them open.
P6$_0$–P6$_7$	Input port P6	Input	Input "H" or "L", or keep them open.



Outline 64P6N-A/64P6Q-A

Fig. 86 Pin connectionwhen operating in parallel input/output mode (M38039FFFP/HP, M38049FFFP/HP)



Outline 64P4B

Fig. 87 Pin connection when operating in parallel input/output mode (M38039FFSP, M38049FFSP)

Read-only Mode

The microcomputer enters the read-only mode by applying $V_{PP}L$ to the V_{PP} pin. In this mode, the user can input the address of a memory location to be read and the control signals at the timing shown in Figure 88, and the M38039FF/M38049FF will output the contents of the user's specified address from data I/O pin to the external. In this mode, the user cannot perform any operation other than read.

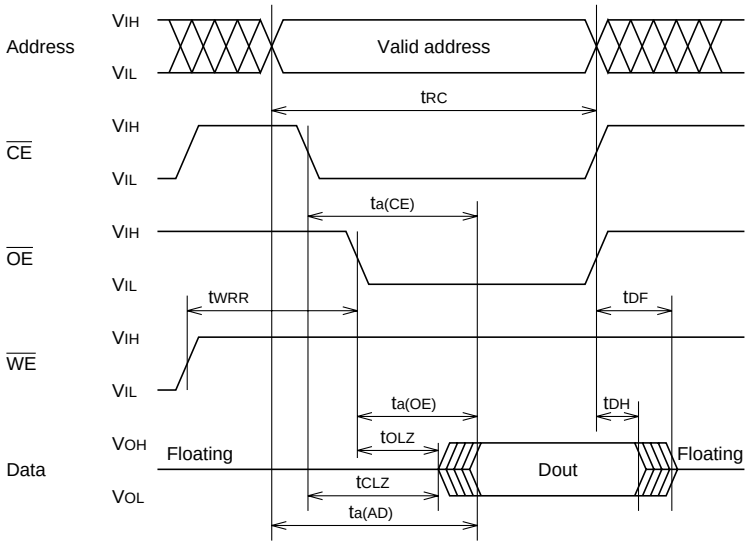


Fig. 88 Read timing

Read/Write Mode

The microcomputer enters the read/write mode by applying $V_{PP}H$ to the V_{PP} pin. In this mode, the user must first input a software command to choose the operation (e. g., read, program, or erase) to be performed on the flash memory (this is called the first cycle), and then input the information necessary for execution of the command (e.g, address and data) and control signals (this is called the second cycle). When this is done, the M38039FF/M38049FF executes the specified operation.

Table 19 shows the software commands and the input/output information in the first and the second cycles. The input address is latched internally at the falling edge of the $\overline{WE}$ input; software commands and other input data are latched internally at the rising edge of the $\overline{WE}$ input.

The following explains each software command. Refer to Figures 89 to 91 for details about the signal input/output timings.

Table 19 Software command (Parallel input/output mode)

Symbol	First cycle		Second cycle	
	Address input	Data input	Address input	Data I/O
Read	×	00_{16}	Read address	Read data (Output)
Program	×	40_{16}	Program address	Program data (Input)
Program verify	×	$C0_{16}$	×	Verify data (Output)
Erase	×	20_{16}	×	20_{16} (Input)
Erase verify	Verify address	$A0_{16}$	×	Verify data (Output)
Reset	×	FF_{16}	×	FF_{16} (Input)
Device identification	×	90_{16}	ADI	DDI (Output)

Note: ADI = Device identification address : manufacturer's code 00000_{16}, device code 00001_{16}
DDI = Device identification data : manufacturer's code $1C_{16}$, device code $D0_{16}$
X can be V_{IL} or V_{IH}.

● **Read command**

The microcomputer enters the read mode by inputting command code "00_{16}" in the first cycle. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. When the address of a memory location to be read is input in the second cycle, with control signals input at the timing shown in Figure 89, the M38039FF/M38049FF outputs the contents of the specified address from the data I/O pins to the external.

The read mode is retained until any other command is latched into the command latch. Consequently, once the M38039FF/M38049FF enters the read mode, the user can read out the successive memory contents simply by changing the input address and executing the second cycle only. Any command other than the read command must be input beginning from its command code over again each time the user execute it. The contents of the command latch immediately after power-on is 00_{16}.

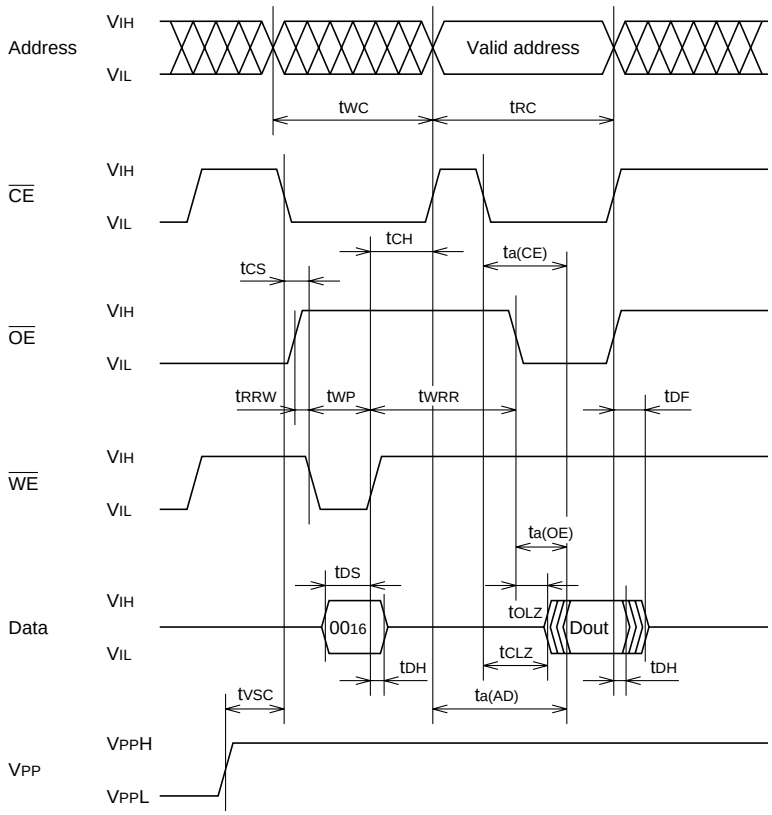


Fig. 89 Timings during reading

● **Program command**

The microcomputer enters the program mode by inputting command code "40_{16}" in the first cycle. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. When the address which indicates a program location and data is input in the second cycle, the M38039FF/M38049FF internally latches the address at the falling edge of the $\overline{WE}$ input and the data at the rising edge of the $\overline{WE}$ input. The M38039FF/M38049FF starts programming at the rising edge of the $\overline{WE}$ input in the second cycle and finishes programming within 10 µs as measured by its internal timer. Programming is performed in units of bytes.

Note: A programming operation is not completed by executing the program command once. Always be sure to execute a program verify command after executing the program command. When the failure is found in this verification, the user must repeatedly execute the program command until the pass. Refer to Figure 92 for the programming flowchart.

● **Program verify command**

The microcomputer enters the program verify mode by inputting command code "$C0_{16}$" in the first cycle. This command is used to verify the programmed data after executing the program command. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. When control signals are input in the second cycle at the timing shown in Figure 90, the M38039FF/M38049FF outputs the programmed address's contents to the external. Since the address is internally latched when the program command is executed, there is no need to input it in the second cycle.

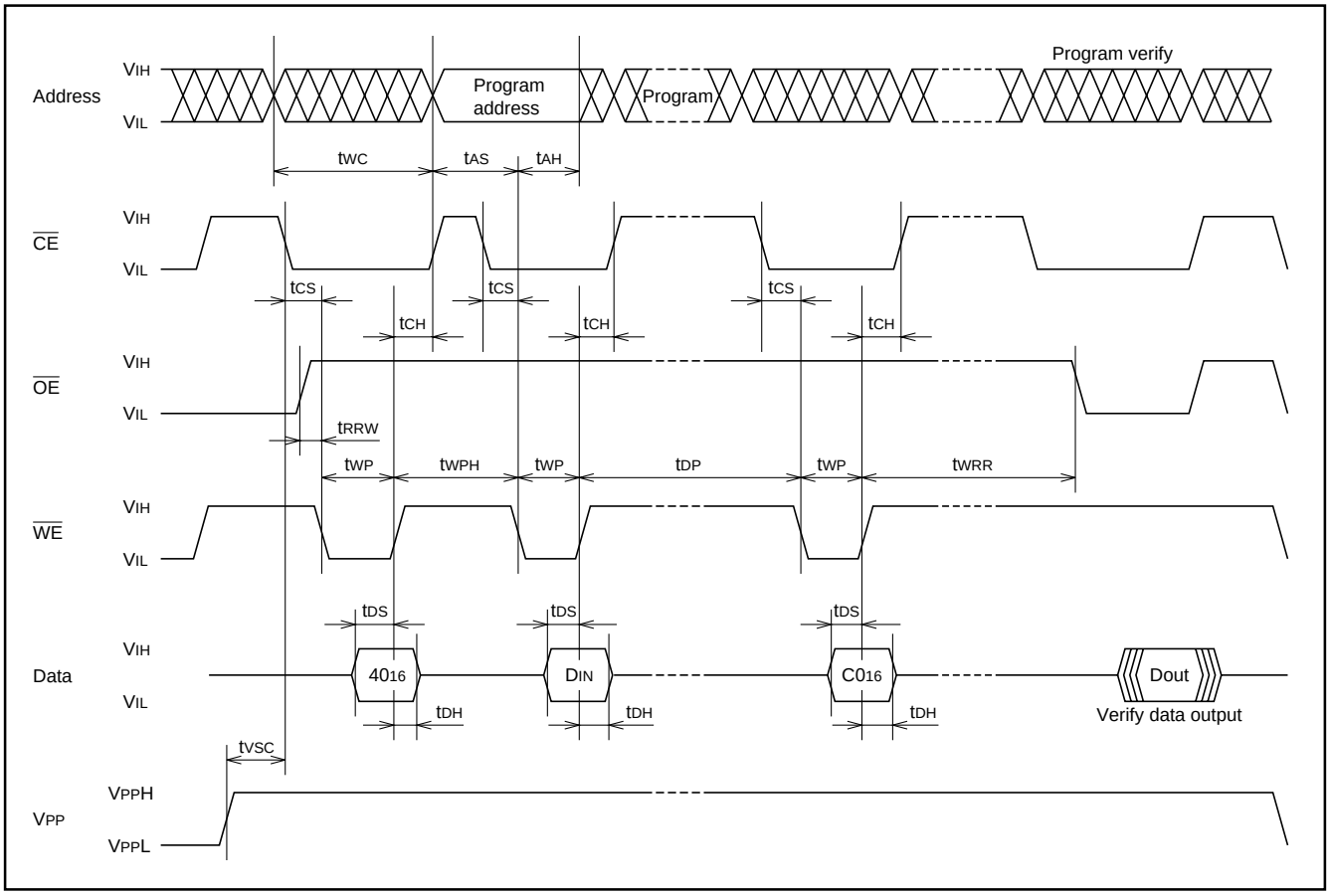


Fig. 90 Input/output timings during programming (Verify data is output at the same timing as for read.)

● **Erase command**

The erase command is executed by inputting command code 20_{16} in the first cycle and command code 20_{16} again in the second cycle. The command code is latched into the internal command latch at the rising edges of the $\overline{WE}$ input in the first cycle and in the second cycle, respectively. The erase operation is initiated at the rising edge of the $\overline{WE}$ input in the second cycle, and the memory contents are collectively erased within 9.5 ms as measured by the internal timer. Note that data 00_{16} must be written to all memory locations before executing the erase command.

Note: An erase operation is not completed by executing the erase command once. Always be sure to execute an erase verify command after executing the erase command. When the failure is found in this verification, the user must repeatedly execute the erase command until the pass. Refer to Figure 92 for the erase flowchart.

● **Erase verify command**

The user must verify the contents of all addresses after completing the erase command. The microcomputer enters the erase verify mode by inputting the verify address and command code $A0_{16}$ in the first cycle. The address is internally latched at the falling edge of the $\overline{WE}$ input, and the command code is internally latched at the rising edge of the $\overline{WE}$ input. When control signals are input in the second cycle at the timing shown in Figure 91, the M38039FF/M38049FF outputs the contents of the specified address to the external.

Note: If any memory location where the contents have not been erased is found in the erase verify operation, execute the operation of "erase → erase verify" over again. In this case, however, the user does not need to write data 00_{16} to memory locations before erasing.

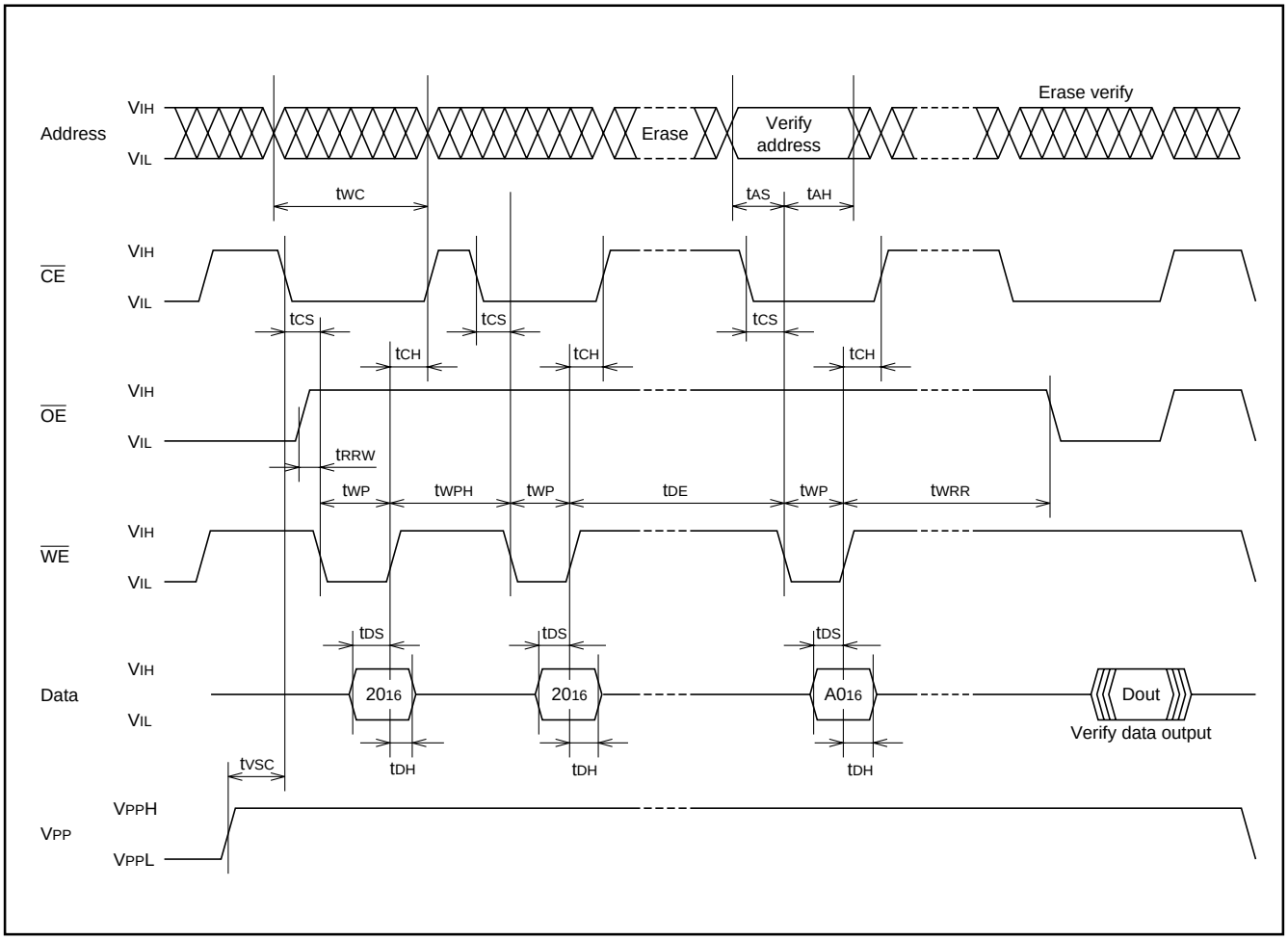


Fig. 91 Input/output timings during erasing (Verify data is output at the same timing as for read.)

● **Reset command**

The reset command provides a means of stopping execution of the erase or program command safely. If the user inputs command code FF_{16} in the second cycle after inputting the erase or program command in the first cycle and again input command code FF_{16} in the third cycle, the erase or program command is disabled (i.e., reset), and the 3803/3804 group is placed in the read mode. If the reset command is executed, the contents of the memory does not change.

● **Device identification code command**

By inputting command code 90_{16} in the first cycle, the user can read out the device identification code. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. At this time, the user can read out manufacture's code $1C_{16}$ (i.e., MITSUBISHI) by inputting 00000_{16} to the address input pins in the second cycle; the user can read out device code $D0_{16}$ (i. e., 1M-bit flash memory) by inputting 00001_{16}.

These command and data codes are input/output at the same timing as for read.

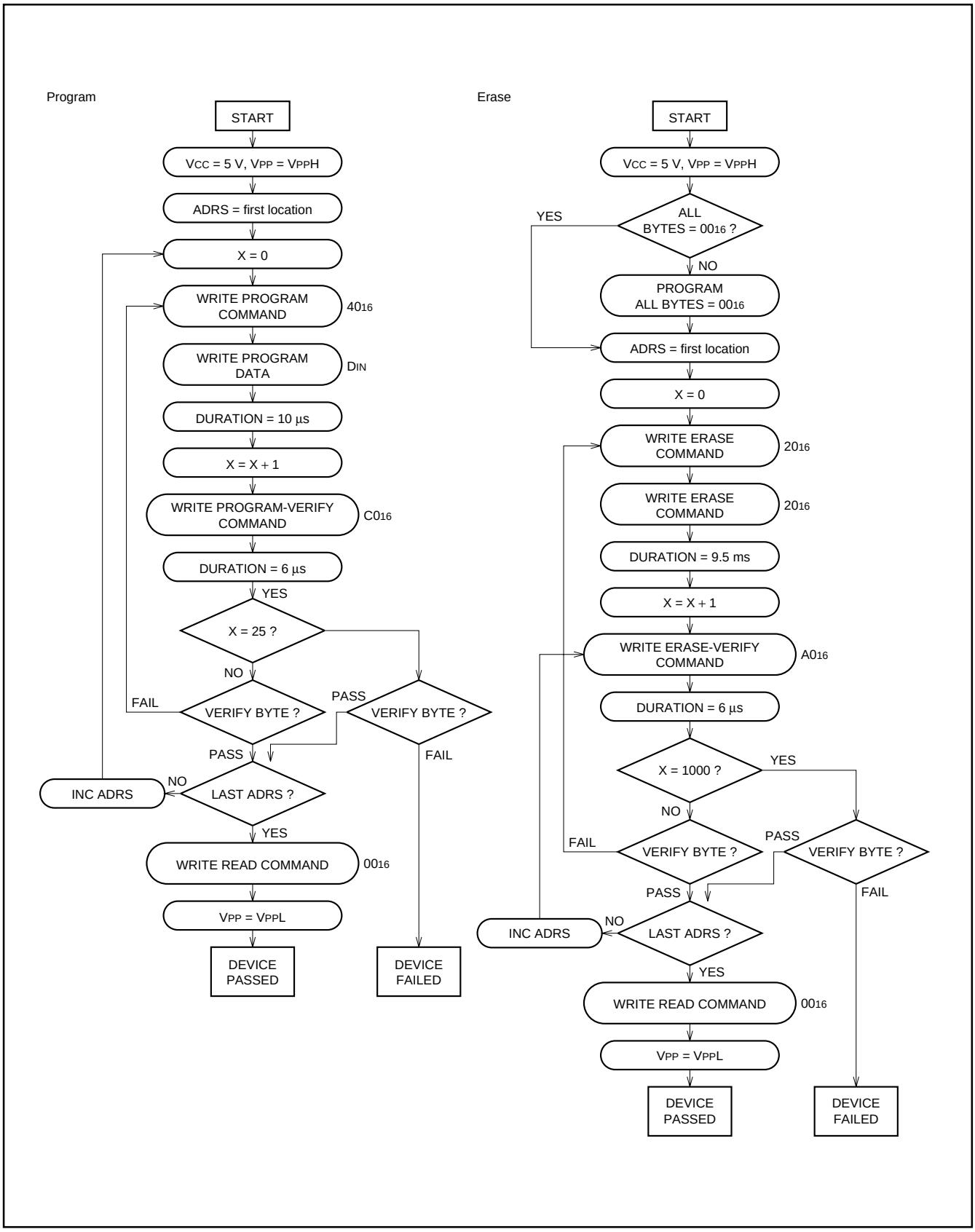


Fig. 92 Programming/Erasing algorithm flow chart

Table 20 DC ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{SB1}	V_{CC} supply current (at standby)	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IH}			1	mA
I_{SB2}		V_{CC} = 5.5 V, $\overline{CE}$ = V_{CC} ± 0.2 V			100	µA
I_{CC1}	V_{CC} supply current (at read)	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IL}, t_{RC} = 150 ns, I_{OUT} = 0 mA			15	mA
I_{CC2}	V_{CC} supply current (at program)	V_{PP} = V_{PPH}			15	mA
I_{CC3}	V_{CC} supply current (at erase)	V_{PP} = V_{PPH}			15	mA
I_{PP1}	V_{PP} supply current (at read)	0≤V_{PP}≤V_{CC}			10	µA
		V_{CC}<V_{PP}≤V_{CC} + 1.0 V			100	µA
		V_{PP} = V_{PPH}			100	µA
I_{PP2}	V_{PP} supply current (at program)	V_{PP} = V_{PPH}			30	mA
I_{PP3}	V_{PP} supply current (at erase)	V_{PP} = V_{PPH}			30	mA
V_{IL}	“L” input voltage		0		0.8	V
V_{IH}	“H” input voltage		2.0		V_{CC}	V
V_{OL}	“L” output voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	“H” output voltage	I_{OH} = –400 µA	2.4			V
V_{OH2}		I_{OH} = –100 µA	V_{CC} –0.4			V
V_{PPL}	V_{PP} supply voltage (read only)		V_{CC}		V_{CC} + 1.0	V
V_{PPH}	V_{PP} supply voltage (read/write)		11.7	12.0	12.6	V

AC ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = 5 V ± 10 %, unless otherwise noted)

Table 21 Read-only mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{RC}	Read cycle time	150		ns
$t_{a(AD)}$	Address access time		150	ns
$t_{a(CE)}$	$\overline{CE}$ access time		150	ns
$t_{a(OE)}$	$\overline{OE}$ access time		55	ns
t_{CLZ}	Output enable time (after $\overline{CE}$)	0		ns
t_{OLZ}	Output enable time (after $\overline{OE}$)	0		ns
t_{DF}	Output floating time (after $\overline{OE}$)		35	ns
t_{DH}	Output valid time (after $\overline{CE}$, $\overline{OE}$, address)	0		ns
t_{WRR}	Write recovery time (before read)	6		µs

Table 22 Read/Write mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{WC}	Write cycle time	150		ns
t_{AS}	Address set up time	0		ns
t_{AH}	Address hold time	60		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	10		ns
t_{WRR}	Write recovery time (before read)	6		µs
t_{RRW}	Read recovery time (before write)	0		µs
t_{CS}	$\overline{CE}$ setup time	20		ns
t_{CH}	$\overline{CE}$ hold time	0		ns
t_{WP}	Write pulse width	60		ns
t_{WPH}	Write pulse waiting time	20		ns
t_{DP}	Program time	10		µs
t_{DE}	Erase time	9.5		ms
t_{VSC}	V_{PP} setup time	1		µs

Note: Read timing of Read/Write mode is same as Read-only mode.

(2) Flash memory mode 2 (serial I/O mode)

The flash memory version of the 3803/3804 group has a function to serially input/output the software commands, addresses, and data required for operation on the internal flash memory (e. g., read, program, and erase) using only a few pins. This is called the serial I/O (input/output) mode. This mode can be selected by driving the SDA (serial data input/output), SCLK (serial clock input), and $\overline{OE}$ pins high after connecting wires as shown in Figures 93, 94 and powering on the V_{CC} pin and then applying $V_{PP}H$ to the V_{PP} pin.

In the serial I/O mode, the user can use six types of software commands: read, program, program verify, erase, erase verify and error check.

Serial input/output is accomplished synchronously with the clock, beginning from the LSB (LSB first).

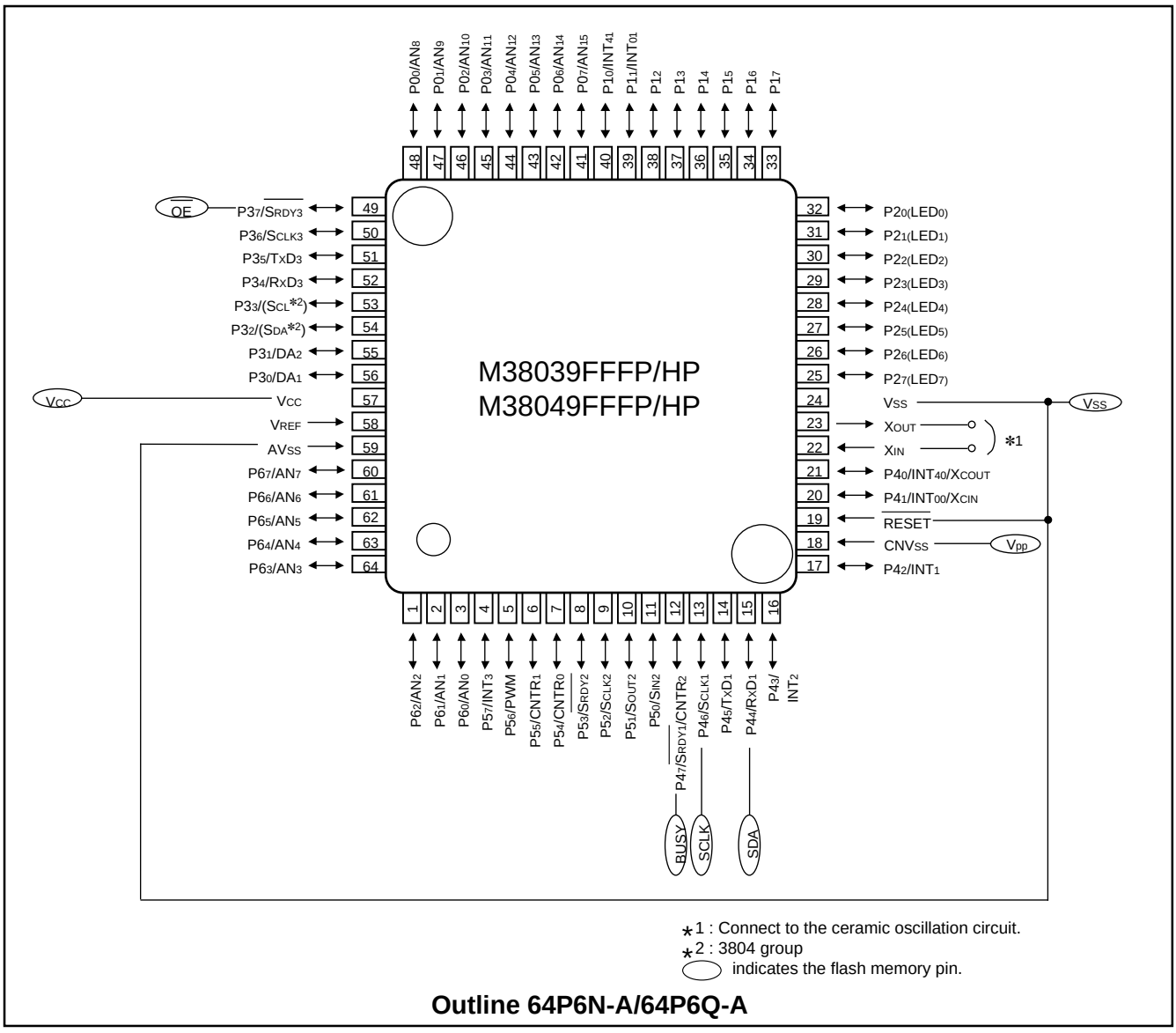
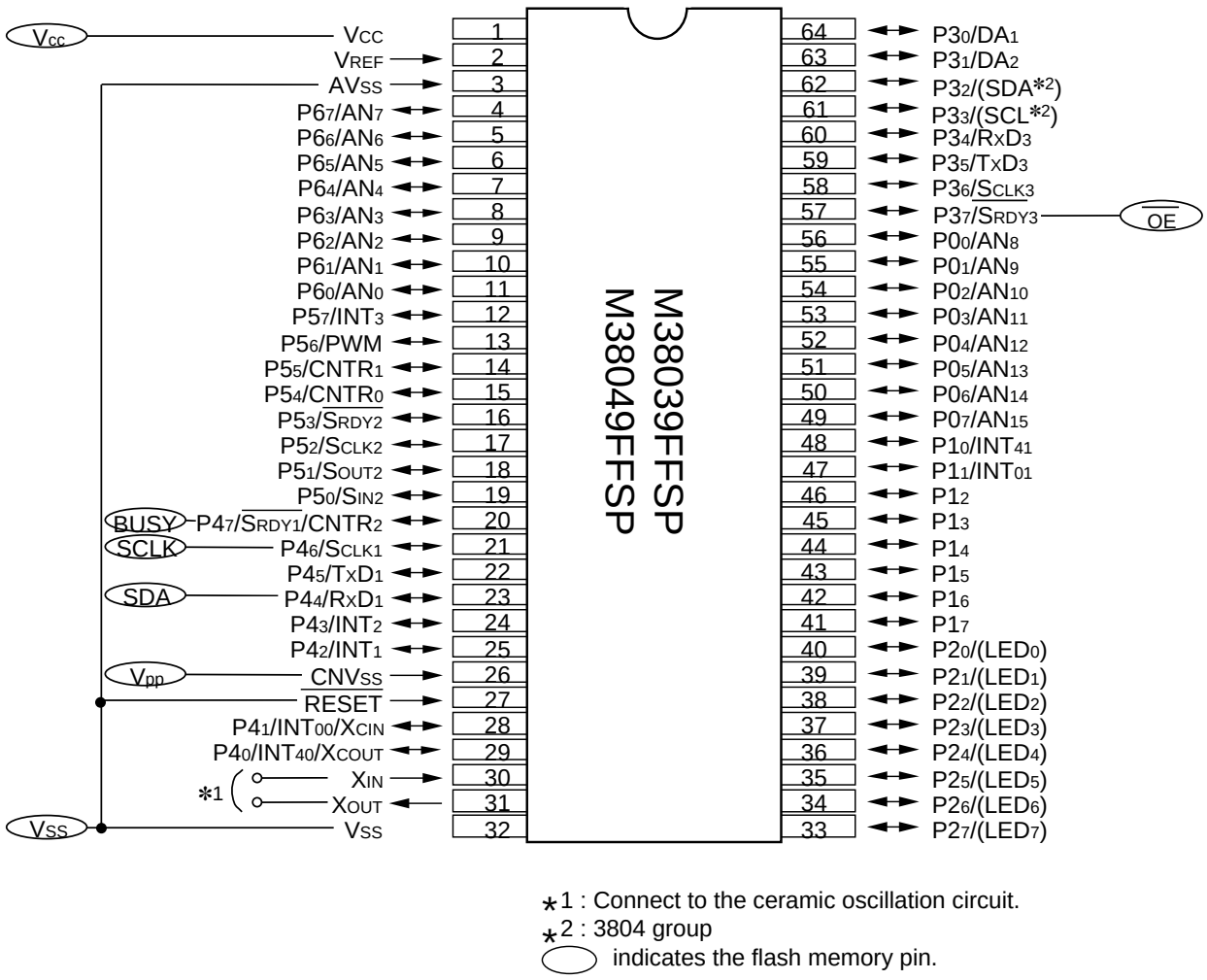


Fig. 93 Pin connection when operating in serial I/O mode (M38039FFFP/HP, M38049FFFP/HP)



*1 : Connect to the ceramic oscillation circuit.
*2 : 3804 group
( ) indicates the flash memory pin.

Outline 64P4B

Fig. 94 Pin connection when operating in serial I/O mode (M38039FFSP, M38049FFSP)

Table 23 Pin description (flash memory serial I/O mode)

Pin	Name	Input /Output	Functions
V_{CC}, V_{SS}	Power supply	—	Supply 5 V ± 10 % to V_{CC} and 0 V to V_{SS}.
CNV$_{SS}$	V_{PP} input	Input	Supply 11.7 V to 12.6 V.
$\overline{\text{RESET}}$	Reset input	Input	Connect to V_{SS}.
X_{IN}	Clock input	Input	Connect a ceramic resonator between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
AV$_{SS}$	Analog supply input	—	Connect to V_{SS}.
V_{REF}	Reference voltage input	Input	Input an arbitrary level between the range of V_{SS} and V_{CC}.
$P0_0$–$P0_7$	Input port P0	Input	Input “H” or “L”, or keep them open.
$P1_0$–$P1_7$	Input port P1	Input	Input “H” or “L”, or keep them open.
$P2_0$–$P2_7$	Input port P2	Input	Input “H” or “L”, or keep them open.
$P3_0$–$P3_6$	Input port P3	Input	Input “H” or “L”, or keep them open.
$P3_7$	Control signal input	Input	$\overline{\text{OE}}$ input pin
$P4_0$–$P4_3$, $P4_5$	Input port P4	Input	Input “H” or “L” to $P4_0$ - $P4_3$, $P4_5$, or keep them open.
$P4_4$	SDA I/O	I/O	This pin is for serial data I/O.
$P4_6$	SCLK input	Input	This pin is for serial clock input.
$P4_7$	BUSY output	Output	This pin is for BUSY signal output.
$P5_0$–$P5_7$	Input port P5	Input	Input “H” or “L”, or keep them open.
$P6_0$–$P6_7$	Input port P6	Input	Input “H” or “L”, or keep them open.

Functional Outline (serial I/O mode)

In the serial I/O mode, data is transferred synchronously with the clock using serial input/output. The input data is read from the SDA pin into the internal circuit synchronously with the rising edge of the serial clock pulse; the output data is output from the SDA pin synchronously with the falling edge of the serial clock pulse. Data is transferred in units of eight bits.

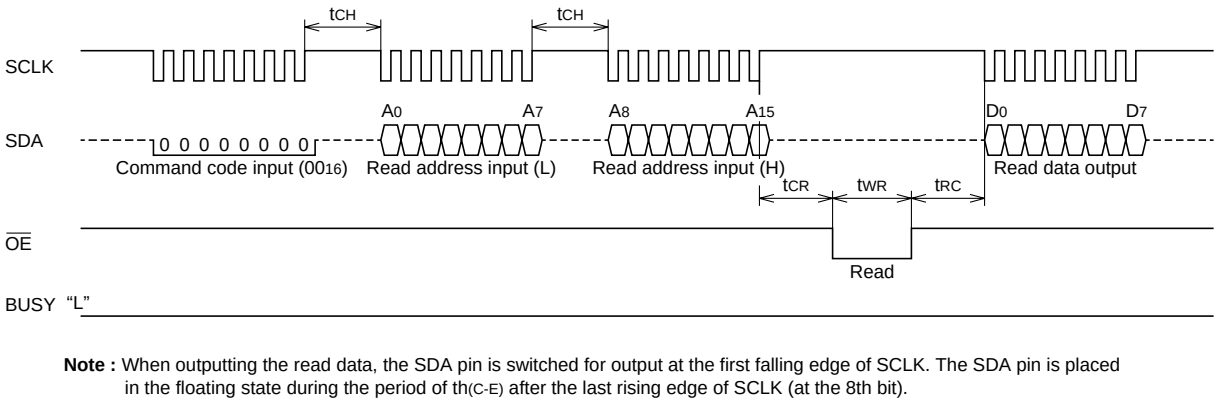
In the first transfer, the user inputs the command code. This is followed by address input and data input/output according to the contents of the command. Table 24 shows the software commands used in the serial I/O mode. The following explains each software command.

Table 24 Software command (serial I/O mode)

Number of transfers / Command	First command code input	Second	Third	Fourth
Read	00_{16}	Read address L (Input)	Read address H (Input)	Read data (Output)
Program	40_{16}	Program address L (Input)	Program address H (Input)	Program data (Input)
Program verify	$C0_{16}$	Verify data (Output)	————	————
Erase	20_{16}	20_{16} (Input)	————	————
Erase verify	$A0_{16}$	Verify address L (Input)	Verify address H (Input)	Verify data (Output)
Error check	80_{16}	Error code (Output)	————	————

● **Read command**

Input command code 00_{16} in the first transfer. Proceed and input the low-order 8 bits and the high-order 8 bits of the address and pull the $\overline{OE}$ pin low. When this is done, the 3803/3804 group reads out the contents of the specified address, and then latchs it into the internal data latch. When the $\overline{OE}$ pin is released back high and serial clock is input to the SCLK pin, the read data that has been latched into the data latch is serially output from the SDA pin.



Note : When outputting the read data, the SDA pin is switched for output at the first falling edge of SCLK. The SDA pin is placed in the floating state during the period of $t_{h(C-E)}$ after the last rising edge of SCLK (at the 8th bit).

Fig. 95 Timings during reading

● **Program command**

Input command code 40$_{16}$ in the first transfer. Proceed and input the low-order 8 bits and the high-order 8 bits of the address and then program data. Programming is initiated at the last rising edge of the serial clock during program data transfer. The BUSY pin is driven high during program operation. Programming is completed within 10 μs as measured by the internal timer, and the BUSY pin is pulled low.

Note : A programming operation is not completed by executing the program command once. Always be sure to execute a program verify command after executing the program command. When the failure is found in the verification, the user must repeatedly execute the program command until the pass in the verification. Refer to Figure 92 for the programming flowchart.

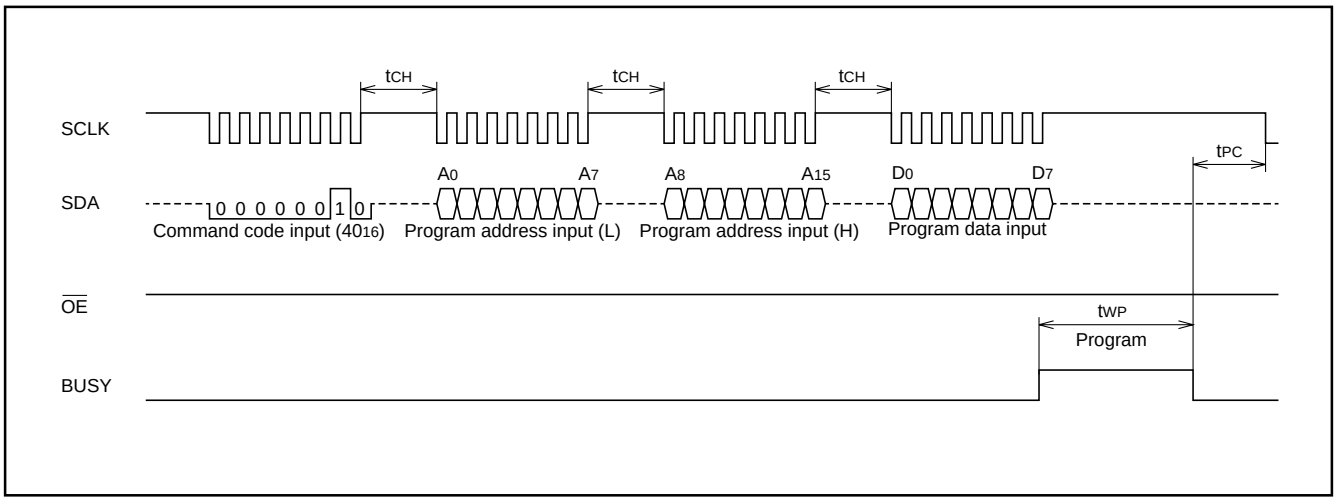
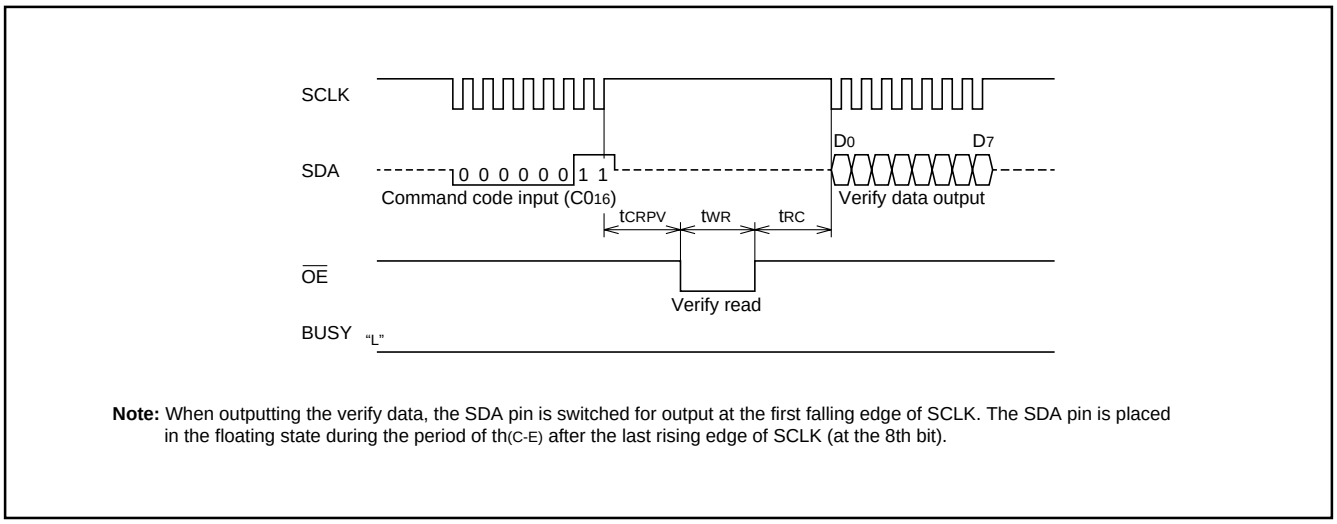


Fig. 96 Timings during programming

● **Program verify command**

Input command code C0$_{16}$ in the first transfer. Proceed and drive the $\overline{OE}$ pin low. When this is done, the 3803/3804 group verify-reads the programmed address's contents, and then latchs it into the internal data latch. When the $\overline{OE}$ pin is released back high and serial clock is input to the SCLK pin, the verify data that has been latched into the data latch is serially output from the SDA pin.



Note: When outputting the verify data, the SDA pin is switched for output at the first falling edge of SCLK. The SDA pin is placed in the floating state during the period of $t_{h(C-E)}$ after the last rising edge of SCLK (at the 8th bit).

Fig. 97 Timings during program verify

● **Erase command**

Input command code 20$_{16}$ in the first transfer and command code 20$_{16}$ again in the second transfer. When this is done, the 3803/3804 group executes an erase command. Erase is initiated at the last rising edge of the serial clock. The BUSY pin is driven high during the erase operation. Erase is completed within 9.5 ms as measured by the internal timer, and the BUSY pin is pulled low. Note that data 00$_{16}$ must be written to all memory locations before executing the erase command.

Note: A erase operation is not completed by executing the erase command once. Always be sure to execute a erase verify command after executing the erase command. When the failure is found in the verification, the user must repeatedly execute the erase command until the pass in the verification. Refer to Figure 92 for the erase flowchart.

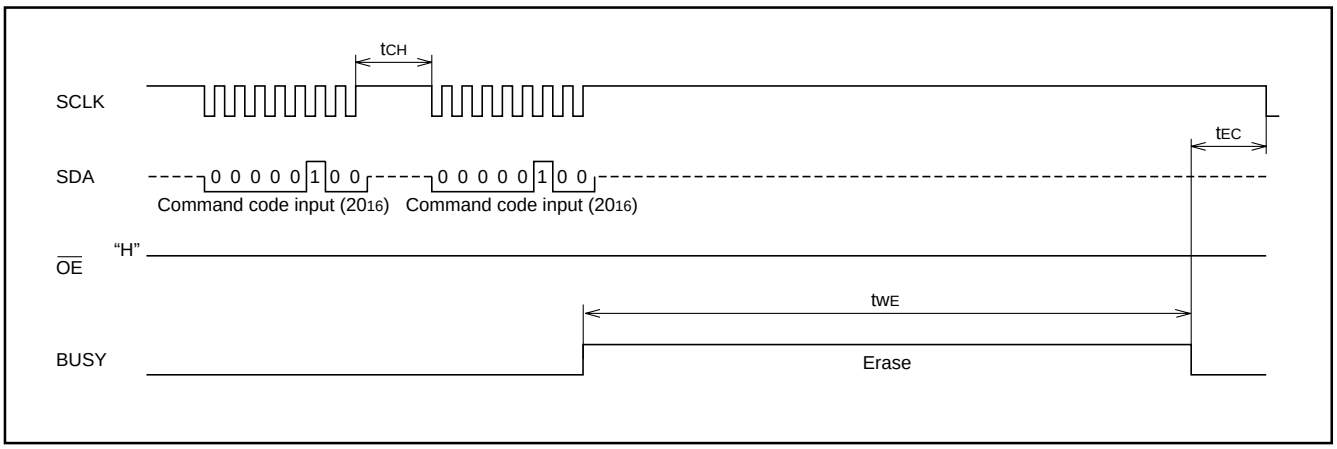
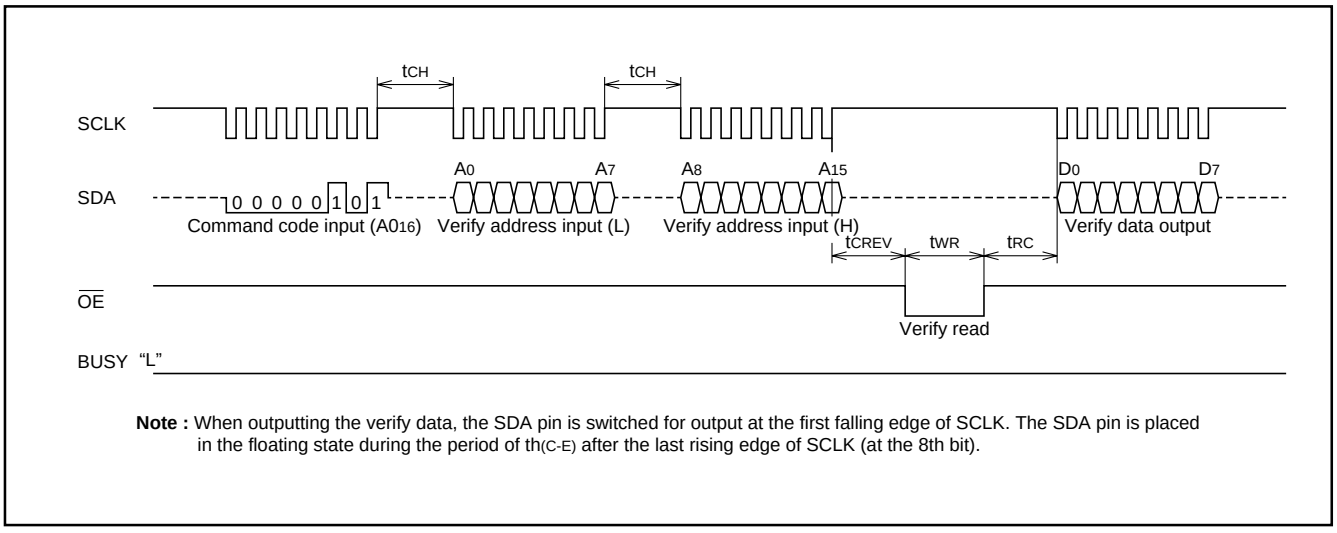


Fig. 98 Timings at erasing

● **Erase verify command**

The user must verify the contents of all addresses after completing the erase command. Input command code A0$_{16}$ in the first transfer. Proceed and input the low-order 8 bits and the high-order 8 bits of the address and pull the $\overline{OE}$ pin low. When this is done, the 3803/3804 group reads out the contents of the specified address, and then latchs it into the internal data latch. When the $\overline{OE}$ pin is released back high and serial clock is input to the SCLK pin, the verify data that has been latched into the data latch is serially output from the SDA pin.

Note: If any memory location where the contents have not been erased is found in the erase verify operation, execute the operation of "erase → erase verify" over again. In this case, however, the user does not need to write data 00$_{16}$ to memory locations before erasing.



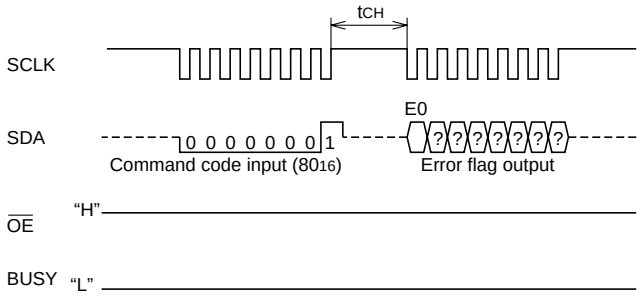
Note : When outputting the verify data, the SDA pin is switched for output at the first falling edge of SCLK. The SDA pin is placed in the floating state during the period of $t_{h(C-E)}$ after the last rising edge of SCLK (at the 8th bit).

Fig. 99 Timings during erase verify

● **Error check command**

Input command code 80_{16} in the first transfer, and the 3803/3804 group outputs error information from the SDA pin, beginning at the next falling edge of the serial clock. If the LSB bit of the 8-bit error information is 1, it indicates that a command error has occurred. A command error means that some invalid commands other than commands shown in Table 24 has been input.

When a command error occurs, the serial communication circuit sets the corresponding flag and stops functioning to avoid an erroneous programming or erase. When being placed in this state, the serial communication circuit does not accept the subsequent serial clock and data (even including an error check command). Therefore, if the user wants to execute an error check command, temporarily drop the V_{PP} pin input to the $V_{PP}L$ level to terminate the serial input/output mode. Then, place the 3803/3804 group into the serial I/O mode back again. The serial communication circuit is reset by this operation and is ready to accept commands. The error flag alone is not cleared by this operation, so the user can examine the serial communication circuit's error conditions before reset. This examination is done by the first execution of an error check command after the reset. The error flag is cleared when the user has executed the error check command. Because the error flag is undefined immediately after power-on, always be sure to execute the error check command.



Note: When outputting the error flag, the SDA pin is switched for output at the first falling edge of the serial clock. The SDA pin is placed in the floating state during the period of $th_{(C-E)}$ after the last rising edge of the serial clock (at the 8th bit).

Fig. 100 Timings at error checking

DC ELECTRICAL CHARACTERISTICS (Ta = 25 °C, VCC = 5 V ± 10 %, VPP = 11.7 V to 12.6 V, unless otherwise noted)

ICC, IPP-relevant standards during read, program, and erase are the same as in the parallel input/output mode. VIH, VIL, VOH, VOL, IIH, and IIL for the SCLK, SDA, BUSY, $\overline{OE}$ pins conform to the microcomputer modes.

Table 25 AC Electrical characteristics
(Ta = 25 °C, VCC = 5 V ± 10 %, VPP = 11.7 V to 12.6 V, f(XIN) = 10 MHz, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tCH	Serial transmission interval	500(Note 1)		ns
tCR	Read waiting time after transmission	500(Note 1)		ns
tWR	Read pulse width	400(Note 2)		ns
tRC	Transfer waiting time after read	500(Note 1)		ns
tCRPV	Waiting time before program verify	6		µs
tWP	Programming time		10	µs
tPC	Transfer waiting time after programming	500(Note 1)		ns
tCREV	Waiting time before erase verify	6		ns
tWE	Erase time		9.5	ns
tEC	Transfer waiting time after erase	500(Note 1)		ns
tc(CK)	SCLK input cycle time	250		ns
tw(CKH)	SCLK high-level pulse width	100		ns
tw(CKL)	SCLK low-level pulse width	100		ns
tr(CK)	SCLK rise time	20		ns
tf(CK)	SCLK fall time	20		ns
td(C-Q)	SDA output delay time	0	90	ns
th(C-Q)	SDA output hold time	0		ns
th(C-E)	SDA output hold time (only the 8th bit)	150(Note 3)	250(Note 4)	ns
tsu(D-C)	SDA input set up time	30		ns
th(C-D)	SDA input hold time	90		ns

Notes 1: When f(XIN) = 10 MHz or less, calculate the minimum value according to formula 1.

Formula 1 : $\frac{5000}{f(X_{IN})} \times 10^6$

2: When f(XIN) = 10 MHz or less, calculate the minimum value according to formula 2.

Formula 2 : $\frac{4000}{f(X_{IN})} \times 10^6$

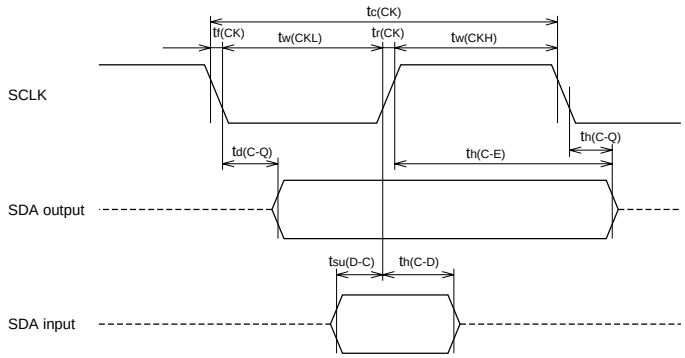
3: When f(XIN) = 10 MHz or less, calculate the minimum value according to formula 3.

Formula 3 : $\frac{1500}{f(X_{IN})} \times 10^6$

4: When f(XIN) = 10 MHz or less, calculate the minimum value according to formula 4

Formula 4 : $\frac{2500}{f(X_{IN})} \times 10^6$

AC waveforms



Test conditions for AC characteristics

- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V
- Input timing voltage : VIL = 0.2 VCC, VIH = 0.8 VCC

(3) Flash memory mode 3 (CPU reprogramming mode)

The 3803/3804 group has the CPU reprogramming mode where a built-in flash memory is handled by the central processing unit (CPU).

In CPU reprogramming mode, the flash memory is handled by writing and reading to/from the flash memory control register (see Figure 101) and the flash command register (see Figure 102).

The CNVSS pin is used as the VPP power supply pin in CPU reprogramming mode. It is necessary to apply the power-supply voltage of VPPH from the external to this pin.

Functional Outline (CPU reprogramming mode)

Figure 101 shows the flash memory control register bit configuration. Figure 102 shows the flash command register bit configuration.

Bit 0 of the flash memory control register is the CPU reprogramming mode select bit. When this bit is set to “1” and VPPH is applied to the CNVss/VPP pin, the CPU reprogramming mode is selected. Whether the CPU reprogramming mode is realized or not is judged by reading the CPU reprogramming mode monitor flag (bit 2 of the flash memory control register).

Bit 1 is a busy flag which becomes “1” during erase and program execution.

Whether these operations have been completed or not is judged by checking this flag after each command of erase and the program is executed.

Bits 4, 5 of the flash memory control register are the erase/program area select bits. These bits specify an area where erase and program is operated. When the erase command is executed after an area is specified by these bits, only the specified area is erased. Only for the specified area, programming is enabled; for the other areas, programming is disabled.

Figure 103 shows the CPU mode register bit configuration in the CPU reprogramming mode.

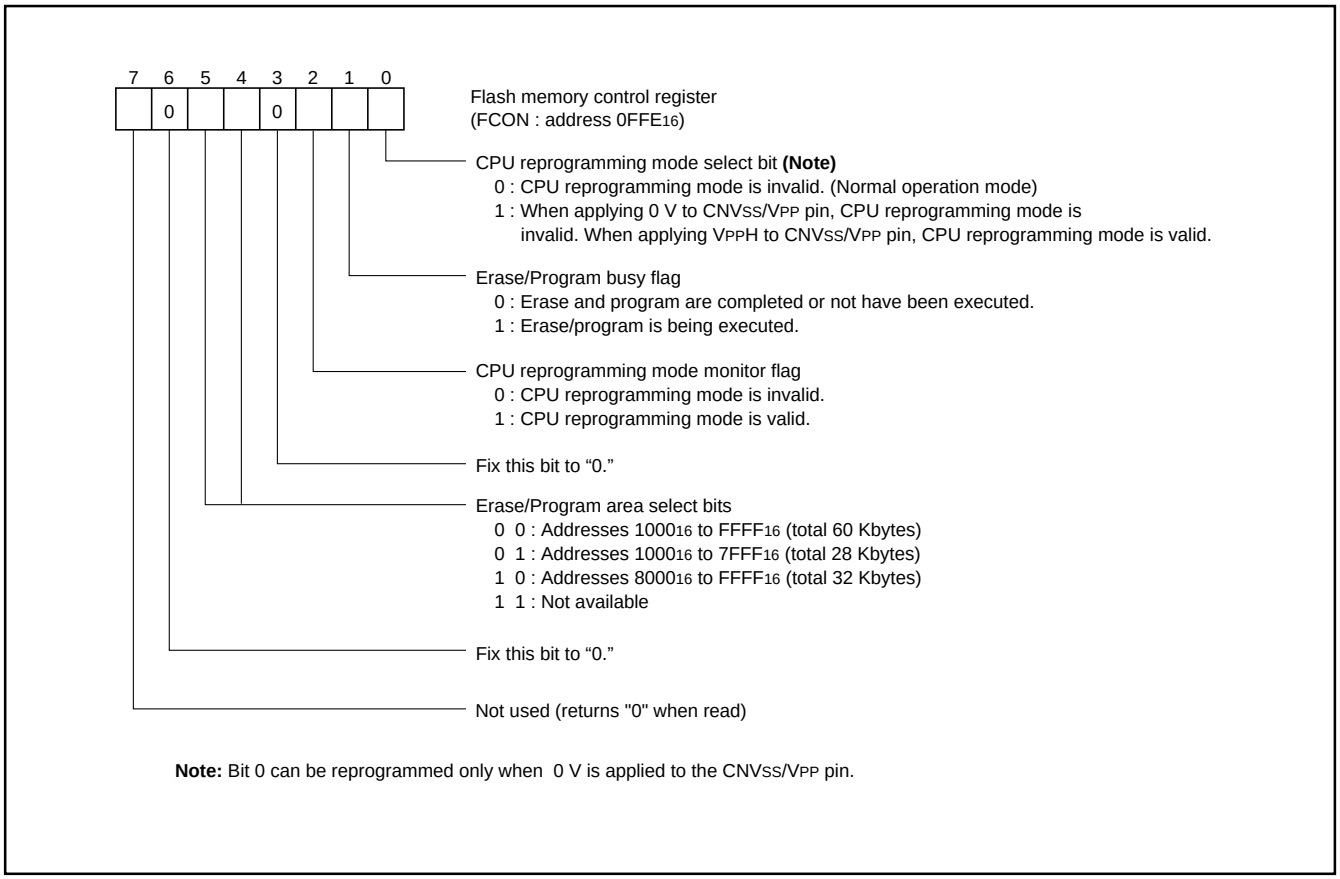


Fig. 101 Flash memory control register bit configuration

● CPU reprogramming mode operation procedure

The operation procedure in CPU reprogramming mode is described below.

< Beginning procedure >

① Apply 0 V to the CNVss/VPP pin for reset release.
② Set the CPU mode register (see Figure 103).
③ After CPU reprogramming mode control program is transferred to internal RAM, jump to this control program on RAM. (The following operations are controlled by this control program).
④ Set "1" to the CPU reprogramming mode select bit.
⑤ Apply VPPH to the CNVSS/VPP pin.
⑥ Wait till CNVSS/VPP pin becomes 12V.
⑦ Read the CPU reprogramming mode monitor flag to confirm whether the CPU reprogramming mode is valid.
⑧ The operation of the flash memory is executed by software-command-writing to the flash command register .

Note: The following are necessary other than this:
- •Control for data which is input from the external (serial I/O etc.) and to be programmed to the flash memory
- •Initial setting for ports etc.
- •Writing to the watchdog timer

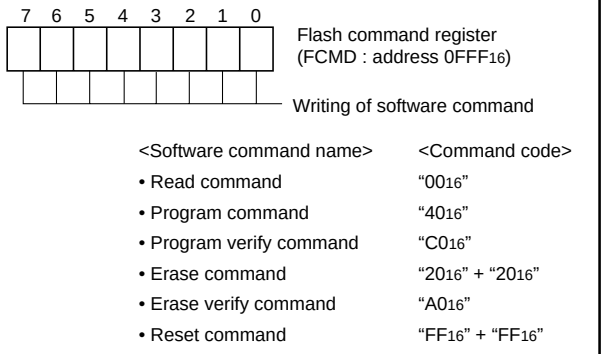
< Release procedure >

① Apply 0 V to the CNVSS/VPP pin.
② Wait till CNVSS/VPP pin becomes 0 V.
③ Set the CPU reprogramming mode select bit to "0."

Each software command is explained as follows.

● Read command

When "00$_{16}$" is written to the flash command register, the 3803/3804 group enters the read mode. The contents of the corresponding address can be read by reading the flash memory (For instance, with the LDA instruction etc.) under this condition.
The read mode is maintained until another command code is written to the flash command register. Accordingly, after setting the read mode once, the contents of the flash memory can continuously be read.
After reset and after the reset command is executed, the read mode is set.



<Software command name>	<Command code>
• Read command	"00$_{16}$"
• Program command	"40$_{16}$"
• Program verify command	"C0$_{16}$"
• Erase command	"20$_{16}$" + "20$_{16}$"
• Erase verify command	"A0$_{16}$"
• Reset command	"FF$_{16}$" + "FF$_{16}$"

Note: The flash command register is write-only register.

Fig. 102 Flash command register bit configuration

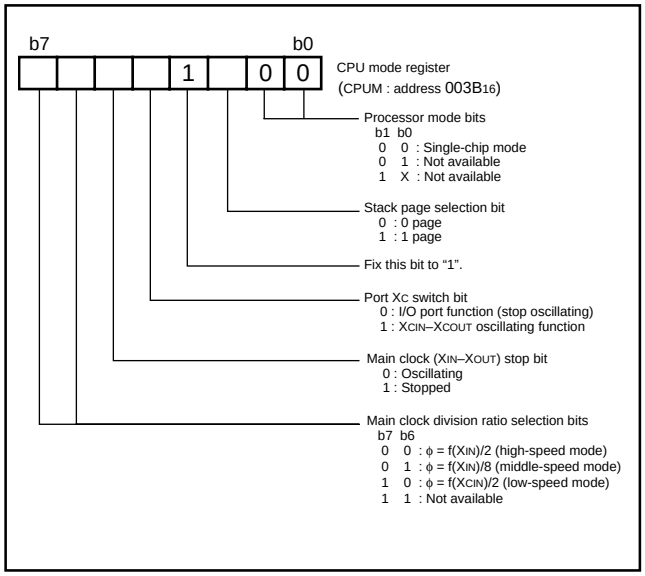


Fig. 103 CPU mode register bit configuration in CPU rewriting mode

● **Program command**

When “40$_{16}$” is written to the flash command register, the 3803/3804 group enters the program mode.

Subsequently to this, if the instruction (for instance, STA or LDM instruction) for writing byte data in the address to be programmed is executed, the control circuit of the flash memory executes the program. The erase/program busy flag of the flash memory control register is set to “1” when the program starts, and becomes “0" when the program is completed. Accordingly, after the write instruction is executed, CPU can recognize the completion of the program by polling this bit.

The programmed area must be specified beforehand by the erase/program area select bits.

During programming, watchdog timer stops with “FFFF$_{16}$” set.

Note: A programming operation is not completed by executing the program command once. Always be sure to execute a program verify command after executing the program command. When the failure is found in this verification, the user must repeatedly execute the program command until the pass. Refer to Figure 104 for the flow chart of the programming.

● **Program verify command**

When “C0$_{16}$" is written to the flash command register, the 3803/3804 group enters the program verify mode. Subsequently to this, if the instruction (for instance, LDA instruction) for reading byte data from the address to be verified (i.e., previously programmed address), the contents which has been written to the address actually is read.

CPU compares this read data with data which has been written by the previous program command. In consequence of the comparison, if not agreeing, the operation of “program → program verify” must be executed again.

● **Erase command**

When writing “20$_{16}$” twice continuously to the flash command register, the flash memory control circuit performs erase to the area specified beforehand by the erase/program area select bits.

Erase/program busy flag of the flash memory control register becomes “1” when erase begins, and it becomes “0" when erase completes. Accordingly, CPU can recognize the completion of erase by polling this bit.

Data “00$_{16}$” must be written to all areas to be erased by the program and the program verify commands before the erase command is executed.

During erasing, watchdog timer stops with “FFFF$_{16}$” set.

Note: The erasing operation is not completed by executing the erase command once. Always be sure to execute an erase verify command after executing the erase command. When the failure is found in this verification, the user must repeatedly execute the erase command until the pass. Refer to Figure 104 for the erasing flowchart.

● **Erase verify command**

When “A0$_{16}$" is written to the flash command register, the 3803/3804 group enters the erase verify mode. Subsequently to this, if the instruction (for instance, LDA instruction) for reading byte data from the address to be verified, the contents of the address is read.

CPU must erase and verify to all erased areas in a unit of address.

If the address of which data is not “FF$_{16}$” (i.e., data is not erased) is found, it is necessary to discontinue erasure verification there, and execute the operation of “erase → erase verify” again.

Note: By executing the operation of “erase → erase verify” again when the memory not erased is found. It is unnecessary to write data “00$_{16}$” before erasing in this case.

● **Reset command**

The reset command is a command to discontinue the program or erase command on the way. When “FF$_{16}$” is written to the command register two times continuously after “40$_{16}$” or “20$_{16}$” is written to the flash command register, the program, or erase command becomes invalid (reset), and the 3803/3804 group enters the reset mode.

The contents of the memory does not change even if the reset command is executed.

DC Electric Characteristics

Note: The characteristic concerning the flash memory part are the same as the characteristic of the parallel I/O mode.

AC Electric Characteristics

Note: The characteristics are the same as the characteristic of the microcomputer mode.

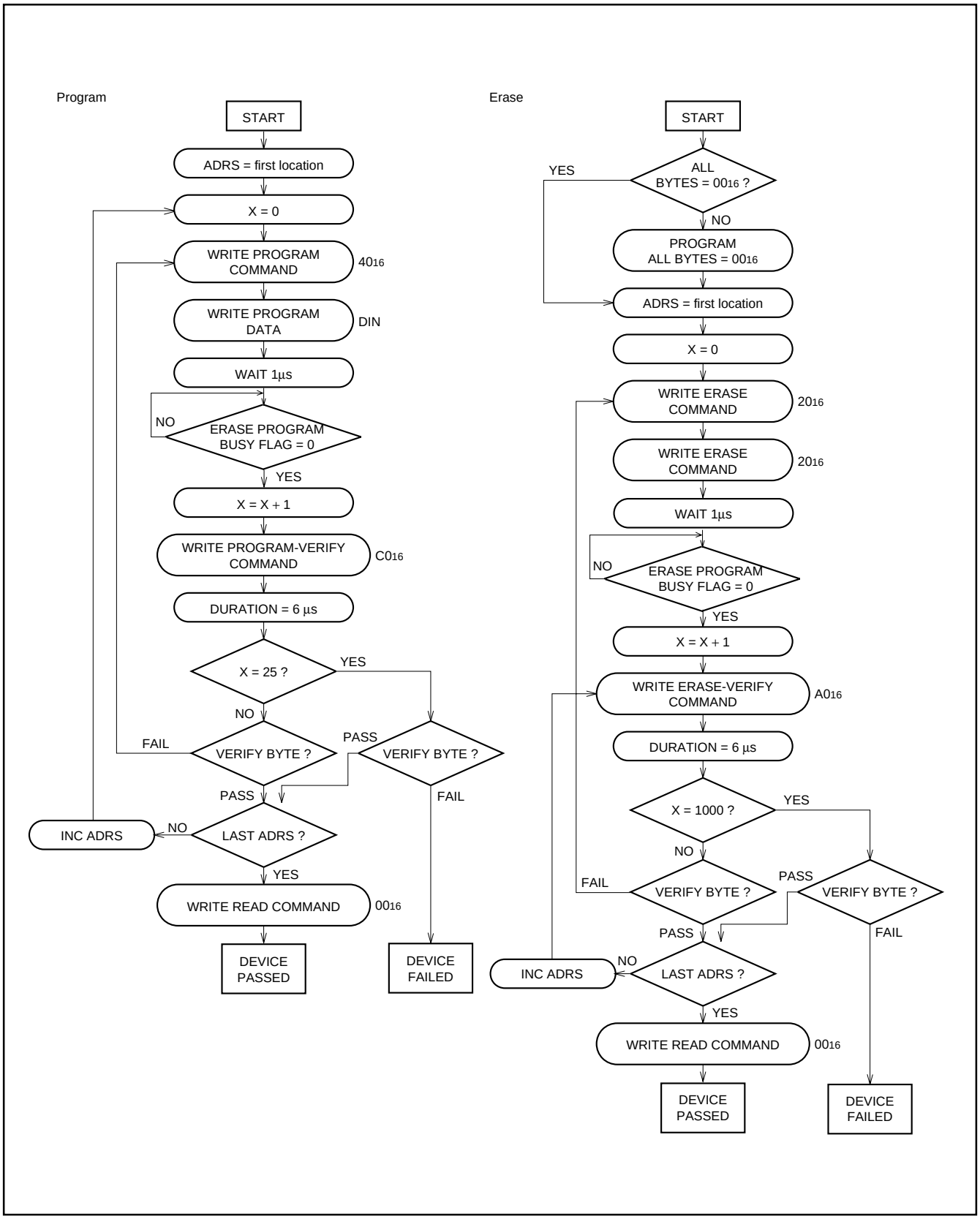


Fig. 104 Flowchart of program/erase operation at CPU reprogramming mode

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The instruction with the addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1."

Serial I/O continues to output the final bit from the TxD pin after transmission is completed. SOUT2 pin for serial I/O2 goes to high impedance after transfer is completed.

When in serial I/Os 1 and 3 (clock-synchronous mode) or in serial I/O2, an external clock is used as synchronous clock, write transmission data to the transmit buffer register or serial I/O2 register, during transfer clock is "H."

A-D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.

Therefore, make sure that f(XIN) is at least on 500 kHz during an A-D conversion.

Do not execute the STP instruction during an A-D conversion.

D-A Converter

The accuracy of the D-A converter becomes rapidly poor under the V_{CC} = 4.0 V or less condition; a supply voltage of $V_{CC} \geq 4.0$ V is recommended. When a D-A converter is not used, set all values of D-Ai conversion registers (i=1, 2) to "00_{16}."

Instruction Execution Time

The instruction execution time is obtained by multiplying the period of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The period of the internal clock ϕ is double of the XIN period in high-speed mode.

NOTES ON USAGE

Handling of Power Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (V_{SS} pin), and between power source pin (V_{CC} pin) and analog power source input pin (AV_{SS} pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 µF–0.1 µF is recommended.

Flash Memory Version

The CNV_{SS} pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.
To improve the noise reduction, connect a track between CNV_{SS} pin and V_{SS} pin or V_{CC} pin with 1 to 10 kΩ resistance.
The mask ROM version track of CNV_{SS} pin has no operational interference even if it is connected to Vss pin or Vcc pin via a resistor.

Electric Characteristic Differences Between Mask ROM and Flash Memory Version MCUs

There are differences in electric characteristics, operation margin, noise immunity,
and noise radiation between Mask ROM and Flash Memory version MCUs due to the difference in the manufacturing processes.
When manufacturing an application system with the Flash Memory version and then switching to use of the Mask ROM version, please perform sufficient evaluations for the commercial samples of the Mask ROM version.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Confirmation Form *
2. Mark Specification Form *
3. Data to be written to ROM, in EPROM form (three identical copies)

* For the mask ROM confirmation and the mark specifications, refer to the “Renesas Technology” Homepage (http://www.renesas.com/en/rom).

ELECTRICAL CHARACTERISTICS

Absolute maximum ratings

Table 27 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltages	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_4$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, V_{REF}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P3_2$, $P3_3$		–0.3 to 5.8	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage CNV_{SS} (Mask ROM version)		–0.3 to V_{CC} +0.3	V
V_I	Input voltage CNV_{SS} (Flash memory version)		–0.3 to 13	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_4$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, X_{OUT}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P3_2$, $P3_3$		–0.3 to 5.8	V
P_d	Power dissipation	T_a = 25 °C	1000 **(Note)**	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–65 to 125	°C

Note: In flat package, this value is 300 mW.

Recommended operating conditions

Table 28 Recommended operating conditions

(V_{CC} = 2.7 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (Mask ROM version)	$f(X_{IN}) \leq 8.4$ MHz	2.7	5.0	5.5	V
		$f(X_{IN}) \leq 12.5$ MHz	4.0	5.0	5.5	
		$f(X_{IN}) \leq 16.8$ MHz	4.5	5.0	5.5	
V_{CC}	Power source voltage (flash memory version)	$f(X_{IN}) \leq 12.5$ MHz	4.0	5.0	5.5	V
		$f(X_{IN}) \leq 16.8$ MHz	4.5	5.0	5.5	
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage (when A-D converter is used)		2.0		V_{CC}	V
	Analog reference voltage (when D-A converter is used)		2.7		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage	AN_0–AN_{15}	AV_{SS}		V_{CC}	V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_4$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$P3_2$, $P3_3$	0.8V_{CC}		5.5	V
V_{IH}	“H” input voltage (when I^2C-BUS input level is selected)	S_{DA}, S_{CL}	0.7V_{CC}		5.5	V
V_{IH}	“H” input voltage (when SMBUS input level is selected)	$\overline{S_{DA}}$, $\overline{S_{CL}}$	1.4		5.5	V
V_{IH}	“H” input voltage	$\overline{RESET}$, X_{IN}, X_{CIN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$	0		0.2V_{CC}	V
V_{IL}	“L” input voltage (when I^2C-BUS input level is selected)	S_{DA}, S_{CL}	0		0.3V_{CC}	V
V_{IL}	“L” input voltage (when SMBUS input level is selected)	$\overline{S_{DA}}$, $\overline{S_{CL}}$	0		0.6	V
V_{IL}	“L” input voltage	$\overline{RESET}$, CNV_{SS}			0.2V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}, X_{CIN}			0.16V_{CC}	V

Table 29 Recommended operating conditions
(V_{CC} = 2.7 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_4$–$P3_7$ **(Note 1)**			–80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 1)**			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$ **(Note 1)**			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P2_0$–$P2_7$ **(Note 1)**			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 1)**			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_4$–$P3_7$ **(Note 1)**			–40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 1)**			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$ **(Note 1)**			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P2_0$–$P2_7$ **(Note 1)**			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 1)**			40	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_4$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 2)**			–10	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 2)**			10	mA
$I_{OL(peak)}$	"L" peak output current	$P2_0$–$P2_7$ **(Note 2)**			20	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_4$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 3)**			–5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 3)**			5	mA
$I_{OL(avg)}$	"L" average output current	$P2_0$–$P2_7$ **(Note 3)**			10	mA
$f(X_{IN})$	Main clock input oscillation frequency **(Note 4)**	Vcc = 4.5–5.5 V			16.8	MHz
		Vcc = 4.0–4.5 V			8.6Vcc–21,9	MHz
		Vcc = 2.7–4.0 V			$\frac{41}{13}V_{CC}-\frac{3}{26}$	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency **(Notes 4, 5)**			32.768	50	kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current I_{OL}(avg), I_{OH}(avg) are average value measured over 100 ms.
4: When the oscillation frequency has a duty cycle of 50%.
5: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

Electrical characteristics

Table 30 Electrical characteristics

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_7$, P3$_0$, P3$_1$, P3$_4$–P3$_7$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$ **(Note 1)**	I_{OH} = –10 mA V_{CC} = 4.0–5.5 V	V_{CC}–2.0			V
		I_{OH} = –1.0 mA V_{CC} = 2.7–5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_7$, P3$_0$–P3$_7$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$	I_{OL} = 10 mA V_{CC} = 4.0–5.5 V			2.0	V
		I_{OL} = 1.6 mA V_{CC} = 2.7–5.5 V			0.4	V
V_{T+}–V_{T-}	Hysteresis CNTR$_0$, CNTR$_1$, CNTR$_2$, INT$_0$–INT$_4$			0.4		V
V_{T+}–V_{T-}	Hysteresis RxD1, SCLK1, SIN2, SCLK2, RxD3, SCLK3			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{\text{RESET}}$			0.5		V
I_{IH}	"H" input current P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_7$, P3$_0$–P3$_7$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$	V_I = V_{CC} (Pin floating. Pull-up transistors "off")			5.0	µA
I_{IH}	"H" input current $\overline{\text{RESET}}$, CNV$_{SS}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4		µA
I_{IL}	"L" input current P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_7$, P3$_0$–P3$_7$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$	V_I = V_{SS} (Pin floating. Pull-up transistors "off")			–5.0	µA
I_{IL}	"L" input current $\overline{\text{RESET}}$,CNV$_{SS}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4		µA
I_{IL}	"L" input current (at Pull-up) P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_7$, P3$_0$, P3$_1$, P3$_4$–P3$_7$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$	V_I = V_{SS} V_{CC} = 5.0 V	–80	–210	–420	µA
		V_I = V_{SS} V_{CC} = 3.0 V	–30	–70	–140	µA
V_{RAM}	RAM hold voltage	When clock stopped	2.0		5.5	V

Note 1: P3$_5$ is measured when the P3$_5$/TxD$_3$ P-channel output disable bit of the UART3 control register (bit 4 of address 0033$_{16}$) is "0".
P4$_5$ is measured when the P4$_5$/TxD$_1$ P-channel output disable bit of the UART1 control register (bit 4 of address 001B$_{16}$) is "0".

Table 31 Electrical characteristics (flash memory version)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	High-speed mode $f(X_{IN})$ = 16.8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			12	22	mA
		High-speed mode $f(X_{IN})$ = 12.5 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			10	18	mA
		High-speed mode $f(X_{IN})$ = 8.4 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			7	13.5	mA
		High-speed mode $f(X_{IN})$ = 16.8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			3.5	6	mA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			60	200	µA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			30	60	µA
		Middle-speed mode $f(X_{IN})$ = 16.8 MHz $f(X_{CIN})$ = stopped Output transistors “off”			6	12	mA
		Middle-speed mode $f(X_{IN})$ = 16.8 MHz (in WIT state) $f(X_{CIN})$ = stopped Output transistors “off”			3	5.5	mA
		Increment when A-D conversion is executed $f(X_{IN})$ = 16.8 MHz			500		µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

Table 32 Electrical characteristics (mask ROM version)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	High-speed mode $f(X_{IN})$ = 16.8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			8	15	mA
		High-speed mode $f(X_{IN})$ = 12.5 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			6.5	12	mA
		High-speed mode $f(X_{IN})$ = 8.4 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			5	9	mA
		High-speed mode $f(X_{IN})$ = 16.8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			2	3.6	mA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			55	200	µA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			40	70	µA
		Low-speed mode (V_{CC} = 3 V) $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			15	40	µA
		Low-speed mode (V_{CC} = 3 V) $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			8	15	µA
		Middle-speed mode $f(X_{IN})$ = 16.8 MHz $f(X_{CIN})$ = stopped Output transistors “off”			4	7	mA
		Middle-speed mode $f(X_{IN})$ = 16.8 MHz (in WIT state) $f(X_{CIN})$ = stopped Output transistors “off”			1.8	3.3	mA
		Increment when A-D conversion is executed $f(X_{IN})$ = 16.8 MHz			500		µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

A-D converter characteristics

Table 33 A-D converter characteristics (1)
(V_{CC} = 2.7 to 5.5 V, V_{REF} = 2.0 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)
10-bit A-D mode (when conversion mode selection bit (bit 7 of address 003816) is "0")

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
–	Resolution					10	bit
–	Absolute accuracy (excluding quantization error)		V_{CC} = V_{REF} = 5.0 V			±4	LSB
t_{CONV}	Conversion time					61	2tc(X_{IN})
R_{LADDER}	Ladder resistor			12	35	100	kΩ
I_{VREF}	Reference power source input current	at A-D converter operated	V_{REF} = 5.0 V	50	150	200	µA
		at A-D converter stopped	V_{REF} = 5.0 V			5	µA
$I_{I(AD)}$	A-D port input current					5.0	µA

Table 34 A-D converter characteristics (2)
(V_{CC} = 2.7 to 5.5 V, V_{REF} = 2.0 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)
8-bit A-D mode (when conversion mode selection bit (bit 7 of address 003816) is "1")

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
–	Resolution					8	bit
–	Absolute accuracy (excluding quantization error)		V_{CC} = V_{REF} = 5.0 V			±2	LSB
t_{CONV}	Conversion time					50	2tc(X_{IN})
R_{LADDER}	Ladder resistor			12	35	100	kΩ
I_{VREF}	Reference power source input current	at A-D converter operated	V_{REF} = 5.0 V	50	150	200	µA
		at A-D converter stopped	V_{REF} = 5.0 V			5	µA
$I_{I(AD)}$	A-D port input current					5.0	µA

D-A converter characteristics

Table 35 D-A converter characteristics
(V_{CC} = 2.7 to 5.5 V, V_{REF} = 2.7 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
–	Resolution					8	Bits
–	Absolute accuracy	4.0 ≤ V_{REF} ≤ 5.5 V				1.0	%
		2.7 ≤ V_{REF} < 4.0 V				2.5	%
tsu	Setting time					3	µs
RO	Output resistor			2	3.5	5	kΩ
I_{VREF}	Reference power source input current **(Note 1)**					3.2	mA

Note 1: Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "0016".

Timing requirements and switching characteristics

Table 36 Timing requirements (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	16			X_{IN} cycle
$t_{C(X_{IN})}$	Main clock input cycle time (Vcc = 4.5–5.5 V)	59.5			ns
	Main clock input cycle time (Vcc = 4.0–4.5 V)	10000 / 86Vcc–219			ns
$t_{WH(X_{IN})}$	Main clock input “H” pulse width (Vcc = 4.5–5.5 V)	25			ns
	Main clock input “H” pulse width (Vcc = 4.0–4.5 V)	4000 / 86Vcc–219			ns
$t_{WL(X_{IN})}$	Main clock input “L” pulse width (Vcc = 4.5–5.5 V)	25			ns
	Main clock input “L” pulse width (Vcc = 4.0–4.5 V)	4000 / 86Vcc–219			ns
$t_{C(X_{CIN})}$	Sub-clock input cycle time	20			µs
$t_{WH(X_{CIN})}$	Sub-clock input “H” pulse width	5			µs
$t_{WL(X_{CIN})}$	Sub-clock input “L” pulse width	5			µs
$t_{C(CNTR)}$	$CNTR_0$–$CNTR_2$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$–$CNTR_2$ input “H” pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$–$CNTR_2$ input “L” pulse width	80			ns
$t_{WH(INT)}$	INT_{00}, INT_{01}, INT_1, INT_2, INT_3, INT_{40}, INT_{41} input “H” pulse width	80			ns
$t_{WL(INT)}$	INT_{00}, INT_{01}, INT_1, INT_2, INT_3, INT_{40}, INT_{41} input “L” pulse width	80			ns
$t_{C(SCLK1)}$, $t_{C(SCLK3)}$	Serial I/O1, serial I/O3 clock input cycle time **(Note)**	800			ns
$t_{WH(SCLK1)}$, $t_{WH(SCLK3)}$	Serial I/O1, serial I/O3 clock input “H” pulse width **(Note)**	370			ns
$t_{WL(SCLK1)}$, $t_{WL(SCLK3)}$	Serial I/O1, serial I/O3 clock input “L” pulse width **(Note)**	370			ns
$t_{su(RxD1\text{-}SCLK1)}$, $t_{su(RxD3\text{-}SCLK3)}$	Serial I/O1, serial I/O3 input setup time	220			ns
$t_{h(SCLK1\text{-}RxD1)}$, $t_{h(SCLK3\text{-}RxD3)}$	Serial I/O1, serial I/O3 input hold time	100			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(SIN2\text{-}SCLK2)}$	Serial I/O2 input setup time	200			ns
$t_{h(SCLK2\text{-}SIN2)}$	Serial I/O2 input hold time	200			ns

Note : When bit 6 of address $001A_{16}$ and bit 6 of address 0032_{16} are “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ and bit 6 of address 0032_{16} are “0” (UART).

Table 37 Timing requirements (2)

(V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	16			X_{IN} cycle
$t_{C(XIN)}$	Main clock input cycle time	$\frac{26 \times 10^3}{82V_{CC}-3}$			ns
$t_{WH(XIN)}$	Main clock input “H” pulse width	$\frac{10000}{82V_{CC}-3}$			ns
$t_{WL(XIN)}$	Main clock input “L” pulse width	$\frac{10000}{82V_{CC}-3}$			ns
$t_{C(XCIN)}$	Sub-clock input cycle time	20			µs
$t_{WH(XCIN)}$	Sub-clock input “H” pulse width	5			µs
$t_{WL(XCIN)}$	Sub-clock input “L” pulse width	5			µs
$t_{C(CNTR)}$	$CNTR_0$–$CNTR_2$ input cycle time	500			ns
$t_{WH(CNTR)}$	$CNTR_0$–$CNTR_2$ input “H” pulse width	230			ns
$t_{WL(CNTR)}$	$CNTR_0$–$CNTR_2$ input “L” pulse width	230			ns
$t_{WH(INT)}$	INT_{00}, INT_{01}, INT_1, INT_2, INT_3, INT_{40}, INT_{41} input “H” pulse width	230			ns
$t_{WL(INT)}$	INT_{00}, INT_{01}, INT_1, INT_2, INT_3, INT_{40}, INT_{41} input “L” pulse width	230			ns
$t_{C(SCLK1)}$, $t_{C(SCLK3)}$	Serial I/O1, serial I/O3 clock input cycle time **(Note)**	2000			ns
$t_{WH(SCLK1)}$, $t_{WH(SCLK3)}$	Serial I/O1, serial I/O3 clock input “H” pulse width **(Note)**	950			ns
$t_{WL(SCLK1)}$, $t_{WL(SCLK3)}$	Serial I/O1, serial I/O3 clock input “L” pulse width **(Note)**	950			ns
$t_{su(RxD1\text{-}SCLK1)}$, $t_{su(RxD3\text{-}SCLK3)}$	Serial I/O1, serial I/O3 input setup time	400			ns
$t_{h(SCLK1\text{-}RxD1)}$, $t_{h(SCLK3\text{-}RxD3)}$	Serial I/O1, serial I/O3 input hold time	200			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su(SIN2\text{-}SCLK2)}$	Serial I/O2 input setup time	400			ns
$t_{h(SCLK2\text{-}SIN2)}$	Serial I/O2 input hold time	300			ns

Note : When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 38 Switching characteristics 1
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{WH} (S_{CLK1}), t_{WH} (S_{CLK3})	Serial I/O1, serial I/O3 clock output “H” pulse width	Fig. 105	$t_{C(SCLK1)}$/2–30 $t_{C(SCLK3)}$/2–30			ns
t_{WL} (S_{CLK1}), t_{WL} (S_{CLK3})	Serial I/O1, serial I/O3 clock output “L” pulse width		$t_{C(SCLK1)}$/2–30 $t_{C(SCLK3)}$/2–30			ns
td (S_{CLK1}-TxD1) , td (S_{CLK3}-TxD3)	Serial I/O1, serial I/O3 output delay time **(Note 1)**				140	ns
tv (S_{CLK1}-TxD1) , tv (S_{CLK3}-TxD3)	Serial I/O1, serial I/O3 output valid time **(Note 1)**		–30			ns
tr (S_{CLK1}) , tr (S_{CLK3})	Serial I/O1, serial I/O3 clock output rising time				30	ns
tf (S_{CLK1}), tf (S_{CLK3})	Serial I/O1, serial I/O3 clock output falling time				30	ns
t_{WH} (S_{CLK2})	Serial I/O2 clock output “H” pulse width		$t_{C(SCLK2)}$/2–160			ns
t_{WL} (S_{CLK2})	Serial I/O2 clock output “L” pulse width		$t_{C(SCLK2)}$/2–160			ns
td (S_{CLK2}-S_{OUT2})	Serial I/O2 output delay time				200	ns
tv (S_{CLK2}-S_{OUT2})	Serial I/O2 output valid time		0			ns
tf (S_{CLK2})	Serial I/O2 clock output falling time				30	ns
tr (CMOS)	CMOS output rising time **(Note 2)**			10	30	ns
tf (CMOS)	CMOS output falling time **(Note 2)**			10	30	ns

Notes 1: When the P45/TxD1 P-channel output disable bit of the UART1 control register (bit 4 of address 001B16) is “0”.
When the P35/TxD3 P-channel output disable bit of the UART3 control register (bit 4 of address 003316) is “0”.
2: The X_{OUT} pin is excluded.

Table 39 Switching characteristics 2
(V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{WH} (S_{CLK1}), t_{WH} (S_{CLK3})	Serial I/O1, serial I/O3 clock output “H” pulse width	Fig. 105	$t_{C(SCLK1)}$/2–50 $t_{C(SCLK3)}$/2–50			ns
t_{WL} (S_{CLK1}), t_{WL} (S_{CLK3})	Serial I/O1, serial I/O3 clock output “L” pulse width		$t_{C(SCLK1)}$/2–50 $t_{C(SCLK3)}$/2–50			ns
td (S_{CLK1}-TxD1) , td (S_{CLK3}-TxD3)	Serial I/O1, serial I/O3 output delay time **(Note 1)**				350	ns
tv (S_{CLK1}-TxD1) , tv (S_{CLK3}-TxD3)	Serial I/O1, serial I/O3 output valid time **(Note 1)**		–30			ns
tr (S_{CLK1}) , tr (S_{CLK3})	Serial I/O1, serial I/O3 clock output rising time				50	ns
tf (S_{CLK1}), tf (S_{CLK3})	Serial I/O1, serial I/O3 clock output falling time				50	ns
t_{WH} (S_{CLK2})	Serial I/O2 clock output “H” pulse width		$t_{C(SCLK2)}$/2–240			ns
t_{WL} (S_{CLK2})	Serial I/O2 clock output “L” pulse width		$t_{C(SCLK2)}$/2–240			ns
td (S_{CLK2}-S_{OUT2})	Serial I/O2 output delay time				400	ns
tv (S_{CLK2}-S_{OUT2})	Serial I/O2 output valid time		0			ns
tf (S_{CLK2})	Serial I/O2 clock output falling time				50	ns
tr (CMOS)	CMOS output rising time **(Note 2)**			20	50	ns
tf (CMOS)	CMOS output falling time **(Note 2)**			20	50	ns

Notes 1: When the P45/TxD1 P-channel output disable bit of the UART1 control register (bit 4 of address 001B16) is “0”.
When the P35/TxD3 P-channel output disable bit of the UART3 control register (bit 4 of address 003316) is “0”.
2: The X_{OUT} pin is excluded.

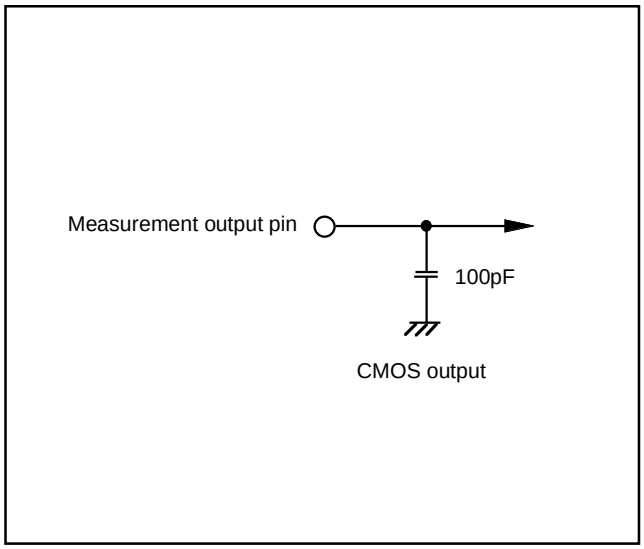


Fig. 105 Circuit for measuring output switching characteristics (1)

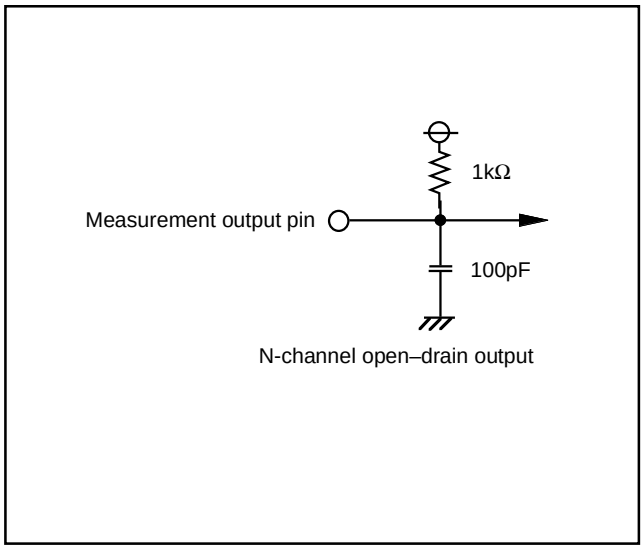


Fig. 106 Circuit for measuring output switching characteristics (2)

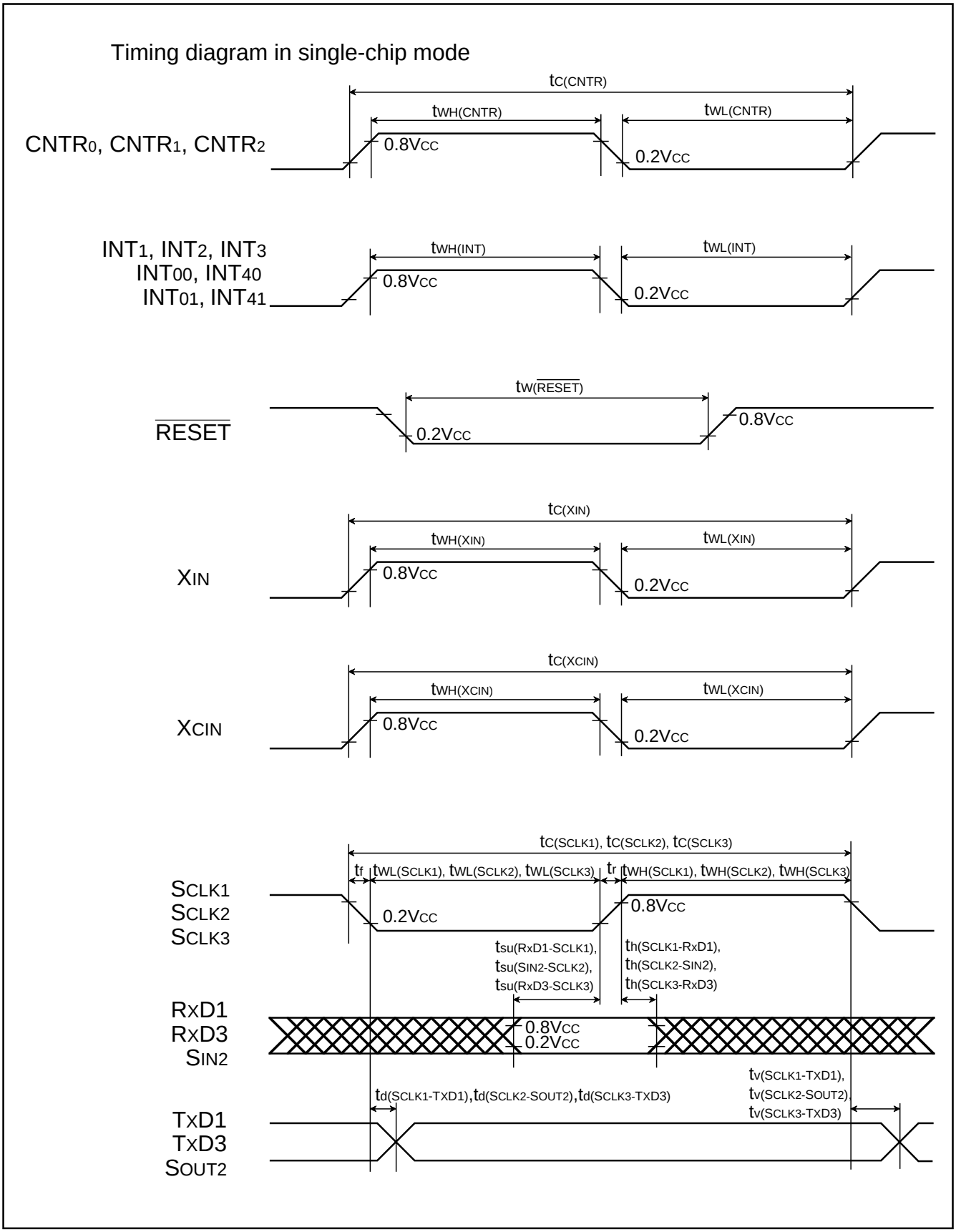


Fig. 107 Timing diagram (in single-chip mode)

Table 40 Multi-master I²C-BUS bus line characteristics

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time for START condition	4.0		0.6		µs
t_{LOW}	Hold time for SCL clock = “0”	4.7		1.3		µs
t_R	Rising time of both SCL and SDA signals		1000	20+0.1Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time for SCL clock = “1”	4.0		0.6		µs
t_F	Falling time of both SCL and SDA signals		300	20+0.1Cb	300	ns
$t_{SU;DAT}$	Data setup time	250		100		ns
$t_{SU;STA}$	Setup time for repeated START condition	4.7		0.6		µs
$t_{SU;STO}$	Setup time for STOP condition	4.0		0.6		µs

Note: C_b = total capacitance of 1 bus line

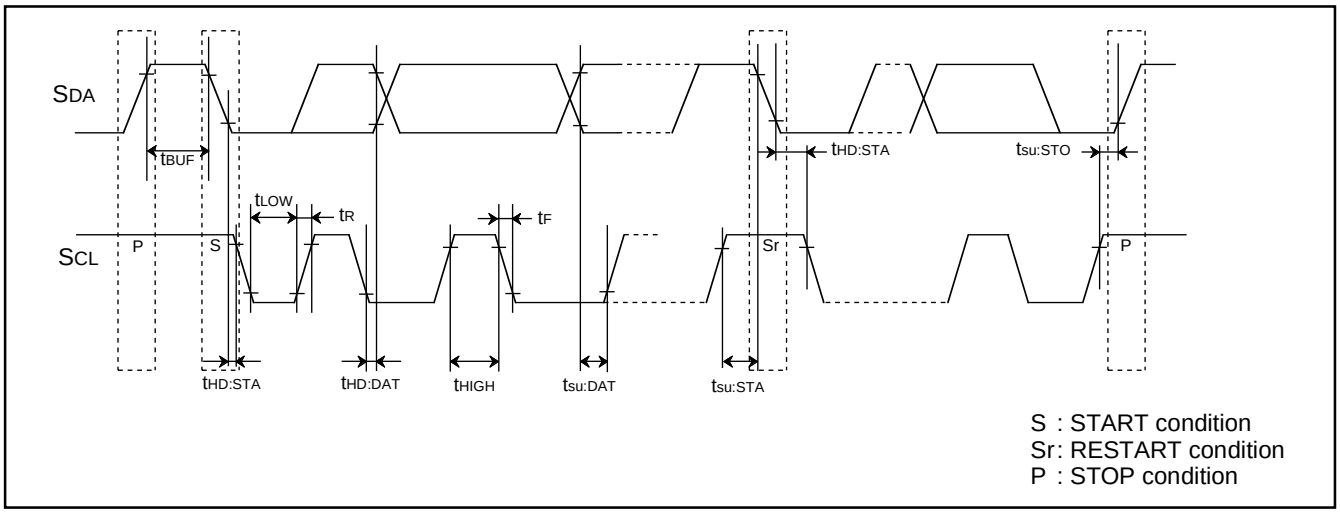


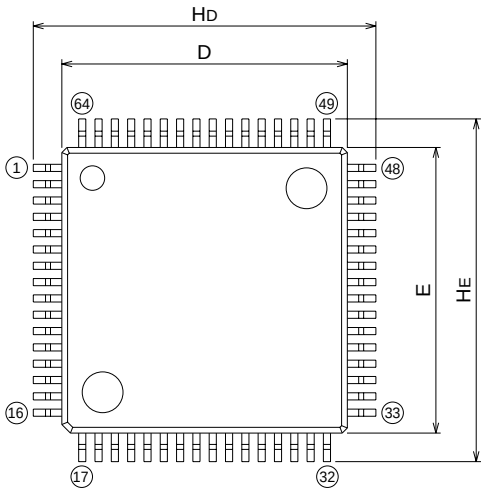
Fig. 108 Timing diagram of multi-master I²C-BUS

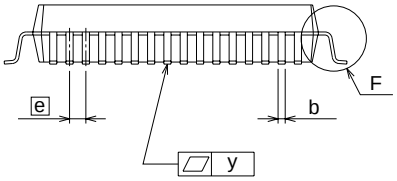
PACKAGE OUTLINE

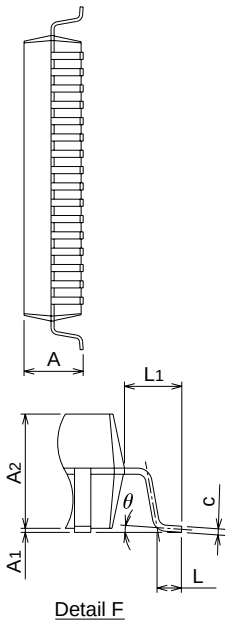
64P6N-A

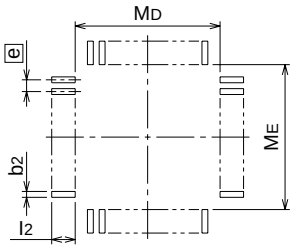
Plastic 64pin 14×14mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP64-P-1414-0.80	–	1.11	Alloy 42









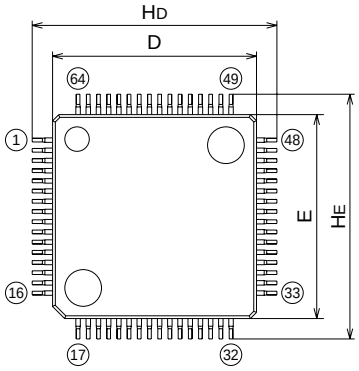
Recommended Mount Pad

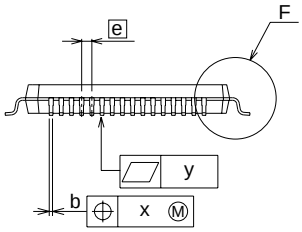
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	13.8	14.0	14.2
e	–	0.8	–
HD	16.5	16.8	17.1
HE	16.5	16.8	17.1
L	0.4	0.6	0.8
L1	–	1.4	–
y	–	–	0.1
θ	0°	–	10°
b2	–	0.5	–
I2	1.3	–	–
MD	–	14.6	–
ME	–	14.6	–

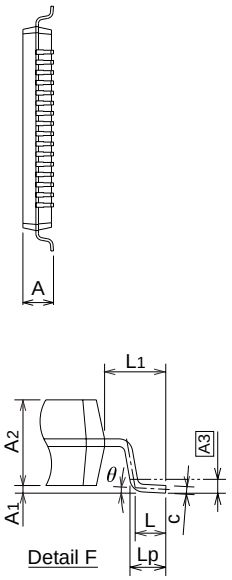
64P6Q-A (MMP)

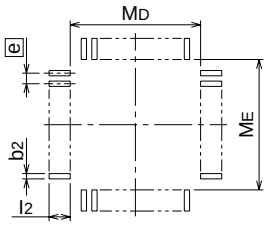
Plastic 64pin 10×10mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1010-0.50	–	–	Cu Alloy









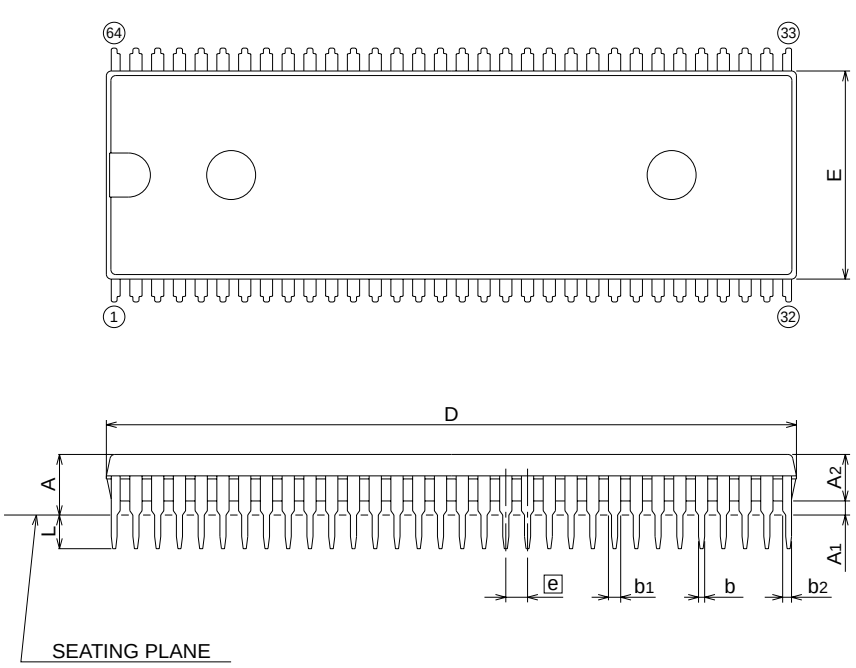
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	9.9	10.0	10.1
E	9.9	10.0	10.1
e	–	0.5	–
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
I2	1.0	–	–
MD	–	10.4	–
ME	–	10.4	–

64P4B

Plastic 64pin 750mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP64-P-750-1.78	–	7.9	Alloy 42



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.08
A_1	0.38	–	–
A_2	–	3.8	–
b	0.4	0.5	0.6
b_1	0.9	1.0	1.3
b_2	0.65	0.75	1.05
c	0.2	0.25	0.32
D	56.2	56.4	56.6
E	16.85	17.0	17.15
e	–	1.778	–
e1	–	19.05	–
L	2.8	–	–
θ	0°	–	15°

REVISION HISTORY	3803/3804 GROUP DATA SHEET

Rev.	Date	Description	
		Page	Summary
0.1	03/15/99		First Edition; Only including overview The issue including all information will be released in April.
1.0	05/25/99		Functional descriptions are added.
2.0	09/09/99	All pages	"PRELIMINARY Notice: This is..." eliminated.
		9	Product names are added into Figure 8.
		10	Product names are added into Table 3.
		34	Explanation of "Timer divider" of "8-bit Timers" is revised.
		52	Explanation of Note 7 is revised.
		60	Explanation of Note 7 is revised.
		63	Explanation of "A-D CONVERTER" is revised. Explanations of Figure 56 are partly revised.
		66	Explanations of "Watchdog Timer Initial Value" and "Watchdog Timer Operations" are revised. Explanations of Figure 60 are partly revised.
		67	Explanation of "MULTI-MASTER I^2C-BUS INTERFACE" is revised. Explanation of Note eliminated. Explanations of Figure 62 are partly revised.
		68	Explanations of "I^2C Data Shift Register" and "I^2C Address Registers 0 to 2" are revised.
		69	Explanation of Bit 5 of "I^2C Clock Control Register" is revised.
		75	Value of "Setup time" and "Hold time" into Table 13 are revised.
		76	Explanation of Bit 5 of "I^2C Special Mode Status Register" is added. Note is added into Figure 73.
		77	Explanation of Bit 1 of "I^2C Special Mode Control Register" is added. Explanation of Bit 6 of "I^2C Special Mode Control Register" is revised. Note is added into Figure 74.
		82	Register Contents of (21) into Figure 78 is revised.
		86	Explanations of Figure 82 are partly revised. Note 2 into Figure 82 is revised.
		117	Table 28 is revised for only flash memory version. Table 29 is added.
3.0	06/28/00	1	"●Minimum instruction execution time" of "FEATURES" is revised.
		1	"●Memory size" of "FEATURES" is revised.
		1	"<Flash memory mode>" of "FEATURES" is revised.
		1	"■Notes" of "FEATURES" is revised.
		9	Figure 8 is partly revised.
		11-13	Explanations of "CENTRAL PROCESSING UNIT (CPU)" are added.
		14	Explanation of bit 3 of "CPU mode register" is revised.

Rev.	Date	Description	
		Page	Summary
3.0	06/28/00	21	(7) into Figure 16 is partly revised.
		22	(14) into Figure 17 is partly revised.
		24	(7) into Figure 19 is partly revised.
		25	(14) into Figure 20 is partly revised.
		37	Explanations of “Timer divider” are partly eliminated.
		37	“●Prescaler 12” is added.
		37	Explanations of “Timer 1 and Timer 2” are partly eliminated.
		37	“Prescaler X and prescaler Y” is added.
		37	Explanations of “Timer X and Timer Y” are partly eliminated.
		37	Explanations of “●Mode selection” and “●Explanation of operation” of “(1) Timer mode” of “Timer X and Timer Y” are partly eliminated.
		37	“●Count source selection” and “●Interrupt” of “(1) Timer mode” of “Timer X and Timer Y” are eliminated.
		37	“●Count source selection” and “●Interrupt” of “(2) Pulse output mode” of “Timer X and Timer Y” are eliminated.
		37	Explanations of “●Explanation of operation” of “(2) Pulse output mode” of “Timer X and Timer Y” are partly added.
		37	Explanations of “■Precautions” of “(2) Pulse output mode” of “Timer X and Timer Y” are partly eliminated.
		38	Explanations of “●Mode selection” and “●Explanation of operation” of “(3) Event counter mode” of “Timer X and Timer Y” are revised.
		38	“●Interrupt” of “(3) Event counter mode” of “Timer X and Timer Y” are eliminated.
		38	“■Precautions” of “(3) Event counter mode” of “Timer X and Timer Y” are added.
		38	“●Count source selection” of “(4) Pulse width measurement mode” of “Timer X and Timer Y” are eliminated.
		38	Explanations of “●Explanation of operation” of “(4) Pulse width measurement mode” of “Timer X and Timer Y” are partly eliminated.
		38	Explanations of “■Precautions” of “(4) Pulse width measurement mode” of “Timer X and Timer Y” are revised.
		39	Bit name into Figure 29 is partly added.
		42	Explanations of “●Mode selection” of “(1) Timer mode” of “●16-bit Timers” are partly added.
		42	Explanations of “●Explanation of operation” of “(1) Timer mode” of “●16-bit Timers” are partly eliminated.
		42	Explanations of “●Mode selection” of “(3) Pulse output mode” of “●16-bit Timers” are partly added.
		43	Explanations of “●Mode selection” of “(4) Pulse period measurement mode” of “●16-bit Timers” are partly added.

Rev.	Date	Description	
		Page	Summary
3.0	06/28/00	43	Explanations of "●Mode selection" of "(5) Pulse width measurement mode" of "●16-bit Timers" are partly added.
		44	Explanations of "●Mode selection" of "(6) Programmable waveform generating mode" of "●16-bit Timers" are partly added.
		44	Explanations of "●Mode selection" of "(7) Programmable one-shot generating mode" of "●16-bit Timers" are partly added.
		45	Figure 32 is partly revised.
		46	Note into Figure 33 is added.
		55	Explanations of "7. Transmit interrupt request when transmit enable bit is set" are revised.
		63	Explanations of "7. Transmit interrupt request when transmit enable bit is set" are revised.
		68	Explanations of "D-A CONVERTER" are partly eliminated.
		70	Figure 64 is partly revised.
		71	Explanations of "[I^2C Slave Address Registers 0 to 2 (S0D0 to S0D2)]" are partly added.
		74	Explanations of "•Bit 3: Arbitration lost detecting flag (AL)" of "[I^2C Status Register (S1)]" are partly added.
		75	Explanations of "•Bit 7: Communication mode specification bit (master/slave specification bit: MST)" of "[I^2C Status Register (S1)]" are partly revised.
		78	"•Bit 7: Data receive mode at Stop/Low-speed mode bit (STR)" of "[I^2C START/STOP Condition Control Register (S2D)]" is eliminated.
		78	Explanations of b7 into Figure 74 are revised.
		79	"•Bit 4: Time out flag (TIOUT)" of "[I^2C Special Mode Status Register (S3)]" is eliminated.
		79	Figure 75 is partly revised.
		80	"•Bit 0: I^2C time out control bit (TOEN)" is eliminated.
		80	"•Bit 4: Time out flag clear bit (TOFCL)" is eliminated.
		80	Figure 76 is partly revised.
		80	Note into Figure 76 is added.
		84	Explanations of "RESET CIRCUIT" are partly revised.
		110	Explanations of "Functional Outline (CPU reprogramming mode)" of "(3) Flash
		111	memory mode 3 (CPU reprogramming mode)" are partly eliminated.
			Explanations of b3, b1, b0 into Figure 103 are partly revised.
		114	Explanations of "Instruction Execution Time" are partly reviesd.
		121	Table 31 is partly eliminated.
		122	Limits of RO into Table 34 are revised.
		123	Limits and unit of $t_w(\overline{RESET})$ into Table 35 are revised.
		123	Symbol of $t_h(S_{CLK3}–RxD_3)$ into Table 35 is revised.

Rev.	Date	Description	
		Page	Summary
3.0	06/28/00	124	Limits and unit of $t_W(\overline{RESET})$ into Table 36 are revised.
		125	Limits of $t_{WH}(S_{CLK1})$, $t_{WH}(S_{CLK3})$ into Tables 37 and 38 are partly added.
4.0	05/15/02	9	Figure 8 is partly revised.
		15	Sub-sub clause name of "●Middle-speed mode automatic switch by program" is partly eliminated.
		21	Figure 16 is partly revised.
		22	Figure 17 is partly revised.
		23	Figure 18 is partly revised.
		24	Figure 19 is partly revised.
		25	Figure 20 is partly revised.
		26	Figure 21 is partly revised.
		31	Explanations of "■Notes" are revised.
		42	Explanations of "●16-bit Timers" are partly revised.
		43	Explanations of "●Explanation of operation" of "(4) Pulse period measurement mode" are revised.
		43	Explanations of "●Explanation of operation" of "(5) Pulse width measurement mode" are revised.
		44	Explanations of "●Explanation of operation" of "(7) Programmable one-shot generating mode" are partly revised.
		54	Explanations of "●Note" of "2.1 Stop of transmission operation" are partly added.
		54	Explanations of "●Note 1 (only transmission operation is stopped)" of "2.3 Stop of transmit/receive operation" are partly added.
		55	Explanations of "5. Data transmission control with referring to transmit shift register completion flag" are partly added.
		56	Figure 46 is partly revised.
		62	Explanations of "●Note" of "2.1 Stop of transmission operation" are partly added.
		62	Explanations of "●Note 1 (only transmission operation is stopped)" of "2.2 Stop of transmit/receive operation" are partly added.
		63	Explanations of "5. Data transmission control with referring to transmit shift register completion flag" are partly added.
		70	Explanations of "MULTI-MASTER I^2C-BUS INTERFACE" are partly revised.
		71	Explanations of "[I^2C Data Shift Register (S0)]" are partly revised.
		76	Explanations of "START Condition Generating Method" are partly revised.
		77	Table 14 is partly revised.
		78	Table 15 is partly revised.
		83	Explanations of "2" of "(2) Start condition generating procedure using multi-master" are partly revised.
		87	Explanations of "CLOCK GENERATING CIRCUIT" are partly revised.
		87	Explanations of "■Note" of "(2) Wait mode" are partly added.
		89	Figure 84 is partly revised.
		91	Explanations of "(1) Flash memory mode 1 (parallel I/O mode)" are partly revised.
		91	Table 16 is partly revised.
		93	Figure 86 is partly revised.
		94	Figure 87 is partly revised.
		95	Explanations of "Read-only Mode" are partly revised.
		95	Explanations of "Read/Write Mode" are partly revised.
		96	Explanations of "●Read command" are partly revised.
		97	Explanations of "●Program command" are partly revised.
		97	Explanations of "●Program verify command" are partly revised.
		98	Explanations of "●Erase verify command" are partly revised.

Rev.	Date	Description	
		Page	Summary
4.0	05/15/02	101	Limits of t_{RC} into Table 21 are revised.
		101	Limits of $t_{a(AD)}$ into Table 21 are revised.
		101	Limits of $t_{a(CE)}$ into Table 21 are revised.
		101	Limits of $t_{a(OE)}$ into Table 21 are revised.
		102	Figure 93 is partly revised.
		103	Figure 94 is partly revised.
		115	"Electric Characteristic Differences Between Mask ROM and Flash Memory Version MCUs" is added.
		115	Explanations of "DATA REQUIRED FOR MASK ORDERS" are partly added.
		116	Explanations of "Note" into Table 27 are partly revised.
		117	V_{CC} into Table 28 are partly added.
		117	Parameter of V_{IH} into Table 28 is partly revised.
		129	64P6Q-A package outline is partly revised.
4.01	Nov. 14, 2003	6	Table 1 is partly revised.
		7	Table 2 is partly revised.
		13	Explanations of "[Processor status register (PS)]" are partly revised.
		19	Table 6 is partly revised.
		20	Table 7 is partly revised.
		31	Explanations of "■Notes" are partly revised.
		73	Figure 67 is partly revised.
		87	Explanations of "(2) Wait mode" is partly revised.
		89	Figure 84 is partly revised.
		93	Figure 86 is partly revised.
		94	Figure 87 is partly revised.
		102	Figure 93 is partly revised.
		103	Figure 94 is partly revised.
		122	Table 35 is partly revised.

Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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