38C2 Group (A Version)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0096-0200Z
Rev.2.00
May 28, 2004

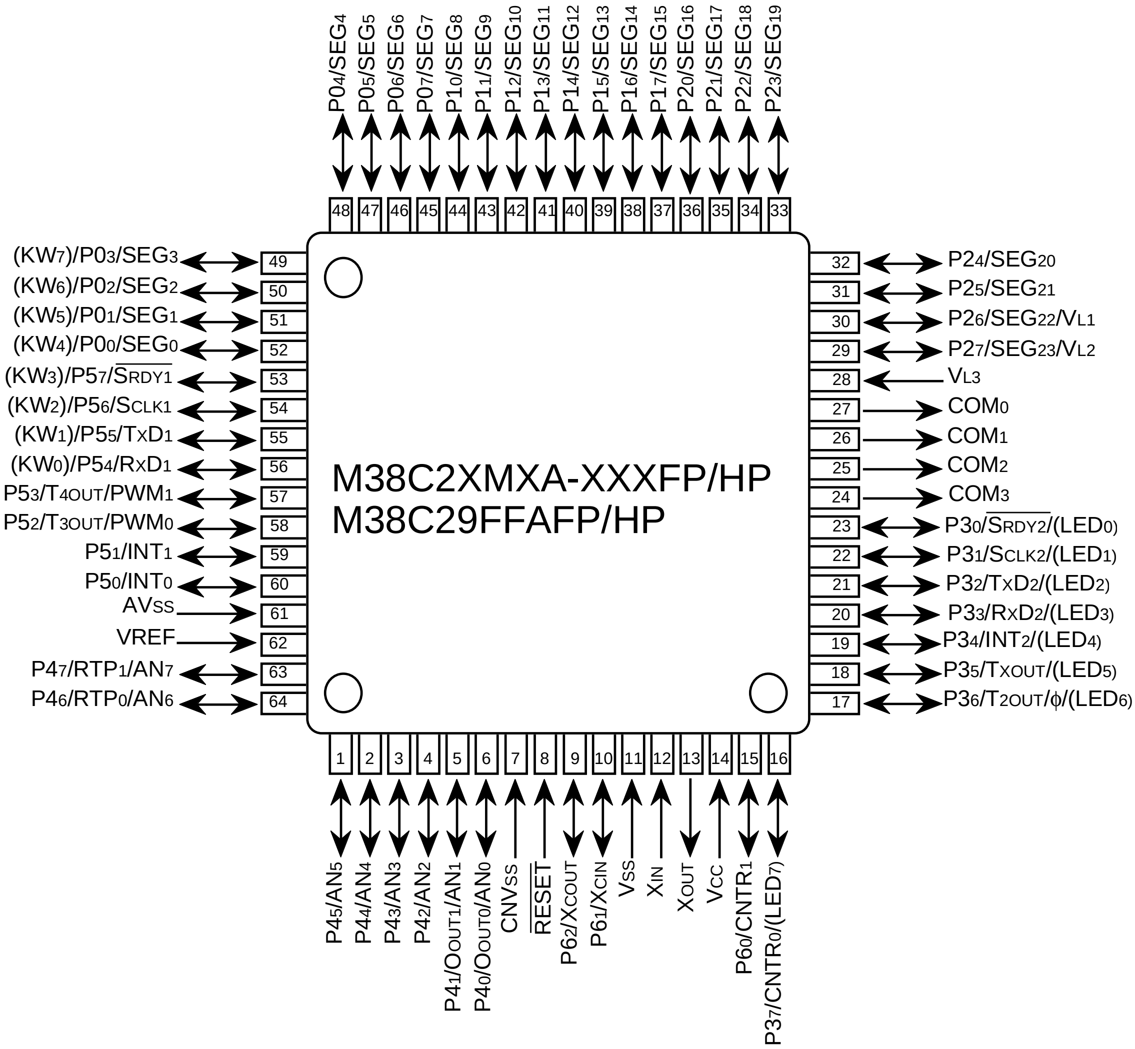
DESCRIPTION

The 38C2 group (A version) is the 8-bit microcomputer based on the 740 family core technology.
The 38C2 (A version) group has an LCD drive control circuit, a 10-channel A-D converter, and a serial I/O as additional functions.
The various microcomputers in the 38C2 group (A version) include variations of internal memory size and packaging. For details, refer to the section on part numbering.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time .... 0.40 µs
  (at 10 MHz oscillation frequency)
- Memory size
  ROM .... 16 K to 60 K bytes
  RAM .... 640 to 2048 bytes
- Programmable input/output ports .... 51 (common to SEG: 24)
- Interrupts .... 18 sources, 16 vectors
- Timers .... 8-bit × 4, 16-bit × 2
- A-D converter .... 10-bit × 8 channels
- Serial I/O .... 8-bit × 2 (UART or Clock-synchronized)
- PWM .... 10-bit × 2, 16-bit × 1 (common to IGBT output)
- LCD drive control circuit
  Bias 1/2, 1/3
  Duty 1/2, 1/3, 1/4
  Common output 4
  Segment output 24
- Two clock generating circuits
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Watchdog timer .... 8-bit × 1
- LED direct drive port 8
  (average current: 15 mA, peak current: 30 mA, total current: 90 mA)
- Power source voltage
  - Mask ROM version
    In frequency/2 mode .... 4.5 to 5.5 V
    (at 10 MHz oscillation frequency)
    In frequency/2 mode .... 4.0 to 5.5 V
    (at 8 MHz oscillation frequency)
    In frequency/4 mode .... 1.8 to 5.5 V
    (at 4 MHz oscillation frequency, A-D operation excluded)
    In low-speed mode .... 1.8 to 5.5 V
    (at 32 kHz oscillation frequency)
  - Flash memory version
    In frequency/2 mode .... 4.5 to 5.5 V
    (at 10 MHz oscillation frequency)
    In frequency/2 mode .... 4.0 to 5.5 V
    (at 8 MHz oscillation frequency)
    In frequency/4 mode .... 2.5 to 5.5 V
    (at 8 MHz oscillation frequency)
    In low-speed mode .... 2.5 to 5.5 V
    (at 32 kHz oscillation frequency)
- Power dissipation
  - In frequency/2 mode (at 8 MHz oscillation frequency, V_{CC} = 5 V)
    Mask ROM version .... 14 mW
    Flash memory version .... 25 mW
  - In low-speed mode (at 32 kHz oscillation frequency, V_{CC} = 3 V)
    Mask ROM version .... 24 µW
    Flash memory version .... 375 µW
- Operating temperature range .... – 20 to 85°C

PIN CONFIGURATION
(TOP VIEW)



Package type : 64P6U-A/64P6Q-A

Fig. 1 M38C2XMXA-XXXFP/HP pin configuration

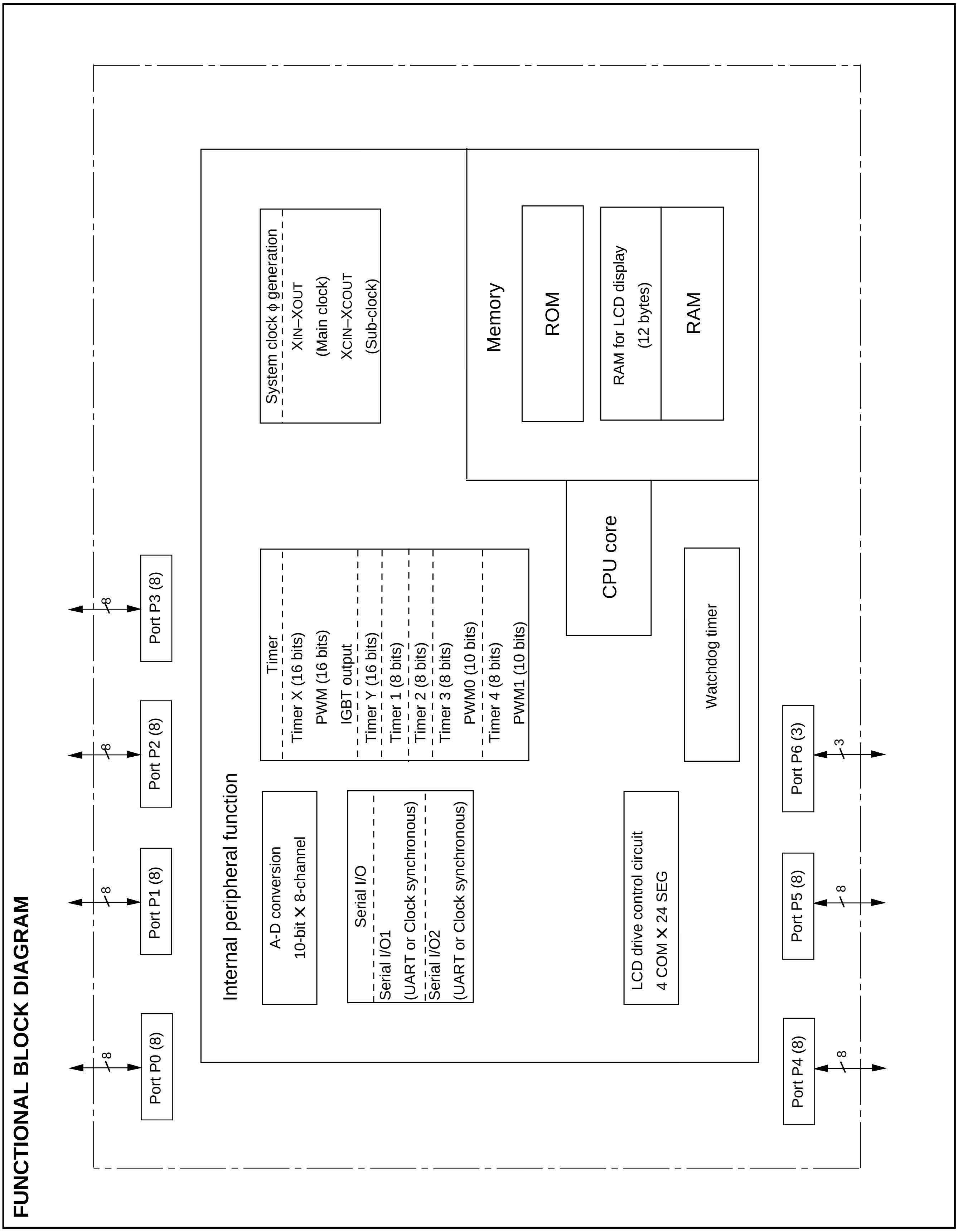


Fig. 2 Functional block diagram

RENESAS

PIN DESCRIPTION

Table 1 Pin description (1)

Pin	Name	Function	Function except a port function	
VCC, VSS	Power source	• Apply voltage of 1.8 V to 5.5 V to VCC, and 0 V to VSS.		
VREF	Analog reference voltage	• Reference voltage input pin for A-D converter.		
AVSS	Analog power source	• GND input pin for A-D converter. Connect to VSS.		
$\overline{\text{RESET}}$	Reset input	• Reset input pin for active "L."		
XIN	Clock input	• Input and output pins for the main clock generating circuit. • Feedback resistor is built in between XIN pin and XOUT pin.		
XOUT	Clock output	• Connect a ceramic resonator or a quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. When an external clock is used, connect the clock source to XIN, and leave XOUT pin open.		
VL3	LCD power source	• Input 0 ≤ VL1 ≤ VL2 ≤ VL3 ≤ VCC voltage. • Input 0 – VL3 voltage to LCD.		
COM0 – COM3	Common output	• LCD common output pins. • COM2 and COM3 are not used at 1/2 duty ratio. • COM3 is not used at 1/3 duty ratio.		
P00/SEG0 – P03/SEG3	I/O port P0	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled in a bit unit.	• LCD segment output pins	• Key input interrupt pins
P04/SEG4 – P07/SEG7				
P10/SEG8 – P17/SEG15	I/O port P1			
P20/SEG16 – P25/SEG21	I/O port P2			
P26/SEG22/VL1 P27/SEG23/VL2				• LCD power source input pins
P30/$\overline{\text{SRDY2}}$ P31/SCLK2 P32/TxD2 P33/RxD2	I/O port P3		• Serial I/O2 function pins	
P34/INT2			• External interrupt pin	
P35/TXOUT P36/T2OUT/φ			• Timer X, Timer 2 output pins	
P37/CNTR0			• Timer X function pin	
P40/OOUT0/AN0 P41/OOUT1/AN1	I/O port P4		• AD converter input pins	• Oscillation external output pins
P42/AN2– P45/AN5				
P46/RTP0/AN6 P47/RTP1/AN7				• Real time port function pins
P50/INT0 P51/INT1	I/O port P5		• External interrupt pins	
P52/T3OUT/PWM0 P53/T4OUT/PWM1			• Timer 3, Timer 4 output pins • PWM output pins	
P54/RxD1 P55/TxD1 P56/SCLK1 P57/$\overline{\text{SRDY1}}$			• Serial I/O1 function pins • Key input interrupt input pins	

PIN DESCRIPTION

Table 2 Pin description (2)

Pin	Name	Function	Function except a port function
$P6_0/CNTR_1$	I/O port P6	• 3-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Timer Y function pin
$P6_1/X_{CIN}$ $P6_2/X_{COUT}$			• Sub clock generating I/O pin (resonator connected)
CNV_{SS}	CNV_{SS}	• V_{PP} power input pin in the flash mode. When MCU is operating, connect to V_{SS}.	

PART NUMBERING

Product M38C2 9 M C A– XXX HP

Package type
FP : 64P6U-A package
HP : 64P6Q-A package

ROM number
Omitted in Flash memory version.

Characteristics
A : A version

ROM/Flash memory size

1 : 4096 bytes	9 : 36864 bytes
2 : 8192 bytes	A : 40960 bytes
3 : 12288 bytes	B : 45056 bytes
4 : 16384 bytes	C : 49152 bytes
5 : 20480 bytes	D : 53248 bytes
6 : 24576 bytes	E : 57344 bytes
7 : 28672 bytes	F : 61440 bytes
8 : 32768 bytes	

The first 128 bytes and the last 2 bytes of ROM are reserved areas ; they cannot be used.

Memory type
M : Mask ROM version
F : Flash memory version

RAM size
0 : 192 bytes
1 : 256 bytes
2 : 384 bytes
3 : 512 bytes
4 : 640 bytes
5 : 768 bytes
6 : 896 bytes
7 : 1024 bytes
8 : 1536 bytes
9 : 2048 bytes

Fig. 3 Part numbering

GROUP EXPANSION

Renesas plans to expand the 38C2 group (A version) as follows.

Memory Type

Support for mask ROM, Flash memory versions

Memory Size

ROM/flash memory size .... 16 K to 60 K bytes
RAM size .... 640 to 2048 bytes

Packages

64P6Q-A .... 0.5 mm-pitch plastic molded QFP
64P6U-A .... 0.8 mm-pitch plastic molded QFP

Memory Expansion Plan

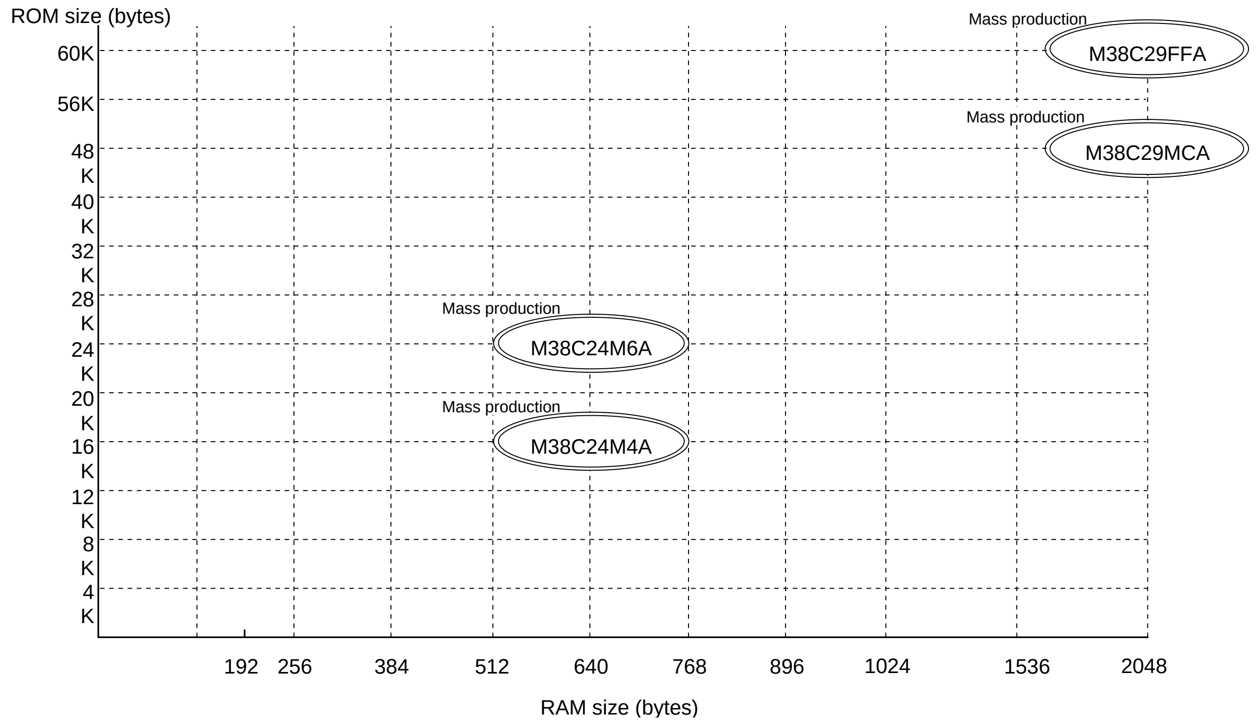


Fig. 4 Memory expansion plan

Currently supported products are listed below.

Table 3 Support products

As of May.2004

Product name	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38C29MCA-XXXFP	49152 (49022)	2048	64P6U-A	Mask ROM version
M38C29MCA-XXXHP			64P6Q-A	Mask ROM version
M38C24M6A-XXXFP	24576 (24446)	640	64P6U-A	Mask ROM version
M38C24M6A-XXXHP			64P6Q-A	Mask ROM version
M38C24M4A-XXXFP	16384 (16254)	640	64P6U-A	Mask ROM version
M38C24M4A-XXXHP			64P6Q-A	Mask ROM version
M38C29FFAFP	61440 (61310)	2048	64P6U-A	Flash memory version
M38C29FFAHP			64P6Q-A	Flash memory version

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The 38C2 group uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

The central processing unit (CPU) has six registers. Figure 5 shows the 740 Family CPU register structure.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as arithmetic data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

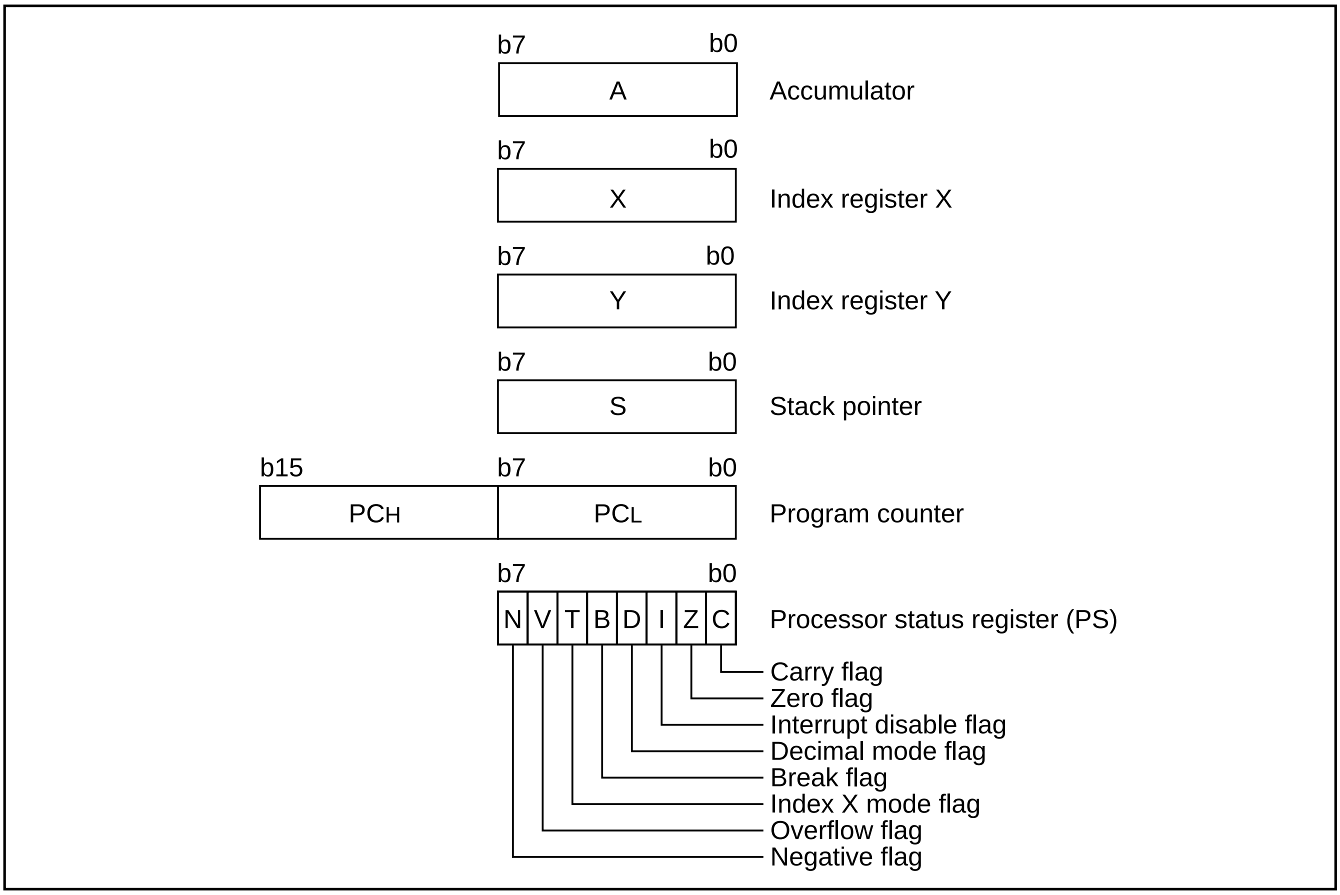


Fig. 5 740 Family CPU register structure

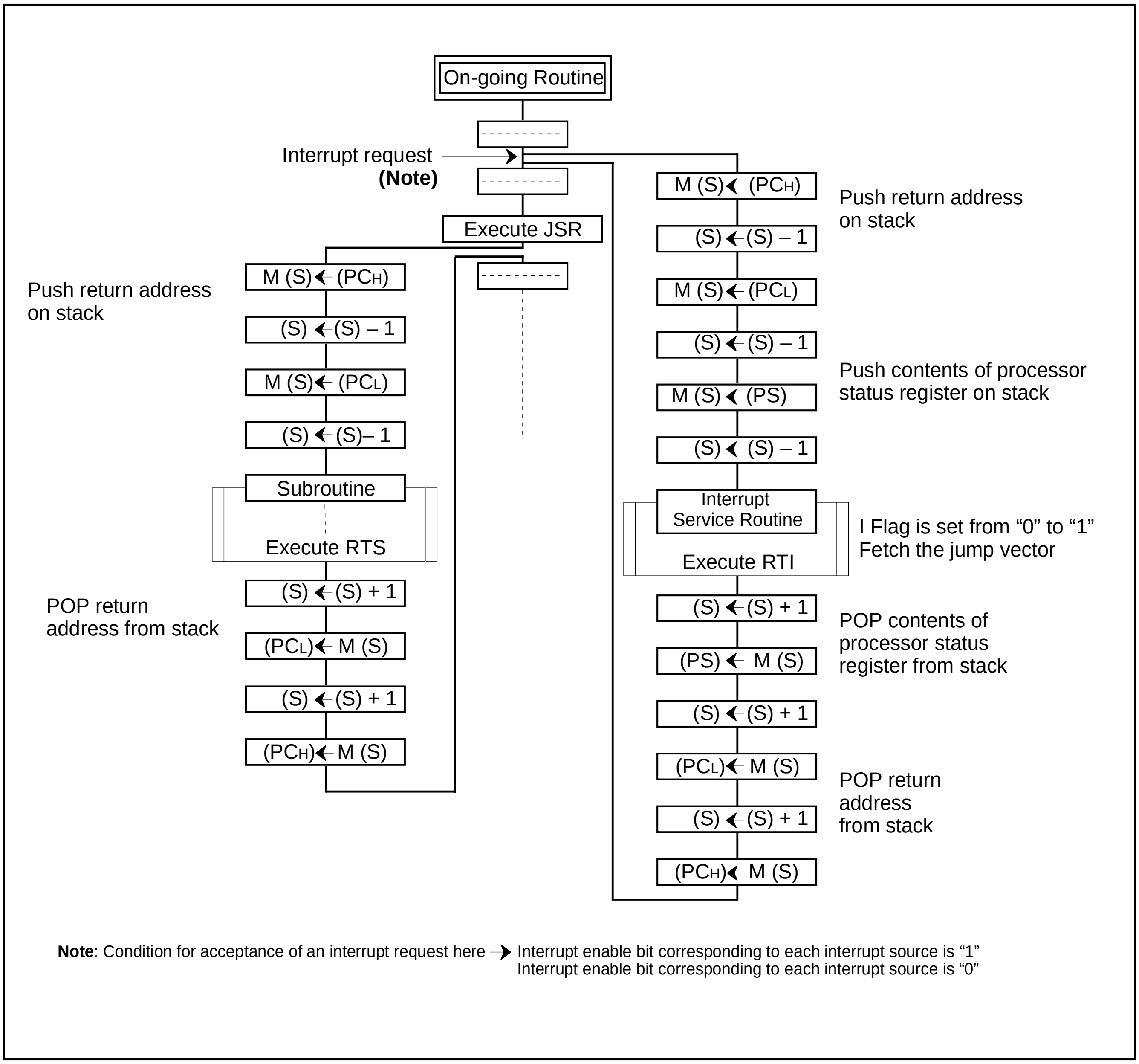


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor Status Register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

- Bit 0: Carry flag (C)
  The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.
- Bit 1: Zero flag (Z)
  The Z flag is set to “1” if the result of an immediate arithmetic operation or a data transfer is “0”, and set to “0” if the result is anything other than “0”.
- Bit 2: Interrupt disable flag (I)
  The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
  Interrupts are disabled when the I flag is “1”.
- Bit 3: Decimal mode flag (D)
  The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”.
  Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.
- Bit 4: Break flag (B)
  The B flag is used to indicate that the current interrupt was generated by the BRK instruction. When the BRK instruction is generated, the B flag is set to “1” automatically. When the other interrupts are generated, the B flag is set to “0”, and the processor status register is pushed onto the stack.
- Bit 5: Index X mode flag (T)
  When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.
- Bit 6: Overflow flag (V)
  The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.
- Bit 7: Negative flag (N)
  The N flag is set to “1” if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] $003B_{16}$

The CPU mode register contains the stack page selection bit and the control bit for the internal system clock.
The CPU mode register is allocated at address $003B_{16}$.

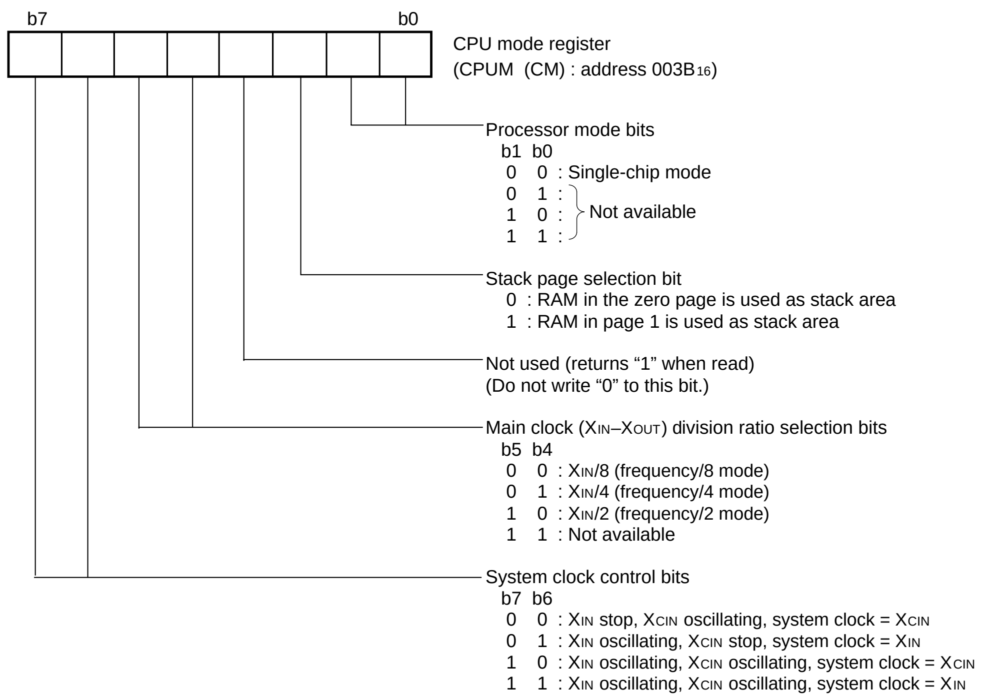


Fig. 7 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$
1536	$063F_{16}$
2048	$083F_{16}$

ROM area

ROM size (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}
36864	7000_{16}	7080_{16}
40960	6000_{16}	6080_{16}
45056	5000_{16}	5080_{16}
49152	4000_{16}	4080_{16}
53248	3000_{16}	3080_{16}
57344	2000_{16}	2080_{16}
61440	1000_{16}	1080_{16}

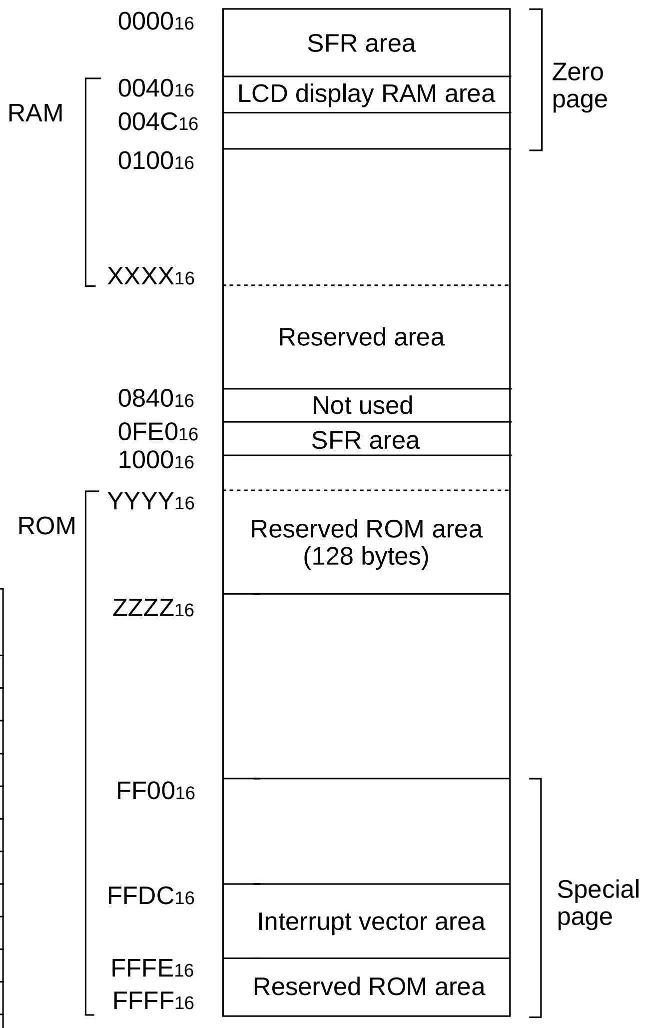


Fig. 8 Memory map diagram

Address	Register	Address	Register
0000_{16}	Port P0 (P0)	0020_{16}	Timer 1 (T1)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Timer 2 (T2)
0002_{16}	Port P1 (P1)	0022_{16}	Timer 3 (T3)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Timer 4 (T4)
0004_{16}	Port P2 (P2)	0024_{16}	PWM01 register (PWM01)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer 12 mode register (T12M)
0006_{16}	Port P3 (P3)	0026_{16}	Timer 34 mode register (T34M)
0007_{16}	Port P3 direction register (P3D)	0027_{16}	
0008_{16}	Port P4 (P4)	0028_{16}	Compare register (low-order) (COMPL)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Compare register (high-order) (COMPH)
$000A_{16}$	Port P5 (P5)	$002A_{16}$	Timer X (low-order) (TXL)
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	Timer X (high-order) (TXH)
$000C_{16}$	Port P6 (P6)	$002C_{16}$	Timer X (extension) (TXEX)
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	Timer Y (low-order) (TYL)
$000E_{16}$		$002E_{16}$	Timer Y (high-order) (TYH)
$000F_{16}$		$002F_{16}$	Timer X mode register (TXM)
0010_{16}		0030_{16}	Timer Y mode register (TYM)
0011_{16}		0031_{16}	
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	
0015_{16}		0035_{16}	
0016_{16}		0036_{16}	
0017_{16}		0037_{16}	Watchdog timer control register (WDTCON)
0018_{16}	Clock output control register (CKOUT)	0038_{16}	LCD power control register (VLCON)
0019_{16}	A-D control register (ADCON)	0039_{16}	LCD mode register (LM)
$001A_{16}$	A-D conversion register (low-order) (ADL)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	A-D conversion register (high-order) (ADH)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Transmit/receive buffer register 1 (TB1/RB1)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Serial I/O1 status register (SIO1STS)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$	Transmit/receive buffer register 2 (TB2/RB2)	$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Serial I/O2 status register (SIO2STS)	$003F_{16}$	Interrupt control register 2 (ICON2)
$0FE0_{16}$	Serial I/O1 control register (SIO1CON)	$0FF0_{16}$	Oscillation output control register (OSCOUT)
$0FE1_{16}$	UART1 control register (UART1CON)	$0FF1_{16}$	PULL register (PULL)
$0FE2_{16}$	Baudrate generator 1 (BRG1)	$0FF2_{16}$	Key input control register (KIC)
$0FE3_{16}$	Serial I/O2 control register (SIO2CON)	$0FF3_{16}$	Timer 1234 mode register (T1234M)
$0FE4_{16}$	UART2 control register (UART2CON)	$0FF4_{16}$	Timer X control register (TXCON)
$0FE5_{16}$	Baudrate generator 2 (BRG2)	$0FF5_{16}$	Timer 12 frequency division selection register (PRE12)
$0FE6_{16}$		$0FF6_{16}$	Timer 34 frequency division selection register (PRE34)
$0FE7_{16}$		$0FF7_{16}$	Timer XY frequency division selection register (PREXY)
$0FE8_{16}$		$0FF8_{16}$	Segment output disable register 0 (SEG0)
$0FE9_{16}$		$0FF9_{16}$	Segment output disable register 1 (SEG1)
$0FEA_{16}$		$0FFA_{16}$	Segment output disable register 2 (SEG2)
$0FEB_{16}$		$0FFB_{16}$	Timer Y mode register 2 (TYM2)
$0FEC_{16}$		$0FFC_{16}$	
$0FED_{16}$		$0FFD_{16}$	
$0FEE_{16}$		$0FFE_{16}$	Flash memory control register (FMCR)
$0FEF_{16}$		$0FFF_{16}$	Reserved area (access disabled)

Fig. 9 Memory map of special function register (SFR)

I/O PORTS

Direction Registers

The I/O ports P0–P6 have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

When “0” is written to the bit of the direction register, the corresponding pin becomes an input pin. As for ports P0–P2, when “1” is written to the bit of the direction register and the segment output disable register, the corresponding pin becomes an output pin. As for ports P3–P6, when “1” is written to the bit of the direction register, the corresponding pin becomes an output pin.

If data is read from a pin set to output, the value of the port latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Pull-up Control

Each individual bit of ports P0–P2 can be pulled up with a program by setting direction registers and segment output disable registers 0 to 2 (addresses $0FF8_{16}$ to $0FFA_{16}$).

The pin is pulled up by setting “0” to the direction register and “1” to the segment output disable register.

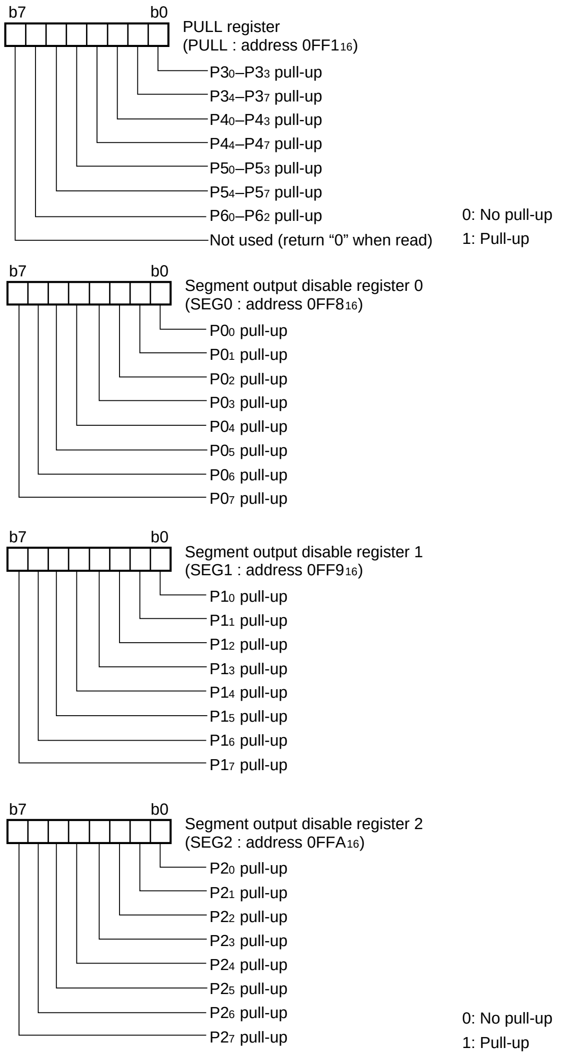
By setting the PULL register (address $0FF1_{16}$), ports P3–P6 can control pull-up with a program.

However, the contents of PULL register do not affect ports programmed as the output ports.

Segment output disable register / Direction register	“0”	“1”
“0”	Input port No pull-up	Input port Pull-up
“1”	Segment output	Port output

Initial state

Fig. 10 Structure of ports P0 to P2



Notes 1: The PULL register and segment output disable register affect only ports programmed as the input ports.

2: When the VL pin input selection bit (VLSEL) of the LCD power control register (address 0038_{16}) is “1”, settings of $P2_6$ and $P2_7$ are invalid.

Fig. 11 Structure of PULL register and segment output disable register

Table 6 List of I/O port function

Pin	Name	Input/Output	I/O format	Non-port function		Related SFRs	Ref. No.
P00/SEG0 – P03/SEG3	Port P0	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	LCD segment output	Key input (key-on wakeup) interrupt input	Segment output disable register 1	(1)
P04/SEG4 – P07/SEG7							(2)
P10/SEG8 – P17/SEG15	Port P1	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output			Segment output disable register 2	
P20/SEG16 – P25/SEG21	Port P2	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output			Segment output disable register 3	
P26/SEG22/VL1 P27/SEG23/VL2					LCD power input		
P30/$\overline{\text{SRDY2}}$ P31/SCLK2 P32/TxD2 P33/RxD2	Port P3	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O		PULL register Serial I/O2 control register Serial I/O2 status register UART2 control register	(3) (4) (5) (6)
P34/INT2				External interrupt input		PULL register Interrupt edge selection register	(7)
P35/TXOUT P36/T2OUT/φ				Timer X output Timer 2 output		PULL register Timer X mode register Timer 12 mode register	(8) (9)
P37/CNTR0				Timer X function input		PULL register Timer X mode register	(7)
P40/OOUT0/AN0 P41/OOUT1/AN1	Port P4	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	A-D conversion input	Oscillation external output	PULL register A-D control register	(11)
P42/AN2– P45/AN5							(10)
P46/RTP0/AN6 P47/RTP1/AN7					Real time port function output	PULL register A-D control register Timer Y mode register	(11)
P50/INT0 P51/INT1	Port P5	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	External interrupt input		PULL register Interrupt edge selection register	(7)
P52/T3OUT/PWM0 P53/T4OUT/PWM1				Timer 3 output Timer 4 output PWM output		PULL register Timer 12 mode register	(9)
P54/RxD1 P55/TxD1 P56/SCLK1 P57/$\overline{\text{SRDY1}}$				Serial I/O1 function I/O	Key input (key-on wakeup) interrupt input	PULL register Serial I/O1 control register Serial I/O1 status register UART1 control register	(12) (13) (14) (15)
P60/CNTR1	Port P6	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Timer Y function input		PULL register Timer Y mode register	(7)
P61/XCIN				Sub-clock oscillation circuit		PULL register	(16)
P62/XCOUT						CPU mode register	(17)
COM0–COM3	Common	Output	LCD common output			LCD mode register	(18)

Notes 1: For details of how to use double/triple function ports as function I/O ports, refer to the applicable sections.
2: Make sure that the input level at each pin is either 0 V or VCC during execution of the STP instruction.
When an input level is at an intermediate potential, a current will flow from VCC to VSS through the input-stage gate.

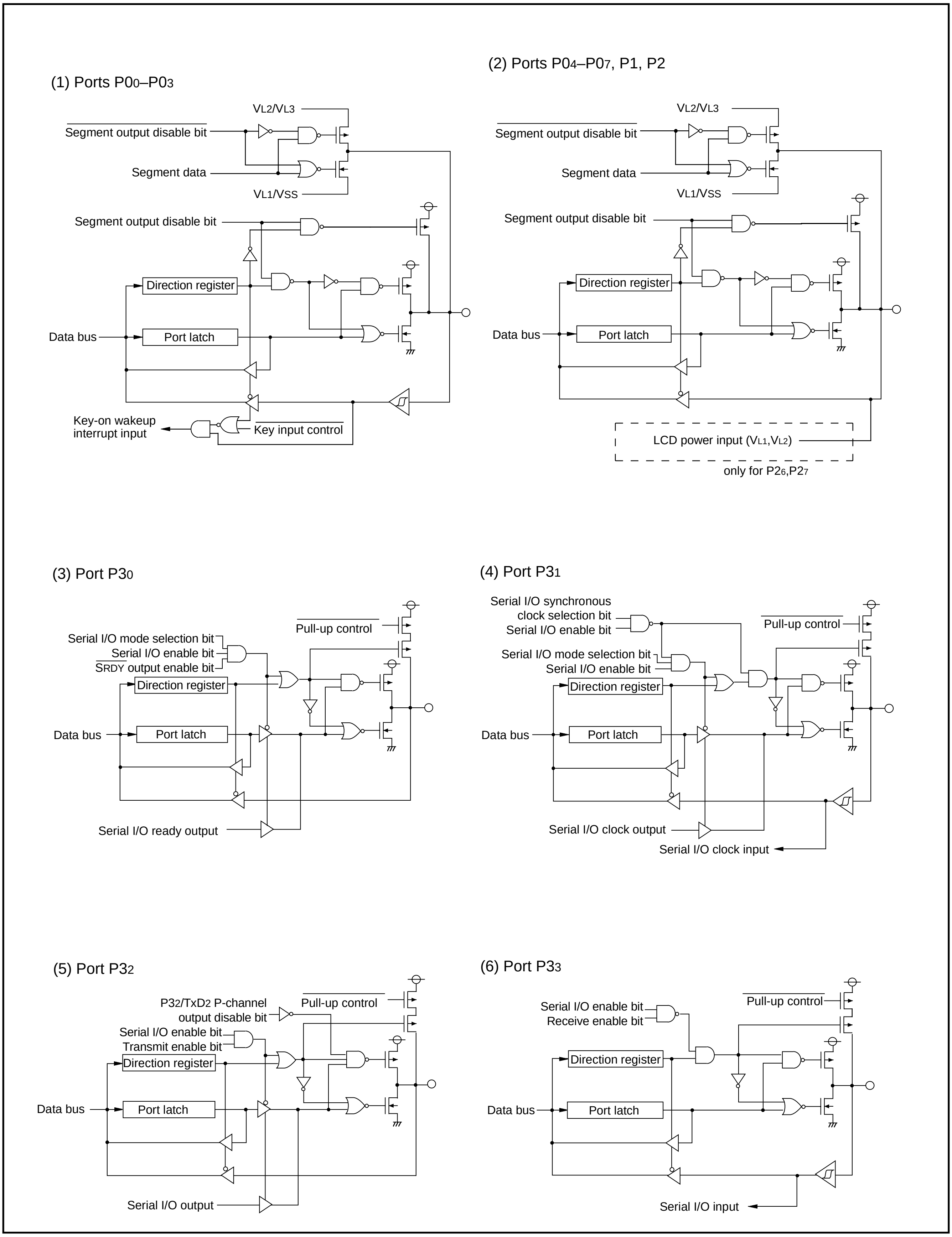


Fig. 12 Port block diagram (1)

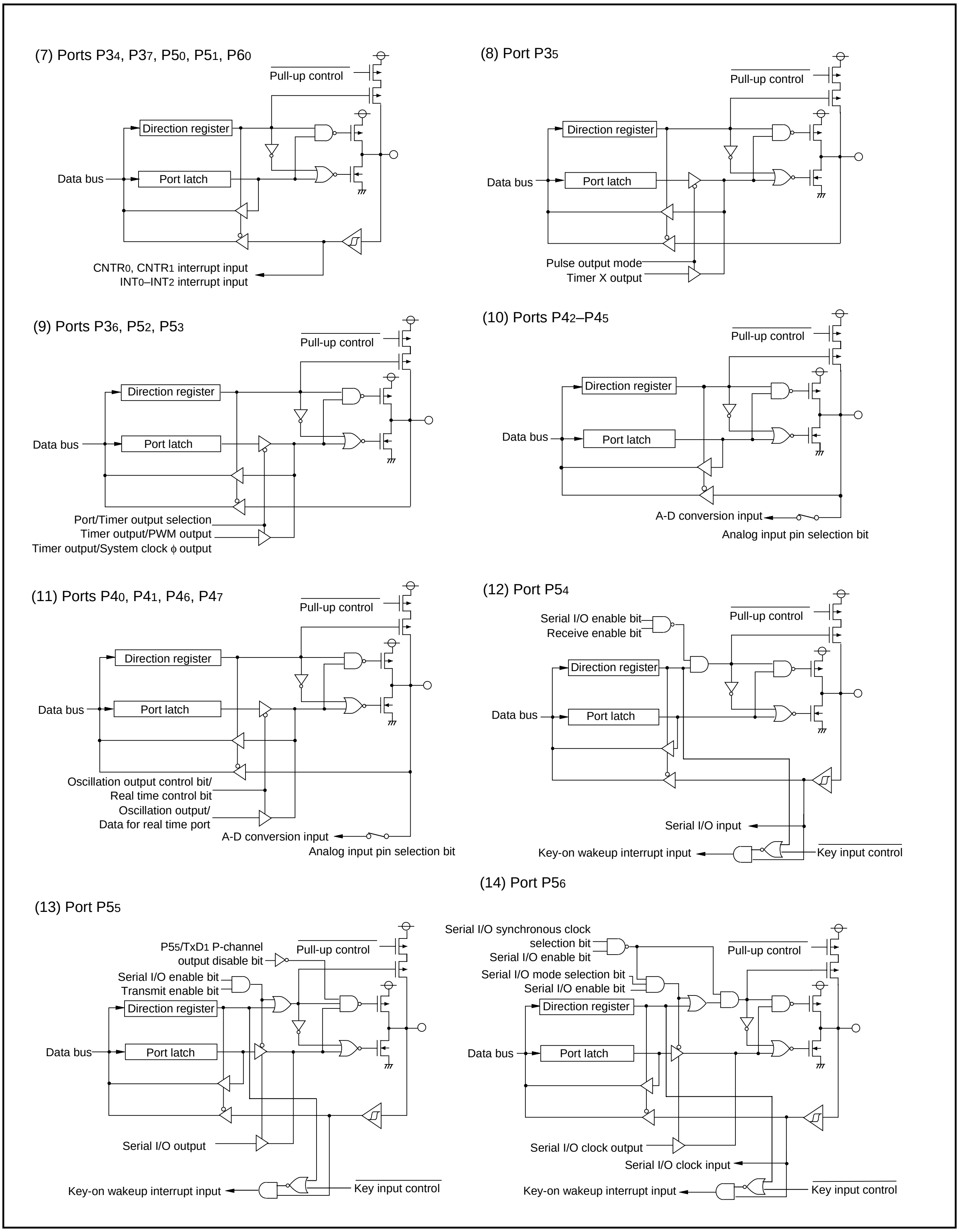


Fig. 13 Port block diagram (2)

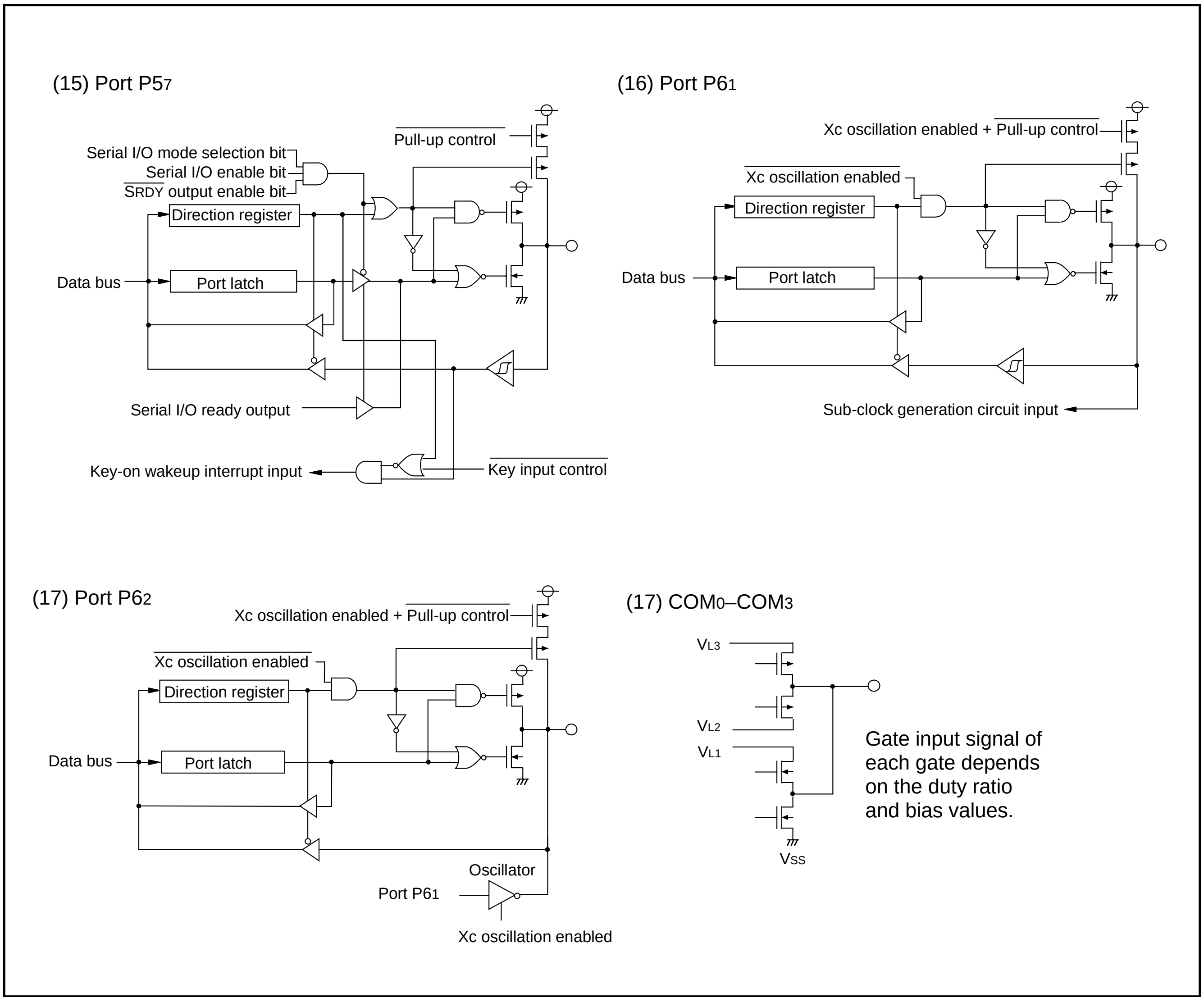


Fig. 14 Port block diagram (3)

INTERRUPTS

Interrupts occur by nineteen sources: six external, twelve internal, and one software.

Interrupt Control

Each interrupt except the BRK instruction interrupt have both an interrupt request bit and an interrupt enable bit, and is controlled by the interrupt disable flag. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”.

Interrupt enable bits can be set or cleared by program. Interrupt request bits can be cleared by program, but cannot be set by software.

The BRK instruction interrupt and reset cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt and reset. If several interrupt requests occur at the same time, the interrupt with highest priority is accepted first.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set to “1” and the corresponding interrupt request bit is set to “0”.
3. The interrupt jump destination address is read from the vector table into the program counter.

■ Notes on Interrupts

When setting the followings, the interrupt request bit may be set to “1”.

•When switching external interrupt active edge
 Related register: Interrupt edge selection register (address $3A_{16}$)
 Timer X control register (address $FF4_{16}$)
 Timer Y mode register (address 30_{16})

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
 Related register: Interrupt edge selection register (address $3A_{16}$)

When not requiring the interrupt occurrence synchronous with these setting, take the following sequence.

①Set the corresponding interrupt enable bit to “0” (disabled).
②Set the interrupt edge select bit (polarity switch bit) or the interrupt source selection bit.
③Set the corresponding interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the corresponding interrupt enable bit to “1” (enabled).

Table 7 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1) High	Vector Addresses (Note 1) Low	Interrupt Request Generating Conditions	Remarks
Reset **(Note 2)**	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
INT_2	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_2 input	Valid when INT_2 interrupt is selected External interrupt (active edge selectable)
Key input (key-on wakeup)				At falling of ports $P0_0$–$P0_3$, $P5_4$–$P5_7$ input logical level AND	Valid when key input interrupt is selected External interrupt (falling valid)
Serial I/O1 receive	5	$FFF5_{16}$	$FFF4_{16}$	At completion of serial I/O1 data receive	Valid only when serial I/O1 is selected
Serial I/O1 transmit	6	$FFF3_{16}$	$FFF2_{16}$	At completion of serial I/O1 transmit shift or transmit buffer is empty	Valid only when serial I/O1 is selected
Serial I/O2 receive	7	$FFF1_{16}$	$FFF0_{16}$	At completion of serial I/O2 data receive	Valid only when serial I/O2 is selected
Serial I/O2 transmit	8	$FFEF_{16}$	$FFEE_{16}$	At completion of serial I/O2 transmit shift or transmit buffer is empty	Valid only when serial I/O2 is selected
Timer X	9	$FFED_{16}$	$FFEC_{16}$	At timer X underflow	
Timer 1	10	$FFEB_{16}$	$FFEA_{16}$	At timer 1 underflow	Valid only when timer 1 interrupt is selected
Timer 2	11	$FFE9_{16}$	$FFE8_{16}$	At timer 2 underflow	Valid only when timer 2 interrupt is selected
Timer 3	12	$FFE7_{16}$	$FFE6_{16}$	At timer 3 underflow	
Timer 4	13	$FFE5_{16}$	$FFE4_{16}$	At timer 4 underflow	
$CNTR_0$	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
Timer Y	15	$FFE1_{16}$	$FFE0_{16}$	At timer Y underflow	
$CNTR_1$				At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
A-D conversion	16	$FFDF_{16}$	$FFDE_{16}$	At completion of A-D conversion	Valid when A-D conversion interrupt is selected
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

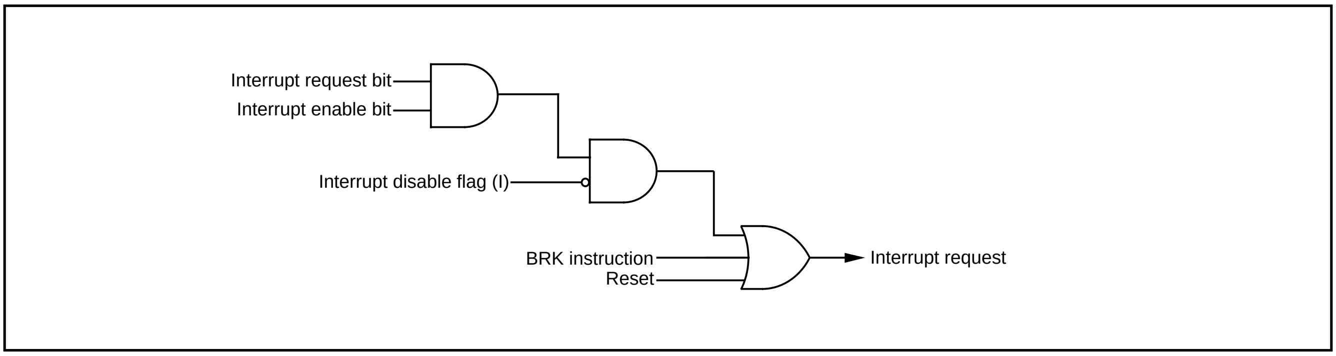


Fig. 15 Interrupt control

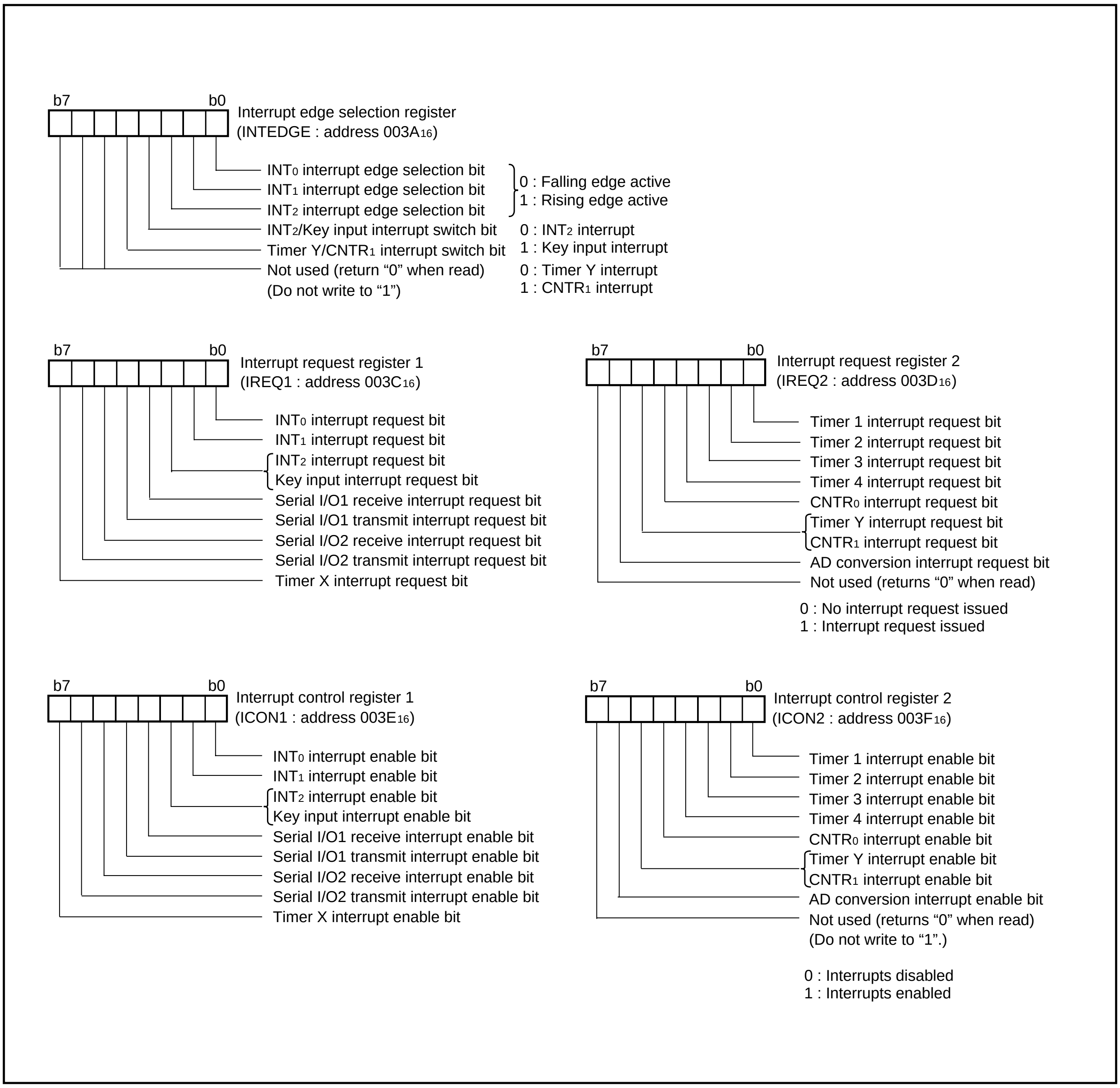


Fig. 16 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake-Up)

A key input interrupt request is generated by detecting the falling edge from any pin of ports P00–P03, P54–P57 that have been set to input mode. In other words, it is generated when AND of input level goes from “1” to “0”. An example of using a key input interrupt is shown in Figure 17, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P54–P57.

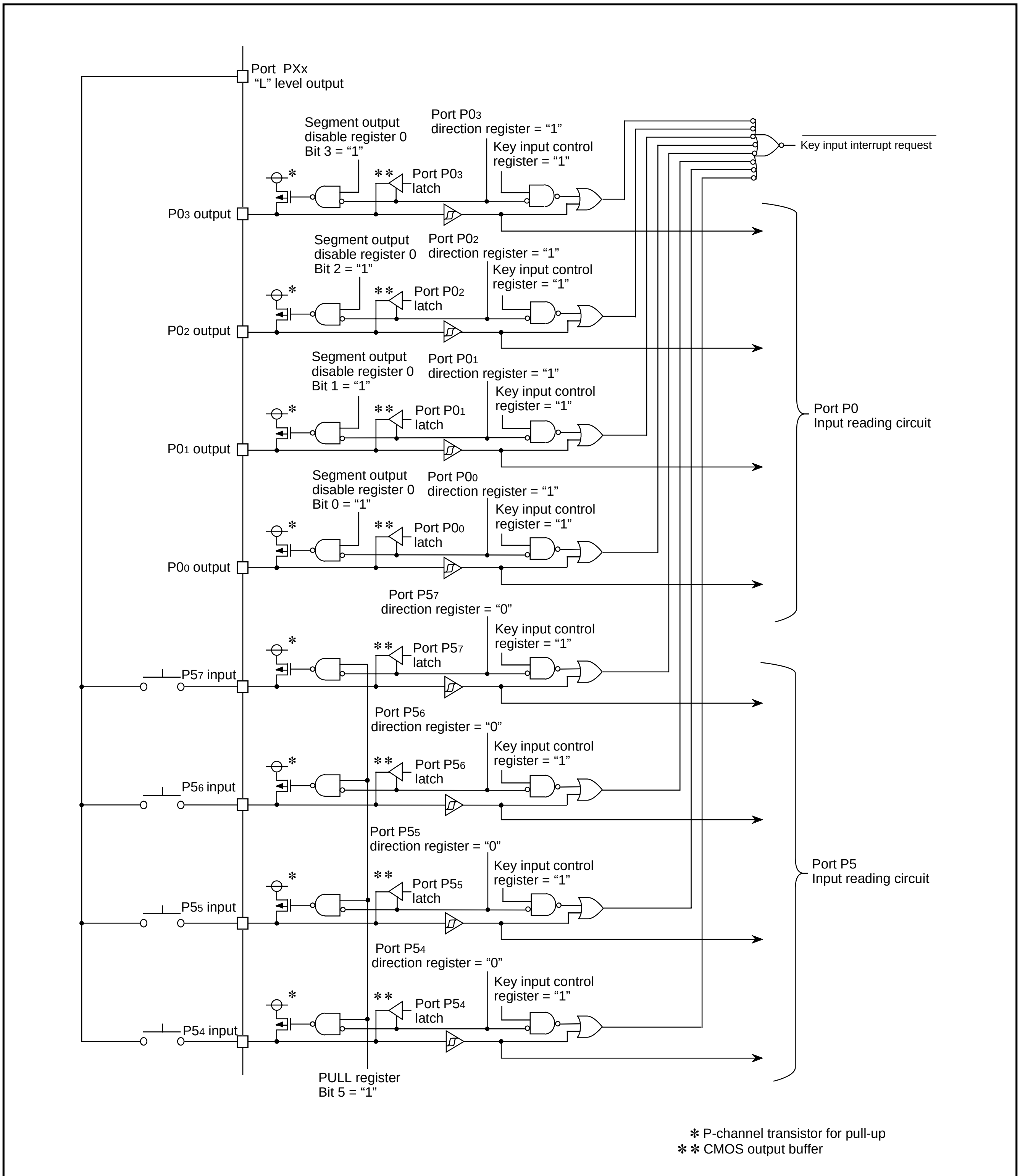


Fig. 17 Connection example when using key input interrupt and ports P0 and P5 block diagram

A key input interrupt is controlled by the key input control register and port direction registers. When the key input interrupt is enabled, set "1" to the key input control register. A key input of any pin of ports $P0_0$–$P0_3$, $P5_4$–$P5_7$ that have been set to input mode is accepted.

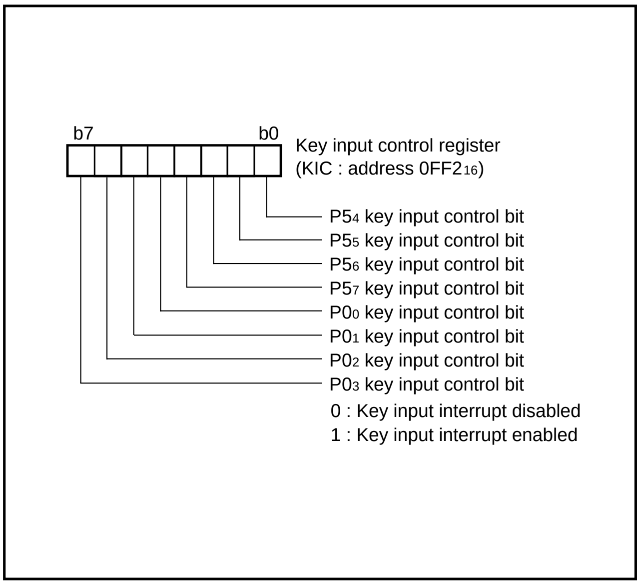


Fig. 18 Structure of key input control register

TIMERS
8-Bit Timer

The 38C2 group has four built-in timers : Timer 1, Timer 2, Timer 3, and Timer 4.
Each timer has the 8-bit timer latch. All timers are down-counters. When the timer reaches “00_{16}”, the contents of the timer latch is reloaded into the timer with the next count pulse. In this mode, the interrupt request bit corresponding to that timer is set to “1”.
The count can be stopped by setting the stop bit of each timer to “1”.

● Frequency Divider For Timer

Timer 1, timer 2, timer 3 and timer 4 have the frequency divider for the count source. The count source of the frequency divider is switched to X_{IN} or X_{CIN} by the CPU mode register. The frequency divider is controlled by each timer division ratio selection bit. The division ratio can be selected from as follows;
1/1, 1/2, 1/16, 1/32, 1/64, 1/128, 1/256, 1/1024 of f(X_{IN}); or f(X_{CIN}).

● Timer 1, Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register.
When f(X_{CIN}) is selected as the count source, counting can be performed regardless of X_{CIN} oscillation. However, when X_{CIN} is stopped, the external pulse input from X_{CIN} pin is counted. Also, by the timer 12 mode register, each time timer 2 underflows, the signal of which polarity is inverted can be output from $P3_6/T_{2OUT}$ pin.
At reset, all bits of the timer 12 mode register are set to “0,” timer 1 is set to “FF_{16}”, and timer 2 is set to “01_{16}”.
When executing the STP instruction, previously set the wait time at return.

● Timer 3, Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register. Also, by the timer 34 mode register, each time timer 3 or timer 4 underflows, the signal of which polarity is inverted can be output from $P5_2/T_{3OUT}$ pin or $P5_3/T_{4OUT}$ pin.

● Timer 3 PWM0 Mode, Timer 4 PWM1 Mode

A PWM rectangular waveform corresponding to the 10-bit accuracy can be output from the $P5_2/PWM_0$ pin and $P5_3/PWM_1$ pin by setting the timer 34 mode register and PWM01 register (refer to Figure 21).
One output pulse is the short interval. Four output pulses are the long interval. The “n” is the value set in the timer 3 (address 0022_{16}) or the timer 4 (address 0023_{16}). The “ts” is one period of timer 3 or timer 4 count source. “H” width of the short interval is obtained by n × ts.
However, in the long interval, “H” width of output pulse is extended for ts which is set by the PWM01 register (address 0024_{16}).

■ Notes on Timer 3 PWM0 Mode, Timer 4 PWM1 Mode

- When PWM output is suspended after starting PWM output, depending on the level of the output pulse at that time to resume an output, the delay of the one section of the short interval may be needed.
  Stop at “H”: No output delay
  Stop at “L”: Output is delayed time of 256 × ts
- In the PWM mode, the follows are performed every cycle of the long interval (4 × 256 × ts).
  •Generation of timer 3, timer 4 interrupt requests
  •Update of timer 3, timer 4

■ Writing to Timer 2, Timer 3, Timer 4

When writing to the latch only, if the write timing to the reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the reload latch.

Timer 12 mode register (T12M: address 0025_{16}) (b7 … b0)

- b0: Timer 1 count stop bit
  - 0 : Count operation
  - 1 : Count stop
- b1: Timer 2 count stop bit
  - 0 : Count operation
  - 1 : Count stop
- b3 b2: Timer 1 count source selection bits
  - 0 0 : Frequency divider for Timer 1
  - 0 1 : $f(X_{CIN})$
  - 1 0 : Underflow of Timer Y
  - 1 1 : Not available
- b5 b4: Timer 2 count source selection bits
  - 0 0 : Underflow of Timer 1
  - 0 1 : $f(X_{CIN})$
  - 1 0 : Frequency divider for Timer 2
  - 1 1 : Not available
- b6: Timer 2 output selection bit ($P3_6$)
  - 0 : I/O port
  - 1 : Timer 2 output
- b7: T_{2OUT} output edge switch bit
  - 0 : Start at “L” output
  - 1 : Start at “H” output

PWM01 register (PWM01: address 0024_{16}) (b7 … b0)

- b1 b0: PWM0 set bits
  - 0 0 : No extended
  - 0 1 : Extended once in four periods
  - 1 0 : Extended twice in four periods
  - 1 1 : Extended three times in four periods
- b3 b2: PWM1 set bits
  - 0 0 : No extended
  - 0 1 : Extended once in four periods
  - 1 0 : Extended twice in four periods
  - 1 1 : Extended three times in four periods
- b4–b7: Not used (returns “0” when read)

Timer 34 mode register (T34M: address 0026_{16}) (b7 … b0)

- b0: Timer 3 count stop bit
  - 0 : Count operation
  - 1 : Count stop
- b1: Timer 4 count stop bit
  - 0 : Count operation
  - 1 : Count stop
- b2: Timer 3 count source selection bit
  - 0 : Frequency divider for Timer 3
  - 1 : Underflow of Timer 2
- b4 b3: Timer 4 count source selection bits
  - 0 0 : Frequency divider for Timer 4
  - 0 1 : Underflow of Timer 3
  - 1 0 : Underflow of Timer 2
  - 1 1 : Not available
- b5: Timer 3 operating mode selection bit
  - 0 : Timer mode
  - 1 : PWM mode
- b6: Timer 4 operating mode selection bit
  - 0 : Timer mode
  - 1 : PWM mode
- b7: Not used (returns “0” when read)

Timer 12 frequency division selection register (PRE12: address $0FF5_{16}$) (b7 … b0)

- b2 b1 b0: Timer 1 frequency division selection bits
  - 0 0 0 : 1/16 × $f(X_{IN})$ or 1/16 × $f(X_{CIN})$
  - 0 0 1 : 1/1 × $f(X_{IN})$ or 1/1 × $f(X_{CIN})$
  - 0 1 0 : 1/2 × $f(X_{IN})$ or 1/2 × $f(X_{CIN})$
  - 0 1 1 : 1/32 × $f(X_{IN})$ or 1/32 × $f(X_{CIN})$
  - 1 0 0 : 1/64 × $f(X_{IN})$ or 1/64 × $f(X_{CIN})$
  - 1 0 1 : 1/128 × $f(X_{IN})$ or 1/128 × $f(X_{CIN})$
  - 1 1 0 : 1/256 × $f(X_{IN})$ or 1/256 × $f(X_{CIN})$
  - 1 1 1 : 1/1024 × $f(X_{IN})$ or 1/1024 × $f(X_{CIN})$
- b5 b4 b3: Timer 2 frequency division selection bits
  - 0 0 0 : 1/16 × $f(X_{IN})$ or 1/16 × $f(X_{CIN})$
  - 0 0 1 : 1/1 × $f(X_{IN})$ or 1/1 × $f(X_{CIN})$
  - 0 1 0 : 1/2 × $f(X_{IN})$ or 1/2 × $f(X_{CIN})$
  - 0 1 1 : 1/32 × $f(X_{IN})$ or 1/32 × $f(X_{CIN})$
  - 1 0 0 : 1/64 × $f(X_{IN})$ or 1/64 × $f(X_{CIN})$
  - 1 0 1 : 1/128 × $f(X_{IN})$ or 1/128 × $f(X_{CIN})$
  - 1 1 0 : 1/256 × $f(X_{IN})$ or 1/256 × $f(X_{CIN})$
  - 1 1 1 : 1/1024 × $f(X_{IN})$ or 1/1024 × $f(X_{CIN})$
- b6, b7: Not used (returns “0” when read)

Timer 1234 mode register (T1234M: address $0FF3_{16}$) (b7 … b0)

- b0: T_{3OUT} output edge switch bit
  - 0 : Start at “L” output
  - 1 : Start at “H” output
- b1: T_{4OUT} output edge switch bit
  - 0 : Start at “L” output
  - 1 : Start at “H” output
- b2: Timer 3 output selection bit ($P5_2$)
  - 0 : I/O port
  - 1 : Timer 3 output
- b3: Timer 4 output selection bit ($P5_3$)
  - 0 : I/O port
  - 1 : Timer 4 output
- b4: Timer 2 write control bit
  - 0 : Write data to both timer latch and timer
  - 1 : Write data to timer latch only
- b5: Timer 3 write control bit
  - 0 : Write data to both timer latch and timer
  - 1 : Write data to timer latch only
- b6: Timer 4 write control bit
  - 0 : Write data to both timer latch and timer
  - 1 : Write data to timer latch only
- b7: Not used (returns “0” when read)

Timer 34 frequency division selection register (PRE34: address $0FF6_{16}$) (b7 … b0)

- b2 b1 b0: Timer 3 frequency division selection bits
  - 0 0 0 : 1/16 × $f(X_{IN})$ or 1/16 × $f(X_{CIN})$
  - 0 0 1 : 1/1 × $f(X_{IN})$ or 1/1 × $f(X_{CIN})$
  - 0 1 0 : 1/2 × $f(X_{IN})$ or 1/2 × $f(X_{CIN})$
  - 0 1 1 : 1/32 × $f(X_{IN})$ or 1/32 × $f(X_{CIN})$
  - 1 0 0 : 1/64 × $f(X_{IN})$ or 1/64 × $f(X_{CIN})$
  - 1 0 1 : 1/128 × $f(X_{IN})$ or 1/128 × $f(X_{CIN})$
  - 1 1 0 : 1/256 × $f(X_{IN})$ or 1/256 × $f(X_{CIN})$
  - 1 1 1 : 1/1024 × $f(X_{IN})$ or 1/1024 × $f(X_{CIN})$
- b5 b4 b3: Timer 4 frequency division selection bits
  - 0 0 0 : 1/16 × $f(X_{IN})$ or 1/16 × $f(X_{CIN})$
  - 0 0 1 : 1/1 × $f(X_{IN})$ or 1/1 × $f(X_{CIN})$
  - 0 1 0 : 1/2 × $f(X_{IN})$ or 1/2 × $f(X_{CIN})$
  - 0 1 1 : 1/32 × $f(X_{IN})$ or 1/32 × $f(X_{CIN})$
  - 1 0 0 : 1/64 × $f(X_{IN})$ or 1/64 × $f(X_{CIN})$
  - 1 0 1 : 1/128 × $f(X_{IN})$ or 1/128 × $f(X_{CIN})$
  - 1 1 0 : 1/256 × $f(X_{IN})$ or 1/256 × $f(X_{CIN})$
  - 1 1 1 : 1/1024 × $f(X_{IN})$ or 1/1024 × $f(X_{CIN})$
- b6, b7: Not used (returns “0” when read)

Fig. 19 Structure of timer related register

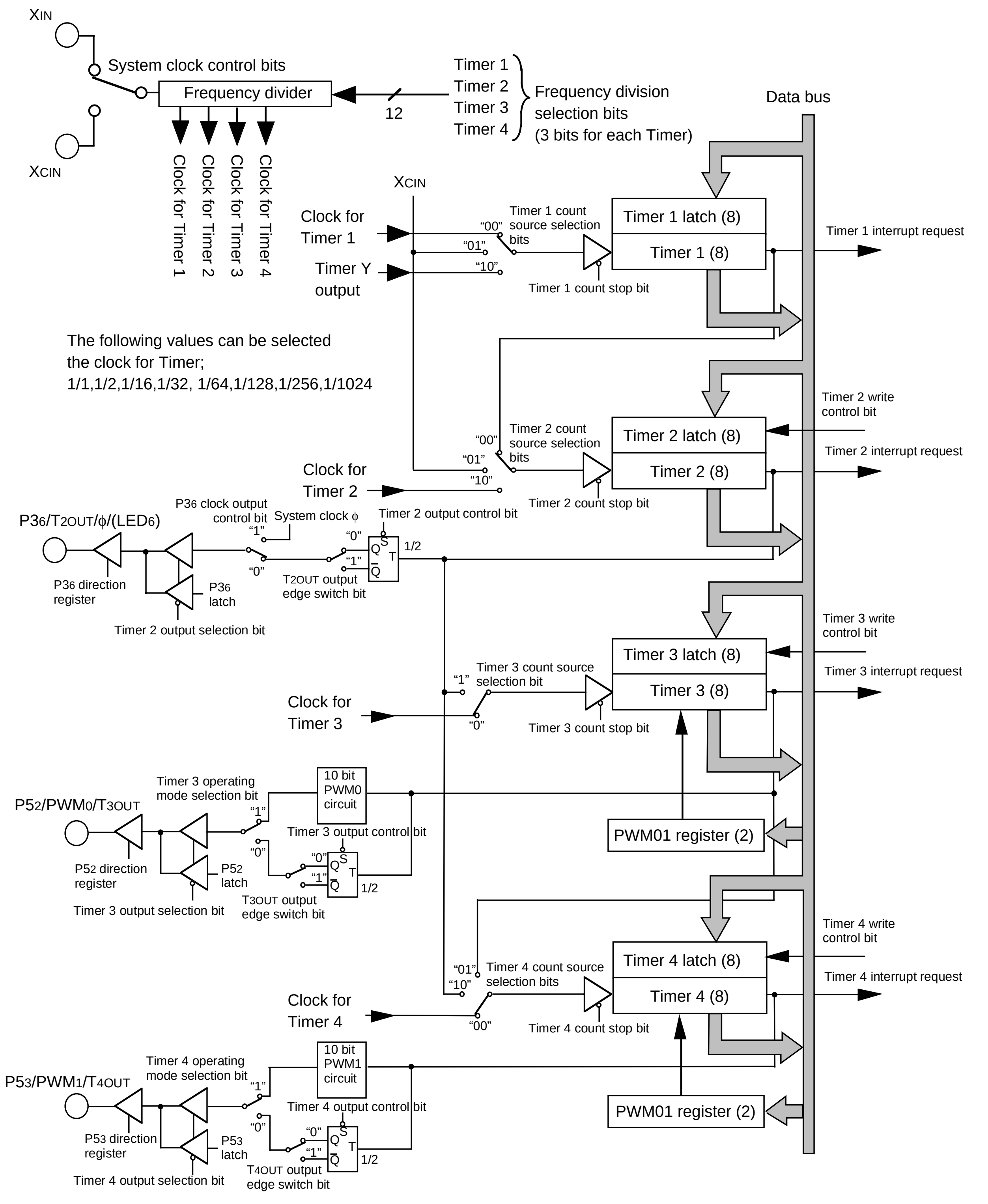


Fig. 20 Block diagram of timers 1, 2, 3 and 4

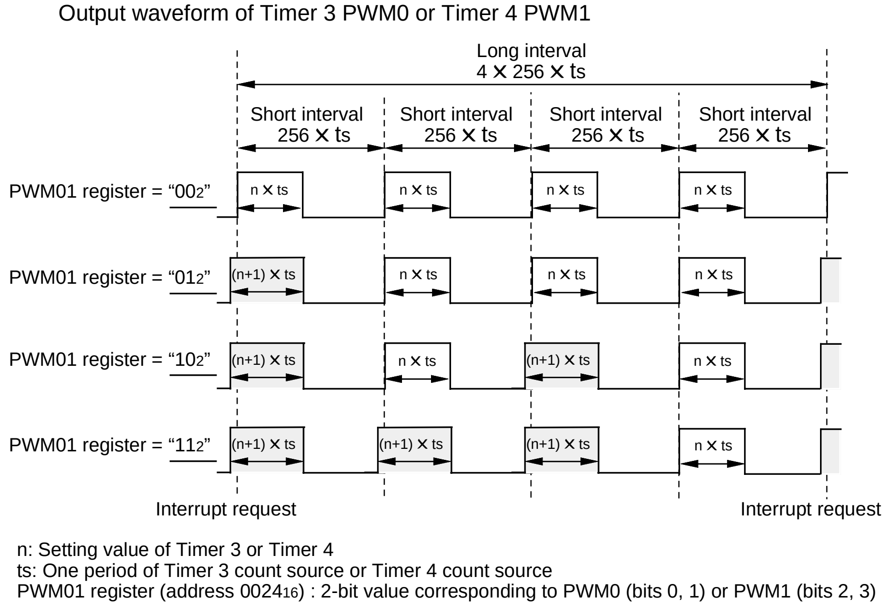


Fig. 21 Waveform of PWM0 and PWM1

16-bit Timer

● Frequency Divider For Timer

Each timer X and timer Y have the frequency dividers for the count source. The count source of the frequency divider is switched to XIN or XCIN by the CPU mode register. The division ratio of each timer can be controlled by each timer division ratio selection bit. The division ratio can be selected from as follows;
1/1, 1/2, 1/16, 1/32, 1/64, 1/128, 1/256, 1/1024 of f(XIN); or f(XCIN).

● Timer X

The timer X count source can be selected by setting the timer X mode register. When f(XCIN) is selected as the count source, counting can be performed regardless of XCIN oscillation. However, when XCIN is stopped, the external pulse input from XCIN pin is counted.
The timer X operates as down-count. When the timer contents reach “0000₁₆”, an underflow occurs at the next count pulse and the timer latch contents are reloaded. After that, the timer continues count-down. When the timer underflows, the interrupt request bit corresponding to the timer X is set to “1”.
Six operating modes can be selected for timer X by the timer X mode register and timer X control register.

(1) Timer Mode

The count source can be selected by setting the timer X mode register. In this mode, timer X operates as the 18-bit counter by setting the timer X register (extension).

(2) Pulse Output Mode

Pulses of which polarity is inverted each time the timer underflows are output from the TXOUT pin. Except for that, this mode operates just as in the timer mode.
When using this mode, set the port sharing the TXOUT pin to output mode.

(3) IGBT Output Mode

After dummy output from the TXOUT pin, count starts with the INT0 pin input as a trigger. In the case that the timer X output edge switch bit is “0”, when the trigger is detected or the timer X underflows, “H” is output from the TXOUT pin. And then, when the count value corresponds with the compare register value, the TXOUT output becomes “L”.
After noise is cleared by noise filters, judging continuous 4-time same levels with sampling clocks to be signals, the INT0 signal can use 4 types of delay time by a delay circuit.
When using this mode, set the port sharing the INT0 pin to input mode and set the port sharing the TXOUT pin to output mode.
When the timer X output control bit 1 or 2 of the timer X control register is set to “1”, the timer X count stop bit is fixed to “1” forcibly by the interrupt signal of INT1 or INT2. And then, the TXOUT output can be set to “L” forcibly at the same time that the timer X stops counting.
Do not write “1” to the timer X register (extension) when using the IGBT output mode.

(4) PWM Mode

IGBT dummy output, an external trigger with the INT0 pin and output control with pins INT1 and INT2 are not used. Except for those, this mode operates just as in the IGBT output mode.
The period of PWM waveform is specified by the timer X set value. In the case that the timer X output edge switch bit is “0”, the “H” interval is specified by the compare register set value.
When using this mode, set the port sharing the TXOUT pin to output mode.
Do not write “1” to the timer X register (extension) when using the PWM mode.

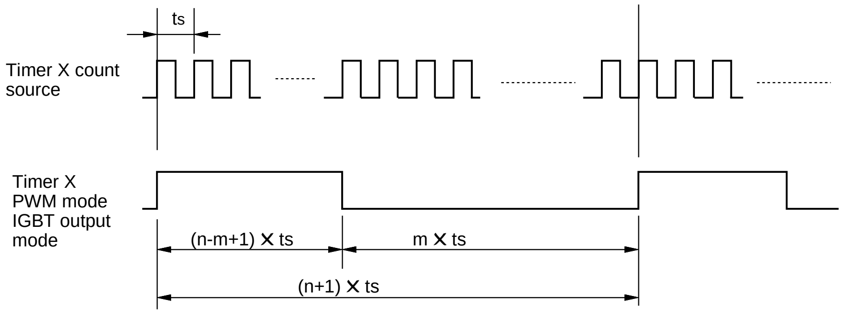


Fig. 22 Waveform of PWM/IGBT

(5) Event Counter Mode

The timer counts signals input through the CNTR0 pin. In this mode, timer X operates as the 18-bit counter by setting the timer X register (extension). When using this mode, set the port sharing the CNTR0 pin to input mode.

In this mode, the window control can be performed by the timer 1 underflow. When the bit 5 (data for control of event counter window) of the timer X mode register is set to “1”, counting is stopped at the next timer 1 underflow. When the bit is set to “0”, counting is restarted at the next timer 1 underflow.

(6) Pulse Width Measurement Mode

In this mode, the count source is the output of frequency divider for timer. In this mode, timer X operates as the 18-bit counter by setting the timer X register (extension). When the bit 6 of the CNTR0 active edge switch bits is “0”, counting is executed during the “H” interval of CNTR0 pin input. When the bit is “1”, counting is executed during the “L” interval of CNTR0 pin input. When using this mode, set the port sharing the CNTR0 pin to input mode.

■ Notes on Timer X

(1) Write Order to Timer X

- In the timer mode, pulse output mode, event counter mode and pulse width measurement mode, write to the following registers in the order as shown below;
  the timer X register (extension),
  the timer X register (low-order),
  the timer X register (high-order).
  Do not write to only one of them.
  When the above mode is set and timer X operates as the 16-bit counter, if the timer X register (extension) is never set after reset is released, setting the timer X register (extension) is not required. In this case, write the timer X register (low-order) first and the timer X register (high-order). However, once writing to the timer X register (extension) is executed, note that the value is retained to the reload latch.

- In the IGBT output and PWM modes, do not write “1” to the timer X register (extension). Also, when “1” is already written to the timer X register, be sure to write “0” to the register before using.
  Write to the following registers in the order as shown below;
  the compare register (high- and low-order),
  the timer X register (extension),
  the timer X register (low-order),
  the timer X register (high-order).
  It is possible to use whichever order to write to the compare register (high- and low-order). However, write both the compare register and the timer X register at the same time.

(2) Read Order to Timer X

- In all modes, read the following registers in the order as shown below;
  the timer X register (extension),
  the timer X register (high-order),
  the timer X register (low-order).
  When reading the timer X register (extension) is not required, read the timer X register (high-order) first and the timer X register (low-order).
  Read order to the compare register is not specified.
- If reading to the timer X register during write operation or writing to it during read operation is performed, normal operation will not be performed.

(3) Write to Timer X

- Which write control can be selected by the timer X write control bit (b3) of the timer X mode register (address $2F_{16}$), writing data to both the latch and the timer at the same time or writing data only to the latch. When writing a value to the timer X address to write to the latch only, the value is set into the reload latch and the timer is updated at the next underflow. After reset release, when writing a value to the timer X address, the value is set into the timer and the timer latch at the same time, because they are written at the same time.
  When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the high-order reload latch.
- Do not switch the timer count source during timer count operation. Stop the timer count before switching it.

(4) Set of Timer X Mode Register

Set the write control bit of the timer X mode register to “1” (write to the latch only) when setting the IGBT output and PWM modes. Output waveform simultaneously reflects the contents of both registers at the next underflow after writing to the timer X register (high-order).

(5) Output Control Function of Timer X

When using the output control function (INT_1 and INT_2) in the IGBT output mode, set the levels of INT_1 and INT_2 to “H” in the falling edge active or to “L” in the rising edge active before switching to the IGBT output mode.

(6) Note on Switch of $CNTR_0$ Active Edge

- When the $CNTR_0$ active edge switch bits are set, at the same time, the interrupt active edge is also affected.
- When the pulse width is measured, set the bit 7 of the $CNTR_0$ active edge switch bits to “0”.

Timer Y

Timer Y is a 16-bit timer. The timer Y count source can be selected by setting the timer Y mode register. When $f(X_{CIN})$ is selected as the count source, counting can be performed regardless of X_{CIN} oscillation. However, when X_{CIN} is stopped, the external pulse input from X_{CIN} pin is counted.
Four operating modes can be selected for timer Y by the timer Y mode register. Also, the real time port can be controlled.

(1) Timer Mode

The timer Y count source can be selected by setting the timer Y mode register.

(2) Period Measurement Mode

The interrupt request is generated at rising or falling edge of $CNTR_1$ pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting. Except for that, this mode operates just as in the timer mode.
The timer value just before the reloading at rising or falling of $CNTR_1$ pin input is retained until the timer Y is read once after the reload.
The rising or falling timing of $CNTR_1$ pin input is found by $CNTR_1$ interrupt. When using this mode, set the port sharing the $CNTR_1$ pin to input mode.

(3) Event Counter Mode

The timer counts signals input through the $CNTR_1$ pin.
Except for that, this mode operates just as in the timer mode.
When using this mode, set the port sharing the $CNTR_1$ pin to input mode.

(4) Pulse Width HL Continuously Measurement Mode

The interrupt request is generated at both rising and falling edges of $CNTR_1$ pin input signal. Except for that, this mode operates just as in the period measurement mode. When using this mode, set the port sharing the $CNTR_1$ pin to input mode.

■ Notes on Timer Y

● $CNTR_1$ Interrupt Active Edge Selection

$CNTR_1$ interrupt active edge depends on the $CNTR_1$ active edge switch bit. However, in pulse width HL continuously measurement mode, $CNTR_1$ interrupt request is generated at both rising and falling edges of $CNTR_1$ pin input signal regardless of the setting of $CNTR_1$ active edge switch bit.

● Timer Y Read/Write Control

- When reading from/writing to timer Y, read from/write to both the high-order and low-order bytes of timer Y. When the value is read, read the high-order bytes first and the low-order bytes next. When the value is written, write the low-order bytes first and the high-order bytes next.
  If reading from the timer Y register during write operation or writing to it during read operation is performed, normal operation will not be performed.
- When writing a value to the timer Y address to write to the latch only, the value is set into the reload latch and the timer is updated at the next underflow. Normally, when writing a value to the timer Y address, the value is set into the timer and the timer latch at the same time, because they are set to write at the same time.
  When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the high-order reload latch.
- Do not switch the timer count source during timer count operation. Stop the timer count before switching it.

● Real Time Port Control

When the real time port function is valid, data for the real time port is output from ports $P4_7$ and $P4_6$ each time the timer Y underflows. (However, if the real time port control bit is changed from “0” to “1” after the data for real time port is set, data is output independent of the timer Y operation.) When the data for the real time port is changed while the real time port function is valid, the changed data is output at the next underflow of timer Y. Before using this function, set the corresponding port direction registers to output mode.

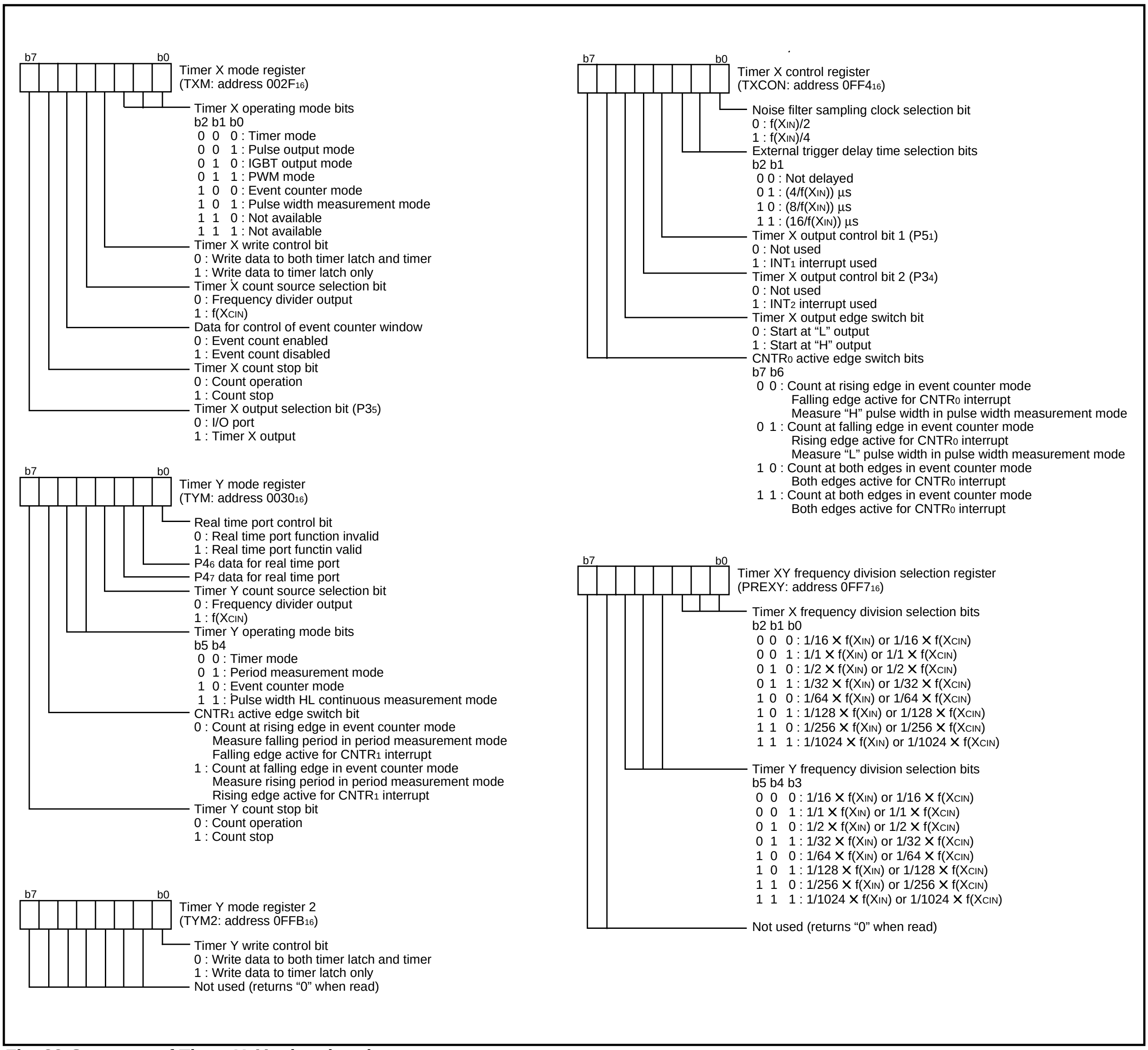
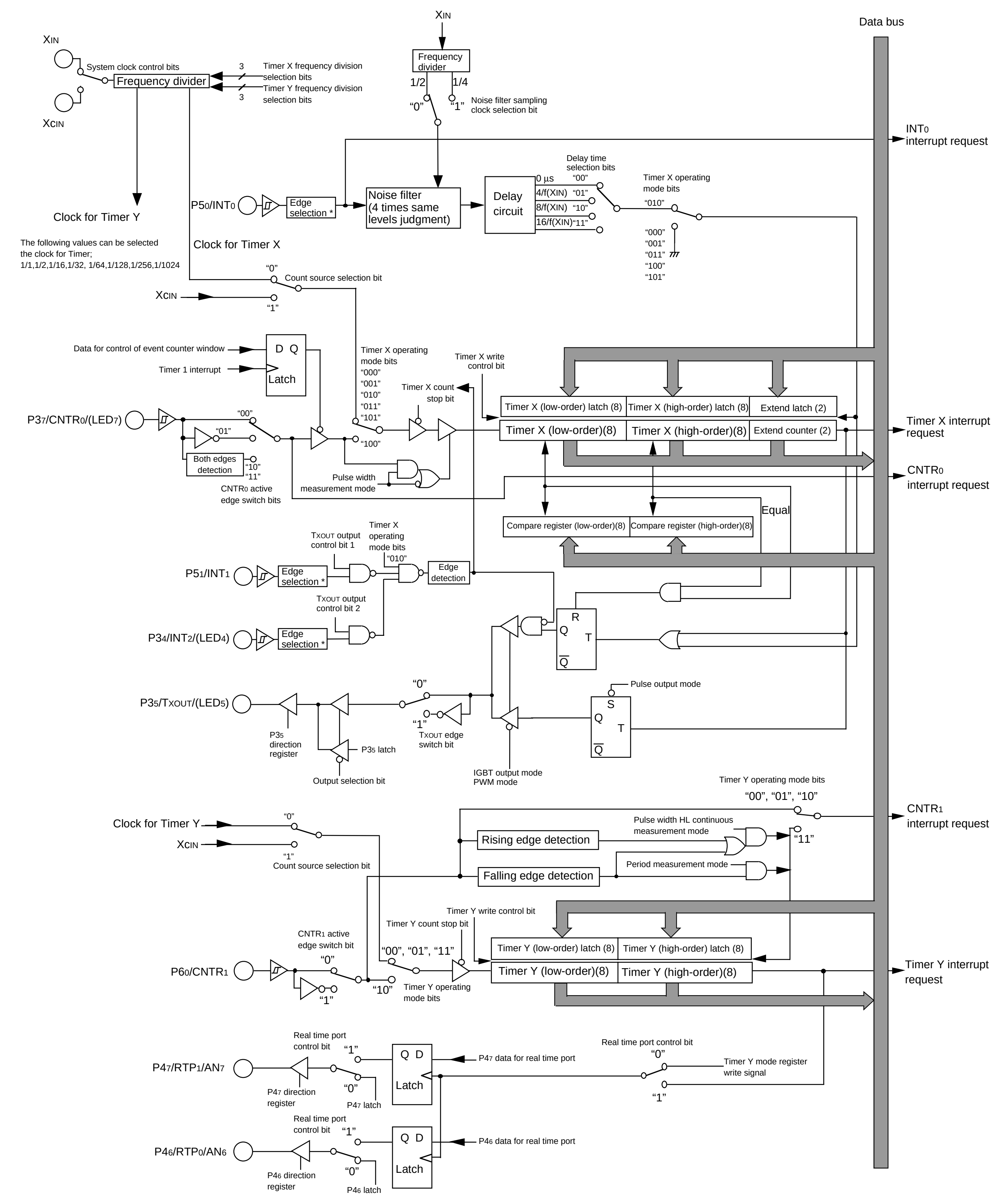


Fig. 23 Structure of Timer X, Y related registers



* Interrupt edges of INT0, INT1, INT2 can be selected by the interrupt edge selection register (address 003A16).
0: Falling edge active
1: Rising edge active

Fig. 24 Block diagram of Timer X, Y

SERIAL I/O

The 38C2 group has built-in two 8-bit serial I/O.
Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O mode selection bit of the serial I/O control register to “1”.
For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

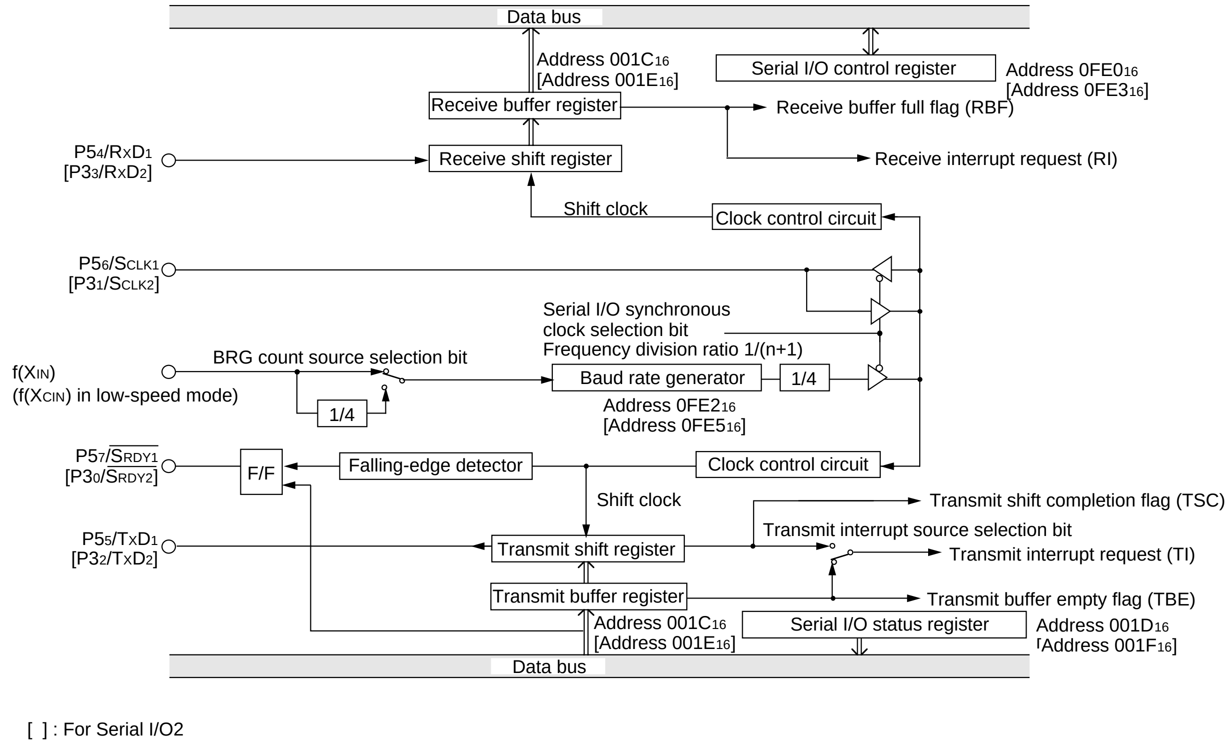
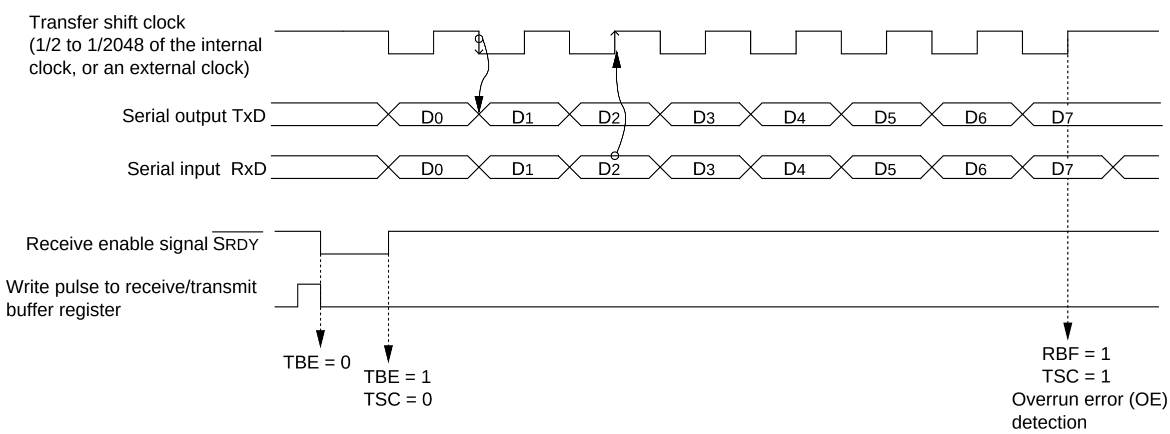


Fig. 25 Block diagram of clock synchronous serial I/O



Notes 1: As the transmit interrupt (TI) source, which can be selected, either when the transmit buffer has emptied (TBE = 1) or after the transmit shift operation has ended (TSC = 1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O control register.
2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes “1” .

Fig. 26 Operation of clock synchronous serial I/O function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by setting the serial I/O mode selection bit of the serial I/O control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

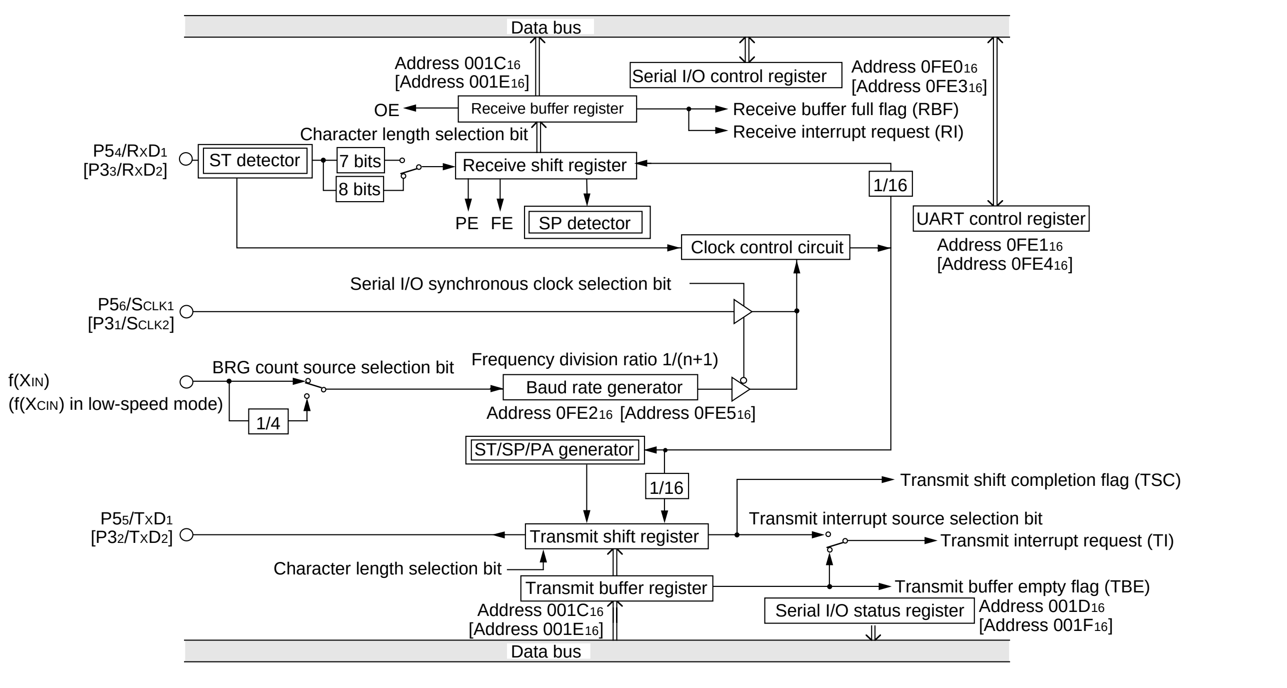
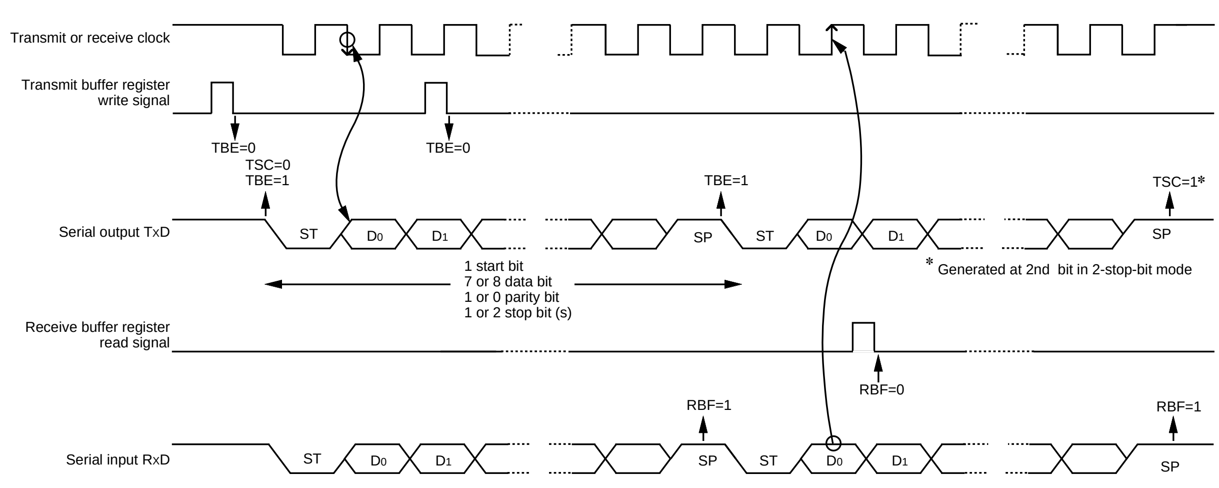


Fig. 27 Block diagram of UART serial I/O



Notes
1: Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1,” can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1”.
4: After data is written to the transmit buffer when TSC flag =“1”, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC flag = “0”.

Fig. 28 Operation of UART serial I/O function

[Transmit Buffer Register/Receive Buffer Register (TB/RB)]

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is “0”.

[Serial I/O Status Register (SIO1STS, SIO2STS)]

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.
Three of the flags (bits 4 to 6) are valid only in UART mode.
The receive buffer full flag (bit 1) is set to “0” when the receive buffer register is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register sets all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively) to “0”. Writing “0” to the serial I/O enable bit SIOE (bit 7 of the serial I/O control register) also sets all the status flags to “0”, including the error flags.
All bits of the serial I/O status register are set to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to “1”, the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O Control Register (SIO1CON, SIO2CON)]

The serial I/O control register consists of eight control bits for the serial I/O function.

[UART Control Register (UART1CON, UART2CON)]

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the $P5_5/TxD_1$ [$P3_2/TxD_2$] pin.

[Baud Rate Generator (BRG1, BRG2)]

The baud rate generator determines the baud rate for serial transfer.
The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

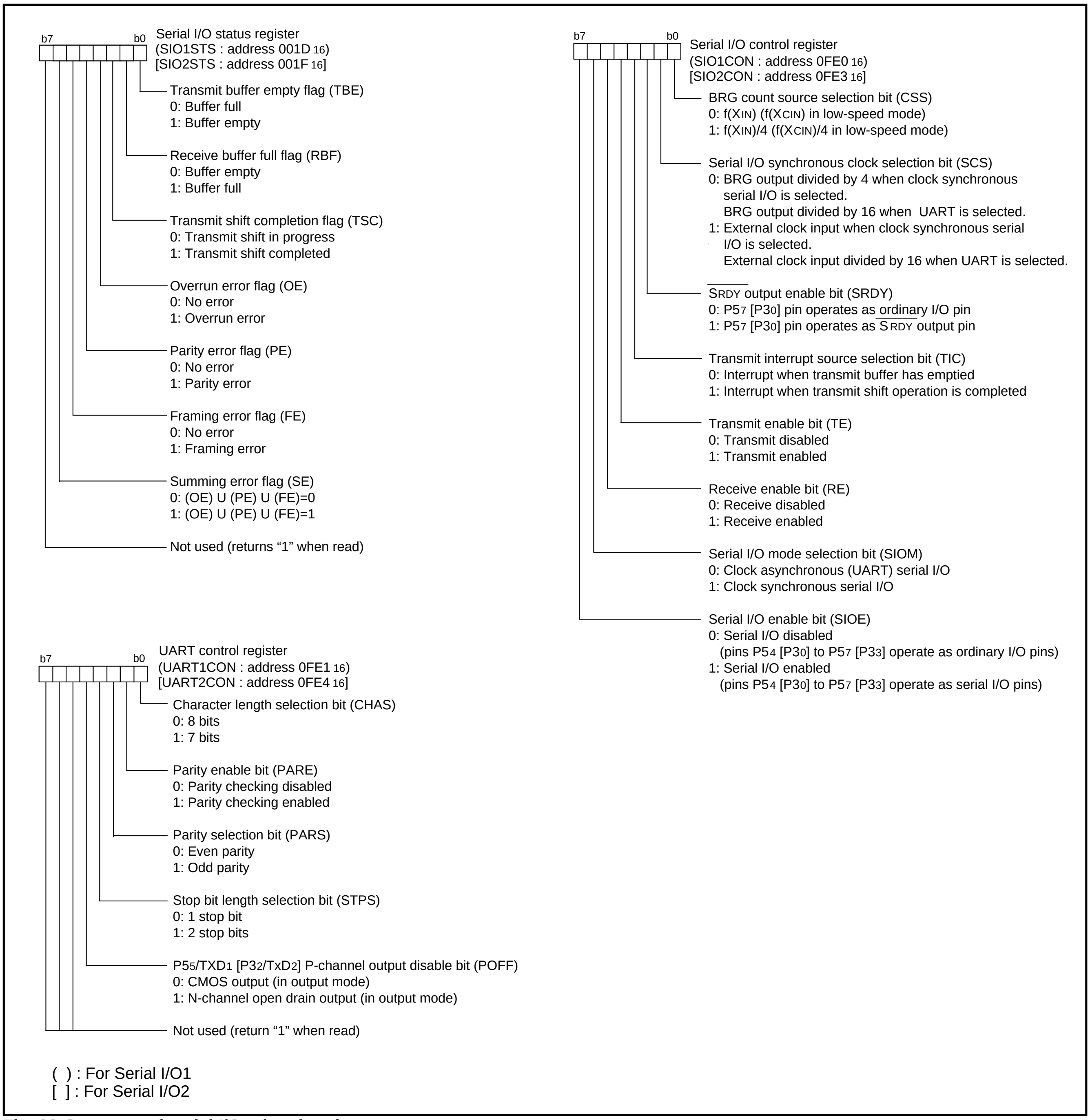


Fig. 29 Structure of serial I/O related registers

■Notes on serial I/O

When setting transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronous with the transmision enabled, take the following sequence.

①Set the serial I/O transmit interrupt enable bit to "0" (disabled).

②Set the transmit enable bit to "1".

③Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.

④Set the serial I/O transmit interrupt enable bit to "1" (enabled).

A-D CONVERTER

The 38C2 group has a 10-bit A-D converter. The A-D converter performs successive approximation conversion.

[A-D Conversion Register (ADL, ADH)]

One of these registers is a high-order register, and the other is a low-order register. The high-order 8 bits of a conversion result is stored in the A-D conversion register (high-order) (address 001B$_{16}$), and the low-order 2 bits of the same result are stored in bit 7 and bit 6 of the A-D conversion register (low-order) (address 001A$_{16}$).
During A-D conversion, do not read these registers.
Also, the connection between the resistor ladder and reference voltage input pin (VREF) can be controlled by the VREF input switch bit (bit 0 of address 001A$_{16}$). When "1" is written to this bit, the resistor ladder is always connected to VREF. When "0" is written to this bit, the resistor ladder is disconnected from VREF except during the A-D conversion.

[A-D Control Register (ADCON)]

This register controls A-D converter. Bits 2 to 0 are analog input pin selection bits. Bit 3 is an AD conversion completion bit and "0" during A-D conversion. This bit is set to "1" upon completion of A-D conversion. A-D conversion is started by setting "0" in this bit.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AVSS and VREF, and outputs the divided voltages.

[Channel Selector]

The channel selector selects one of the input ports P4$_7$/AN$_7$–P4$_0$/AN$_0$ and inputs it to the comparator.

[Comparator and Control Circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and store the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD conversion interrupt request bit to "1."
Note that because the comparator consists of a capacitor coupling, set the A-D clock frequency to 250 kHz or more during an A-D conversion.
Also, when the STP instruction is executed during the A-D conversion, the A-D conversion is stopped immediately, the A-D conversion completion bit is set to "1", and the interrupt request is generated.

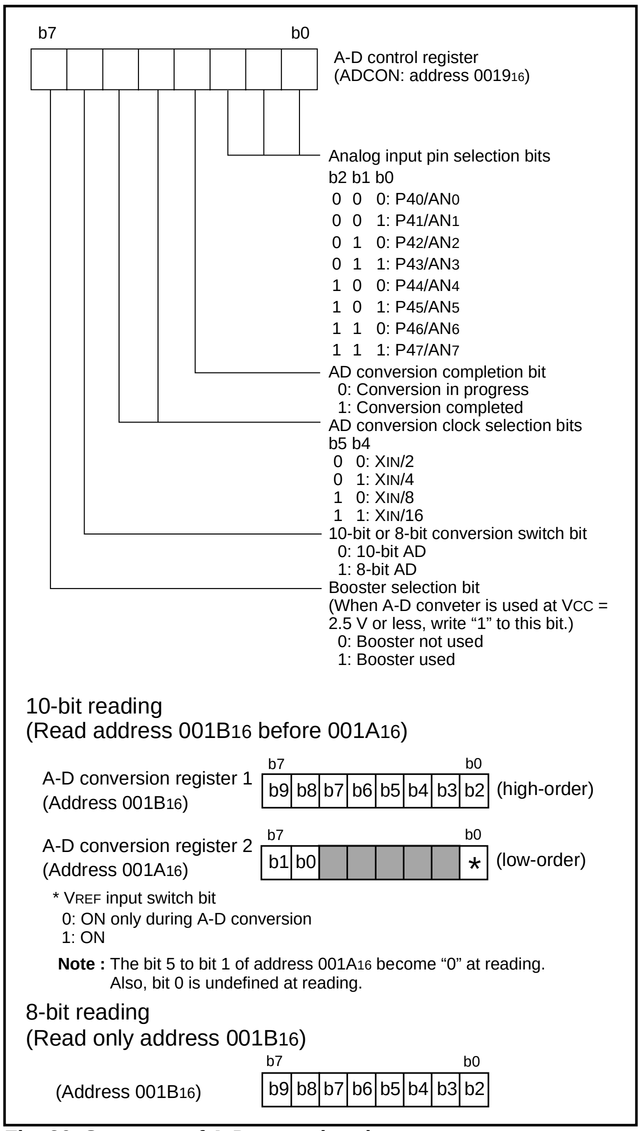


Fig. 30 Structure of A-D control register

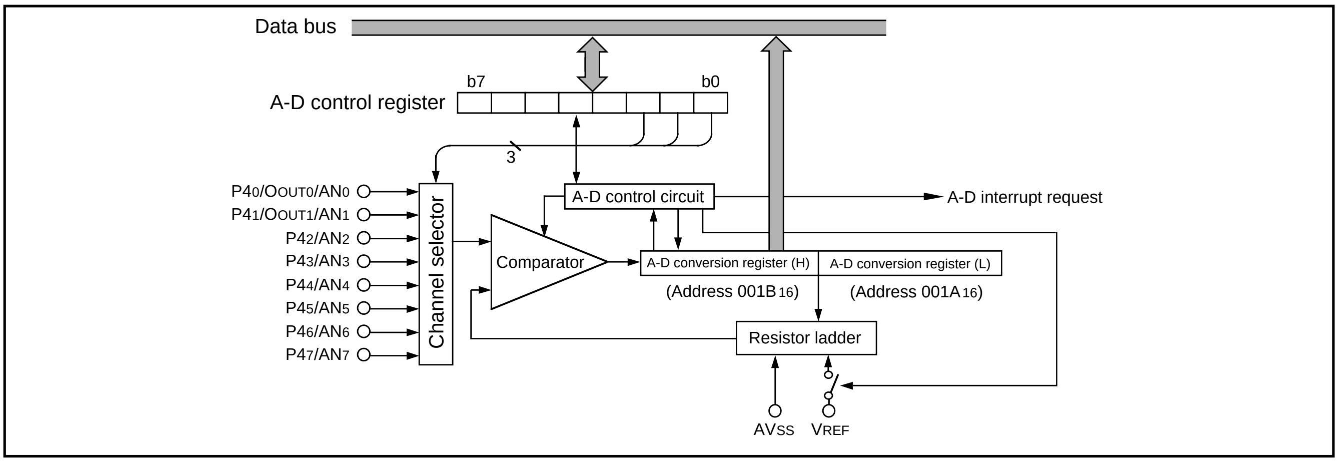


Fig. 31 Block diagram of A-D converter

LCD DRIVE CONTROL CIRCUIT

The 38C2 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

- LCD display RAM
- Segment output disable register
- LCD mode register
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

A maximum of 24 segment output pins and 4 common output pins can be used.

Up to 96 pixels can be controlled for an LCD display. When the LCD enable bit is set to "1" after data is set in the LCD mode register, the segment output disable register, and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 8 Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixels
2	48 dots or 8 segment LCD 6 digits
3	72 dots or 8 segment LCD 9 digits
4	96 dots or 8 segment LCD 12 digits

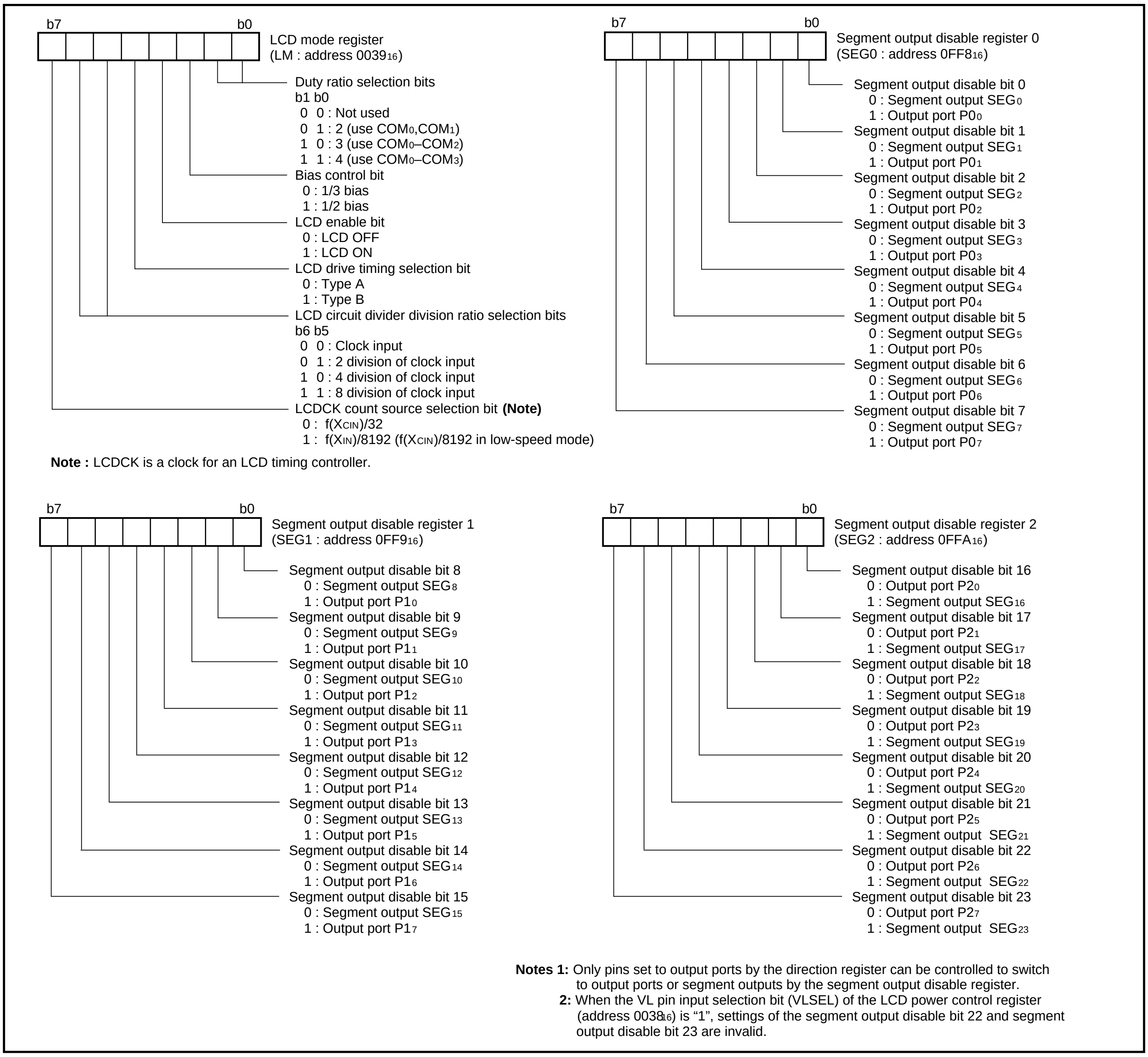


Fig. 32 Structure of LCD related registers

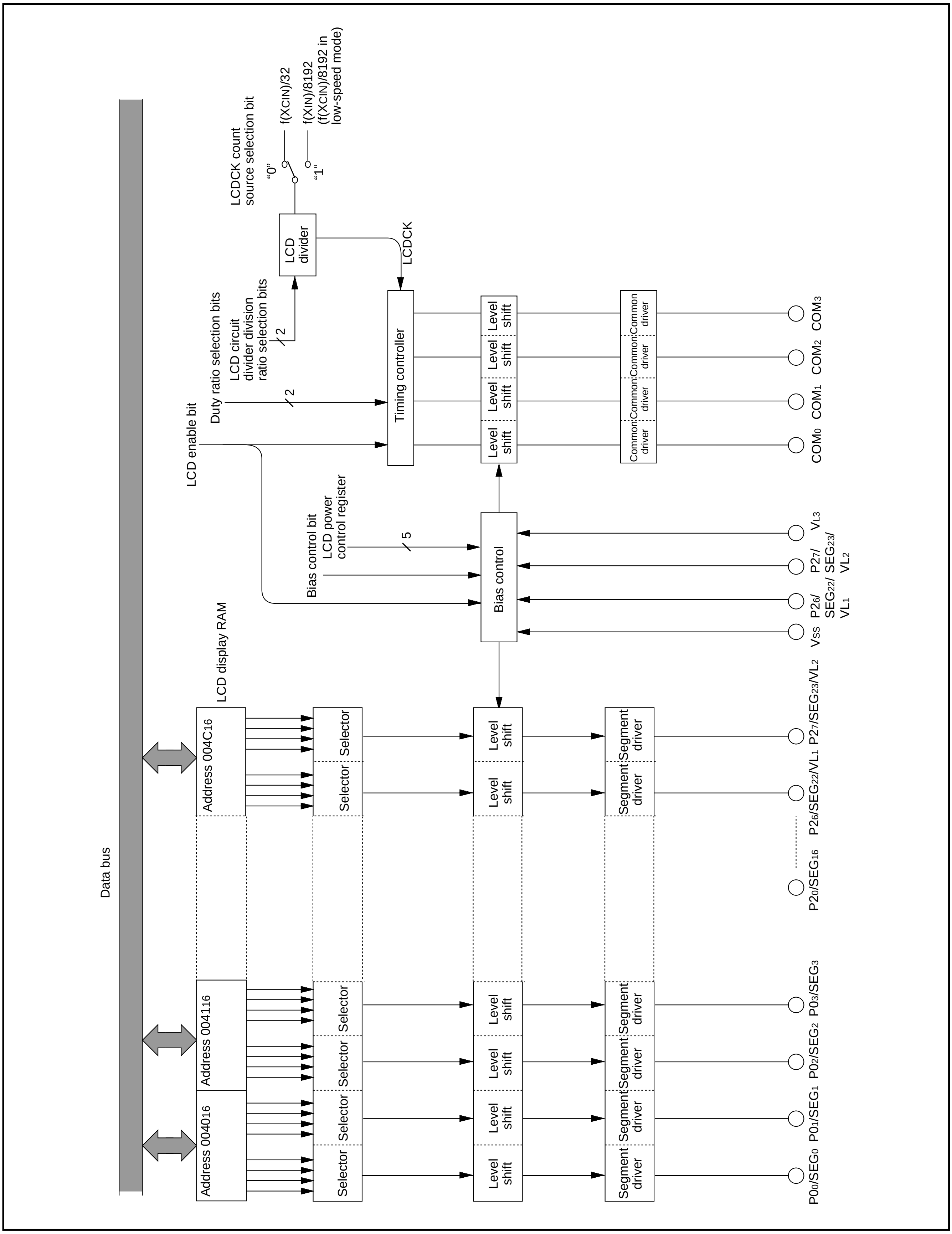


Fig. 33 Block diagram of LCD controller/driver

Bias Control and Applied Voltage to LCD Power Input Pins

When the voltage is applied from the LCD power input pins (V_{L1}–V_{L3}), set the VL pin input selection bit (bit 5 of the LCD power control register) and V_{L3} connection bit (bit 6 of LCD power control register) to “1”, apply the voltage value shown in Table 9 according to the bias value. In this case, SEG_{22} pin and SEG_{23} pin cannot be used.
Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Table 9 Bias control and applied voltage to V_{L1}–V_{L3}

Bias value	Voltage value
1/3 bias	$V_{L3}=V_{LCD}$ $V_{L2}=2/3\ V_{LCD}$ $V_{L1}=1/3\ V_{LCD}$
1/2 bias	$V_{L3}=V_{LCD}$ $V_{L2}=V_{L1}=1/2\ V_{LCD}$

Note : V_{LCD} is the maximum value of supplied voltage for the LCD panel.

Common Pin and Duty Ratio Control

The common pins (COM_0–COM_3) to be used are determined by duty ratio. Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register). When reset is released, V_{CC} voltage is output from the common pin.

Table 10 Duty ratio control and common pins used

Duty ratio	Duty ratio selection bits		Common pins used
	Bit 1	Bit 0	
2	0	1	COM_0, COM_1
3	1	0	COM_0–COM_2
4	1	1	COM_0–COM_3

Note: Unused common pin outputs the unselected waveform.

Segment Signal Output Pin

The segment signal output pins (SEG_0–SEG_{23}) are shared with ports P0–P2. When these pins are used as the segment signal output pins, set the direction registers of the corresponding pins to “1”, and set the segment output disable register to “0”.
Also, these pins are set to the input port after reset, the V_{CC} voltage is output by the pull-up resistor.

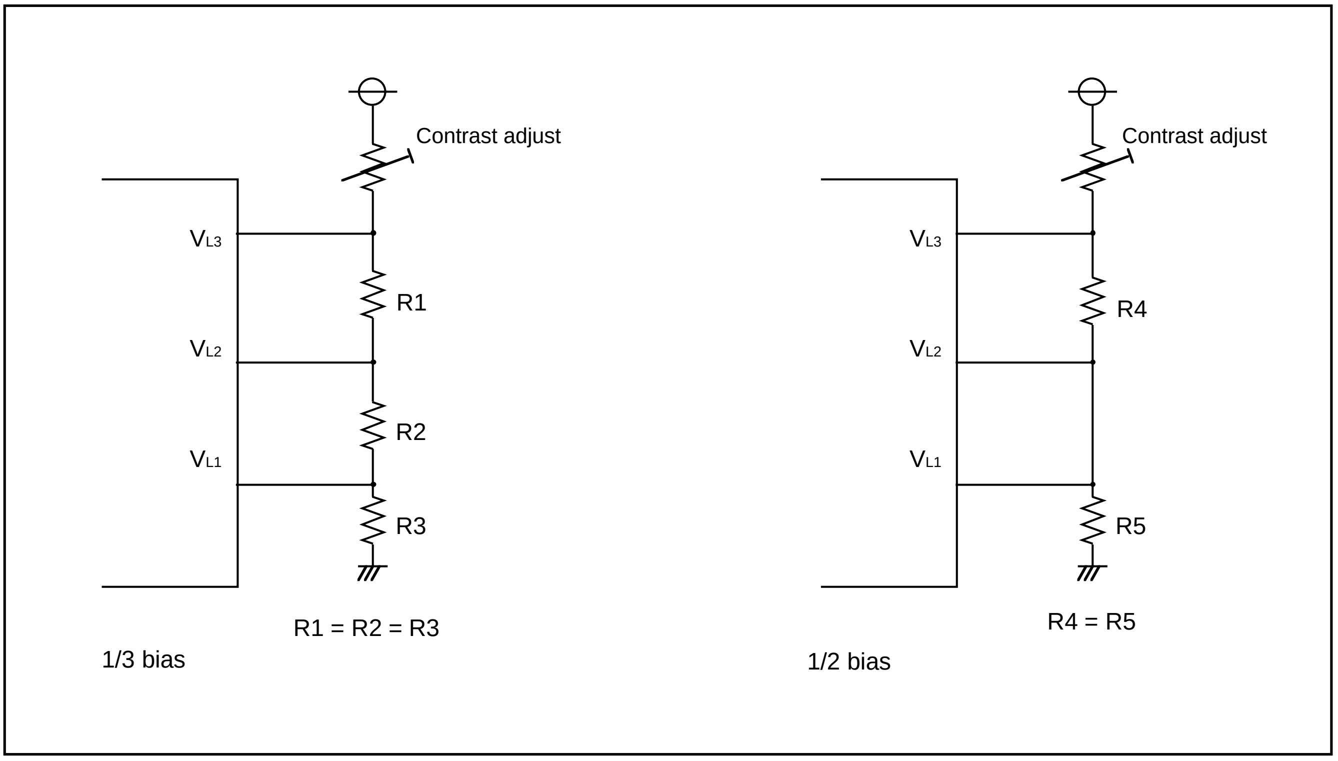
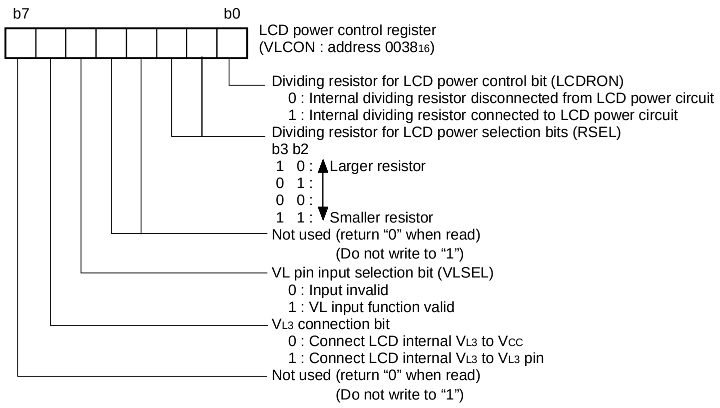


Fig. 34 Example of circuit at each bias (at external power input)

LCD Power Circuit

The LCD power circuit has the dividing resistor for LCD power which can be connected/disconnected with the LCD power control register.



Notes 1: When voltage is applied to V_{L1} to V_{L3} by using the external resistor, write "10_2" to dividing resistor for LCD power selection bits.
2: Setting to the VL pin input selection bit (VLSEL) = "1" has the most priority than setting to the port P2 direction register (address 0005_{16}) and segment output disable register 2 (address $0FFA_{16}$).
3: When the LCD drive control circuit is used at V_{L3} = V_{CC}, apply V_{CC} to V_{L3} pin and write "1" to V_{L3} connection bit.

Fig. 35 Structure of LCD power control register

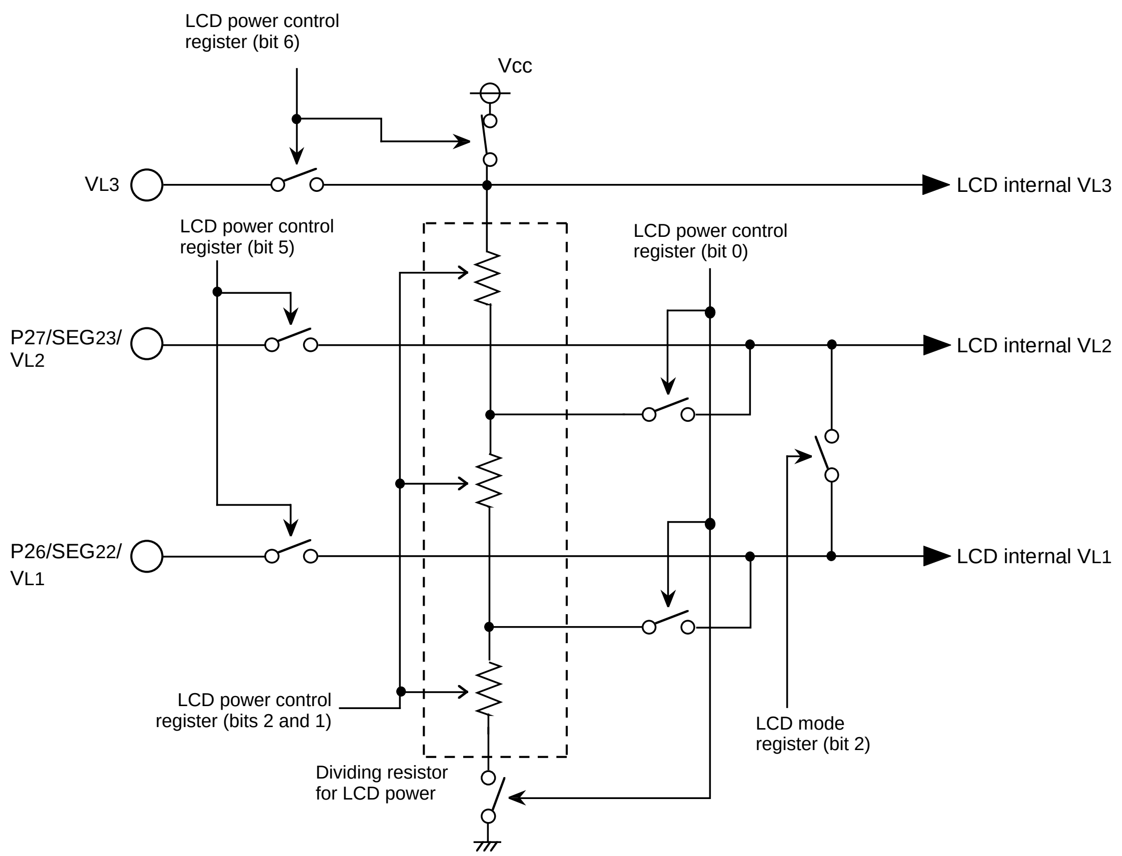


Fig. 36 VL block diagram

LCD Display RAM

The 12-byte area of address 0040_{16} to $004B_{16}$ is the designated RAM for the LCD display. When “1” is written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

For the LCD drive timing, type A or type B can be selected.
The LCD drive timing is selected by the timing selection bit (bit 4 of LCD mode register).
Type A is selected by setting the LCD drive timing selection bit to “0”, type B is selected by setting the bit to “1”. Type A is selected after reset.

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(\mathrm{LCDCK})=\frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency}=\frac{f(\mathrm{LCDCK})}{\text{duty ratio}}$$

■ Note

(1) When the STP instruction is executed, the following bits are set to “0”;
- LCD enable bit (bit 3 of LCD mode register)
- Bits other than bit 6 of the LCD power control register.

(2) When the voltage is applied to V_{L1} to V_{L3} by using the external resistor, write “10_2” to dividing resistor for LCD power selection bits (RSEL) of the LCD power control register (address 0038_{16}).

(3) When the LCD drive control circuit is used at V_{L3} = V_{CC}, apply V_{CC} to V_{L3} pin and write “1” to V_{L3} connection bit of the LCD power control register (address 0038_{16}).

Address \ Bit	7	6	5	4	3	2	1	0
0040_{16}	SEG_1				SEG_0			
0041_{16}	SEG_3				SEG_2			
0042_{16}	SEG_5				SEG_4			
0043_{16}	SEG_7				SEG_6			
0044_{16}	SEG_9				SEG_8			
0045_{16}	SEG_{11}				SEG_{10}			
0046_{16}	SEG_{13}				SEG_{12}			
0047_{16}	SEG_{15}				SEG_{14}			
0048_{16}	SEG_{17}				SEG_{16}			
0049_{16}	SEG_{19}				SEG_{18}			
$004A_{16}$	SEG_{21}				SEG_{20}			
$004B_{16}$	SEG_{23}				SEG_{22}			
	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0

Fig. 37 LCD display RAM map

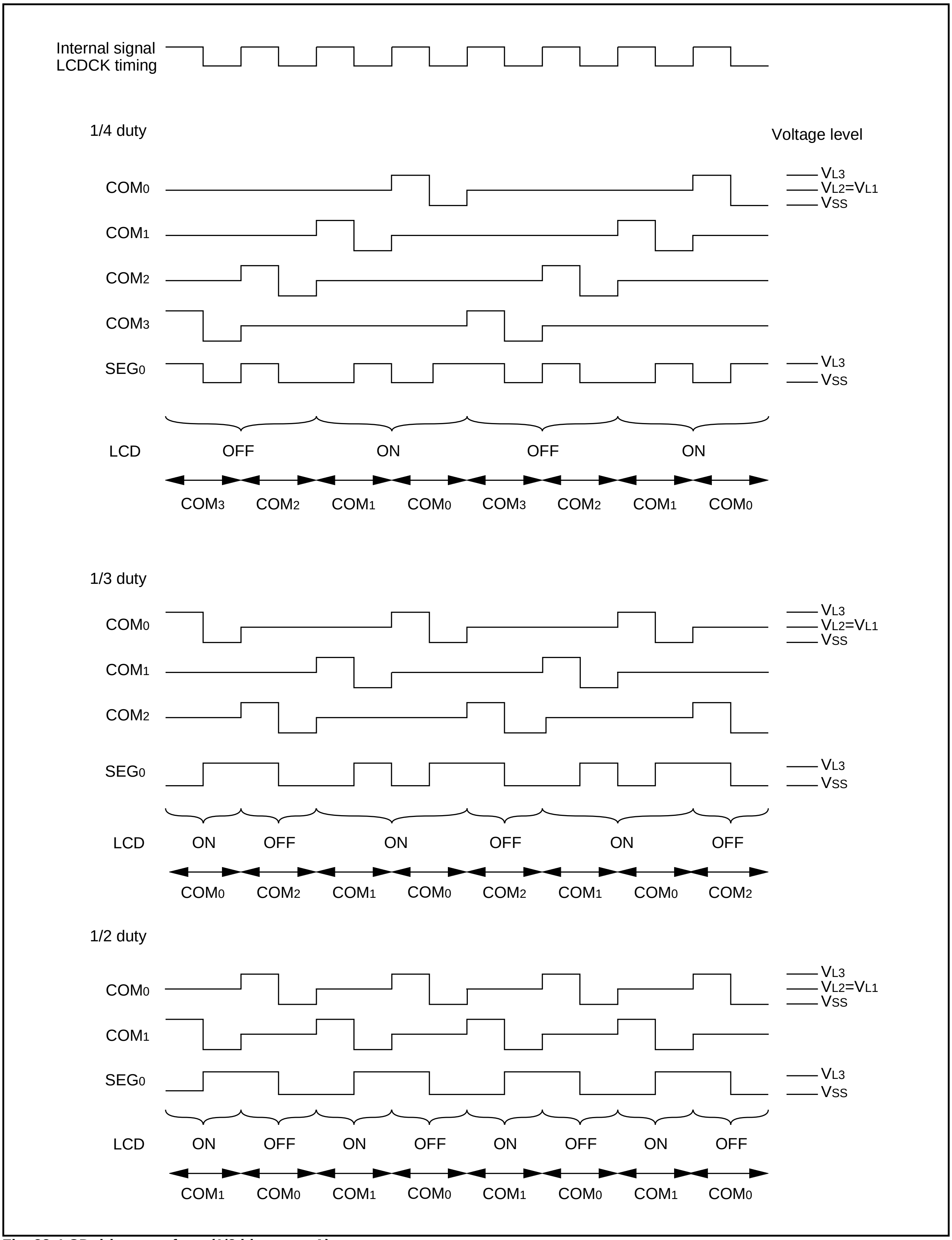


Fig. 38 LCD drive waveform (1/2 bias, type A)

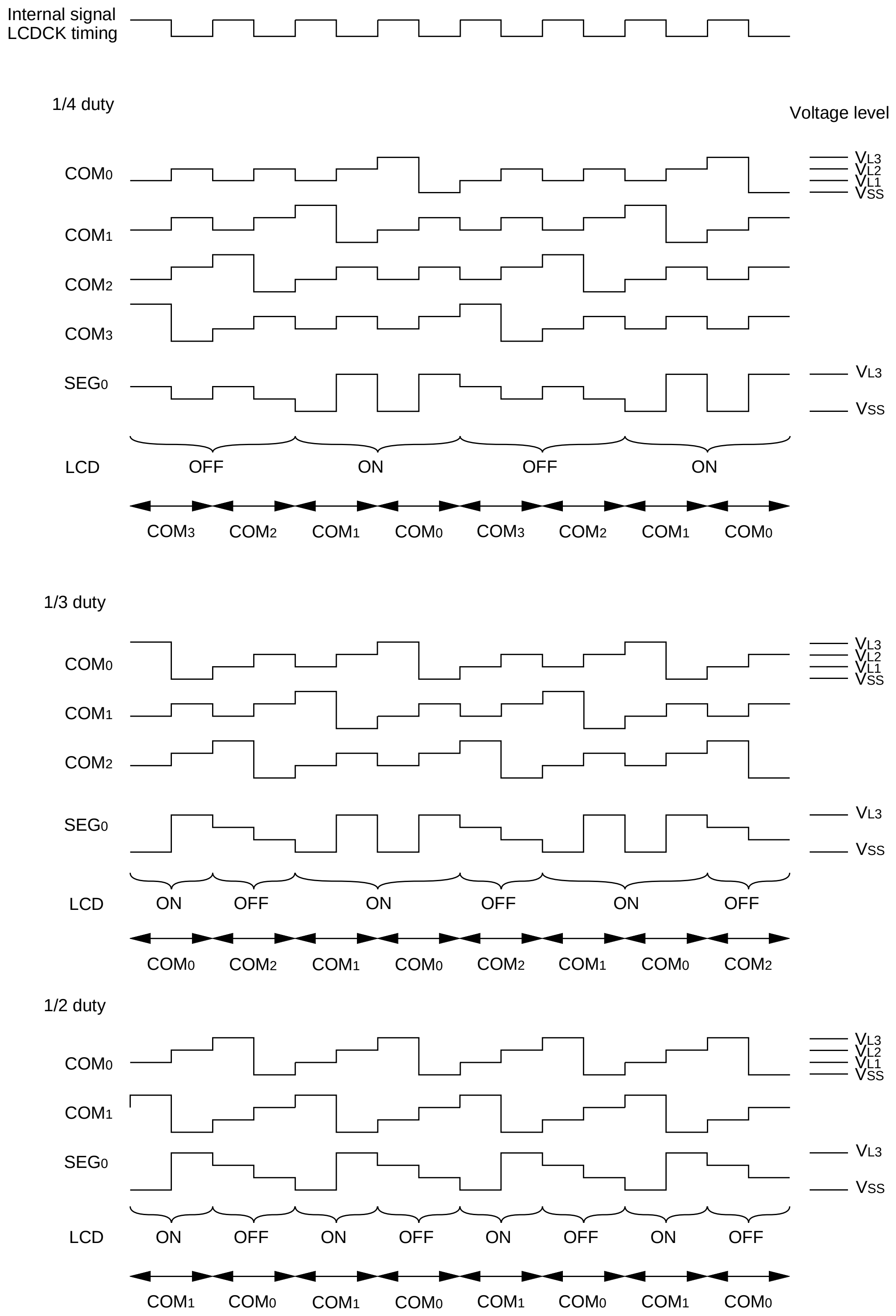


Fig. 39 LCD drive waveform (1/3 bias, type A)

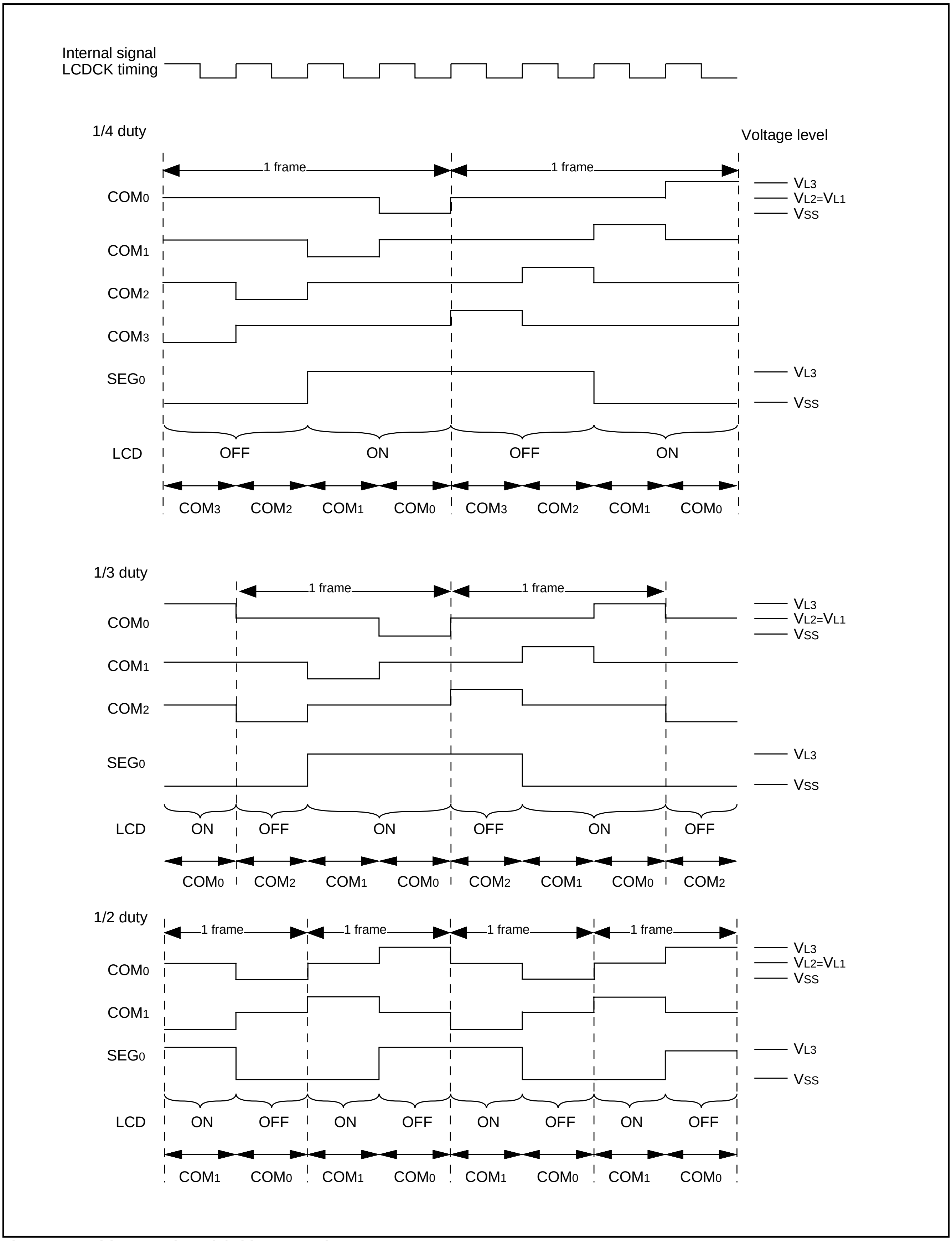


Fig. 40 LCD drive waveform (1/2 bias, type B)

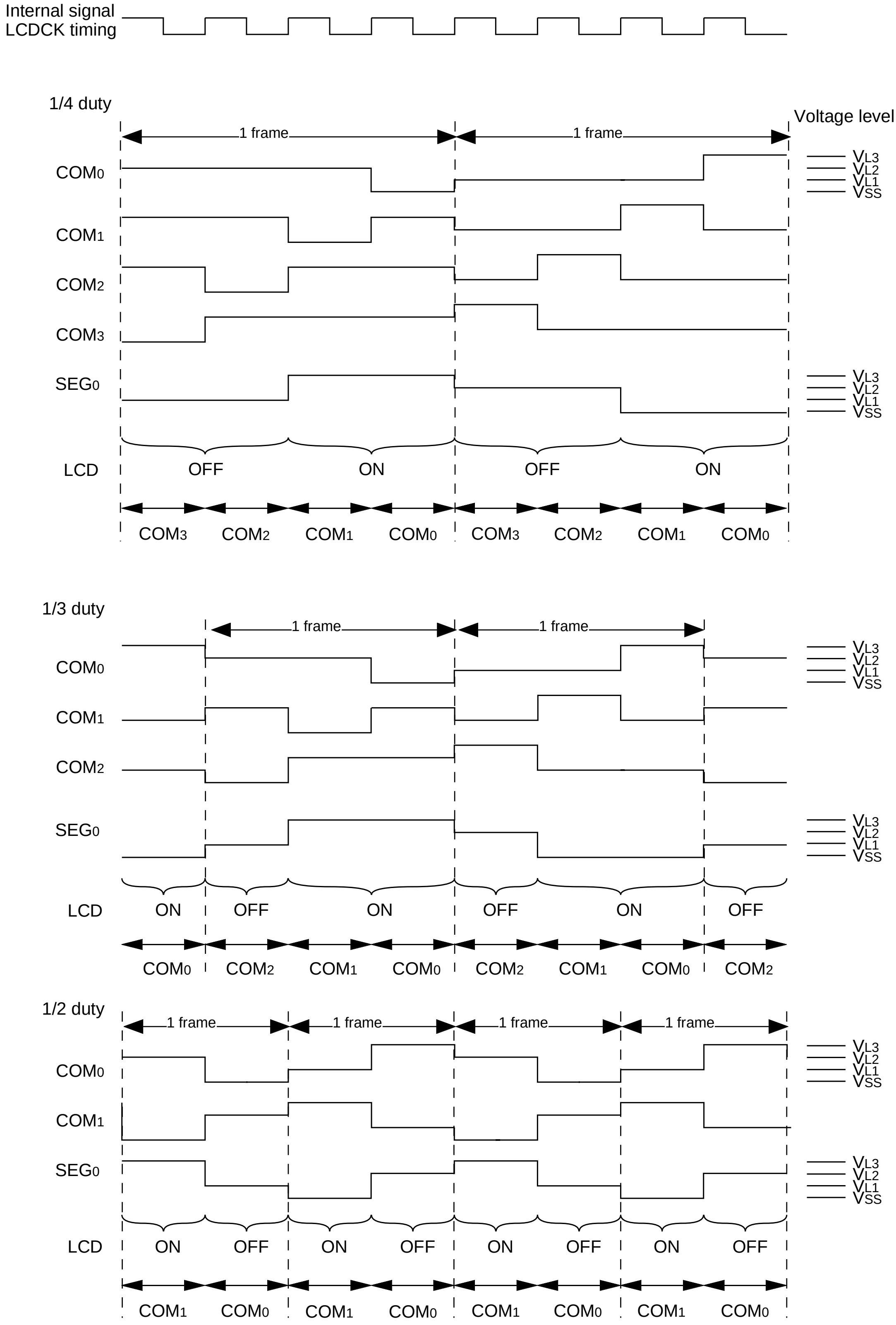


Fig. 41 LCD drive waveform (1/3 bias, type B)

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit counter.

Initial Value of Watchdog Timer

At reset or writing to the watchdog timer control register, each watchdog timer is set to “FF16.” Instructions such as STA, LDM and CLB to generate the write signals can be used.
The written data in bits 0 to 5 are not valid, and the above values are set.

Standard Operation of Watchdog Timer

The watchdog timer is in the stop state at reset and the watchdog timer starts to count down by writing an optional value in the watchdog timer control register. An internal reset occurs at an underflow of the watchdog timer. Then, reset is released after the reset release time is elapsed, the program starts from the reset vector address. Normally, writing to the watchdog timer control register before an underflow of the watchdog timer is programmed. If writing to the watchdog control register is not executed, the watchdog timer does not operate.

When reading the watchdog timer control register is executed, the contents of the high-order 6-bit counter and the STP instruction disable bit (bit 6), and the count source selection bit (bit 7) are read out. When the STP instruction disable bit is “0”, the STP instruction is valid. The STP instruction is disabled by writing to “1” to this bit. In this time, when the STP instruction is executed, it is handled as the undefined instruction, the internal reset occurs. This bit cannot be set to “0” by program. This bit is “0” after reset.
The time until the underflow of the watchdog timer control register after writing to the watchdog timer control register is executed is as follows (when the bit 7 of the watchdog timer control register is “0”) ;

- at frequency/2/4/8 mode (f(XIN)) = 8 MHz): 32.768 ms
- at low-speed mode (f(XCIN) = 32 KHz): 8.19s

■ Note

The watchdog timer continues to count even during the wait time set by timer 1 and timer 2 to release the stop state and in the wait mode. Accordingly, do not underflow the watchdog timer in this time.

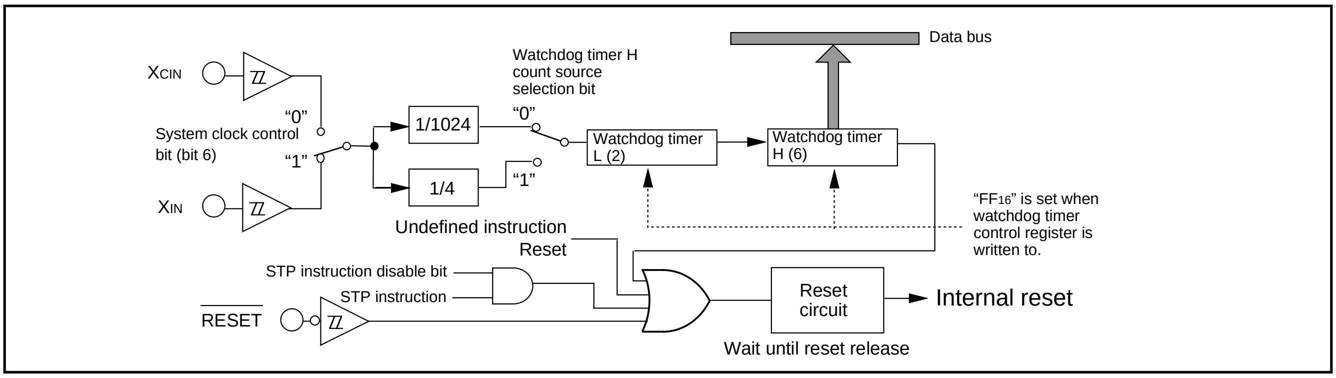


Fig. 42 Block diagram of Watchdog timer

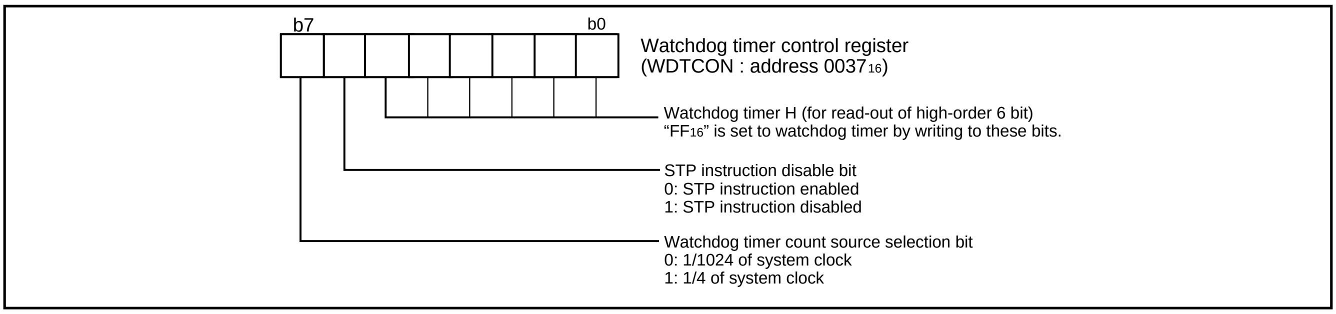


Fig. 43 Structure of Watchdog timer control register

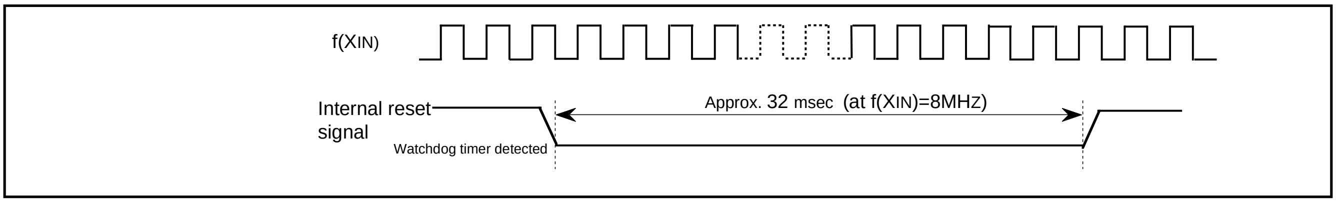


Fig. 44 Timing diagram of reset output

CLOCK OUTPUT FUNCTION

A system clock ϕ can be output from I/O port P3₆.The triple function of I/O port, timer 2 output function and system clock ϕ output function is performed by the clock output control register (address 0018₁₆) and the timer 2 output selection bit of the timer 12 mode register (address 0025₁₆).

In order to output a system clock ϕ from I/O port P3₆, set the timer 2 output selection bit and bit 0 of the clock output control register to "1".

When the clock output function is selected, a clock is output while the direction register of port P3₆ is set to the output mode.

P3₆ is switched to the port output or the output (timer 2 output and the clock output) except port at the cycle after the timer 2 output control bit is switched.

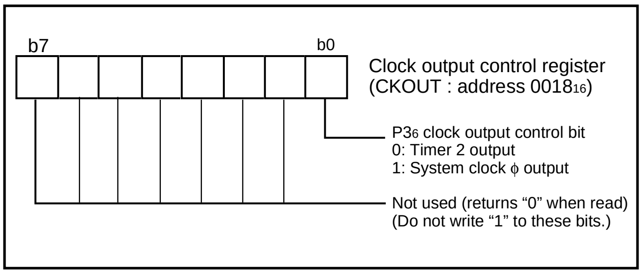


Fig. 45 Structure of clock output control register

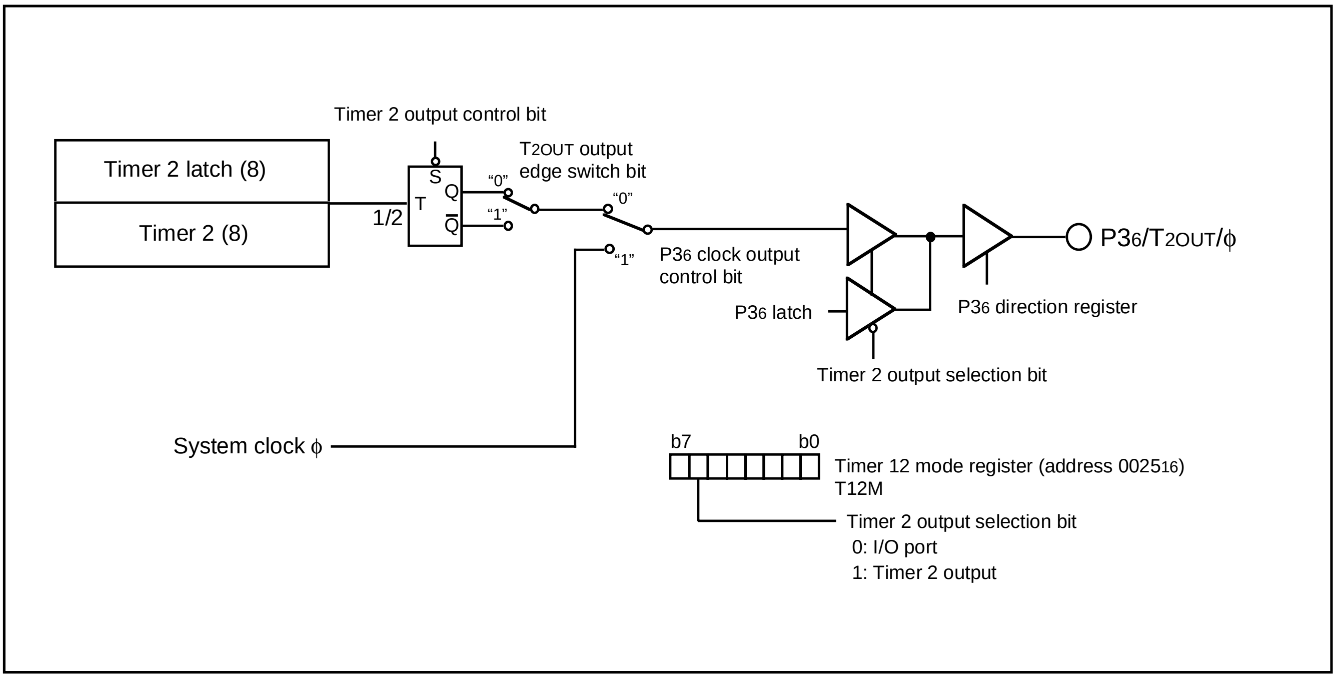


Fig. 46 Block diagram of Clock output function

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 µs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between V_{CC} (min.) and 5.5 V, and the quartz-crystal oscillator should be stable), reset is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage meets V_{IL} spec. when a power source voltage passes V_{CC} (min.).

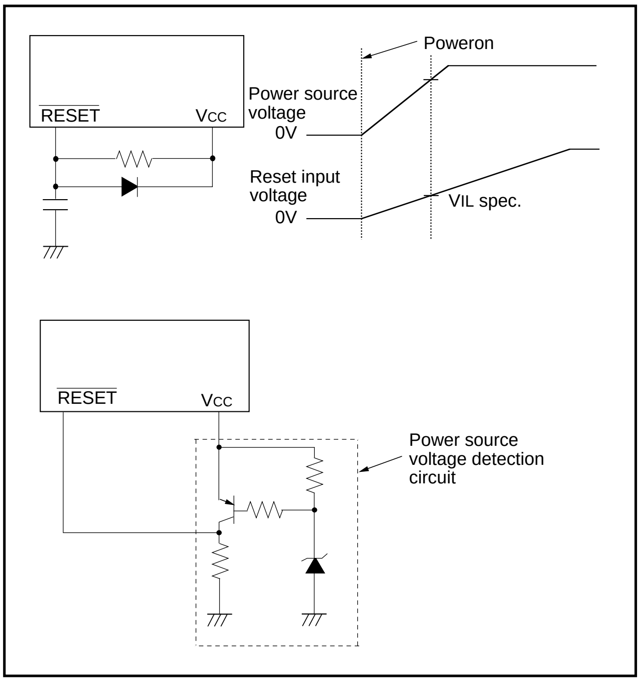
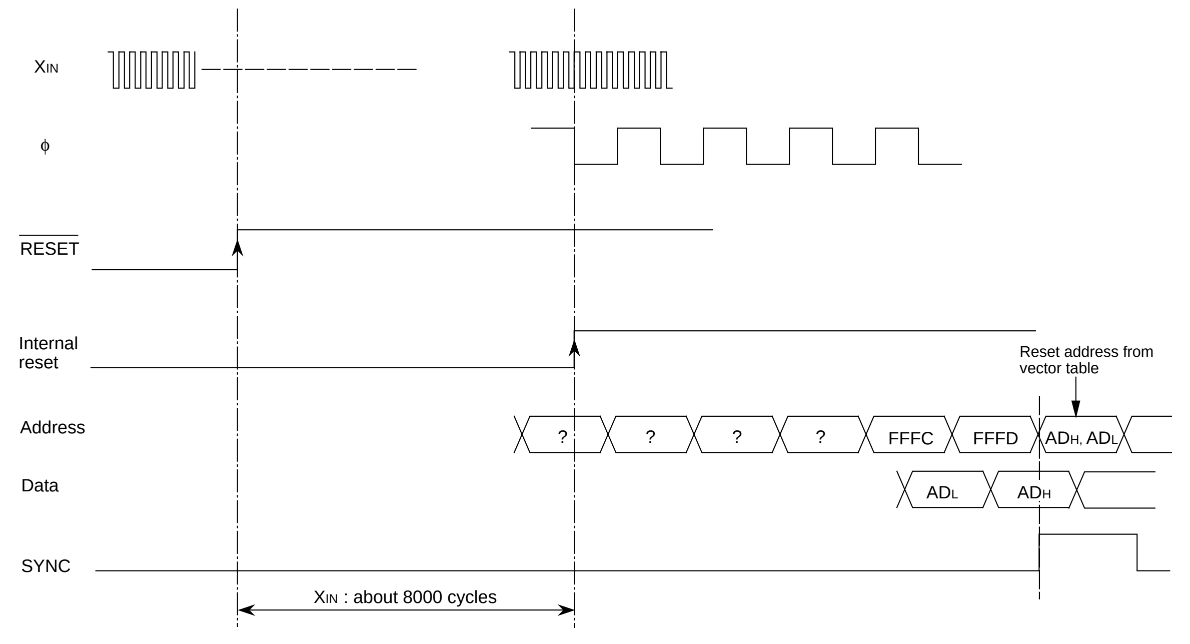


Fig. 47 Reset circuit example



Note 1: The frequency relation of f(XIN) and f(φ) is f(XIN) = 8 • f(φ).
2: The question marks (?) indicate an undefined state that depends on the previous state.

Fig. 48 Reset sequence

	Register	Address	Register contents
(1)	Port P0	0000_{16}	00_{16}
(2)	Port P0 direction register	0001_{16}	00_{16}
(3)	Port P1	0002_{16}	00_{16}
(4)	Port P1 direction register	0003_{16}	00_{16}
(5)	Port P2	0004_{16}	00_{16}
(6)	Port P2 direction register	0005_{16}	00_{16}
(7)	Port P3	0006_{16}	00_{16}
(8)	Port P3 direction register	0007_{16}	00_{16}
(9)	Port P4	0008_{16}	00_{16}
(10)	Port P4 direction register	0009_{16}	00_{16}
(11)	Port P5	$000A_{16}$	00_{16}
(12)	Port P5 direction register	$000B_{16}$	00_{16}
(13)	Port P6	$000C_{16}$	00_{16}
(14)	Port P6 direction register	$000D_{16}$	00_{16}
(15)	Clock output control register	0018_{16}	00_{16}
(16)	A-D control register	0019_{16}	08_{16}
(17)	Serial I/O1 status register	$001D_{16}$	1 0 0 0 0 0 0 0
(18)	Serial I/O2 status register	$001F_{16}$	1 0 0 0 0 0 0 0
(19)	Timer 1	0020_{16}	FF_{16}
(20)	Timer 2	0021_{16}	01_{16}
(21)	Timer 3	0022_{16}	FF_{16}
(22)	Timer 4	0023_{16}	FF_{16}
(23)	PWM01 register	0024_{16}	00_{16}
(24)	Timer 12 mode register	0025_{16}	00_{16}
(25)	Timer 34 mode register	0026_{16}	00_{16}
(26)	Compare register (low-order)	0028_{16}	00_{16}
(27)	Compare register (high-order)	0029_{16}	00_{16}
(28)	Timer X (low-order)	$002A_{16}$	FF_{16}
(29)	Timer X (high-order)	$002B_{16}$	FF_{16}
(30)	Timer X (extension)	$002C_{16}$	00_{16}
(31)	Timer Y (low-order)	$002D_{16}$	FF_{16}
(32)	Timer Y (high-order)	$002E_{16}$	FF_{16}
(33)	Timer X mode register	$002F_{16}$	00_{16}
(34)	Timer Y mode register	0030_{16}	00_{16}
(35)	Watchdog timer control register	0037_{16}	0 0 1 1 1 1 1 1
(36)	LCD power control register	0038_{16}	00_{16}
(37)	LCD mode register	0039_{16}	00_{16}
(38)	Interrupt edge selection register	$003A_{16}$	00_{16}
(39)	CPU mode register	$003B_{16}$	0 1 0 0 1 0 0 0
(40)	Interrupt request register 1	$003C_{16}$	00_{16}
(41)	Interrupt request register 2	$003D_{16}$	00_{16}
(42)	Interrupt control register 1	$003E_{16}$	00_{16}
(43)	Interrupt control register 2	$003F_{16}$	00_{16}
(44)	Serial I/O1 control register	$0FE0_{16}$	00_{16}
(45)	UART1 control register	$0FE1_{16}$	1 1 1 0 0 0 0 0
(46)	Serial I/O2 control register	$0FE3_{16}$	00_{16}
(47)	UART2 control register	$0FE4_{16}$	1 1 1 0 0 0 0 0
(48)	Oscillation output control register	$0FF0_{16}$	00_{16}
(49)	PULL register	$0FF1_{16}$	00_{16}
(50)	Key input control register	$0FF2_{16}$	00_{16}
(51)	Timer 1234 mode register	$0FF3_{16}$	00_{16}
(52)	Timer X control register	$0FF4_{16}$	00_{16}
(53)	Timer 12 frequency division selection register	$0FF5_{16}$	00_{16}
(54)	Timer 34 frequency division selection register	$0FF6_{16}$	00_{16}
(55)	Timer XY frequency division selection register	$0FF7_{16}$	00_{16}
(56)	Segment output disable register 0	$0FF8_{16}$	FF_{16}
(57)	Segment output disable register 1	$0FF9_{16}$	FF_{16}
(58)	Segment output disable register 2	$0FFA_{16}$	FF_{16}
(59)	Timer Y mode register 2	$0FFB_{16}$	00_{16}
(60)	Flash memory control register	$0FFE_{16}$	X X X 0 0 0 0 1
(61)	Processor status register	(PS)	X X X X X 1 X X
(62)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

X: Not fixed

Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 49 Internal status at reset

CLOCK GENERATING CIRCUIT

The 38C2 group has two built-in oscillation circuits; main clock XIN–XOUT and sub-clock XCIN–XCOUT. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feedback resistor exists on-chip. However, an external feedback resistor is needed between XCIN and XCOUT.

To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open. The sub clock XCIN-XCOUT oscillation circuit cannot directly input clocks that are externally generated. Accordingly, be sure to cause an external resonator to oscillate.

Immediately after poweron, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency Control
(1) Frequency/8 Mode

The system clock ϕ is the frequency of XIN divided by 8. After reset is released, this mode is selected.

(2) Frequency/4 Mode

The system clock ϕ is the frequency of XIN divided by 4.

(3) Frequency/2 Mode

The system clock ϕ is the frequency of XIN divided by 2.

(4) Low-speed Mode

The system clock ϕ is the frequency of XCIN divided by 2. In the low-speed mode, the low-power dissipation operation can be performed when the main clock XIN is stopped by setting the bit 7 of the CPU mode register to "0". In this case, when main clock XIN oscillation is restarted, generate the wait time until the oscillation is stable by program after the bit 7 of the CPU mode register is set to "1".

■ Notes on Clock Generating Circuit

If you switch the mode between frequency/2/4, or 8 and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode, set the frequency in the condition that f(XIN) > 3•f(XCIN).

Oscillation Control
(1) Stop Mode

If the STP instruction is executed, the system clock ϕ stops at an "H" level, and main clock and sub-clock oscillators stop.

In this time, values set previously to timer 1 latch and timer 2 latch are loaded automatically to timer 1 and timer 2. Set the values to generate the wait time required for oscillation stabilization to timer 1 latch and timer 2 latch (low-order 8 bits of timer 1 and high-order 8 bits of timer 2) before the STP instruction.

The frequency divider for timer 1 is used for the timer 1 count source, and the output of timer 1 is forcibly connected to timer 2. In this time, bits 0 to 5 of the timer 12 mode register are cleared to "0".

The values of the timer 12 frequency divider selection register are not changed.

Set the interrupt enable bits of the timer 1 and timer 2 to disabled ("0") before executing the STP instruction.

Oscillator restarts when reset occurs or an interrupt request is received, but the system clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

(2) Wait Mode

If the WIT instruction is executed, only the system clock ϕ stops at an "H" state. The states of main clock and sub clock are the same as the state before executing the WIT instruction, and oscillation does not stop. Since supply of system clock ϕ is started immediately after the interrupt is received, the instruction can be executed immediately.

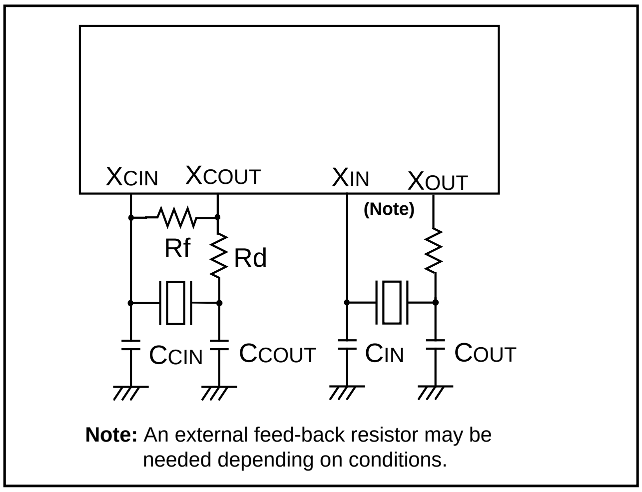


Fig. 50 Ceramic resonator circuit

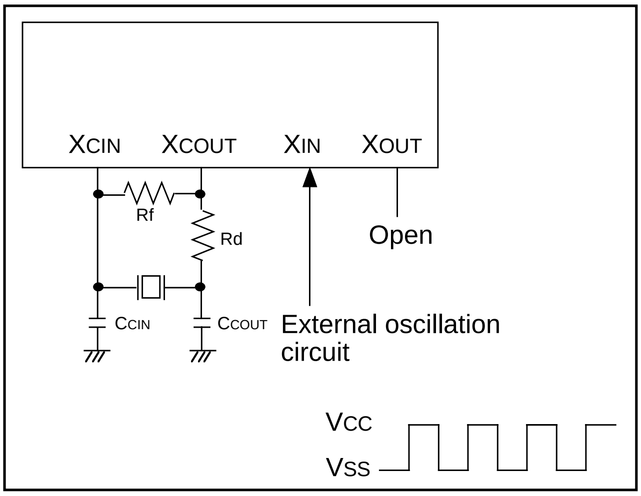


Fig. 51 External clock input circuit

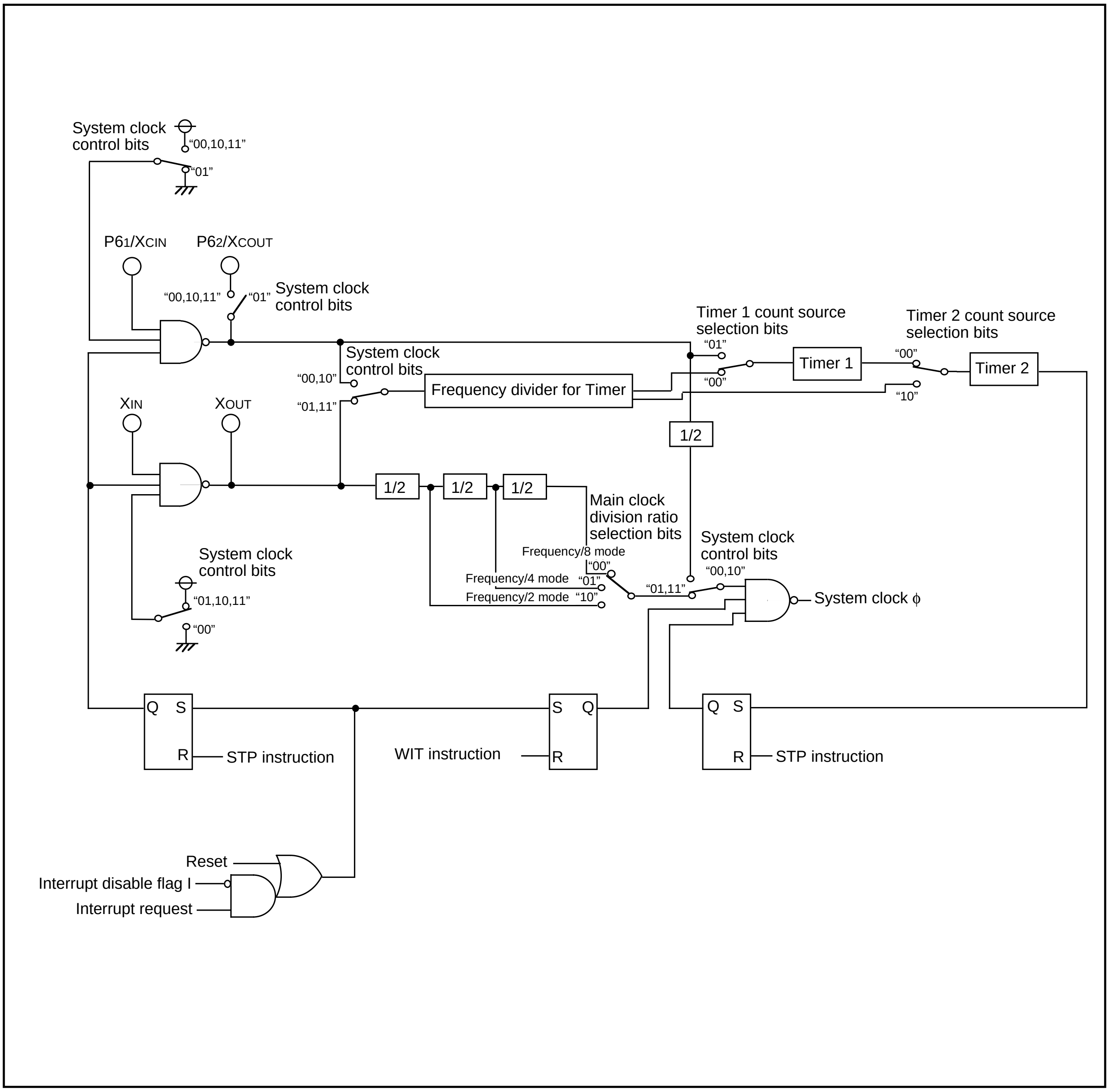
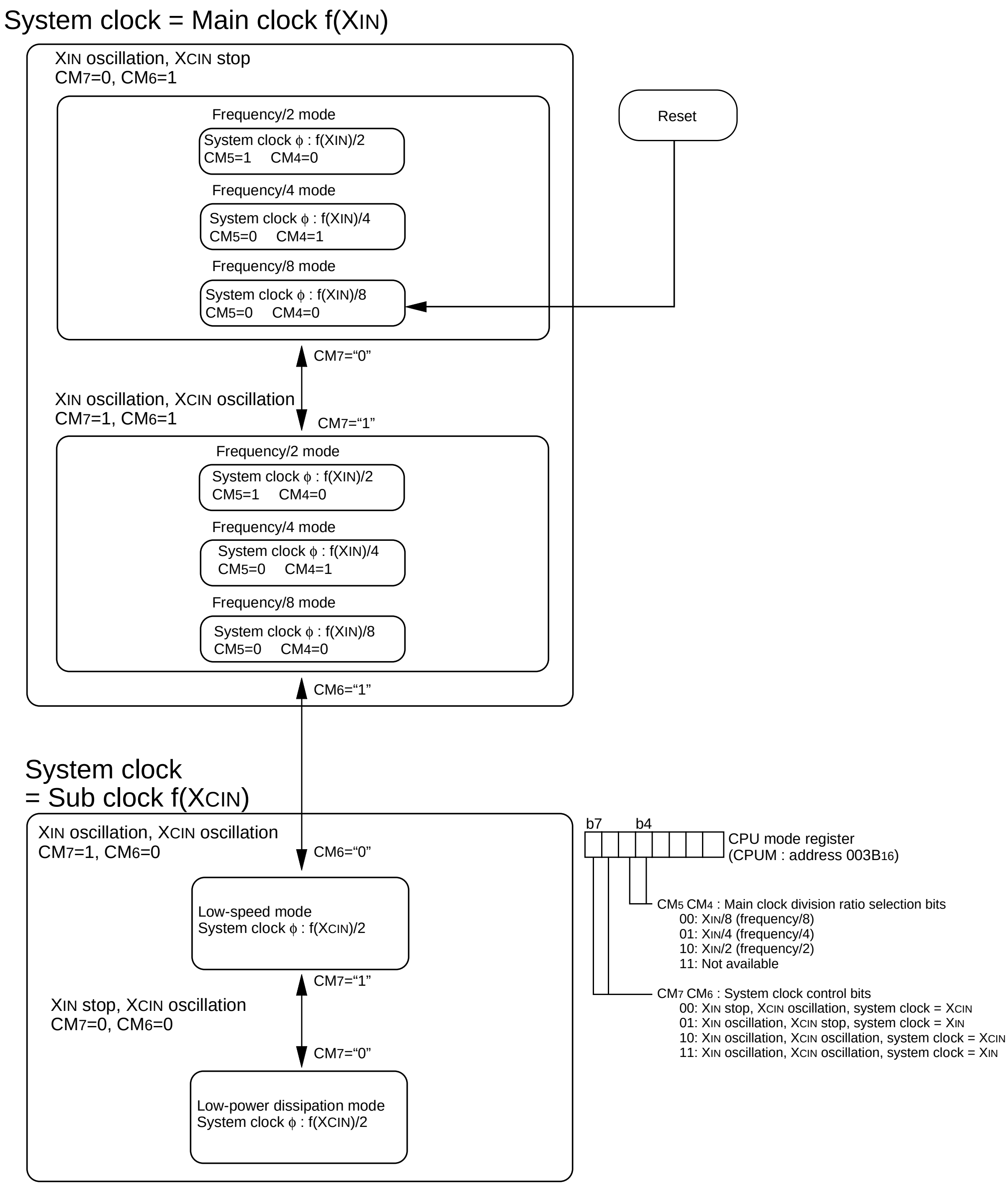


Fig. 52 Clock generating circuit block diagram



Notes 1: When the mode is switched from frequency/2/4/8 to the low-speed mode, or the opposite is performed, change CM7 at first, and then, change CM6 after the oscillation of the changed mode is stabilized.
2: The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
3: Timer and LCD operate in the wait mode.
4: When the stop mode is ended, a delay time can be set by connecting timer 1 and timer 2.

Fig. 53 State transitions of system clock

RENESAS

Oscillation External Output Function

The 38C2 group has the oscillation external output function to output the rectangular waveform of the clock obtained by the oscillation circuits from $P4_1$ and $P4_0$.

In order to validate the oscillation external output function, set $P4_0$ or $P4_1$, or both to the output mode (set the corresponding direction register to “1”).

The level of the XCOUT external output signal becomes “H” by the $P4_0$/$P4_1$ oscillation output control bits (bits 0 and 1) of the oscillation output control register (address $0FF0_{16}$) in the following states;

- the function to output the signal from the XCOUT pin externally is selected
- the sub clock (XCIN–XCOUT) is in the stop oscillating or stop mode.

Likewise, the level of the XOUT external output signal becomes “H” by the $P4_0$/$P4_1$ oscillation output control bits (bits 0 and 1) of the oscillation output control register (address $0FF0_{16}$) in the following states;

- the function to output the signal from the XOUT pin externally is selected
- the main clock (XIN–XOUT) is in the stop oscillating or stop mode.

■ Note

When the signal from the XOUT pin or XCOUT pin of the oscillation circuit is input directly to the circuit except this MCU and used, the system operation may be unstabilized.

In order to share the oscillation circuit safely, use the clock output from $P4_0$ and $P4_1$ by this function for the circuits except this MCU.

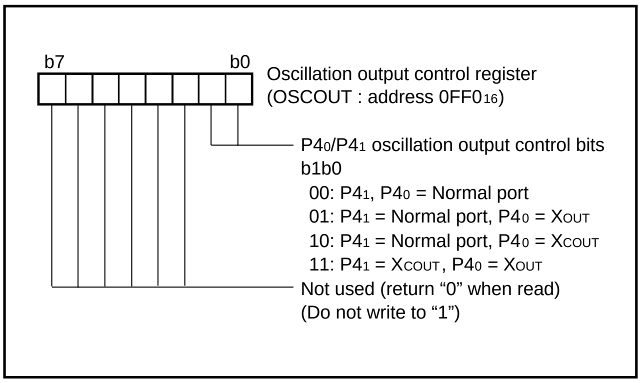


Fig. 54 Structure of oscillation output control register

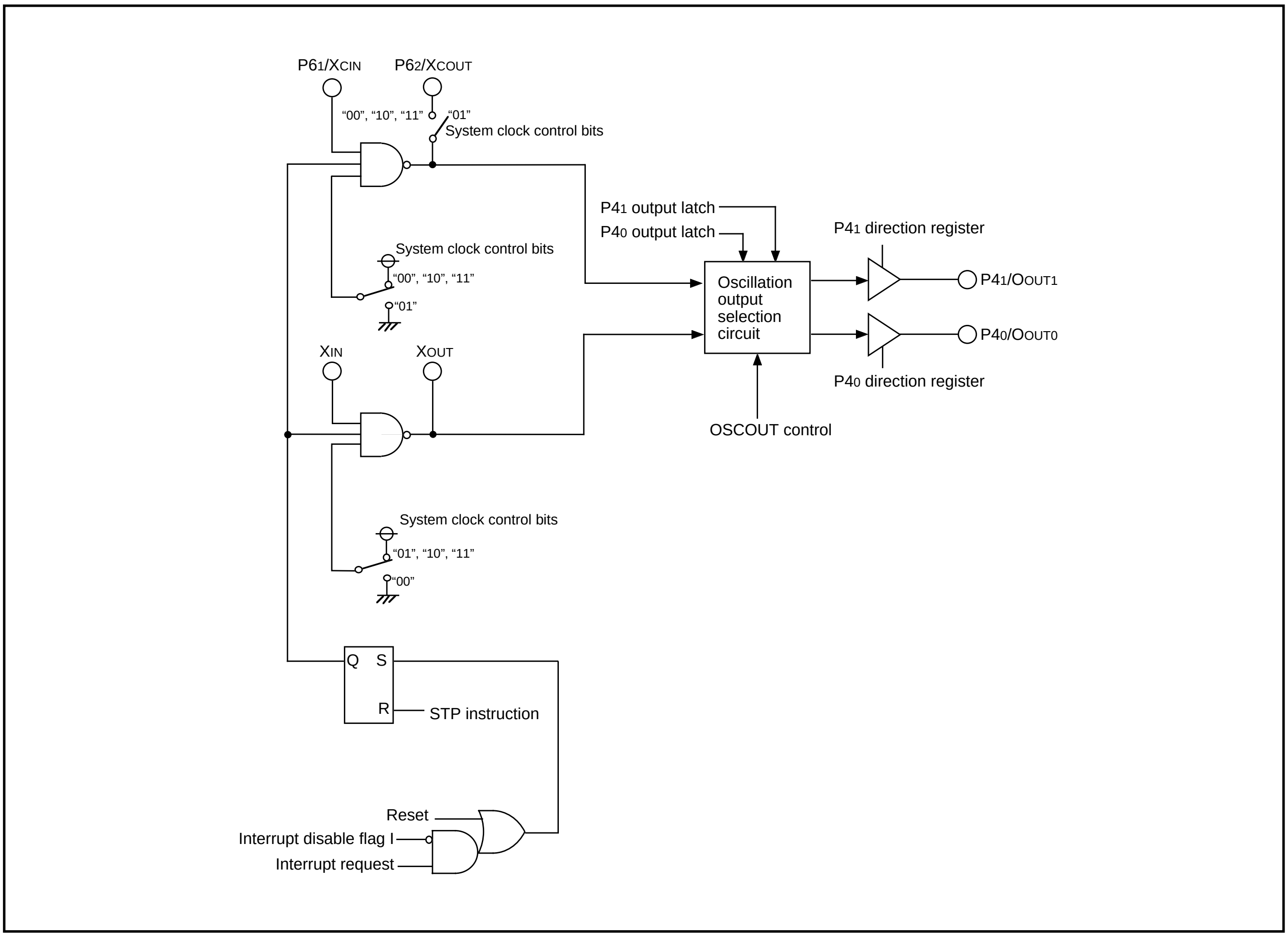


Fig. 55 Block diagram of Oscillation output function

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is “1.” After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to “1,” then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing an SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

- If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
- The timers share the one frequency divider to generate the count source. Accordingly, when each timer starts operating, initializing the frequency divider is not executed. Therefore, when the frequency divider is selected for the count source, the delay of the maximum one cycle of the count source is generated until the timer starts counting or the waveform is output from timer starts operating. Also, the count source cannot be checked externally.

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is “1”
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to “1.”
Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Therefore, set the A-D clock frequency to 250 kHz or more.
Also, when the STP instruction is executed during the A-D conversion, the A-D conversion is stopped immediately, the A-D conversion completion bit is set to “1”, and the interrupt request is generated.

Instruction Execution Time

The instruction execution time is obtained by multiplying the number of cycles shown in the list of machine instructions by the period of the internal clock ϕ.

NOTES ON USE

VL3 pin

When LCD drive control circuit is not used, connect VL3 to VCC.

Countermeasures against noise

(1) Shortest wiring length

① Wiring for RESET pin

Make the length of wiring which is connected to the RESET pin as short as possible. Especially, connect a capacitor across the RESET pin and the VSS pin with the shortest possible wiring (within 20mm).

● Reason

The width of a pulse input into the RESET pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the RESET pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

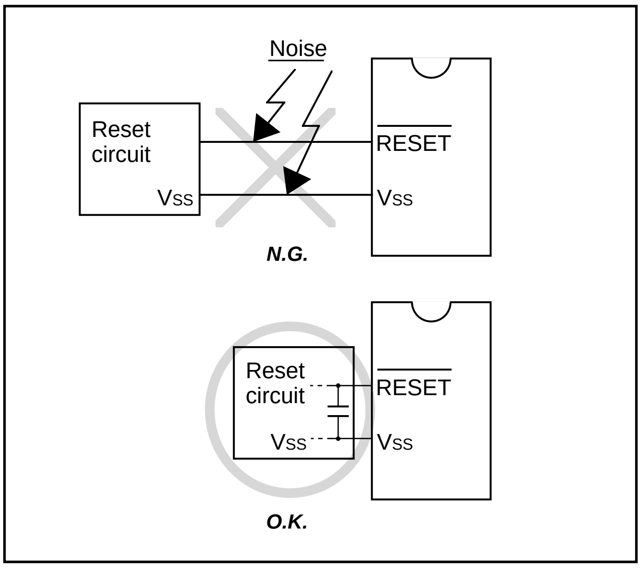


Fig. 56 Wiring for the RESET pin

② Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the VSS pin of a microcomputer as short as possible.
- Separate the VSS pattern only for oscillation from other VSS patterns.

● Reason

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the VSS level of a microcomputer and the VSS level of an oscillator, the correct clock will not be input in the microcomputer.

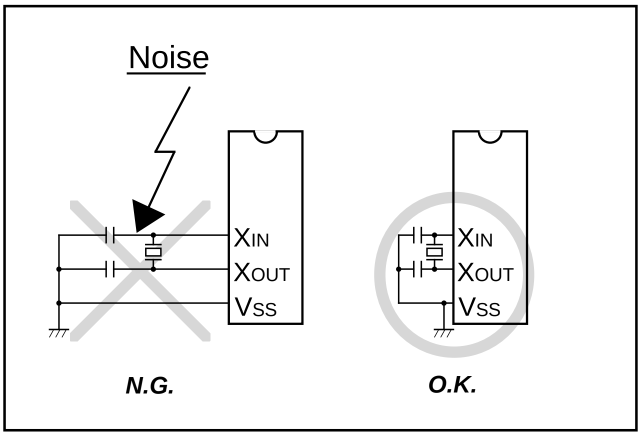


Fig. 57 Wiring for clock I/O pins

(2) Connection of bypass capacitor across VSS line and VCC line

Connect an approximately 0.1 μF bypass capacitor across the VSS line and the VCC line as follows:

- Connect a bypass capacitor across the VSS pin and the VCC pin at equal length.
- Connect a bypass capacitor across the VSS pin and the VCC pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for VSS line and VCC line.
- Connect the power source wiring via a bypass capacitor to the VSS pin and the VCC pin.

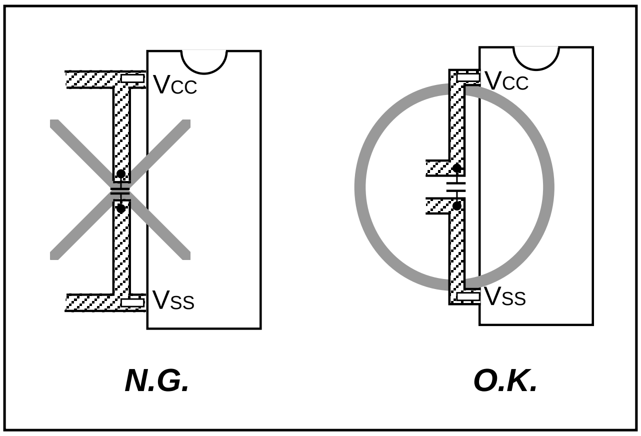


Fig. 58 Bypass capacitor across the VSS line and the VCC line

(3) Oscillator concerns
Take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

① Keeping oscillator away from large current signal lines
Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

● Reason
In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

② Installing oscillator away from signal lines where potential levels change frequently
Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

● Reason
Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

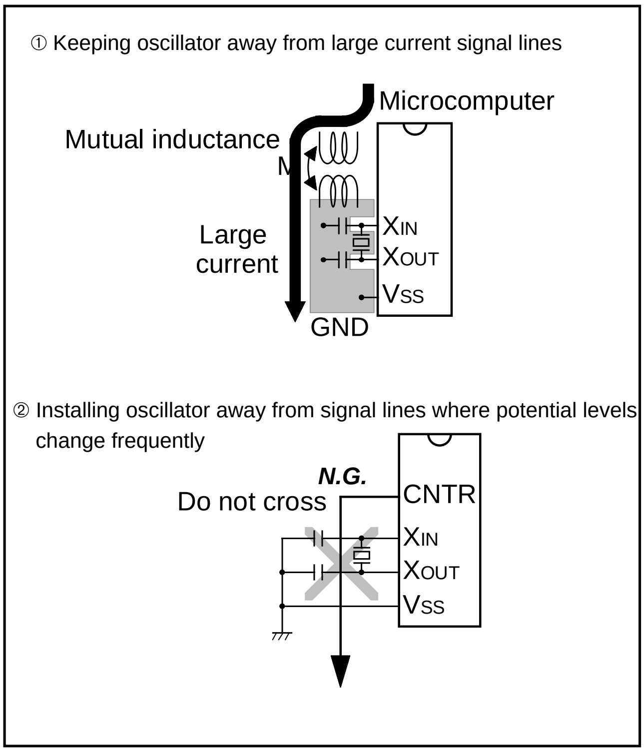


Fig. 59 Wiring for a large current signal line/Writing of signal lines where potential levels change frequently

(4) Wiring to VPP pin of flash memory version
Connect an approximately 10 kΩ resistor to the VPP pin the shortest possible in series and also to the VSS pin.

Note: Even when a circuit which included an approximately 10 kΩ resistor is used in the Mask ROM version, the microcomputer operates correctly.

● Reason
The VPP pin of the flash memory version is the power source input pin for the built-in flash memory. When programming/erasing in the built-in flash memory, the impedance of the VPP pin is low to allow the electric current for writing/erasing flow into the flash memory. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the built-in flash memory, which may cause a program runaway.

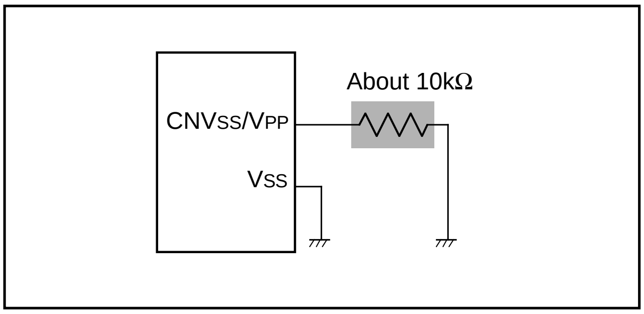


Fig. 60 Wiring for the VPP pin of flash memory

Electric Characteristic Differences Between Mask ROM and Flash memory Version MCUs

There are differences in electric characteristics, operation margin, noise immunity, and noise radiation between the mask ROM and flash memory version MCUs due to the difference in the manufacturing processes.
When manufacturing an application system with the flash memory version and then switching to use of the mask ROM version, please perform sufficient evaluations for the commercial samples of the Mask ROM version.

Oscillation Circuit Constant

(1) Determine an oscillation circuit constant after consulting the oscillator manufacturer about the matching characteristic evaluation.
(2) Since oscillation circuit constants may be differences between the flash memory version and the mask ROM version, evaluate them, respectively.

FLASH MEMORY MODE

The 38C2 group (A version)'s flash memory version has an internal new DINOR (DIvided bit line NOR) flash memory that can be rewritten with a single power source when VCC is 4.5 to 5.5 V, and 2 power sources when VCC is 3.0 to 4.5 V.

For this flash memory, three flash memory modes are available in which to read, program, and erase: the parallel I/O and standard serial I/O modes in which the flash memory can be manipulated using a programmer and the CPU rewrite mode in which the flash memory can be manipulated by the Central Processing Unit (CPU).

Summary

Table 11 lists the summary of the 38C2 group (A version)'s flash memory version.

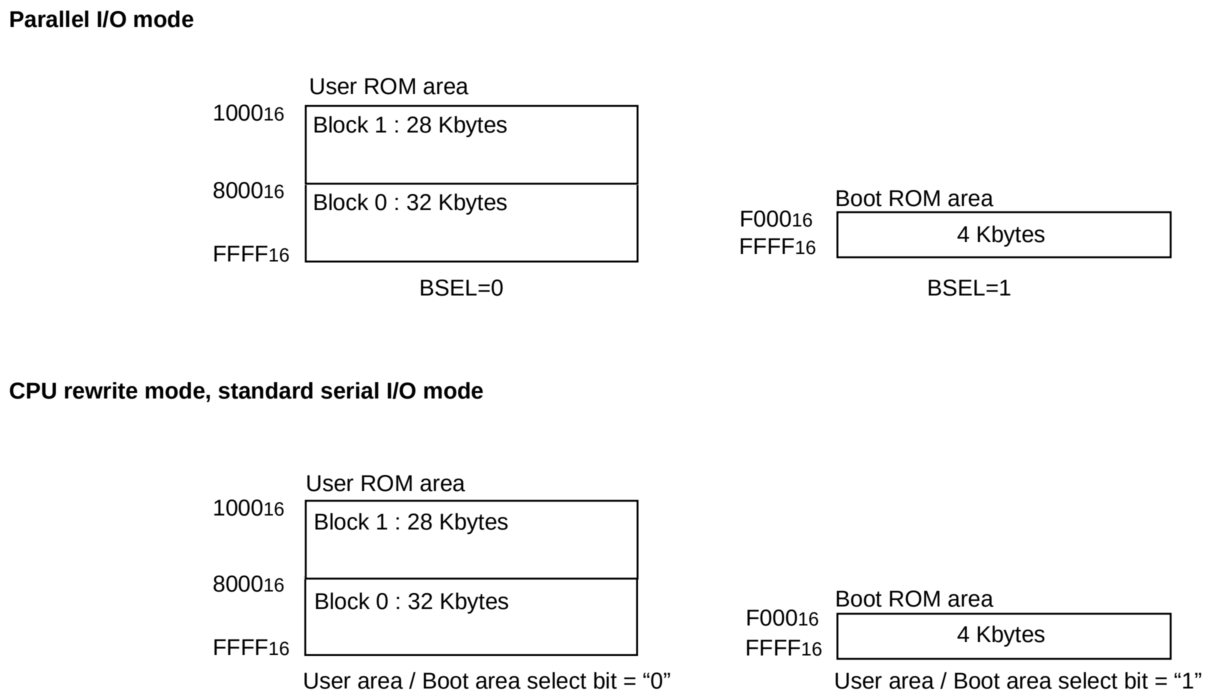
This flash memory version has some blocks on the flash memory as shown in Figure 61 and each block can be erased.

In addition to the ordinary User ROM area to store the MCU operation control program, the flash memory has a Boot ROM area that is used to store a program to control rewriting in CPU rewrite and standard serial I/O modes. This Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. However, the user can write a rewrite control program in this area that suits the user's application system. This Boot ROM area can be rewritten in only parallel I/O mode.

Table 11 Summary of 38C2 group (A version)'s flash memory version

Item		Specifications
Power source voltage (Vcc)		VCC = 2.5 to 5.5 V (Note 1)
		VCC = 2.5 to (VCC at program/erase) + 0.5 V (Note 2)
Program/Erase VPP voltage (VPP)		VPP = 4.5 to 5.5 V, VCC = 3.0 to 5.5 V
Flash memory mode		3 modes; Parallel I/O mode, Standard serial I/O mode, CPU rewrite mode
Erase block division	User ROM area	Refer to Fig. 61.
	Boot ROM area	Not divided (4K bytes) (Note 3)
Program method		In units of bytes
Erase method		Block erase
Program/Erase control method		Program/Erase control by software command
Number of commands		5 commands
Number of program/Erase times		100 times
ROM code protection		Available in parallel I/O mode and standard serial I/O mode

Notes 1: It is the rating value when Vcc = 5.0 to 5.5 V at program/erase.
2: It is the rating value when Vcc = 3.0 to 5.0 V at program/erase.
3: The Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. This Boot ROM area can be erased and written in only parallel I/O mode.



Product name	Flash memory top address
M38C29FFA	1000_{16}

Notes 1: The Boot ROM area can be rewritten in only parallel I/O mode. (Access to any other areas is inhibited.)
2: To specify a block, use the maximum address in the block.

Fig. 61 Block diagram of built-in flash memory

(1) CPU Rewrite Mode

In CPU rewrite mode, the internal flash memory can be operated on (read, program, or erase) under control of the Central Processing Unit (CPU).
In CPU rewrite mode, only the User ROM area shown in Figure 61 can be rewritten; the Boot ROM area cannot be rewritten. Make sure the program and block erase commands are issued for only the User ROM area and each block area.
The control program for CPU rewrite mode can be stored in either User ROM or Boot ROM area. In the CPU rewrite mode, because the flash memory cannot be read from the CPU, the rewrite control program must be transferred to internal RAM area before it can be executed.

Boot Mode

The control program for CPU rewrite mode must be written into the User ROM or Boot ROM area in parallel I/O mode beforehand. (If the control program is written into the Boot ROM area, the standard serial I/O mode becomes unusable.)
See Figure 61 for details about the Boot ROM area.
Normal microcomputer mode is entered when the microcomputer is reset with pulling CNVSS pin low. In this case, the CPU starts operating using the control program in the User ROM area.
When the microcomputer is reset by pulling the $P4_1(\overline{CE})$ pin high, the CNVSS pin high, the CPU starts operating (start address of program is stored into addresses $FFFC_{16}$ and $FFFD_{16}$) using the control program in the Boot ROM area. This mode is called the "Boot mode". Also, User ROM area can be rewritten using the control program in the Boot ROM area.

Block Address

Block addresses refer to the maximum address of each block. These addresses are used in the block erase command.

Outline Performance (CPU Rewrite Mode)

CPU rewrite mode is usable in the single-chip or Boot mode. The only User ROM area can be rewritten.

In CPU rewrite mode, the CPU erases, programs and reads the internal flash memory as instructed by software commands. This rewrite control program must be transferred to internal RAM area before it can be executed.

The MCU enters CPU rewrite mode by applying 4.5 V to 5.5 V to the CNVSS pin and setting "1" to the CPU rewrite mode select bit (bit 1 of address $0FFE_{16}$). Then, software commands can be accepted.

Use software commands to control program and erase operations. Whether a program or erase operation has terminated normally or in error can be verified by reading the status register.

Figure 62 shows the flash memory control register.

Bit 0 of the flash memory control register is the RY/$\overline{BY}$ status flag used exclusively to read the operating status of the flash memory. During programming and erase operations, it is "0" (busy). Otherwise, it is "1" (ready).

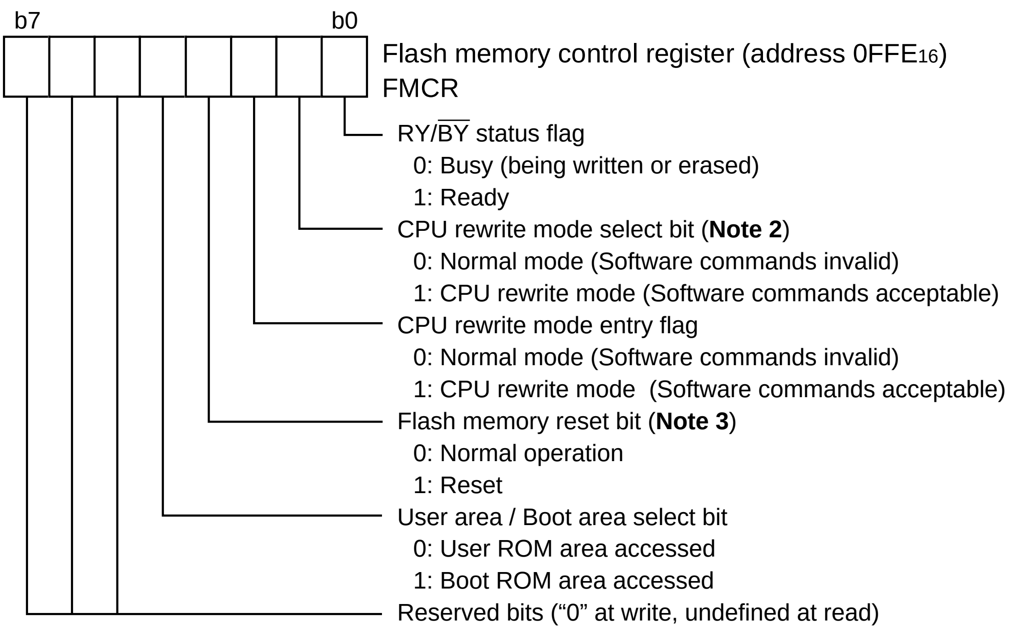
Bit 1 of the flash memory control register is the CPU rewrite mode select bit. When this bit is set to "1", the MCU enters CPU rewrite mode. And then, software commands can be accepted. In CPU rewrite mode, the CPU becomes unable to access the internal flash memory directly. Therefore, use the control program in the internal RAM for write to bit 1. To set this bit 1 to "1", it is necessary to write "0" and then write "1" in succession to bit 1. The bit can be set to "0" by only writing "0".

Bit 2 of the flash memory control register is the CPU rewrite mode entry flag. This flag indicates "1" in CPU rewrite mode, so that reading this flag can check whether CPU rewrite mode has been entered or not.

Bit 3 of the flash memory control register is the flash memory reset bit used to reset the control circuit of internal flash memory. This bit is used when exiting CPU rewrite mode and when flash memory access has failed. When the CPU rewrite mode select bit is "1", setting "1" for this bit resets the control circuit. To release the reset, it is necessary to set this bit to "0".

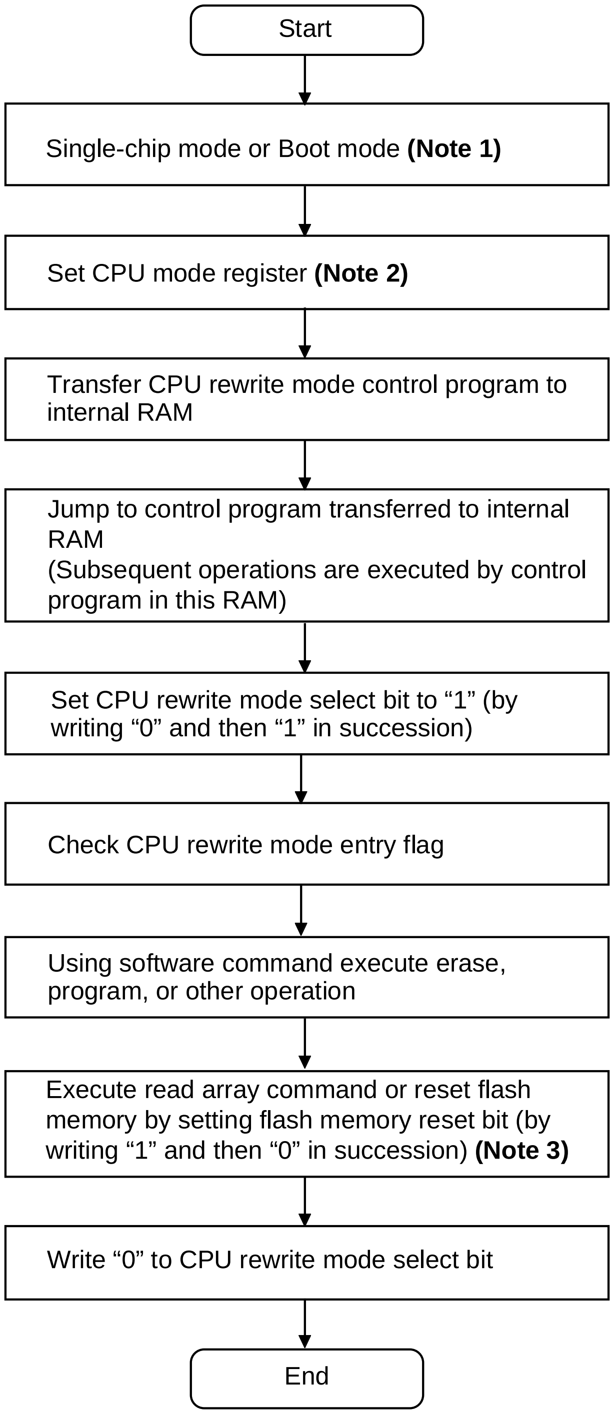
Bit 4 of the flash memory control register is the User area/Boot area select bit. When this bit is set to "1", Boot ROM area is accessed, and CPU rewrite mode in Boot ROM area is available. In Boot mode, this bit is set to "1" automatically. Programming of this bit must be executed on program of the internal RAM.

Figure 63 shows a flowchart for setting/releasing CPU rewrite mode.



Notes **1**: The contents of flash memory control register are "XXX00001" just after reset release.
2: For this bit to be set to "1", the user needs to write "0" and then "1" to it in succession. Use the control program in the RAM for write to this bit.
3: This bit is valid when the CPU rewrite mode select bit is "1". Set this bit 3 to "0" subsequently after setting bit 3 to "1".

Fig. 62 Structure of flash memory control register



Notes 1: When starting the MCU in the single-chip mode, supply 4.5 to 5.5 V to the CNVss pin until checking the CPU rewrite mode entry flag.

2: Set the main clock as follows depending on the X_{IN} divider select bits of clock control register (bits 4, 5 of address $003F_{16}$):

3: Before exiting the CPU rewrite mode after completing erase or program operation, always be sure to execute the read array command or reset the flash memory.

Fig. 63 CPU rewrite mode set/release flowchart

Notes on CPU Rewrite Mode

Take the notes described below when rewriting the flash memory in CPU rewrite mode.

●Operation speed

During CPU rewrite mode, set the system clock ϕ to 4.0 MHz or less using the main clock division ratio selection bits (bits 4 and 5 of address $003B_{16}$).

●Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during CPU rewrite mode.

●Interrupts inhibited against use

The interrupts cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory.

●Watchdog timer

If the watchdog timer has been already activated, internal reset due to an underflow will not occur because the watchdog timer is surely cleared during program or erase.

●Reset

Reset is always valid. The MCU is activated using the boot mode at release of reset in the condition of CNVss = “H”, so that the program will begin at the address which is stored in addresses $FFFC_{16}$ and $FFFD_{16}$ of the boot ROM area.

Software Commands

Table 12 lists the software commands.

After setting the CPU rewrite mode select bit to "1", execute a software command to specify an erase or program operation.

Each software command is explained below.

●Read Array Command (FF16)

The read array mode is entered by writing the command code "FF16" in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the contents of the specified address are read out at the data bus (D0 to D7).

The read array mode is retained until another command is written.

●Read Status Register Command (7016)

When the command code "7016" is written in the first bus cycle, the contents of the status register are read out at the data bus (D0 to D7) by a read in the second bus cycle.

The status register is explained in the next section.

●Clear Status Register Command (5016)

This command is used to clear the bits SR4 and SR5 of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code "5016" in the first bus cycle.

●Program Command (4016)

Program operation starts when the command code "4016" is written in the first bus cycle. Then, if the address and data to program are written in the 2nd bus cycle, program operation (data programming and verification) will start.

Whether the write operation is completed can be confirmed by read status register or the RY/$\overline{\text{BY}}$ status flag. When the program starts, the read status register mode is entered automatically and the contents of the status register is read at the data bus (D0 to D7). The status register bit 7 (SR7) is set to "0" at the same time the write operation starts and is returned to "1" upon completion of the write operation. In this case, the read status register mode remains active until the read array command (FF16) is written.

The RY/$\overline{\text{BY}}$ status flag of the flash memory control register is "0" during write operation and "1" when the write operation is completed as is the status register bit 7.

At program end, program results can be checked by reading the status register.

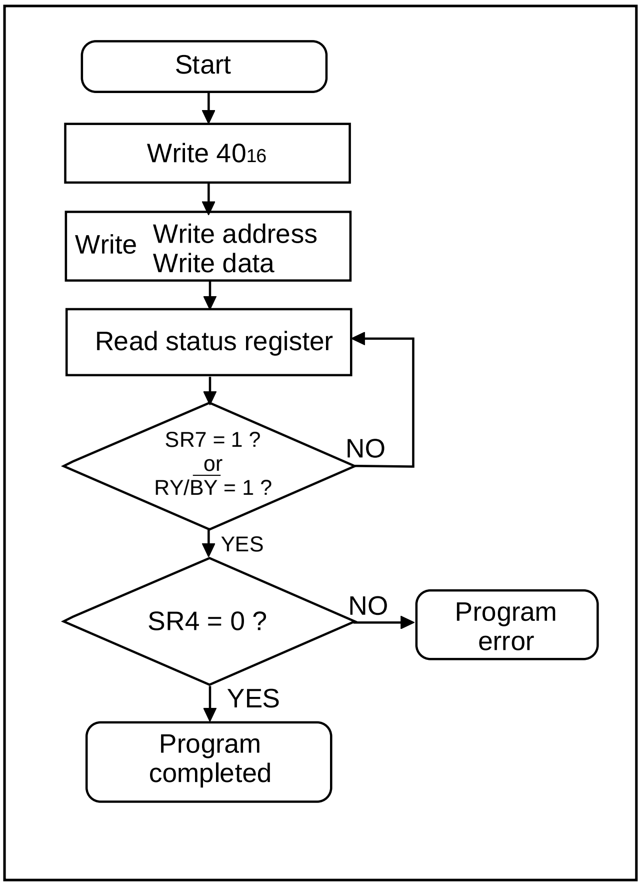


Fig. 64 Program flowchart

Table 12 List of software commands (CPU rewrite mode)

Command	Cycle number	First bus cycle			Second bus cycle		
		Mode	Address	Data (D0 to D7)	Mode	Address	Data (D0 to D7)
Read array	1	Write	X **(Note 4)**	FF16			
Read status register	2	Write	X	7016	Read	X	SRD **(Note 1)**
Clear status register	1	Write	X	5016			
Program	2	Write	X	4016	Write	WA **(Note 2)**	WD **(Note 2)**
Block erase	2	Write	X	2016	Write	BA **(Note 3)**	D016

Notes 1: SRD = Status Register Data
2: WA = Write Address, WD = Write Data
3: BA = Block Address to be erased (Input the maximum address of each block.)
4: X denotes a given address in the User ROM area.

●Block Erase Command (20_{16}/$D0_{16}$)

By writing the command code "20_{16}" in the first bus cycle and the confirmation command code "$D0_{16}$" and the block address in the second bus cycle that follows, the block erase (erase and erase verify) operation starts for the block address of the flash memory to be specified.

Whether the block erase operation is completed can be confirmed by read status register or the RY/$\overline{\text{BY}}$ status flag of flash memory control register. At the same time the block erase operation starts, the read status register mode is automatically entered, so that the contents of the status register can be read out. The status register bit 7 (SR7) is set to "0" at the same time the block erase operation starts and is returned to "1" upon completion of the block erase operation. In this case, the read status register mode remains active until the read array command (FF_{16}) is written.

The RY/$\overline{\text{BY}}$ status flag is "0" during block erase operation and "1" when the block erase operation is completed as is the status register bit 7.

After the block erase ends, erase results can be checked by reading the status register. For details, refer to the section where the status register is detailed.

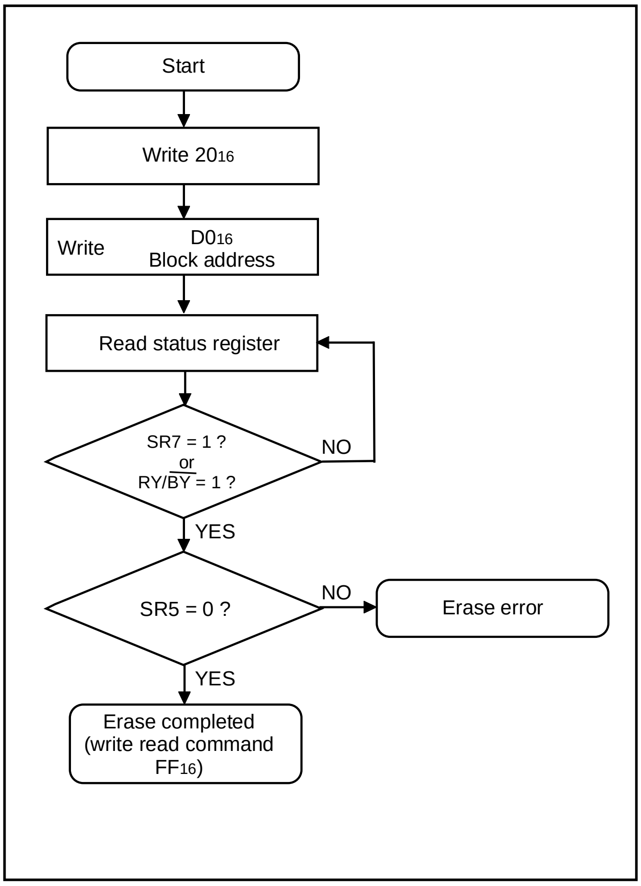


Fig. 65 Erase flowchart

Status Register

The status register shows the operating status of the flash memory and whether erase operations and programs ended successfully or in error. It can be read in the following ways:

(1) By reading an arbitrary address from the User ROM area after writing the read status register command (70_{16})
(2) By reading an arbitrary address from the User ROM area in the period from when the program starts or erase operation starts to when the read array command (FF_{16}) is input.

Also, the status register can be cleared by writing the clear status register command (50_{16}).
After reset, the status register is set to "80_{16}".
Table 13 shows the status register. Each bit in this register is explained below.

•Sequencer status (SR7)
The sequencer status indicates the operating status of the flash memory. This bit is set to "0" (busy) during write or erase operation and is set to "1" when these operations ends.
After power-on, the sequencer status is set to "1" (ready).

•Erase status (SR5)
The erase status indicates the operating status of erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is reset to "0".

•Program status (SR4)
The program status indicates the operating status of write operation. When a write error occurs, it is set to "1".
The program status is reset to "0" when it is cleared.

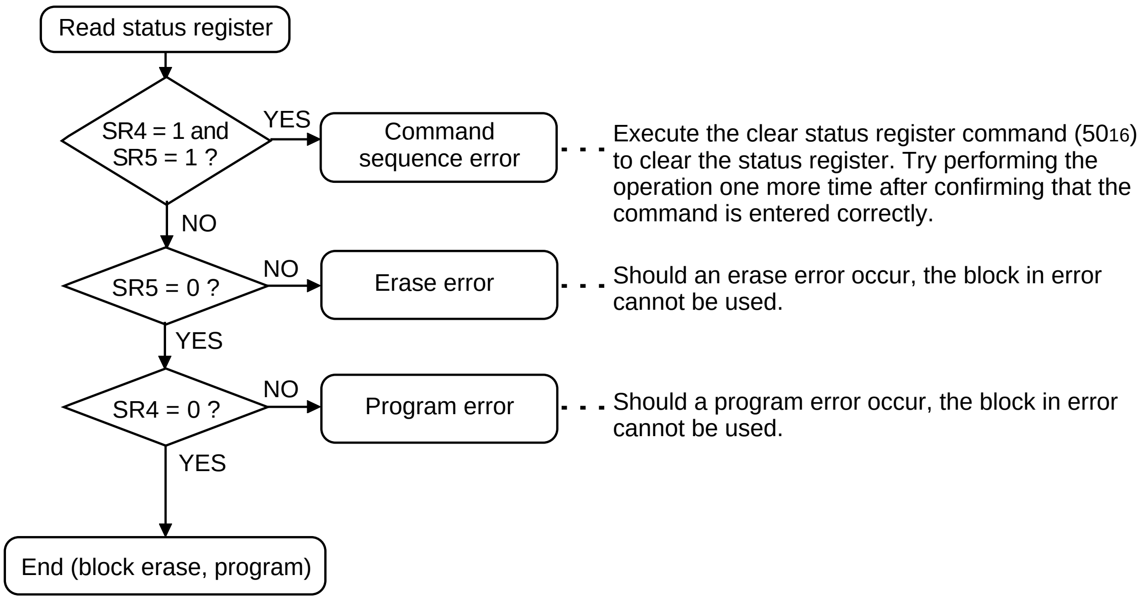
If "1" is written for any of the SR5 and SR4 bits, the read array, program, and block erase commands are not accepted. Before executing these commands, execute the clear status register command (50_{16}) and clear the status register.
Also, if any commands are not correct, both SR5 and SR4 are set to "1".

Table 13 Definition of each bit in status register

Each bit of SRD bits	Status name	Definition	
		"1"	"0"
SR7 (bit7)	Sequencer status	Ready	Busy
SR6 (bit6)	Reserved	-	-
SR5 (bit5)	Erase status	Terminated normally	Terminated normally
SR4 (bit4)	Program status	Terminated normally	Terminated normally
SR3 (bit3)	Reserved	-	-
SR2 (bit2)	Reserved	-	-
SR1 (bit1)	Reserved	-	-
SR0 (bit0)	Reserved	-	-

Full Status Check

By performing full status check, it is possible to know the execution results of erase and program operations. Figure 66 shows a full status check flowchart and the action to be taken when each error occurs.



Note: When one of SR5 and SR4 is set to “1”, none of the read array, program, and block erase commands is accepted. Execute the clear status register command (50_{16}) before executing these commands.

Fig. 66 Full status check flowchart and remedial procedure for errors

Functions To Inhibit Rewriting Flash Memory Version

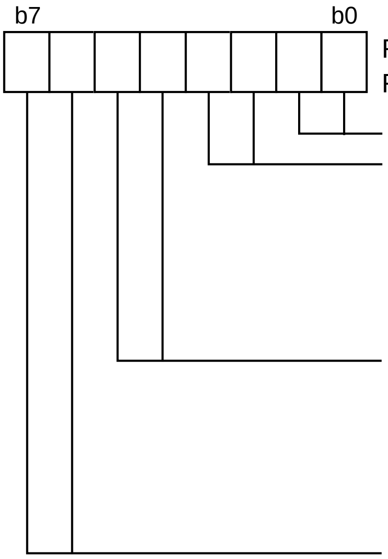
To prevent the contents of internal flash memory from being read out or rewritten easily, this MCU incorporates a ROM code protect function for use in parallel I/O mode and an ID code check function for use in standard serial I/O mode.

●ROM Code Protect Function

The ROM code protect function is the function to inhibit reading out or modifying the contents of internal flash memory by using the ROM code protect control address (address $FFDB_{16}$) in parallel I/O mode. Figure 67 shows the ROM code protect control address (address $FFDB_{16}$). (This address exists in the User ROM area.)

If one or both of the pair of ROM code protect bits is set to “0”, the ROM code protect is turned on, so that the contents of internal flash memory are protected against readout and modification. The ROM code protect is implemented in two levels. If level 2 is selected, the flash memory is protected even against readout by a shipment inspection LSI tester, etc. When an attempt is made to select both level 1 and level 2, level 2 is selected by default.

If both of the two ROM code protect reset bits are set to “00”, the ROM code protect is turned off, so that the contents of internal flash memory can be readout or modified. Once the ROM code protect is turned on, the contents of the ROM code protect reset bits cannot be modified in parallel I/O mode. Use the serial I/O or CPU rewrite mode to rewrite the contents of the ROM code protect reset bits.



ROM code protect control address (address $FFDB_{16}$)
ROMCP (FF_{16} when shipped)

Reserved bits (“1” at read/write)

ROM code protect level 2 set bits (ROMCP2) (**Notes 1, 2**)
b3b2
0 0: Protect enabled
0 1: Protect enabled
1 0: Protect enabled
1 1: Protect disabled

ROM code protect reset bits (**Note 3**)
b5b4
0 0: Protect removed
0 1: Protect set bits effective
1 0: Protect set bits effective
1 1: Protect set bits effective

ROM code protect level 1 set bits (ROMCP1) (**Note 1**)
b7b6
0 0: Protect enabled
0 1: Protect enabled
1 0: Protect enabled
1 1: Protect disabled

Notes 1: When ROM code protect is turned on, the internal flash memory is protected against readout or modification in parallel I/O mode.
2: When ROM code protect level 2 is turned on, ROM code readout by a shipment inspection LSI tester, etc. also is inhibited.
3: The ROM code protect reset bits can be used to turn off ROM code protect level 1 and ROM code protect level 2. However, since these bits cannot be modified in parallel I/O mode, they need to be rewritten in serial I/O mode or CPU rewrite mode.

Fig. 67 Structure of ROM code protect control address

ID Code Check Function

Use this function in standard serial I/O mode. When the contents of the flash memory are not blank, the ID code sent from the programmer is compared with the ID code written in the flash memory to see if they match. If the ID codes do not match, the commands sent from the programmer are not accepted. The ID code consists of 8-bit data, and its areas are $FFD4_{16}$ to $FFDA_{16}$. Write a program which has had the ID code preset at these addresses to the flash memory.

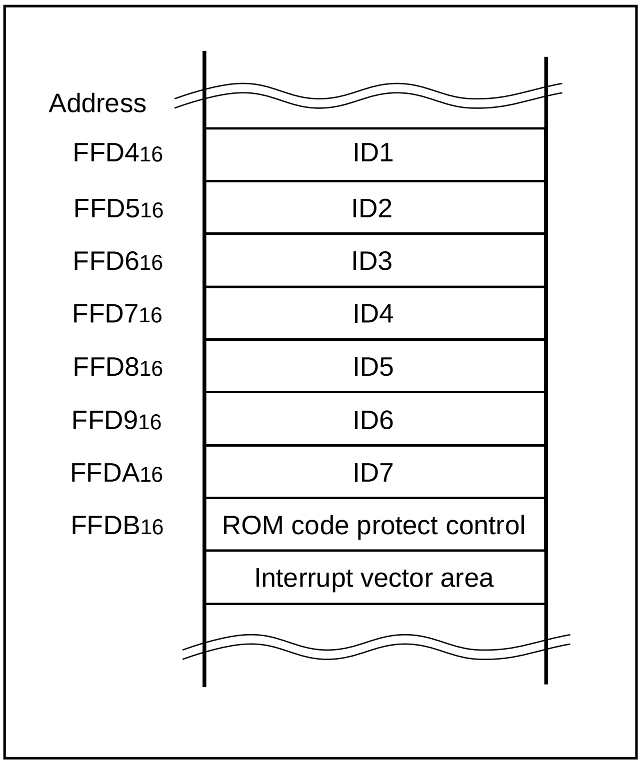


Fig. 68 ID code store addresses

(2) Parallel I/O Mode

The parallel I/O mode is used to input/output software commands, address and data in parallel for operation (read, program and erase) to internal flash memory.

Use the external device (writer) only for 38C2 Group group (A version)'s flash memory version. For details, refer to the user's manual of each writer manufacturer.

User ROM and Boot ROM Areas

In parallel I/O mode, the User ROM and Boot ROM areas shown in Figure 61 can be rewritten. Both areas of flash memory can be operated on in the same way.

Program and block erase operations can be performed only in the User ROM area.

The Boot ROM area is 4 Kbytes in size and located at addresses $F000_{16}$ through $FFFF_{16}$. Make sure program and block erase operations are always performed within this address range. (Access to any location outside this address range is prohibited.)

In the Boot ROM area, an erase block operation is applied to only one 4 Kbyte block. The boot ROM area has had a standard serial I/O mode control program stored in it when shipped from our factory. Therefore, using the MCU in standard serial I/O mode, do not rewrite to the Boot ROM area.

(3) Standard serial I/O Mode

The standard serial I/O mode inputs and outputs the software commands, addresses and data needed to operate (read, program, erase, etc.) the internal flash memory. This I/O is clock synchronized serial. This mode requires a purpose-specific peripheral unit.

The standard serial I/O mode is different from the parallel I/O mode in that the CPU controls flash memory rewrite (uses the CPU rewrite mode), rewrite data input and so forth. The standard serial I/O mode is started by connecting "H" to the $P4_1$ ($\overline{CE}$) pin and "H" to the CNV_{SS} pin (when V_{CC} = 4.5 to 5.5 V, connect to V_{CC}, and when V_{CC} = 3.0 to 4.5 V, apply 4.5 V to 5.5 V to Vpp from an external source), and releasing the reset operation. (In the ordinary microcomputer mode, set CNVss pin to "L" level.)

This control program is written in the Boot ROM area when the product is shipped from Renesas. Accordingly, make note of the fact that the standard serial I/O mode cannot be used if the Boot ROM area is rewritten in parallel I/O mode. Figure 69 shows the pin connections for the standard serial I/O mode.

In standard serial I/O mode, serial data I/O uses the four UART2 pins S_{CLK2}, RxD_2, TxD_2 and $\overline{S_{RDY2}}$ (BUSY). The S_{CLK2} pin is the transfer clock input pin through which an external transfer clock is input. The TxD_2 pin is for CMOS output. The $\overline{S_{RDY2}}$ (BUSY) pin outputs "L" level when ready for reception and "H" level when reception starts. Serial data I/O is transferred serially in 8-bit units.

In standard serial I/O mode, only the User ROM area shown in Figure 61 can be rewritten. The Boot ROM area cannot.

In standard serial I/O mode, a 7-byte ID code is used. When there is data in the flash memory, commands sent from the peripheral unit (programmer) are not accepted unless the ID code matches.

Outline Performance (Standard Serial I/O Mode)

In standard serial I/O mode, software commands, addresses and data are input and output between the MCU and peripheral units (serial programer, etc.) using 4-wire clock-synchronized serial I/O (UART2).

In reception, software commands, addresses and program data are synchronized with the rise of the transfer clock that is input to the S_{CLK2} pin, and are then input to the MCU via the RxD_2 pin. In transmission, the read data and status are synchronized with the fall of the transfer clock, and output from the TxD_2 pin.

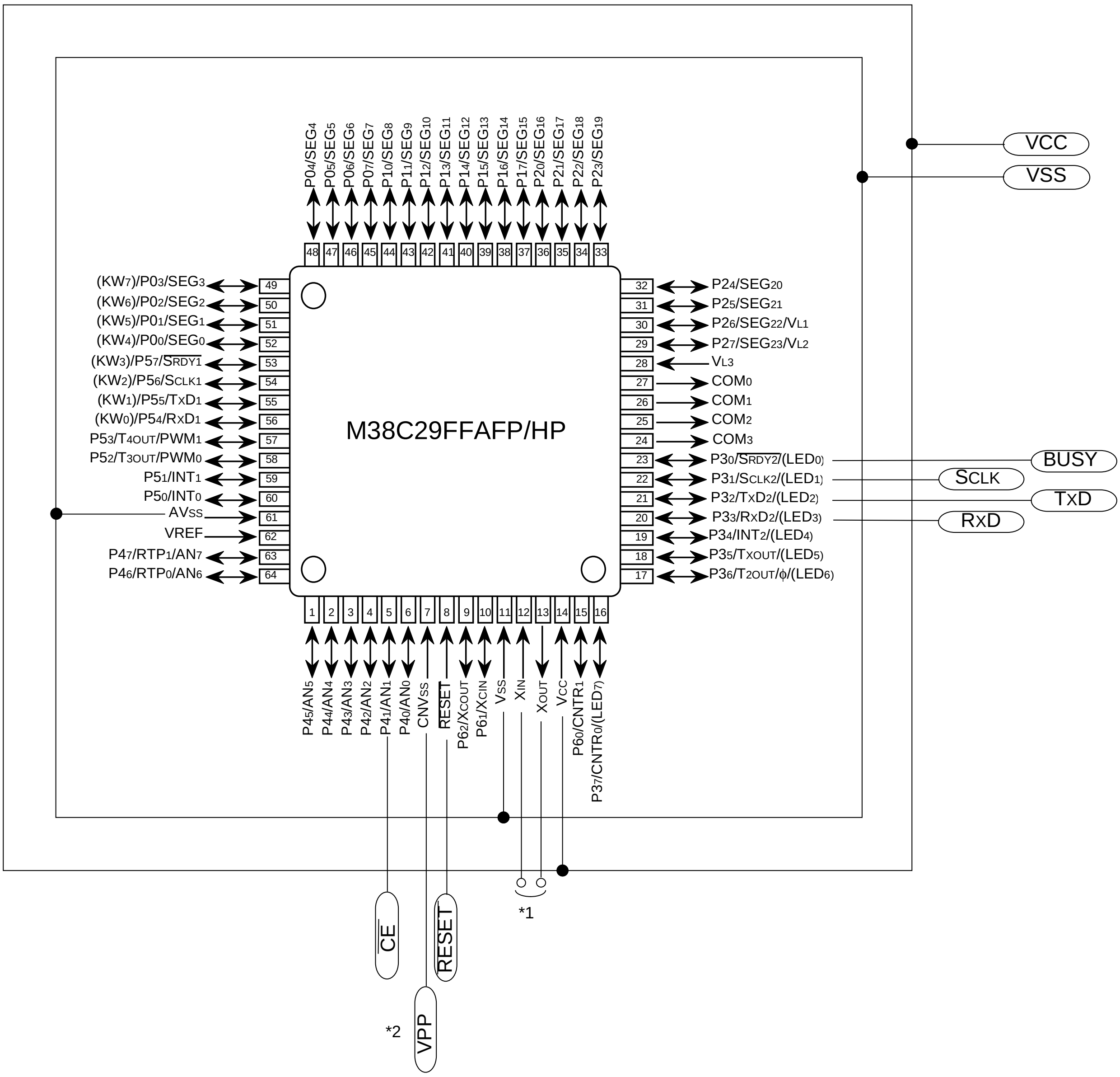
The TxD_2 pin is for CMOS output. Transfer is in 8-bit units with LSB first.

When busy, such as during transmission, reception, erasing or program execution, the $\overline{S_{RDY2}}$ (BUSY) pin is "H" level. Accordingly, always start the next transfer after the $\overline{S_{RDY2}}$ (BUSY) pin is "L" level.

Also, data and status registers in a memory can be read after inputting software commands. Status, such as the operating state of the flash memory or whether a program or erase operation ended successfully or not, can be checked by reading the status register. Here following explains software commands, status registers, etc.

Table 14 Description of pin function (Flash Memory Serial I/O Mode)

Pin name	Signal name	I/O	Function
V_{CC},V_{SS}	Power supply		Apply guaranteed voltage of program/erase to the Vcc pin and 0 V to the Vss pin.
CNV_{SS}	CNV_{SS}	I	Connect this pin to Vcc at Vcc = 4.5 to 5.5 V. Connect this pin to V_{PP} at Vcc = 3.0 to 4.5 V.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin. When X_{IN} oscillation is stable, input “L” level for 2 µs or more.
X_{IN}	Clock input	I	Connect a ceramic resonator or crystal oscillator between the X_{IN} and X_{OUT} pins. When entering an externally driven clock, enter it from X_{IN} and input the inverted signal of X_{IN} pin to X_{OUT} pin.
X_{OUT}	Clock output	O	
AV_{SS}	Analog power supply		Connect to Vss.
V_{REF}	Analog reference voltage	I	Apply reference voltage of A-D to this pin.
$P0_0$–$P0_7$	I/O port P0	I/O	Input “L” or “H” level, or keep open.
$P1_0$–$P1_7$	I/O port P1	I/O	Input “L” or “H” level, or keep open.
$P2_0$–$P2_7$	I/O port P2	I/O	Input “L” or “H” level, or keep open.
$P3_0$	BUSY output	O	BUSY signal output pin.
$P3_1$	SCLK input	I	Serial clock input pin.
$P3_2$	TXD output	O	Serial data output pin.
$P3_3$	RXD input	I	Serial data input pin.
$P3_4$–$P3_7$	I/O port P3	I/O	Input “L” or “H” level, or keep open.
$P4_0$	I/O port P4	I/O	Input “L” or “H” level, or keep open.
$P4_1$	$\overline{\text{CE}}$ input	I	Input “H” level.
$P4_2$–$P4_7$	I/O port P4	I/O	Input “L” or “H” level, or keep open.
$P5_0$–$P5_7$	I/O port P5	I/O	Input “L” or “H” level, or keep open.
$P6_0$	I/O port P6	I/O	Input “L” or “H” level, or keep open.
$P6_1$/X_{CIN}	I/O port P6/Sub clock input	I/O	When these pins are used for sub-clock, connect a quartz-crystal oscillator between the X_{CIN} and X_{COUT} pins. When entering an externally driven clock, enter it from X_{CIN} and leave X_{OUT} open. When these pins are used as port, input “L” or “H” level, or keep open.
$P6_2$/X_{COUT}	I/O port P6/Sub clock output	I/O	
COM_0–COM_3	Common output	O	When the LCD control circuit is not used, keep open.
VL_3	Power supply for LCD		Apply LCD power source to this pin. When the LCD drive control circuit is not used, connect this pin to Vcc.



Mode setup method

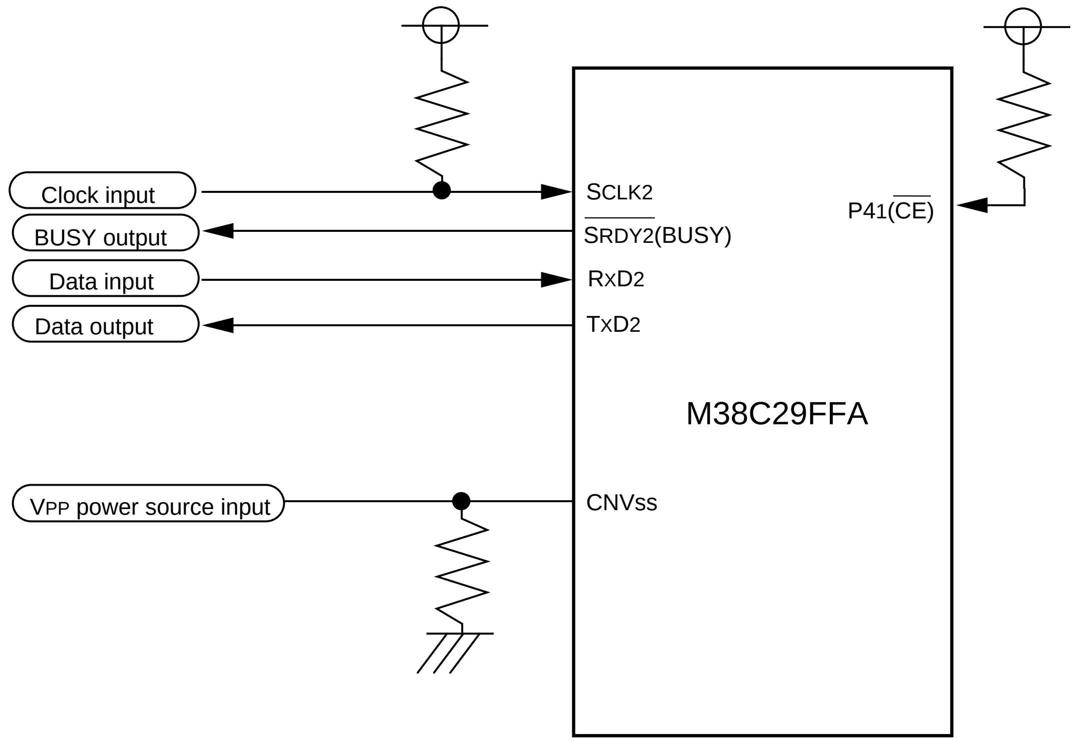
Signal	Value
CNVss	4.5 to 5.5 V
$\overline{\text{CE}}$	Vcc
$\overline{\text{RESET}}$	Vss→Vcc

*1.Connect to oscillation circuit.
*2.Connect to Vcc when Vcc=4.5 to 5.5V.
Connect to VPP (=4.5 to 5.5V) when Vcc=3.0 to 4.5V.

Fig. 69 Pin connection diagram in serial I/O mode

Example Circuit Application for Standard Serial I/O Mode

Figure 70 shows a circuit application for the standard serial I/O mode. Control pins will vary according to a programmer, therefore see a programmer manual for more information.



Notes 1: Control pins and external circuitry will vary according to a programmer. For more information, see the programmer manual.

2: In this example, the Vpp power supply is supplied from an external source (programmer). To use the user’s power source, connect to 4.5 V to 5.5 V.

Fig. 70 Example circuit application for standard serial I/O mode

ELECTRICAL CHARACTERISTICS (Flash memory version)

Absolute Maximum Ratings

Table 15 Absolute maximum ratings (Flash memory version)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage P00–P07, P10–P17, P20–P27, P30–P37, P40–P47, P50–P57, P60–P62		–0.3 to V_{CC}+0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to 6.5	V
V_I	Input voltage $\overline{\text{RESET}}$, X_{IN}		–0.3 to V_{CC}+0.3	V
V_I	Input voltage CNVSS		–0.3 to 6.5	V
V_O	Output voltage P00–P07, P10–P17, P20–P27	At output port	–0.3 to V_{CC}+0.3	V
		At segment output	–0.3 to V_{L3}+0.3	V
V_O	Output voltage COM0–COM3		–0.3 to V_{L3}+0.3	V
V_O	Output voltage P30–P37, P40–P47, P50–P57, P60–P62		–0.3 to V_{CC}+0.3	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC}+0.3	V
P_d	Power dissipation	Ta = 25°C	300	mW
T_{opr}	Operating temperature	At MCU operation	–20 to 85	°C
		At flash memory mode	25 ± 5	°C
T_{stg}	Storage temperature		–40 to 125	°C

Recommended Operating Conditions

Table 16 Recommended operating conditions (Flash memory version)

(Vcc = 2.5 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Power source voltage **(Note 1)**	f(φ) = 5 MHz	4.5	5.0	5.5 **(Note 3)**	V
		f(φ) = 4 MHz	4.0	5.0	5.5 **(Note 3)**	V
		f(φ) = 2 MHz	2.5	5.0	5.5 **(Note 3)**	V
		Low-speed mode	2.5	5.0	5.5 **(Note 3)**	V
		Oscillation start voltage **(Note 2)**	0.15 × f + 1.3			V
V_{SS}	Power source voltage			0		V
V_{L3}	Power source voltage for LCD		2.5		5.5	V
V_{REF}	A-D converter reference voltage		2.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage AN0–AN7		AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage	P04–P07, P10–P17, P20–P27, P30, P32, P35, P36, P40–P47, P52, P53, P62	0.7V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	P00–P03, P31, P33, P34, P37, P50, P51, P54–P57, P60, P61	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{\text{RESET}}$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	X_{CIN} **(Note 4)**	1.5		V_{CC}	V
V_{IL}	"L" input voltage	P04–P07, P10–P17, P20–P27, P30, P32, P35, P36, P40–P47, P52, P53, P62	0		0.3V_{CC}	V
V_{IL}	"L" input voltage	P00–P03, P31, P33, P34, P37, P50, P51, P54–P57, P60, P61, CNVSS	0		0.2V_{CC}	V
V_{IL}	"L" input voltage	$\overline{\text{RESET}}$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage	X_{IN}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage	X_{CIN} **(Note 5)**	0		0.4	V

Notes 1: When using the A-D converter, refer to "A-D Converter Characteristics".

2: The oscillation start voltage and the oscillation start time differ in accordance with an oscillator, a circuit constant, or temperature, etc. When power supply voltage is low and the high frequency oscillator is used, an oscillation start will require sufficient conditions.
f: This is the X_{IN} oscillator's oscillation frequency (≥ 1 MHz). For example, when oscillation frequency is 8 MHz, substitute "8".

3: It is the rating value when V_{CC} = 5.0 to 5.5 V at program/erase. The value is (V_{CC} at program/erase) + 0.5 V when V_{CC} = 3.0 to 5.0 V at program/erase.

4: When the X_{CIN}/P61 pin is not connected to an oscillator, refer to V_{IH} for P61.

5: When the X_{CIN}/P61 pin is not connected to an oscillator, refer to V_{IL} for P61.

Table 17 Recommended operating conditions (Flash memory version)
(Vcc = 2.5 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current **(Note 1)** P00–P07, P10–P17, P20–P27, P30–P37			–20	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current **(Note 1)** P40–P47, P50–P57, P60–P62			–20	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** P00–P07, P10–P17, P20–P27			20	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** P40–P47, P50, P51, P54–P57, P60–P62			20	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** P30–P37, P52, P53			110	mA
$\Sigma I_{OH(avg)}$	"H" total average output current **(Note 1)** P00–P07, P10–P17, P20–P27, P30–P37			–10	mA
$\Sigma I_{OH(avg)}$	"H" total average output current **(Note 1)** P40–P47, P50–P57, P60–P62			–10	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note 1)** P00–P07, P10–P17, P20–P27			10	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note 1)** P40–P47, P50, P51, P54–P57, P60–P62			10	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note 1)** P30–P37, P52, P53			90	mA
$I_{OH(peak)}$	"H" peak output current **(Note 2)** P00–P07, P10–P17, P20–P27			–1.0	mA
$I_{OH(peak)}$	"H" peak output current **(Note 2)** P30–P37, P40–P47, P50–P57, P60–P62			–5.0	mA
$I_{OL(peak)}$	"L" peak output current **(Note 2)** P00–P07, P10–P17, P20–P27			10	mA
$I_{OL(peak)}$	"L" peak output current **(Note 2)** P40–P47, P50, P51, P54–P57, P60–P62			10	mA
$I_{OL(peak)}$	"L" peak output current **(Note 2)** P30–P37, P52, P53			30	mA
$I_{OH(avg)}$	"H" average output current **(Note 3)** P00–P07, P10–P17, P20–P27			–0.5	mA
$I_{OH(avg)}$	"H" average output current **(Note 3)** P30–P37, P40–P47, P50–P57, P60–P62			–2.5	mA
$I_{OL(avg)}$	"L" average output current **(Note 3)** P00–P07, P10–P17, P20–P27			5.0	mA
$I_{OL(avg)}$	"L" average output current **(Note 3)** P40–P47, P50, P51, P54–P57, P60–P62			5.0	mA
$I_{OL(avg)}$	"L" average output current **(Note 3)** P30–P37, P52, P53			15	mA

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current is average value measured over 100 ms.

Table 18 Recommended operating conditions (Flash memory version)

(Vcc = 2.5 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
f(CNTR0) f(CNTR1)	Timer X and Timer Y Input frequency (duty cycle 50%)	(4.5 V ≤ VCC ≤ 5.5 V)			5.0	MHz
		(4.0 V ≤ VCC < 4.5 V)			2 × VCC–4	MHz
		(VCC < 4.0 V)			VCC	MHz
f(Tclk)	Timer X, Timer Y, Timer 1, Timer 2, Timer 3 and Timer 4 Clock input frequency (Count source frequency of each timer)	(4.5 V ≤ VCC ≤ 5.5 V)			10.0	MHz
		(4.0 V ≤ VCC < 4.5 V)			4 × VCC–8	MHz
		(VCC < 4.0 V)			2 × VCC	MHz
f(ϕ)	System clock ϕ frequency	(4.5 V ≤ VCC ≤ 5.5 V)			5.0	MHz
		(4.0 V ≤ VCC < 4.5 V)			2 × VCC–4	MHz
		(VCC < 4.0 V)			VCC	MHz
f(XIN)	Main clock input oscillation frequency **(Notes 1, 3)**	(4.5 V ≤ VCC ≤ 5.5 V)	1.0		10.0	MHz
		(2.5 V ≤ VCC < 4.5 V)	1.0		8.0	MHz
f(XCIN)	Sub-clock input oscillation frequency **(Notes 1, 2, 3)**			32.768	50	kHz

Notes 1: When the oscillation frequency has a duty cycle of 50%.

2: When using the microcomputer in low-speed mode, set the clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

3: The oscillation start voltage and the oscillation start time differ in accordance with an oscillator, a circuit constant, or temperature, etc. When power supply voltage is low and the high frequency oscillator is used, an oscillation start will require sufficient conditions.

Electrical Characteristics

Table 19 Electrical characteristics (Flash memory version)

(V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$	I_{OH} = –1 mA	V_{CC}–2.0			V
		I_{OH} = –0.25 mA V_{CC} = 2.5 V	V_{CC}–0.8			V
V_{OH}	"H" output voltage $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$	I_{OH} = –5 mA	V_{CC}–2.0			V
		I_{OH} = –1.5 mA	V_{CC}–0.5			V
		I_{OH} = –1.25 mA V_{CC} = 2.5 V	V_{CC}–0.8			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$, $P5_1$, $P5_4$–$P5_7$, $P6_0$–$P6_2$	I_{OL} = 10 mA			2.0	V
		I_{OL} = 3 mA			0.5	V
		I_{OL} = 2.5 mA V_{CC} = 2.5 V			0.8	V
V_{OL}	"L" output voltage $P3_0$–$P3_7$, $P5_2$, $P5_3$	I_{OL} = 15 mA			2.0	V
		I_{OL} = 4 mA V_{CC} = 2.5 V			0.8	V
V_{T+}–V_{T-}	Hysteresis INT_0–INT_2, $CNTR_0$, $CNTR_1$, $P0_0$–$P0_3$, $P5_4$–$P5_7$			0.5		V
V_{T+}–V_{T-}	Hysteresis S_{CLK1}, S_{CLK2}, RxD_1, RxD_2			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$	V_I = V_{SS} Pull-up "OFF"			–5.0	µA
		V_{CC} = 5.0 V, V_I = V_{SS} Pull-up "ON"	–60	–120	–240	µA
		V_{CC} = 3.0 V, V_I = V_{SS} Pull-up "ON"	–25	–40	–100	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA

Table 20 Electrical characteristics (Flash memory version)
(Vcc = 2.5 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
VRAM	RAM hold voltage	When clock is stopped		1.8		5.5	V
ICC	Power source current	Frequency/2 mode, Vcc = 5 V f(XIN) = 10 MHz f(XCIN) = 32.768 kHz Output transistors “OFF”, A-D converter in operating			6.0	8.6	mA
		Frequency/2 mode, Vcc = 5 V f(XIN) = 8 MHz f(XCIN) = 32.768 kHz Output transistors “OFF”, A-D converter in operating			5.0	7.2	mA
		Frequency/2 mode, Vcc = 5 V f(XIN) = 8 MHz (in WIT state) f(XCIN) = 32.768 kHz Output transistors “OFF”, A-D converter stopped			1.0	2.0	mA
		Low-speed mode, VCC = 5 V, Ta ≤ 55 °C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors “OFF”			150	200	µA
		Low-speed mode, VCC = 5 V, Ta = 25 °C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors “OFF”			6	10	µA
		Low-speed mode, VCC = 3 V, Ta ≤ 55 °C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors “OFF”			125	165	µA
		Low-speed mode, VCC = 3 V, Ta = 25 °C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors “OFF”			4	8	µA
		All oscillation stopped (in STP state) Output transistors “OFF”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

Table 21 Direct-electrical characteristics (Flash memory version)
(Vcc = 4.5 to 5.5 V, Ta = 25 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
IPP1	VPP Power source current (at read)	VPP = VCC, at flash memory mode			100	µA
IPP2	VPP Power source current (at programming)				60	mA
IPP3	VPP Power source current (at erase)				30	mA
VPP	VPP Power source voltage	At flash memory mode	4.5		5.5	V

A-D Converter Characteristics

Table 22 A-D converter characteristics (Flash memory version)

(Vcc = 2.5 to 5.5 V, Vss = AVss = 0 V, Ta = –20 to 85 °C, Port state = stopped, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy (quantification error excluded)	VCC = VREF = 5 V AD clock frequency = 5 MHz 10bitAD mode			±6	LSB
		VCC = VREF = 4 V AD clock frequency = 4 MHz 10bitAD mode				
		VCC = VREF = 2.5 V AD clock frequency = 500 kHz 10bitAD mode, booster effective			±5	
		VCC = VREF = 5 V AD clock frequency = 4 MHz 8bitAD mode			±2	
		VCC = VREF = 2.5 V AD clock frequency = 1 MHz				
Tconv	Conversion time	8bitAD mode, booster effective AD conversion clock selection bit :XIN/2,			tc(XIN)×121 (Note)	µs
RLADDER	Ladder resistor	10bitAD mode	12	35	100	kΩ
IVREF	Reference input current		50	150	200	µA
IIA	Analog input current	VREF = 5 V			5.0	µA

Note: When “Frequency/4, 8 or 16” is selected by the AD conversion clock selection bit, the above conversion time is multiplied by 2, 4 or 8.

LCD Power Supply Characteristics

Table 23 LCD power supply characteristics (when connecting division resistors for LCD power supply) (Flash memory version)

(Vcc = 2.5 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
RLCD	Division resistor for LCD power supply (Note)	RSEL = “10”				200		kΩ
		RSEL = “11”				5		
		LCD drive timing A	LCD circuit division ratio = divided by 1	RSEL = “01”		120		
				RSEL = “00”		90		
			LCD circuit division ratio = divided by 2	RSEL = “01”		150		
				RSEL = “00”		120		
			LCD circuit division ratio = divided by 4	RSEL = “01”		170		
				RSEL = “00”		150		
			LCD circuit division ratio = divided by 8	RSEL = “01”		190		
				RSEL = “00”		170		
		LCD drive timing B	LCD circuit division ratio = divided by 1	RSEL = “01”		150		
				RSEL = “00”		120		
			LCD circuit division ratio = divided by 2	RSEL = “01”		170		
				RSEL = “00”		150		
			LCD circuit division ratio = divided by 4	RSEL = “01”		190		
				RSEL = “00”		170		
			LCD circuit division ratio = divided by 8	RSEL = “01”		190		
				RSEL = “00”		190		

Note: The value is the average of each one division resistor.

Timing Requirements And Switching Characteristics

Table 24 Timing requirements 1 (Flash memory version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{w}(\overline{RESET})$	Reset input "L" pulse width		2			µs
$t_{c}(X_{IN})$	Main clock input cycle time (X_{IN} input)	(4.5 V ≤ V_{CC} ≤ 5.5 V)	100		1000	ns
		(4.0 V ≤ V_{CC} < 4.5 V)	1000(4 × V_{CC} - 8)		1000	ns
$t_{WH}(X_{IN})$	Main clock input "H" pulse width	(4.5 V ≤ V_{CC} ≤ 5.5 V)	40		500	ns
		(4.0 V ≤ V_{CC} < 4.5 V)	45		500	ns
$t_{WL}(X_{IN})$	Main clock input "L" pulse width	(4.5 V ≤ V_{CC} ≤ 5.5 V)	40		500	ns
		(4.0 V ≤ V_{CC} < 4.5 V)	45		500	ns
$t_{c}(X_{CIN})$	Sub clock input cycle time		20			µs
$t_{WH}(X_{CIN})$	Sub clock input "H" pulse width		9			µs
$t_{WL}(X_{CIN})$	Sub clock input "L" pulse width		9			µs
$t_{c}(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	(4.5 V ≤ V_{CC} ≤ 5.5 V)	200			ns
		(4.0 V ≤ V_{CC} < 4.5 V)	1000(2 × V_{CC} - 4)			ns
$t_{WH}(CNTR)$	$CNTR_0$, $CNTR_1$ input "H" pulse width	(4.5 V ≤ V_{CC} ≤ 5.5 V)	85			ns
		(4.0 V ≤ V_{CC} < 4.5 V)	105			ns
$t_{WL}(CNTR)$	$CNTR_0$, $CNTR_1$ input "L" pulse width	(4.5 V ≤ V_{CC} ≤ 5.5 V)	85			ns
		(4.0 V ≤ V_{CC} < 4.5 V)	105			ns
$t_{WH}(INT)$	INT_0–INT_2 input "H" pulse width		80			ns
$t_{WL}(INT)$	INT_0–INT_2 input "L" pulse width		80			ns
$t_{c}(S_{CLK})$	Serial I/O1, 2 clock input cycle time (Note)		800			ns
$t_{WH}(S_{CLK})$	Serial I/O1, 2 clock input "H" pulse width (Note)		370			ns
$t_{WL}(S_{CLK})$	Serial I/O1, 2 clock input "L" pulse width (Note)		370			ns
$t_{su}(RxD\text{-}S_{CLK})$	Serial I/O1, 2 input setup time		220			ns
$t_{h}(S_{CLK}\text{-}RxD)$	Serial I/O1, 2 input hold time		100			ns

Note : When bit 6 of address $0FE0_{16}$ or $0FE3_{16}$ is "1" (clock synchronous).
Divide this value by four when bit 6 of address $0FE0_{16}$ or $0FE3_{16}$ is "0" (UART).

Table 25 Timing requirements 2 (Flash memory version)

(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w}(\overline{RESET})$	Reset input "L" pulse width	2			µs
$t_{c}(X_{IN})$	Main clock input cycle time (X_{IN} input)	125		1000	ns
$t_{WH}(X_{IN})$	Main clock input "H" pulse width	50		500	ns
$t_{WL}(X_{IN})$	Main clock input "L" pulse width	50		500	ns
$t_{c}(X_{CIN})$	Sub clock input cycle time	20			µs
$t_{WH}(X_{CIN})$	Sub clock input "H" pulse width	9			µs
$t_{WL}(X_{CIN})$	Sub clock input "L" pulse width	9			µs
$t_{c}(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	750/(V_{CC}–1)			ns
$t_{WH}(CNTR)$	$CNTR_0$, $CNTR_1$ input "H" pulse width	t_{c}(CNTR)/2–20			ns
$t_{WL}(CNTR)$	$CNTR_0$, $CNTR_1$ input "L" pulse width	t_{c}(CNTR)/2–20			ns
$t_{WH}(INT)$	INT_0–INT_2 input "H" pulse width	230			ns
$t_{WL}(INT)$	INT_0–INT_2 input "L" pulse width	230			ns
$t_{c}(S_{CLK})$	Serial I/O1, 2 clock input cycle time (Note)	2000			ns
$t_{WH}(S_{CLK})$	Serial I/O1, 2 clock input "H" pulse width (Note)	950			ns
$t_{WL}(S_{CLK})$	Serial I/O1, 2 clock input "L" pulse width (Note)	950			ns
$t_{su}(RxD\text{-}S_{CLK})$	Serial I/O1, 2 input setup time	400			ns
$t_{h}(S_{CLK}\text{-}RxD)$	Serial I/O1, 2 input hold time	200			ns

Note : When bit 6 of address $0FE0_{16}$ or $0FE3_{16}$ is "1" (clock synchronous).
Divide this value by four when bit 6 of address $0FE0_{16}$ or $0FE3_{16}$ is "0" (UART).

Table 26 Switching characteristics 1 (Flash memory version)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Typ.	Max.	Unit
t_{WH}(SCLK)	Serial I/O1, 2 clock output "H" pulse width		t_C(SCLK)/2–30			ns
t_{WL}(SCLK)	Serial I/O1, 2 clock output "L" pulse width		t_C(SCLK)/2–30			ns
t_d(SCLK-TxD)	Serial I/O1, 2 output delay time **(Note 1)**				140	ns
t_v(SCLK-TxD)	Serial I/O1, 2 output valid time **(Note 1)**		–30			ns
t_r(SCLK)	Serial I/O1, 2 clock output rising time				30	ns
t_f(SCLK)	Serial I/O1, 2 clock output falling time				30	ns
t_r(CMOS)	CMOS output rising time	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (**Note 2**)		25	40	ns
		$P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$ (**Note 2**)		15	30	ns
t_f(CMOS)	CMOS output falling time	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (**Note 2**) $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$ (**Note 2**)		15	30	ns

Notes 1: When the P-channel output disable bit (bit 4 of address $0FE1_{16}$ or $0FE4_{16}$) is "0."
2: The XOUT, XCOUT pins are excluded.

Table 27 Switching characteristics 2 (Flash memory version)
(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Typ.	Max.	Unit
t_{WH}(SCLK)	Serial I/O1, 2 clock output "H" pulse width		t_C(SCLK)/2–80			ns
t_{WL}(SCLK)	Serial I/O1, 2 clock output "L" pulse width		t_C(SCLK)/2–80			ns
t_d(SCLK-TxD)	Serial I/O1, 2 output delay time **(Note 1)**				400	ns
t_v(SCLK-TxD)	Serial I/O1, 2 output valid time **(Note 1)**		–30			ns
t_r(SCLK)	Serial I/O1, 2 clock output rising time				80	ns
t_f(SCLK)	Serial I/O1, 2 clock output falling time				80	ns
t_r(CMOS)	CMOS output rising time	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (**Note 2**)		60	120	ns
		$P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$ (**Note 2**)		40	80	ns
t_f(CMOS)	CMOS output falling time	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (**Note 2**) $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$ (**Note 2**)		40	80	ns

Notes 1: When the P-channel output disable bit (bit 4 of address $0FE1_{16}$ or $0FE4_{16}$) is "0."
2: The XOUT, XCOUT pins are excluded.

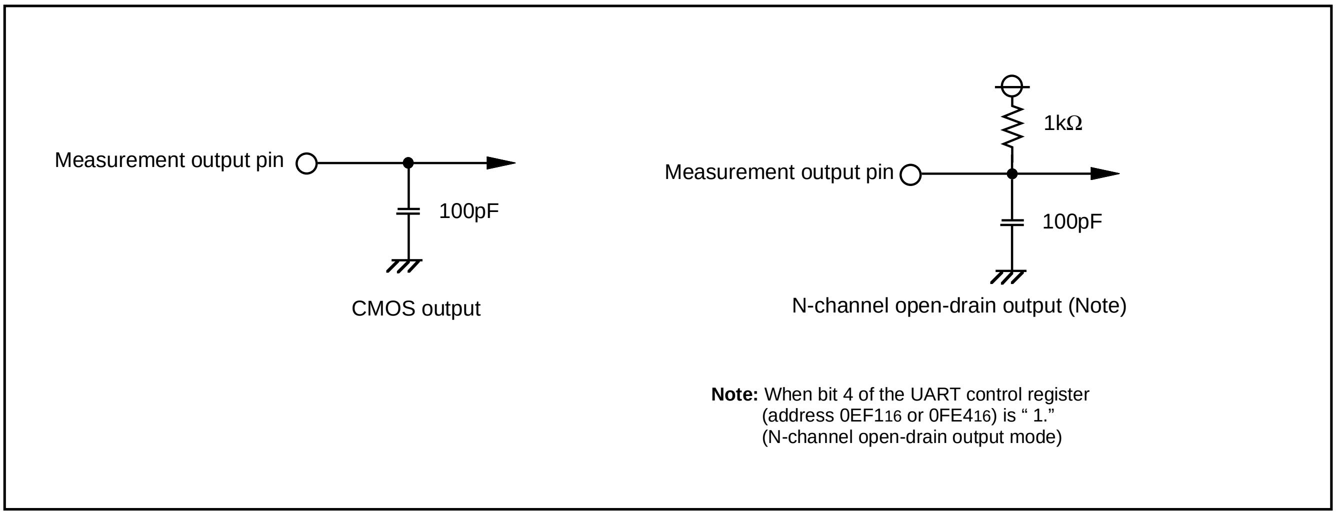


Fig. 71 Circuit for measuring output switching characteristics

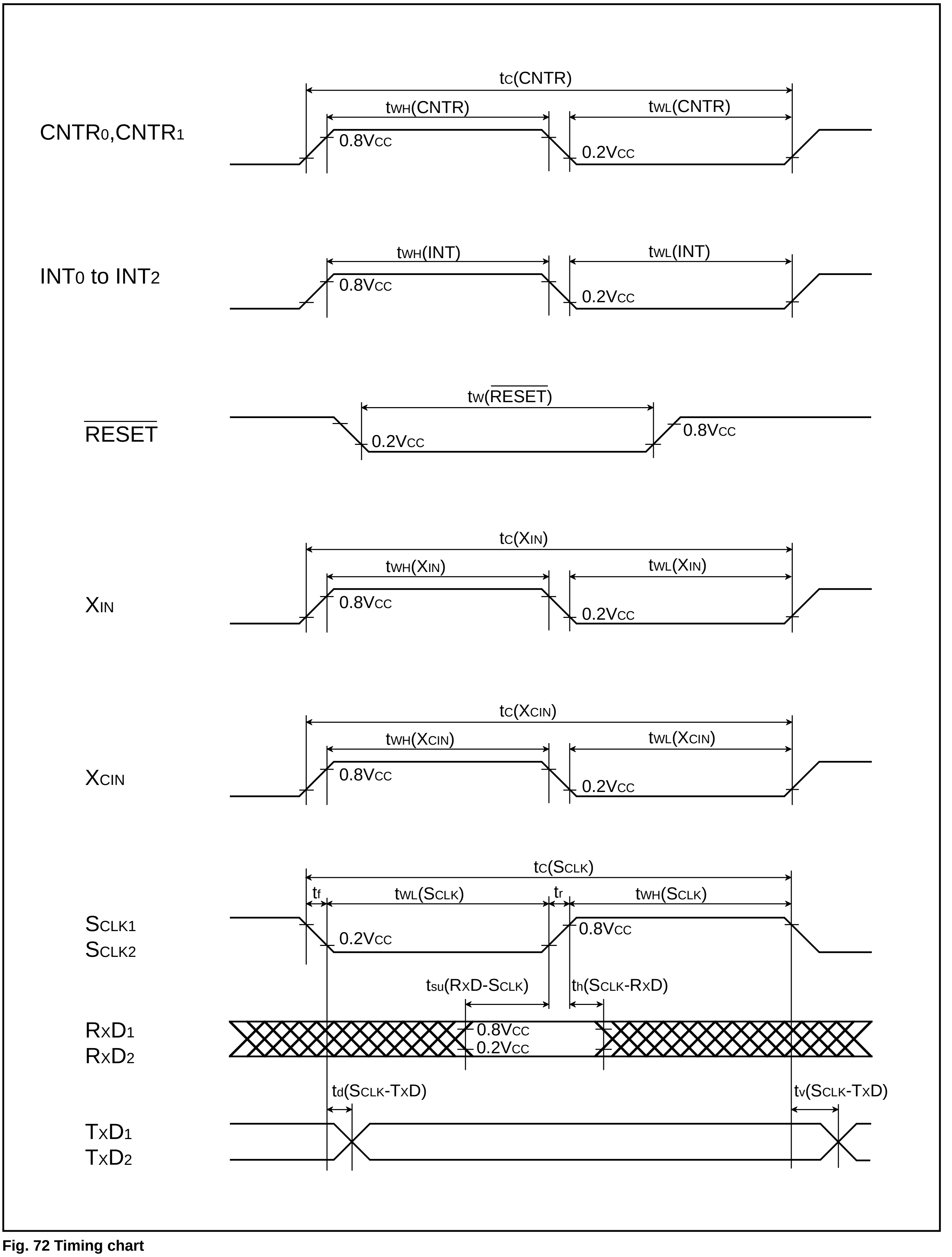


Fig. 72 Timing chart

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Table 28 Absolute maximum ratings (Mask ROM version)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$		–0.3 to V_{CC}+0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to 6.5	V
V_I	Input voltage $\overline{RESET}$, X_{IN}, CNV_{SS}		–0.3 to V_{CC}+0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$	At output port	–0.3 to V_{CC}+0.3	V
		At segment output	–0.3 to V_{L3}+0.3	V
V_O	Output voltage COM_0–COM_3		–0.3 to V_{L3}+0.3	V
V_O	Output voltage $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$		–0.3 to V_{CC}+0.3	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC}+0.3	V
P_d	Power dissipation	Ta = 25°C	300	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Recommended Operating Conditions

Table 29 Recommended operating conditions (Mask ROM version)
(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter			Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Power source voltage **(Note 1)**	f(ϕ) = 5 MHz		4.5	5.0	5.5	V
		f(ϕ) = 4 MHz		4.0	5.0	5.5	V
		f(ϕ) = 2 MHz		2.0	5.0	5.5	V
		f(ϕ) = 1 MHz		1.8	5.0	5.5	V
		Low-speed mode		1.8	5.0	5.5	V
		Oscillation start voltage **(Note 2)**		$0.15 \times f + 1.3$			V
V_{SS}	Power source voltage				0		V
V_{L3}	Power source voltage for LCD			2.5		5.5	V
V_{REF}	A-D converter reference voltage			2.0		V_{CC}	V
AV_{SS}	Analog power source voltage				0		V
V_{IA}	Analog input voltage AN0–AN7			AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage	P04–P07, P10–P17, P20–P27, P30, P32, P35, P36, P40–P47, P52, P53, P62		$0.7V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage	P00–P03, P31, P33, P34, P37, P50, P51, P54–P57, P60, P61		$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{\text{RESET}}$	2.2 V ≤ V_{CC} ≤ 5.5 V	$0.8V_{CC}$		V_{CC}	V
			V_{CC} ≤ 2.2 V	$V_{CC} - \frac{65 \times V_{CC} - 99}{100}$		V_{CC}	
V_{IH}	"H" input voltage	X_{IN}		$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage	X_{CIN} **(Note 3)**		1.5		V_{CC}	V
V_{IL}	"L" input voltage	P04–P07, P10–P17, P20–P27, P30, P32, P35, P36, P40–P47, P52, P53, P62		0		$0.3V_{CC}$	V
V_{IL}	"L" input voltage	P00–P03, P31, P33, P34, P37, P50, P51, P54–P57, P60, P61, CNV_{SS}		0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage	$\overline{\text{RESET}}$	2.2 V ≤ V_{CC} ≤ 5.5 V	0		$0.2V_{CC}$	V
			V_{CC} ≤ 2.2 V	0		$\frac{65 \times V_{CC} - 99}{100}$	
V_{IL}	"L" input voltage	X_{IN}		0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage	X_{CIN} **(Note 4)**		0		0.4	V

Notes 1: When using the A-D converter, refer to "A-D Converter Characteristics".
2: The oscillation start voltage and the oscillation start time differ in accordance with an oscillation start time differ accordance with an oscillator, a circuit constant, or temperature, etc. When power supply voltage is low and the high frequency oscillator is used, an oscillation start will require sufficient conditions.
f: This is an oscillator's oscillation frequency (≥ 1 MHz). For example, when oscillation frequency is 8 MHz, substitute "8".
3: When the X_{CIN}/P61 pin is not connected to an oscillator, refer to V_{IH} for P61.
4: When the X_{CIN}/P61 pin is not connected to an oscillator, refer to V_{IL} for P61.

Table 30 Recommended operating conditions (Mask ROM version)

(Vcc = 1.8 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–20	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current **(Note 1)** $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$			–20	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$			20	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** $P4_0$–$P4_7$, $P5_0$, $P5_1$, $P5_4$–$P5_7$, $P6_0$–$P6_2$			20	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** $P3_0$–$P3_7$, $P5_2$, $P5_3$			110	mA
$\Sigma I_{OH(avg)}$	"H" total average output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–10	mA
$\Sigma I_{OH(avg)}$	"H" total average output current **(Note 1)** $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$			–10	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$			10	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note 1)** $P4_0$–$P4_7$, $P5_0$, $P5_1$, $P5_4$–$P5_7$, $P6_0$–$P6_2$			10	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note 1)** $P3_0$–$P3_7$, $P5_2$, $P5_3$			90	mA
$I_{OH(peak)}$	"H" peak output current **(Note 2)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$			–1.0	mA
$I_{OH(peak)}$	"H" peak output current **(Note 2)** $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$			–5.0	mA
$I_{OL(peak)}$	"L" peak output current **(Note 2)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$			10	mA
$I_{OL(peak)}$	"L" peak output current **(Note 2)** $P4_0$–$P4_7$, $P5_0$, $P5_1$, $P5_4$–$P5_7$, $P6_0$–$P6_2$			10	mA
$I_{OL(peak)}$	"L" peak output current **(Note 2)** $P3_0$–$P3_7$, $P5_2$, $P5_3$			30	mA
$I_{OH(avg)}$	"H" average output current **(Note 3)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$			–0.5	mA
$I_{OH(avg)}$	"H" average output current **(Note 3)** $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$			–2.5	mA
$I_{OL(avg)}$	"L" average output current **(Note 3)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$			5.0	mA
$I_{OL(avg)}$	"L" average output current **(Note 3)** $P4_0$–$P4_7$, $P5_0$, $P5_1$, $P5_4$–$P5_7$, $P6_0$–$P6_2$			5.0	mA
$I_{OL(avg)}$	"L" average output current **(Note 3)** $P3_0$–$P3_7$, $P5_2$, $P5_3$			15	mA

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is average value measured over 100 ms.

Table 31 Recommended operating conditions (Mask ROM version)

(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
f(CNTR0) f(CNTR1)	Timer X and Timer Y Input frequency (duty cycle 50%)	(4.5 V ≤ V_{CC} ≤ 5.5 V)			5.0	MHz
		(4.0 V ≤ V_{CC} < 4.5 V)			2×V_{CC}–4	MHz
		(2.0 V ≤ V_{CC} < 4.0 V)			V_{CC}	MHz
		(V_{CC} < 2.0 V)			5×V_{CC}–8	MHz
f(Tclk)	Timer X, Timer Y, Timer 1, Timer 2, Timer 3 and Timer 4 Clock input frequency (Count source frequency of each timer)	(4.5 V ≤ V_{CC} ≤ 5.5 V)			10.0	MHz
		(4.0 V ≤ V_{CC} < 4.5 V)			4×V_{CC}–8	MHz
		(2.0 V ≤ V_{CC} < 4.0 V)			2×V_{CC}	MHz
		(V_{CC} < 2.0 V)			10×V_{CC}–16	MHz
f(ϕ)	System clock ϕ frequency	(4.5 V ≤ V_{CC} ≤ 5.5 V)			5.0	MHz
		(4.0 V ≤ V_{CC} < 4.5 V)			2×V_{CC}–4	MHz
		(2.0 V ≤ V_{CC} < 4.0 V)			V_{CC}	MHz
		(V_{CC} < 2.0 V)			5×V_{CC}–8	MHz
f(X_{IN})	Main clock input oscillation frequency **(Notes 1, 3)**	(4.5 V ≤ V_{CC} ≤ 5.5 V)	1.0		10.0	MHz
		(2.0 V ≤ V_{CC} < 4.5 V)	1.0		8.0	MHz
		(V_{CC} < 2.0 V)	1.0		20×V_{CC}–32	MHz
f(X_{CIN})	Sub-clock input oscillation frequency **(Notes 1, 2, 3)**			32.768	50	kHz

Notes 1: When the oscillation frequency has a duty cycle of 50%.

2: When using the microcomputer in low-speed mode, set the clock input oscillation frequency on condition that f(X_{CIN}) < f(X_{IN})/3.

3: The oscillation start voltage and the oscillation start time differ in accordance with an oscillator, a circuit constant, or temperature, etc. When power supply voltage is low and the high frequency oscillator is used, an oscillation start will require sufficient conditions.

Electrical Characteristics

Table 32 Electrical characteristics (Mask ROM version)
(V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$	I_{OH} = –1 mA	V_{CC}–2.0			V
		I_{OH} = –0.25 mA V_{CC} = 1.8 V	V_{CC}–0.8			V
V_{OH}	"H" output voltage $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$	I_{OH} = –5 mA	V_{CC}–2.0			V
		I_{OH} = –1.5 mA	V_{CC}–0.5			V
		I_{OH} = –1.25 mA V_{CC} = 1.8 V	V_{CC}–0.8			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$, $P5_1$, $P5_4$–$P5_7$, $P6_0$–$P6_2$	I_{OL} = 10 mA			2.0	V
		I_{OL} = 3 mA			0.5	V
		I_{OL} = 2.5 mA V_{CC} = 1.8 V			0.8	V
V_{OL}	"L" output voltage $P3_0$–$P3_7$, $P5_2$, $P5_3$	I_{OL} = 15 mA			2.0	V
		I_{OL} = 4 mA V_{CC} = 1.8 V			0.8	V
V_{T+}–V_{T-}	Hysteresis INT_0–INT_2, $CNTR_0$, $CNTR_1$, $P0_0$–$P0_3$, $P5_4$–$P5_7$			0.5		V
V_{T+}–V_{T-}	Hysteresis S_{CLK1}, S_{CLK2}, RxD_1, RxD_2			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$	V_I = V_{SS} Pull-up "OFF"			–5.0	µA
		V_{CC} = 5.0 V, V_I = V_{SS} Pull-up "ON"	–60	–120	–240	µA
		V_{CC} = 1.8 V, V_I = V_{SS} Pull-up "ON"	–5.0	–20	–40	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA

Table 33 Electrical characteristics (Mask ROM version)

(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{RAM}	RAM hold voltage	When clock is stopped	1.8		5.5	V
I_{CC}	Power source current	Frequency/2 mode, V_{CC} = 5 V f(X_{IN}) = 10 MHz f(X_{CIN}) = 32.768 kHz Output transistors “OFF”, A-D converter in operating		3.4	5.1	mA
		Frequency/2 mode, V_{CC} = 5 V f(X_{IN}) = 8 MHz f(X_{CIN}) = 32.768 kHz Output transistors “OFF”, A-D converter in operating		2.7	4.2	mA
		Frequency/2 mode, V_{CC} = 5 V f(X_{IN}) = 8 MHz (in WIT state) f(X_{CIN}) = 32.768 kHz Output transistors “OFF”, A-D converter stopped		1.0	2.0	mA
		Low-speed mode, V_{CC} = 5 V, Ta ≤ 55 °C f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz Output transistors “OFF”		14	21	µA
		Low-speed mode, V_{CC} = 5 V, Ta = 25 °C f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz (in WIT state) Output transistors “OFF”		6	10	µA
		Low-speed mode, V_{CC} = 3 V, Ta ≤ 55 °C f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz Output transistors “OFF”		8	13	µA
		Low-speed mode, V_{CC} = 3 V, Ta = 25 °C f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz (in WIT state) Output transistors “OFF”		4	8	µA
		All oscillation stopped (in STP state) Output transistors “OFF”: Ta = 25 °C		0.1	1.0	µA
		All oscillation stopped (in STP state) Output transistors “OFF”: Ta = 85 °C			10	µA

A-D Converter Characteristics

Table 34 A-D converter characteristics (Mask ROM version)

(V_{CC} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85°C, Port state = stopped, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution				10	Bits
—	Absolute accuracy (quantification error excluded)	V_{CC} = V_{REF} = 5 V AD clock frequency = 5 MHz 10bitAD mode			±5	LSB
		V_{CC} = V_{REF} = 4 V AD clock frequency = 4 MHz 10bitAD mode				
		V_{CC} = V_{REF} = 2.2 V AD clock frequency = 500 kHz 10bitAD mode, booster effective			±4	
		V_{CC} = V_{REF} = 5 V AD clock frequency = 4 MHz 8bitAD mode			±2	
		V_{CC} = V_{REF} = 2.2 V AD clock frequency = 1 MHz 8bitAD mode, booster effective				
T_{conv}	Conversion time	AD conversion clock selection bit :X_{IN}/2, 10bitAD mode			$t_c(X_{IN}) \times 121$ (Note)	µs
R_{LADDER}	Ladder resistor		12	35	100	kΩ
I_{VREF}	Reference input current	V_{REF} = 5 V	50	150	200	µA
I_{IA}	Analog input current				5.0	µA

Note: When “Frequency/4, 8 or 16” is selected by the AD conversion clock selection bit, the above conversion time is multiplied by 2, 4 or 8.

LCD Power Supply Characteristics

Table 35 LCD power supply characteristics (when connecting division resistors for LCD power supply) (Mask ROM version)

(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits Min.	Limits Typ.	Limits Max.	Unit
R_{LCD}	Division resistor for LCD power supply (Note)	RSEL = “10”				200		kΩ
		RSEL = “11”				5		
		LCD drive timing A	LCD circuit division ratio = divided by 1	RSEL = “01”		120		
				RSEL = “00”		90		
			LCD circuit division ratio = divided by 2	RSEL = “01”		150		
				RSEL = “00”		120		
			LCD circuit division ratio = divided by 4	RSEL = “01”		170		
				RSEL = “00”		150		
			LCD circuit division ratio = divided by 8	RSEL = “01”		190		
				RSEL = “00”		170		
		LCD drive timing B	LCD circuit division ratio = divided by 1	RSEL = “01”		150		
				RSEL = “00”		120		
			LCD circuit division ratio = divided by 2	RSEL = “01”		170		
				RSEL = “00”		150		
			LCD circuit division ratio = divided by 4	RSEL = “01”		190		
				RSEL = “00”		170		
			LCD circuit division ratio = divided by 8	RSEL = “01”		190		
				RSEL = “00”		190		

Note: The value is the average of each one division resistor.

Timing Requirements And Switching Characteristics

Table 36 Timing requirements 1 (Mask ROM version)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{w}(\overline{RESET})$	Reset input "L" pulse width		2			µs
$t_{c}(X_{IN})$	Main clock input cycle time (X_{IN} input)	(4.5 V ≤ Vcc ≤ 5.5 V)	100		1000	ns
		(4.0 V ≤ Vcc < 4.5 V)	1000/(4 × Vcc – 8)		1000	ns
$t_{WH}(X_{IN})$	Main clock input "H" pulse width	(4.5 V ≤ Vcc ≤ 5.5 V)	40		500	ns
		(4.0 V ≤ Vcc < 4.5 V)	45		500	ns
$t_{WL}(X_{IN})$	Main clock input "L" pulse width	(4.5 V ≤ Vcc ≤ 5.5 V)	40		500	ns
		(4.0 V ≤ Vcc < 4.5 V)	45		500	ns
$t_{c}(X_{CIN})$	Sub clock input cycle time		20			µs
$t_{WH}(X_{CIN})$	Sub clock input "H" pulse width		9			µs
$t_{WL}(X_{CIN})$	Sub clock input "L" pulse width		9			µs
$t_{c}(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	(4.5 V ≤ Vcc ≤ 5.5 V)	200			ns
		(4.0 V ≤ Vcc < 4.5 V)	1000/(2 × Vcc – 4)			ns
$t_{WH}(CNTR)$	$CNTR_0$, $CNTR_1$ input "H" pulse width	(4.5 V ≤ Vcc ≤ 5.5 V)	85			ns
		(4.0 V ≤ Vcc < 4.5 V)	105			ns
$t_{WL}(CNTR)$	$CNTR_0$, $CNTR_1$ input "L" pulse width	(4.5 V ≤ Vcc ≤ 5.5 V)	85			ns
		(4.0 V ≤ Vcc < 4.5 V)	105			ns
$t_{WH}(INT)$	INT_0–INT_2 input "H" pulse width		80			ns
$t_{WL}(INT)$	INT_0–INT_2 input "L" pulse width		80			ns
$t_{c}(S_{CLK})$	Serial I/O1, 2 clock input cycle time (Note)		800			ns
$t_{WH}(S_{CLK})$	Serial I/O1, 2 clock input "H" pulse width (Note)		370			ns
$t_{WL}(S_{CLK})$	Serial I/O1, 2 clock input "L" pulse width (Note)		370			ns
$t_{su}(RxD\text{-}S_{CLK})$	Serial I/O1, 2 input setup time		220			ns
$t_{h}(S_{CLK}\text{-}RxD)$	Serial I/O1, 2 input hold time		100			ns

Note : When bit 6 of address $0FE0_{16}$ or $0FE3_{16}$ is "1" (clock synchronous).
Divide this value by four when bit 6 of address $0FE0_{16}$ or $0FE3_{16}$ is "0" (UART).

Table 37 Timing requirements 2 (Mask ROM version)

(V_{CC} = 1.8 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_w(\overline{RESET})$	Reset input "L" pulse width		2			µs
$t_c(X_{IN})$	Main clock input cycle time (X_{IN} input)	2.0 V ≤ V_{CC} ≤ 4.0 V	125		1000	ns
		V_{CC} < 2.0 V	250/(5×V_{CC}–8)		1000	ns
$t_{WH}(X_{IN})$	Main clock input "H" pulse width	2.0 V ≤ V_{CC} ≤ 4.0 V	50		500	ns
		V_{CC} < 2.0 V	$t_c(X_{IN})$/2–12.5		500	ns
$t_{WL}(X_{IN})$	Main clock input "L" pulse width	2.0 V ≤ V_{CC} ≤ 4.0 V	50		500	ns
		V_{CC} < 2.0 V	$t_c(X_{IN})$/2–12.5		500	ns
$t_c(X_{CIN})$	Sub clock input cycle time		20			µs
$t_{WH}(X_{CIN})$	Sub clock input "H" pulse width		9			µs
$t_{WL}(X_{CIN})$	Sub clock input "L" pulse width		9			µs
$t_c(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	2.0 V ≤ V_{CC} ≤ 4.0 V	1000/V_{CC}			ns
		V_{CC} < 2.0 V	1000/(5×V_{CC}–8)			ns
$t_{WH}(CNTR)$	$CNTR_0$, $CNTR_1$ input "H" pulse width		$t_c(CNTR)$/2–20			ns
$t_{WL}(CNTR)$	$CNTR_0$, $CNTR_1$ input "L" pulse width		$t_c(CNTR)$/2–20			ns
$t_{WH}(INT)$	INT_0–INT_2 input "H" pulse width		230			ns
$t_{WL}(INT)$	INT_0–INT_2 input "L" pulse width		230			ns
$t_c(S_{CLK})$	Serial I/O1, 2 clock input cycle time (Note)		2000			ns
$t_{WH}(S_{CLK})$	Serial I/O1, 2 clock input "H" pulse width (Note)		950			ns
$t_{WL}(S_{CLK})$	Serial I/O1, 2 clock input "L" pulse width (Note)		950			ns
$t_{su}(RxD\text{-}S_{CLK})$	Serial I/O1, 2 input setup time		400			ns
$t_h(S_{CLK}\text{-}RxD)$	Serial I/O1, 2 input hold time		200			ns

Note : When bit 6 of address $0FE0_{16}$ or $0FE3_{16}$ is "1" (clock synchronous).
Divide this value by four when bit 6 of address $0FE0_{16}$ or $0FE3_{16}$ is "0" (UART).

Table 38 Switching characteristics 1 (Mask ROM version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
t_{WH}(SCLK)	Serial I/O1, 2 clock output “H” pulse width		t_C(SCLK)/2–30			ns
t_{WL}(SCLK)	Serial I/O1, 2 clock output “L” pulse width		t_C(SCLK)/2–30			ns
t_d(SCLK-TxD)	Serial I/O1, 2 output delay time **(Note 1)**				140	ns
t_v(SCLK-TxD)	Serial I/O1, 2 output valid time **(Note 1)**		–30			ns
t_r(SCLK)	Serial I/O1, 2 clock output rising time				30	ns
t_f(SCLK)	Serial I/O1, 2 clock output falling time				30	ns
t_r(CMOS)	CMOS output rising time	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (**Note 2**)		25	40	ns
		$P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$ (**Note 2**)		15	30	ns
t_f(CMOS)	CMOS output falling time	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (**Note 2**) $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$ (**Note 2**)		15	30	ns

Notes 1: When the P-channel output disable bit (bit 4 of address $0FE1_{16}$ or $0FE4_{16}$) is “0.”
2: The XOUT, XCOUT pins are excluded.

Table 39 Switching characteristics 2 (Mask ROM version)

(V_{CC} = 1.8 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
t_{WH}(SCLK)	Serial I/O1, 2 clock output “H” pulse width		t_C(SCLK)/2–80			ns
t_{WL}(SCLK)	Serial I/O1, 2 clock output “L” pulse width		t_C(SCLK)/2–80			ns
t_d(SCLK-TxD)	Serial I/O1, 2 output delay time **(Note 1)**				400	ns
t_v(SCLK-TxD)	Serial I/O1, 2 output valid time **(Note 1)**		–30			ns
t_r(SCLK)	Serial I/O1, 2 clock output rising time				80	ns
t_f(SCLK)	Serial I/O1, 2 clock output falling time				80	ns
t_r(CMOS)	CMOS output rising time	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (**Note 2**)		60	120	ns
		$P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$ (**Note 2**)		40	80	ns
t_f(CMOS)	CMOS output falling time	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (**Note 2**) $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$ (**Note 2**)		40	80	ns

Notes 1: When the P-channel output disable bit (bit 4 of address $0FE1_{16}$ or $0FE4_{16}$) is “0.”
2: The XOUT, XCOUT pins are excluded.

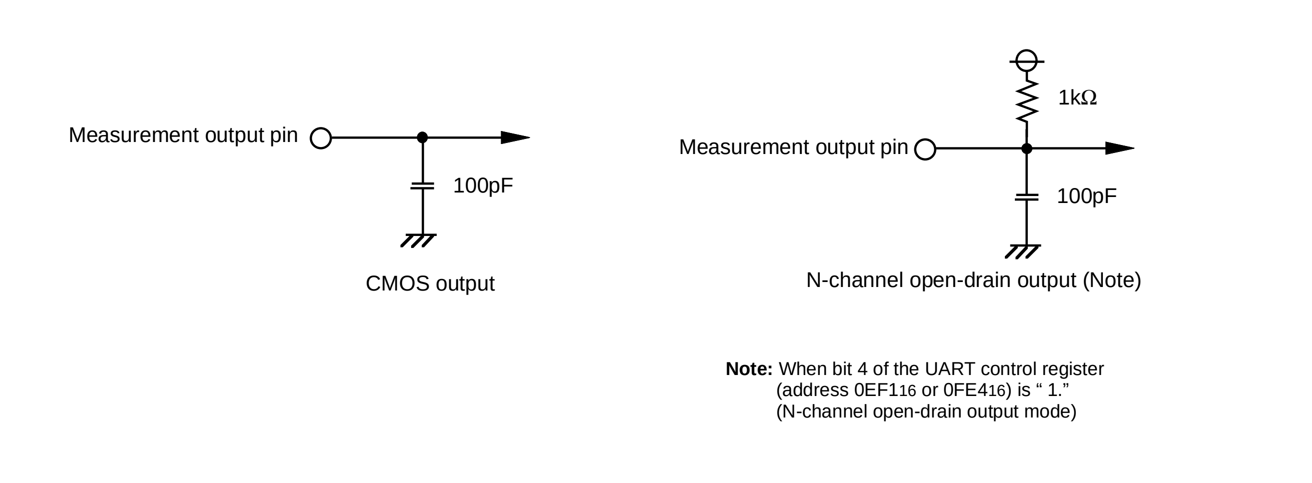


Fig. 73 Circuit for measuring output switching characteristics

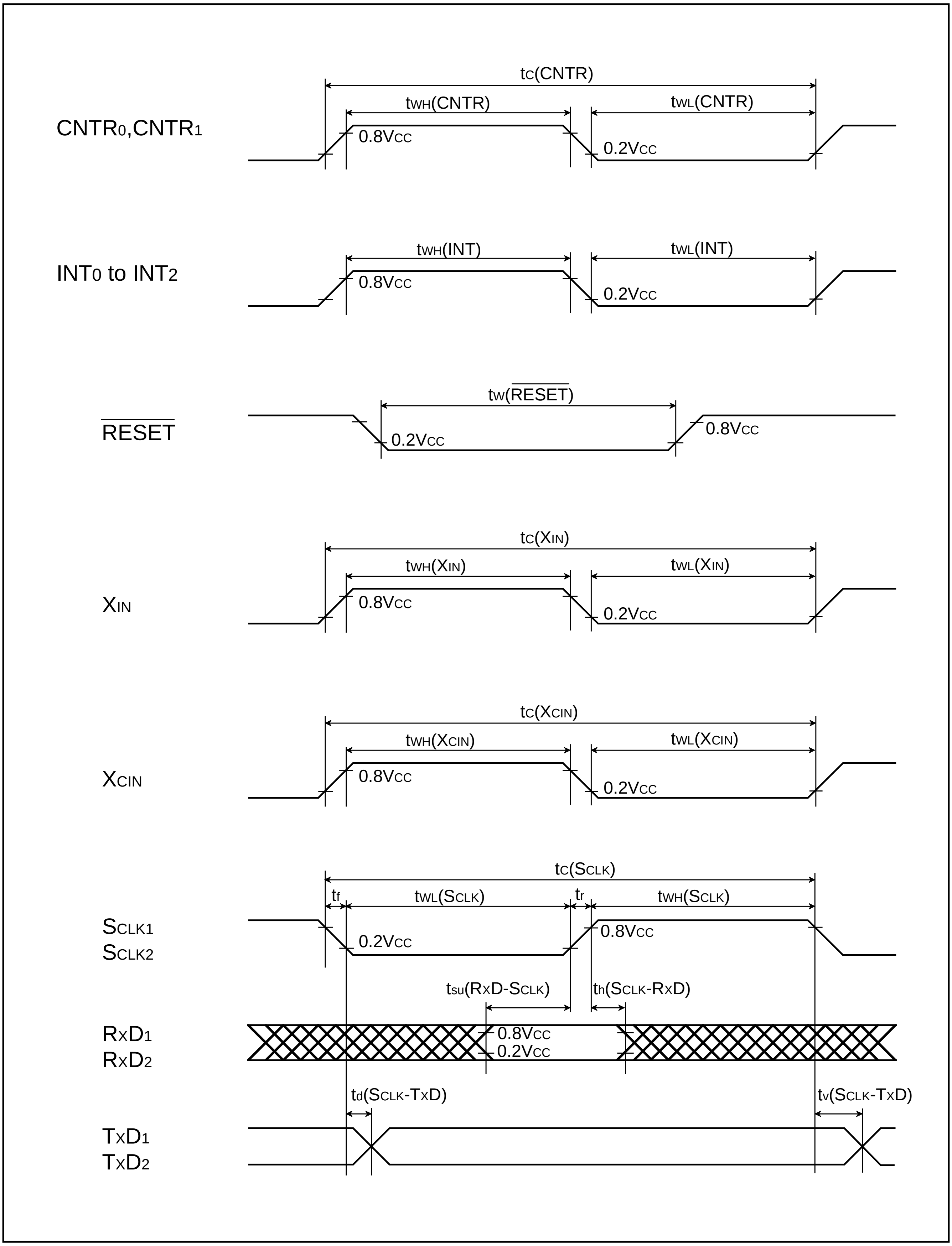


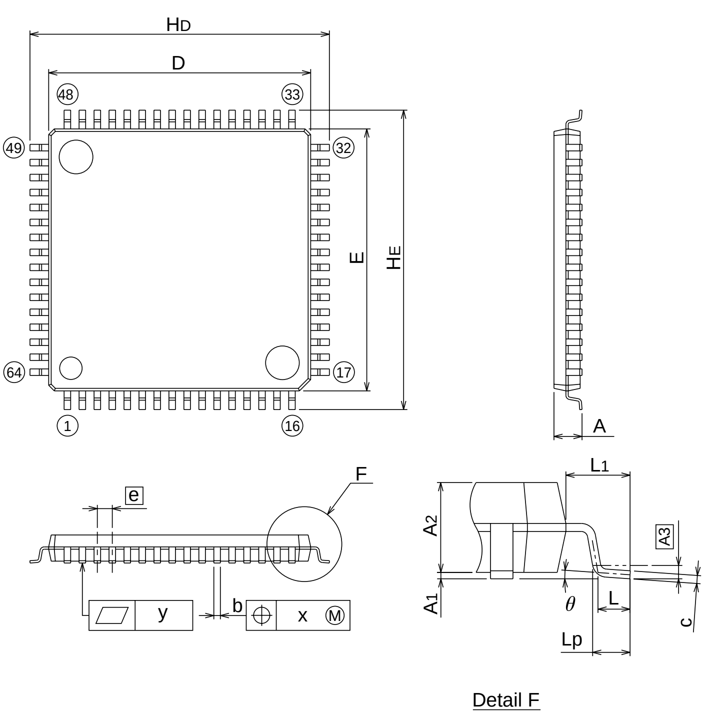
Fig. 74 Timing chart

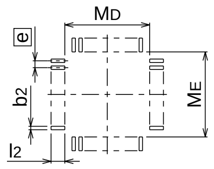
PACKAGE OUTLINE

64P6U-A

Plastic 64pin 14X14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1414-0.8	—		Cu Alloy





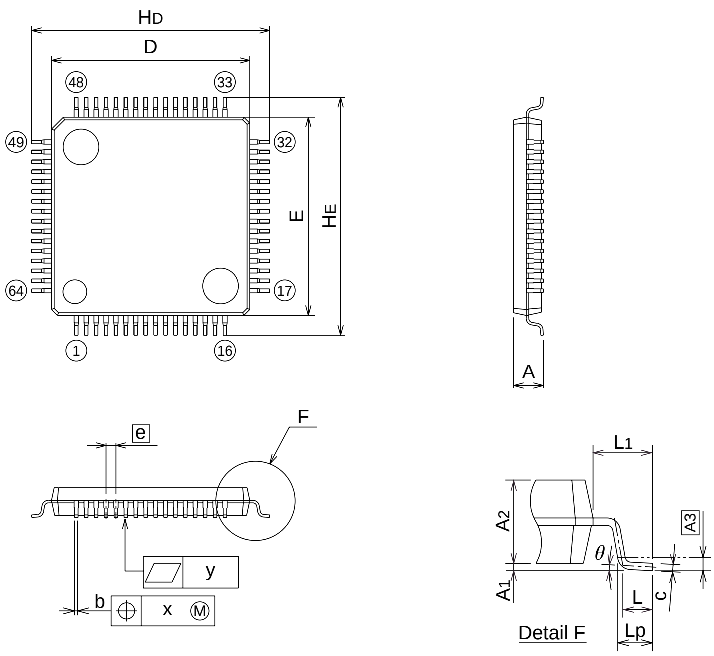
Recommended Mount Pad

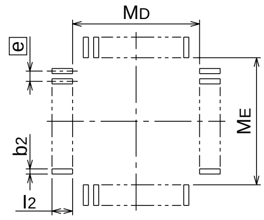
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A_1	0	0.1	0.2
A_2	—	1.4	—
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
$\boxed{e}$	—	0.8	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
L	0.3	0.5	0.7
L_1	—	1.0	—
Lp	0.45	0.6	0.75
$\boxed{A3}$	—	0.25	—
x	—	—	0.2
y	—	—	0.1
θ	0¡	—	8¡
b_2	—	0.5	—
I_2	0.95	—	—
M_D	—	14.4	—
M_E	—	14.4	—

64P6Q-A

Plastic 64pin 10X10mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1010-0.5	—		Cu Alloy





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A_1	0	0.1	0.2
A_2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	9.9	10.0	10.1
E	9.9	10.0	10.1
$\boxed{e}$	—	0.5	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
L	0.3	0.5	0.7
L_1	—	1.0	—
Lp	0.45	0.6	0.75
$\boxed{A3}$	—	0.25	—
x	—	—	0.08
y	—	—	0.1
θ	0¡	—	10¡
b_2	—	0.225	—
I_2	1.0	—	—
M_D	—	10.4	—
M_E	—	10.4	—

APPENDIX

NOTES ON PROGRAMMING

1. Processor status register

(1) Initializing of processor status register

Flags which affect program execution must be initialized after a reset.

In particular, it is essential to initialize the T and D flags because they have an important effect on calculations.

<Reason>

After a reset, the contents of the processor status register (PS) are undefined except for the I flag which is “1”.

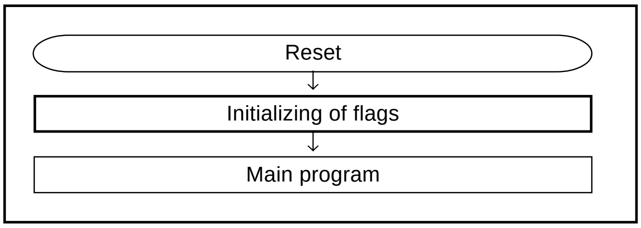


Fig.1 Initialization of processor status register

(2) How to reference the processor status register

To reference the contents of the processor status register (PS), execute the **PHP** instruction once then read the contents of (S+1). If necessary, execute the **PLP** instruction to return the PS to its original status.

A **NOP** instruction should be executed after every **PLP** instruction.

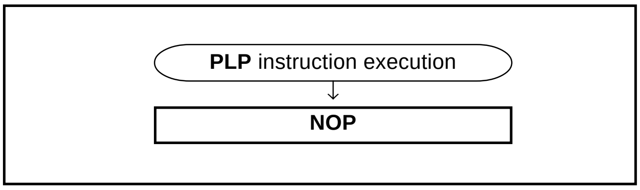


Fig. 2 Sequence of PLP instruction execution

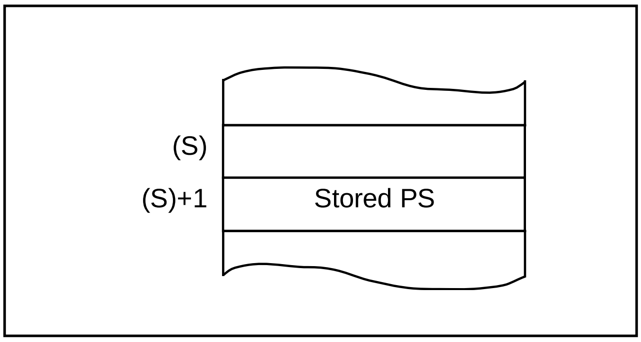


Fig. 3 Stack memory contents after PHP instruction execution

2. Decimal calculations

(1) Execution of decimal calculations

The **ADC** and **SBC** are the only instructions which will yield proper decimal notation, set the decimal mode flag (D) to “1” with the **SED** instruction. After executing the **ADC** or **SBC** instruction, execute another instruction before executing the **SEC**, **CLC**, or **CLD** instruction.

(2) Notes on status flag in decimal mode

When decimal mode is selected, the values of three of the flags in the status register (the N, V, and Z flags) are invalid after a **ADC** or **SBC** instruction is executed.

The carry flag (C) is set to “1” if a carry is generated as a result of the calculation, or is cleared to “0” if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to “0” before each calculation. To check for a borrow, the C flag must be initialized to “1” before each calculation.

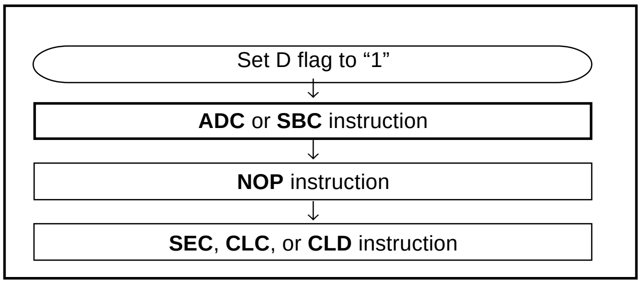


Fig. 4 Status flag at decimal calculations

3. JMP instruction

When using the **JMP** instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

4. BRK instruction

When the BRK instruction is executed with the following conditions satisfied, the interrupt execution is started from the address of interrupt vector which has the highest priority.

- Interrupt request bit and interrupt enable bit are set to “1”.
- Interrupt disable flag (I) is set to “1” to disable interrupt.

5. Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

6. Read-modify-write instruction

Do not execute a read-modify-write instruction to the read invalid address (memory and SFR).

The read-modify-write instruction operates in the following sequence: read one-byte of data from memory, modify the data, write the data back to original memory. The following instructions are classified as the read-modify-write instructions in the 740 Family.

- Bit management instructions: CLB, SEB
- Shift and rotate instructions: ASL, LSR, ROL, ROR, RRF
- Add and subtract instructions: DEC, INC
- Logical operation instructions (1’s complement): COM

Add and subtract/logical operation instructions (ADC, SBC, AND, EOR, and ORA) when T flag = “1” operate in the way as the read-modify-write instruction. Do not execute the read invalid memory and SFR.

<Reason>

When the read-modify-write instruction is executed to read invalid memory and SFR, the instruction may cause the following consequence: the instruction reads unspecified data from the memory due to the read invalid condition. Then the instruction modifies this unspecified data and writes the data to the memory. The result will be random data written to the memory or some unexpected event.

NOTES ON PERIPHERAL FUNCTIONS
Notes on I/O Ports

1. Pull-up control register

When using each port which built in pull-up resistor as an output port, the pull-up control bit of corresponding port becomes invalid, and pull-up resistor is not connected.

<Reason>

Pull-up control is effective only when each direction register is set to the input mode.

2. Modifying output data with bit managing instruction

When the port latch of an I/O port is modified with the bit managing instruction **(Note)**, the value of the unspecified bit may be changed.

<Reason>

I/O ports can be set to input or output mode in a bit unit. When reading or writing are performed to the port Pi (i = 0–7) register, the microcomputer operates as follows.

• Port in input mode
  -Read-access: reads pin's level (The contents of port latch and pin's level are unrelated.)
  -Write-access: writes data to port latch (The contents of port latch and pin's level are unrelated.)

• Port in output mode
  -Read-access: reads port latch (The contents of port latch and pin's level are unrelated.)
  -Write-access: writes data to port latch (The contents of port latch are output from the pin.)

The bit managing instructions are read-modify-write form instructions for reading and writing data by a byte unit.

Therefore, when the bit managing instructions are executed to the port set to input mode, the instruction read the pin's states, modify the specification bit, and then write data to the port latch. At this time, if the contents of the original port latch are different from the pins's level, the contents of the port latch of bit which is not specified by instruction will change.

In addition to this, if the bit managing instructions are executed to the port Pi register in order to setting output data when port Pi is configured as a mixed input and output port, the contents of the port latch of bit in the input mode which is not specified by instruction may change.

Note: Bit managing instructions: SEB instruction, CLB instruction

3. Port direction register

The port direction registers are write-only registers. Therefore, the following instructions cannot be used to this register:

• LDA instruction
• Memory operation instruction when T flag is "1"
• Instructions operating in addressing mode that modifies direction register
• Bit test instructions such as BBC and BBS
• Bit modification instructions such as CLB and SEB
• Arithmetic instructions using read-modify-write form instructions such as ROR

The LDM, STA instructions etc. are used for setting of the direction register.

Notes on Termination of Unused Pins

1. Terminate unused pins

Perform the following wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

(1) I/O ports

Set the I/O ports for the input mode and connect each pin to VCC or VSS through each resistor of 1 kΩ to 10 kΩ. The port which can select a built-in pull-up resistor can also use the built-in pull-up resistor. When using the I/O ports as the output mode, open them at "L" or "H".

• When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
• Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

2. Termination remarks

(1) Input ports

Do not open them.

<Reason>

• If the input level is undefined, the power source current may increase.
• An effect due to noise may be easily produced as compared with "1. (1) I/O ports" shown on the above.

(2) I/O ports setting as input mode

[1] Do not open in the input mode.

<Reason>

• The power source current may increase depending on the first-stage circuit.
• An effect due to noise may be easily produced as compared with "1. (1) I/O ports" shown on the above.

[2] I/O ports :

Do not connect to VCC or VSS directly.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur.

[3] I/O ports :

Do not connect multiple ports in a lump to VCC or VSS through a resistor.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

Notes on Interrupts

1. Unused interrupts

Set the interrupt enable bit for unused interrupts to “0” (disabled).

2. Change of relevant register settings

When not requiring for the interrupt occurrence synchronous with the following case, take the sequence shown in Figure 5.

•When selecting external interrupt active edge

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

Set the corresponding interrupt enable bit to “0” (disabled) .

↓

Set the interrupt edge select bit, active edge switch bit, or the interrupt source select bit.

↓

NOP (One or more instructions)

↓

Set the corresponding interrupt request bit to “0” (no interrupt request issued).

↓

Set the corresponding interrupt enable bit to “1” (enabled).

Fig. 5 Sequence of changing relevant register

<Reason>

When setting the followings, the interrupt request bit may be set to “1”.

•When selecting external interrupt active edge

INT_0 interrupt edge selection bit

(bit 0 of interrupt edge selection register (address $003A_{16}$))

INT_1 interrupt edge selection bit

(bit 1 of interrupt edge selection register (address $003A_{16}$))

INT_2 interrupt edge selection bit

(bit 2 of interrupt edge selection register (address $003A_{16}$))

$CNTR_0$ active edge switch bit

(bit 6 of timer X control register (address $0FF4_{16}$))

$CNTR_1$ active edge switch bit

(bit 6 of timer Y mode register (address 0030_{16}))

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

Interrupt edge selection register (address $003A_{16}$)

3. Check of interrupt request bit

When executing the **BBC** or **BBS** instruction to an interrupt request bit of an interrupt request register immediately after this bit is set to “0”, take the following sequence.

<Reason>

If the BBC or BBS instruction is executed immediately after an interrupt request bit of an interrupt request register is cleared to “0”, the value of the interrupt request bit before being cleared to “0” is read.

Set the interrupt request bit to “0” (no interrupt issued)

↓

NOP (one or more instructions)

↓

Execute the **BBC** or **BBS** instruction

Fig. 6 Sequence of check of interrupt request bit

Notes on Timer

1. When n (0 to 255) is written to a timer latch, the frequency divisin ratio is 1/(n+1).
2. The timers share the one frequency divider to generate the count source. Accordingly, when each timer starts operating, initializing the frequency divider is not executed. Therefore, when the frequency divider is selected for the count source, the delay of the maximum one cycle of the count source is generated until the timer starts counting or the waveform is output from timer starts operating. Also, the count source cannot be checked externally.
3. Set the timer which is not used as follows:

• Stop the count (when using a timer with stop control)

• Set “0” to the corresponding interrupt enable bit

Notes on Timer X

1. $CNTR_0$ active edge selection

• The $CNTR_0$ active edge selection bit (bit 6 of timer X mode register) also effects the active edge of the generation of the $CNTR_0$ interrupt request.

• When the pulse width is measured, set the bit 7 of the $CNTR_0$ active edge switch bits to “0”.

2. Write order to timer X

• In the timer mode, pulse output mode, event counter mode and pulse width measurement mode, write to the following registers in the order as shown below;

the timer X register (extension),
the timer X register (low-order),
the timer X register (high-order).

Do not write to only one of them.

When the above mode is set and timer X operates as the 16-bit counter, if the timer X register (extension) is never set after reset is released, setting the timer X register (extension) is not required. In this case, write the timer X register (low-order) first and the timer X register (high-order). However, once writing to the timer X register (extension) is executed, note that the value is retained to the reload latch.

• In the IGBT output and PWM modes, do not write “1” to the timer X register (extension). Also, when “1” is already written to the timer X register, be sure to write “0” to the register before using.

Write to the following registers in the order as shown below;

the compare register (high- and low-order),
the timer X register (extension),
the timer X register (low-order),
the timer X register (high-order).

It is possible to use whichever order to write to the compare register (high- and low-order). However, write both the compare register and the timer X register at the same time.

3. Read order to timer X

• In all modes, read the following registers in the order as shown below;

  the timer X register (extension),
  the timer X register (high-order),
  the timer X register (low-order).

  When reading the timer X register (extension) is not required, read the timer X register (high-order) first and the timer X register (low-order). Read order to the compare register is not specified.

• If reading to the timer X register during write operation or writing to it during read operation is performed, normal operation will not be performed.

4. Write to timer X

• Which write control can be selected by the timer X write control bit (b3) of the timer X mode register (address $002F_{16}$), writing data to both the latch and the timer at the same time or writing data only to the latch. When writing a value to the timer X address to write to the latch only, the value is set into the reload latch and the timer is updated at the next underflow. After reset release, when writing a value to the timer X address, the value is set into the timer and the timer latch at the same time, because they are written at the same time.

  When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the high-order reload latch.

• Do not switch the timer count source during timer count operation. Stop the timer count before switching it.

5. Set of timer X mode register

Set the write control bit of the timer X mode register to “1” (write to the latch only) when setting the IGBT output and PWM modes.
Output waveform simultaneously reflects the contents of both registers at the next underflow after writing to the timer X register (high-order).

6. When selecting timer X pulse width measurement mode

When selecting the timer X pulse width measurement mode, enable (set “0”) data for the event couter window control (bit 5 of timer X mode register (address $002F_{16}$)).
<Reason>
When data for the event counter window control is set to “1” (disabled), the CNTR0 input is not accepted after timer 1 underflow because this bit controls the CNTR0 input.

7. IGBT output mode

•Do not write “1” to the timer X register (extension) when using the IGBT output mode.

•When using the IGBT output mode, set the port sharing the INT_0 pin to input mode and set the port sharing the T_{XOUT} pin to output mode. When using the output control function (INT_1, INT_2), set the port sharing the INT_1, INT_2 pin to input mode.

• When using the output control function (INT_1 and INT_2) in the IGBT output mode, set the levels of INT_1 and INT_2 to “H” in the falling edge active or to “L” in the rising edge active before switching to the IGBT output mode. Set the level of INT_0 to “H” in the falling edge active or to “L” in the rising edge active before switching to the IGBT output mode.

•When setting the timer X output control bit 1 or 2 (bit 3 or 4 of timer X control register (address $0FF4_{16}$)) to “1” and initializing the output of the T_{XOUT} pin by interrupt signal of INT_1 or INT_2, while the output level from the T_{XOUT} pin changes after setting the timer X output control bit 1 or 2 to “1”, the following delay will occur.

  Minimum: Analog delay
  Maximum: Timer X count source 1 cycle + Analog delay

•In the following case, the timer X interrupti request bit (bit 7 of interrupt request register 1 (address $003C_{16}$)) is set to “1”.

  •When Timer X underflow
  •When input from INT_0 pin is detected at the time of IGBT output mode

Notes on Timer Y

1. Timer Y read/write control

• When reading from/writing to timer Y, read from/write to both the high-order and low-order bytes of timer Y. When the value is read, read the high-order bytes first and the low-order bytes next. When the value is written, write the low-order bytes first and the high-order bytes next.

  If reading from the timer Y register during write operation or writing to it during read operation is performed, normal operation will not be performed.

• When writing a value to the timer Y address to write to the latch only, the value is set into the reload latch and the timer is updated at the next underflow. Normally, when writing a value to the timer Y address, the value is set into the timer and the timer latch at the same time, because they are set to write at the same time.

  When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the high-order reload latch.

• Do not switch the timer count source during timer count operation. Stop the timer count before switching it.

2. $CNTR_1$ interrupt active edge selection

$CNTR_1$ interrupt active edge depends on the $CNTR_1$ active edge switch bit. However, in pulse width HL continuously measurement mode, $CNTR_1$ interrupt request is generated at both rising and falling edges of $CNTR_1$ pin input signal regardless of the setting of $CNTR_1$ active edge switch bit.

Notes on Timers 1 to 4

1. Cascading connection

• When using cascading connection, set the value of timer in the order of the timer 1 register, the timer 2 register, the timer 3 register, and the timer 4 register after the count source selection of timer 1 to 4.

<Reason>

• When the count source of timers 1 to 4 is selected, the timer counting value may become arbitrary value because a thin pulse is generated in count input of timer.

2. Timer 3PWM0 mode, timer 4PWM1 mode

• When PWM output is suspended after starting PWM output, depending on the level of the output pulse at that time to resume an output, the delay of the one section of the short interval may be needed.

Stop at “H”: No output delay

Stop at “L”: Output is delayed time of 256 × ts

• In the PWM mode, the follows are performed every cycle of the long interval (4 × 256 × ts).

  • Generation of timer 3, timer 4 interrupt requests
  • Update of timer 3, timer 4

• When “L” is output from the $P5_2/T_{3OUT}/PWM_0$ pin continuously in the timer 3PMW0 mode, set the $P5_2/T_{3OUT}/PWM_0$ pin as I/O port by set the timer 3 output selection bit to “0” before “L” is output. Do not set “00_{16}” to timer 3 in this mode. The value which can be set are 1-255.

• When “L” is output from the $P5_3/T_{4OUT}/PWM_1$ pin continuously in the timer 4PMW1 mode, set the $P5_3/T_{4OUT}/PWM_1$ pin as I/O port by set the timer 4 output selection bit to “0” before “L” is output. Do not set “00_{16}” to timer 4 in this mode. The value which can be set are 1-255.

3. Writing to Timer 2, Timer 3, Timer 4

When writing to the latch only, if the write timing to the reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the reload latch.

Notes on Serial I/O1

1. Writing to baud rate generator (BRG)

Write data to BRG while the transmission and reception operations are stopped.

2. Setting procedure when using serial I/O1 transmit interrupt

When the serial I/O1 transmit interrupt is used, take the following sequence.

①Set the serial I/O1 transmit interrupt enable bit (bit 4 of interrupt control register 1 (address $003E_{16}$)) to “0” (disabled).

②Set the transmit enable bit (bit 4 of serial I/O1 control register (address $0FE0_{16}$)) to “1”.

③Set the serial I/O1 transmit interrupt request bit (bit 3 of interrupt request register 1 (address $003C_{16}$)) to “0” (no interrupt request issued) after 1 or more instruction has executed.

④Set the serial I/O1 transmit interrupt enable bit to “1” (enabled).

<Reason>

When the transmission enable bit is set to “1”, the transmit buffer empty flag (bit 0 of serial I/O1 status register (address $001D_{16}$)) and the transmit shift register completion flag are set to “1”.

Therefore, the serial I/O1 transmit interrupt request bit is set to “1” regardless of the state of the transmit interrupt source selection bit (bit 3 of serial I/O1 control register).

3. Data transmission control with referring to transmit shift register completion flag

After the transmit data is written to the transmit buffer register (address 0018_{16}), the transmit shift register completion flag (bit 2 of serial I/O1 status reguster (address $001D_{16}$)) changes from “1” to “0” with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

4. Setting serial I/O1 control register again

Set the serial I/O1 control register again after the transmission and the reception circuits are reset by setting both the transmit enable bit and the receive enable bit to “0”.

Set both the transmit enable bit (TE) and the receive enable bit (RE) to “0”

↓

Set the bits 0 to 3 and bit 6 of the serial I/O1 control register

↓

Set both the transmit enable bit (TE) and the receive enable bit (RE), or one of them to “1”

Can be set with the **LDM** instruction at the same time

Fig. 7 Sequence of setting serial I/O1 control register again

5. Pin state after transmit completion

The TxD pin holds the state of the last bit of the transmission after transmission completion. When the internal clock is selected for the transmit clock in the clock synchronous serial I/O mode, the S_{CLK1} pin holds “H”.

6. Serial I/O1 enable bit during transmit operation

When the serial I/O1 enable bit (bit 7 of serial I/O1 control register (address $0FE0_{16}$)) is set to “0” (serial I/O1 disabled) when data transmission is in progress, the transmission progress internally. However, the external data transfer is terminated because the pins become regular I/O ports. In addition to this, when data is written to the transmission buffer register, data transmission is started internally. When the serial I/O1 enable bit is set to “1”, the transmission is output to the TxD pin in the middle of the transfer.

7. Transmission control when external clock is selected

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to “1” at “H” of the S_{CLK1} input level. Also, write the transmit data to the transmit buffer register at “H” of the S_{CLK1} input level.

8. Receive operation in clock synchronous serial I/O mode

When receiving data in the clock synchronous serial I/O mode, set not only the receive enable bit but also the transmit enable bit to “1”. Then write dummy data to the transmission buffer register. When the internal clock is selected as the synchronous clock, the synchronous clock is output at this point and the receive operation is started. When the external clock is selected as the transfer clock, the serial I/O becomes ready for data receive at this point and, when the external clock is input to the clock input pin, the receive operation is started. The $P4_5$/TxD pin outputs the dummy data written in the transmission buffer register.

9. Transmit and receive operation in clock synchronous serial I/O mode

When stopping transmitting and receiving operations in the clock synchronous serial I/O mode, set the receive enable bit and the transmit enable bit to "0" simultaneously. If only one of them is stopped the receive or transmit operation may loose synchronization, causing a bit slippage.

Notes on Serial I/O2

1. Switching synchronous clock

When switching the synchronous clock by the serial I/O2 mode selection bit (bit 6 of serial I/O2 control register (address $0FE3_{16}$)), initialize the serial I/O2 counter (write data to transmit/receive buffer register 2 (address $001E_{16}$)).

2. Notes when selecting external clock

When an external clock is selected as the synchronous clock, the TxD_2 pin holds the output level of D_7 after transmission is completed. However, if the clock is input to the serial I/O continuously, the transmit/receive buffer register continue the shift operation and output data from the TxD_2 pin continuously.

A write operation to the transmit/receive buffer register 2 must be performed when the S_{CLK2} pin is "H".

When the internal clock is selected as the synchronous clock, the TxD_2 pin holds the high-impedance state after transmission.

Notes on Programming for Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{S_{RDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{S_{RDY}}$ output enable bit to "1."

Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

Notes on A-D Converter

1. Analog input pin

Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01 µF to 1 µF. Further, be sure to verify the operation of application products on the user side.

<Reason>

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A-D conversion precision to be worse.

2. Read A-D conversion register

How to read the A-D conversion register at 10-bit A-D conversion and 8-bit A-D conversion is shown in Fig. 8.

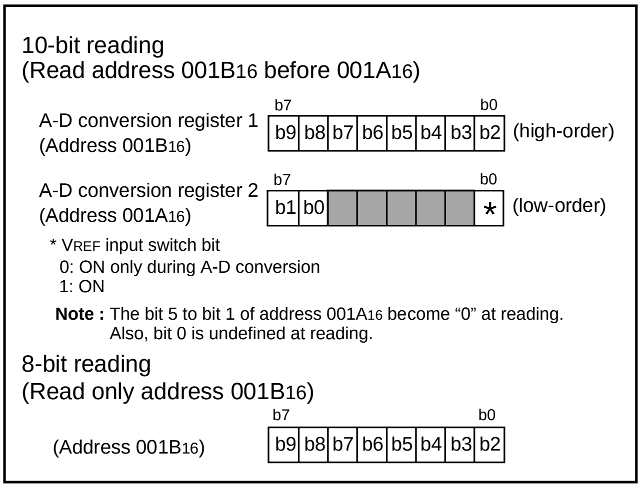


Fig. 8 A-D conversion register reading

3. Analog power source input pin AVss

The AVss pin is an analog power source input pin. Regardless of using the A-D conversion function or not, connect it as following :

• AVSS : Connect to the VSS line

<Reason>

If the AVss pin is opened, the microcomputer may have a failure because of noise or others.

4. Reference voltage input pin VREF

Connect an approximately 1000 pF capacitor across the AVss pin and the VREF pin. Besides, connect the capacitor across the VREF pin and the AVss pin at equal length as close as possible.

5. Clock frequency during A-D conversion

Use the A-D converter in the following conditions:

• Select XIN-XOUT as system clock ϕ by the system clock selection bit (bit 7 of CPU mode register (address $003B_{16}$)). When selecting XCIN-XCOUT as system clock ϕ, the A-D conversion function cannot be used.

• f(XIN) is 500 kHz or more.

• Do not execute the STP or WIT instruction during A-D conversion.

<Reason>

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. This may cause the A-D conversion precision to be worse.

6. Write to A-D conversion completion bit durng A-D conversion

When "0" is set to the A-D conversion completion bit by the program during A-D conversion, re-conversion is performed.

7. Write during A-D conversion

The A-D converter will not operate normally if one of the following operation is applied during the A-D conversion:

• Writing to CPU mode register
• Writing to A-D control register

8. Notes on programming for A-D conversion

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low. Therefore, set the A-D clock frequency to 250 kHz or more. Also, when the STP instruction is executed during the A-D conversion, the A-D conversion is stopped immediately, the A-D conversion completion bit is set to "1", and the interrupt request is generated.

Notes on LCD Drive Control Circuit

1. Count source for LCDCK

The LCDCK count source selection bit (bit 7 of LCD mode register (address 0039_{16})) is set to “0” after reset, selecting f(X_{CIN})/32. The sub clock has stopped after reset. Therefore, turn on LCD after starting the oscillation and stabilizing the oscillation. Select the LCDCK count source after the corresponding clock source becomes stable.

2. STP instruction

When executing the STP instruction, bits 0 to 5 and bit 7 of the LCD power supply control register and the LCD enable bit (bit 3 of LCD mode register) are set to “0”. Set these bits again after returning from stop mode.

3. When not using LCD

When not using an LCD, leave the LCD segment and common pins open. Connect the V_{L1} pin to Vss, and the V_{L2} and V_{L3} pins to Vcc.

4. LCD drive power supply

(1) Power supply capacitor may be insufficient with the division resistance for LCD power supply, and the characteristic of the LCD panel. In this case, there is the method of connecting the bypass capacitor about 0.1–0.33 µF to V_{L1}–V_{L3} pins. The example of a strengthening measure of the LCD drive power supply is shown in Figure 9.

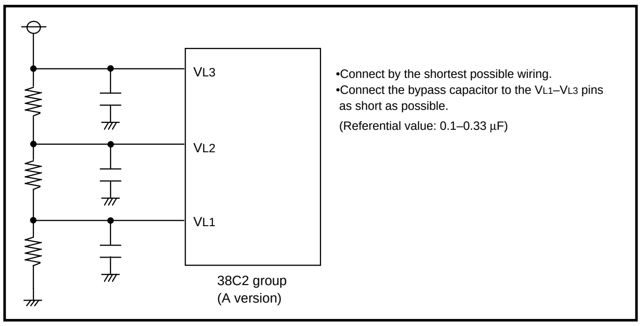


Fig. 9 Strengthening measure example of LCD drive power supply

(2) When the LCD drive control circuit is used at V_{L3} = V_{CC}, apply V_{CC} to V_{L3} pin and write “1” to V_{L3} connection bit (bit 6 of the LCD power control register (address 0038_{16})).

(3) When the voltage is applied to V_{L1} to V_{L3} by using the external resistor, write “10_2” to dividing resistor for LCD power selection bits (RSEL) of the LCD power control register (address 0038_{16}).

5. Segment output disable register

(1) Only pins set to output ports by the direction register can be controlled to switch to output ports or segment outputs by the segment output disable register.

(2) When the VL pin input selection bit (VLSEL) of the LCD power control register (address 0038_{16}) is “1”, settings of the segment output disable bit 22 and segment output disable bit 23 are invalid.

6. Data setting to LCD display RAM

When writing a data into the LCD display RAM during LCD being turned ON (LCD enable bit = “1”), write the confirmed data. Do not write temporarily on the LCD display RAM because this might cause the LCD display flickering. Figure 10 shows the write procedure for LCD display RAM when LCD is on.

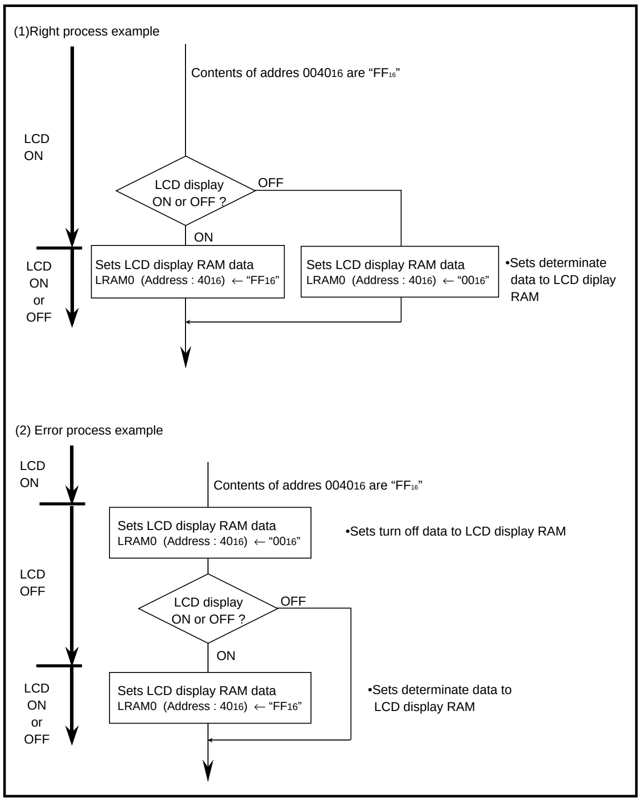


Fig. 10 Write procedure for LCD display RAM when LCD is on

Notes on Watchdog Timer

1. The watchdog timer is operating during the wait mode. Write data to the watchdog timer control register to prevent timer underflow.
2. The watchdog timer stops during the stop mode. However, the watchdog timer is running during the wait time (time set by timer 1 and timer 2) and the watchdog timer control register must be written just before executing the STP instruction.
3. The count source of the watchdog timer is affected by the system clock ϕ selected by the system clock selection bits (bits 6, 7 of CPU mode register (address $003B_{16}$)).

Notes on Reset Circuit

1. Reset input voltage control

Make sure that the reset input voltage is less than 0.2 Vcc for Vcc(min).

2. Countermeasures for reset signal slow rising

In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and the Vss pin. Use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following:

•Make the length of the wiring which is connected to a capacitor as short as possible.

•Be sure to verify the operation of application products on the user side.

<Reason>

If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

3. Port state immediately after reset

Table 1 shows the each pin state during $\overline{\text{RESET}}$ pin is “L”.

Table 1 Each pin state during $\overline{\text{RESET}}$ pin is “L”

Pin name	Pin state
P0–P2 (SEG_0–SEG_{23})	Input mode (with pull-up)
P3, P4, P5, $P6_0$–$P6_2$	Input mode (high-impedance)
COM_0–COM_3	Vcc level input

4. Frequency relation of $f(X_{IN})$ and $f(\phi)$

The frequency relation of $f(X_{IN})$ and $f(\phi)$ is $f(X_{IN}) = 8 \bullet f(\phi)$.

Notes on Reset Circuit

1. Mode transition

(1) Both the main clock (X_{IN}-X_{OUT}) and sub-clock (X_{CIN}-X_{COUT}) need time for the oscillations to stabilize. The mode transition between middle-/high-speed and low-speed mode must be performed after the corresponding clock becomes stable. The sub-clock, needs extra time to stabilize particularly when executing operations after power-on and stop mode. The main and sub clocks require the following condition for mode transition.

$f(X_{IN}) > 3 \times f(X_{CIN})$

(2) The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.

2. State transitions of system clock

When the mode is switched from frequency/2/4/8 to the low-speed mode, or the opposite is performed, change CM_7 (bit 7 of system clock control bits of CPU mode register (address $003B_{16}$)) at first, and then, change CM_6 (bit 6 of system clock control bits of CPU mode register (address $003B_{16}$)) after the oscillation of the changed mode is stabilized.

3. Wait mode

Timer and LCD operate in the wait mode.

Notes on Oscillation External Output Function

When the signal from the X_{OUT} pin or X_{COUT} pin of the oscillation circuit is input directly to the circuit except this MCU and used, the system operation may be unstabilized.

In order to share the oscillation circuit safely, use the clock output from $P4_0$ and $P4_1$ by the oscillation external output function for the circuits except this MCU.

NOTES ON HARDWARE
Handling of Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (V_{SS} pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF–0.1μF is recommended.

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REVISION HISTORY	38C2 Group (A VERSION) Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 13, 2003	–	First edition issued
2.00	May. 28, 2004	28 49 70 72 93 to 100	Explanations of “(5) Output Control Function of Timer X” are partly eliminated. Figure 50 is partly revised. Explanations of “Software Commands” of Rev.1.00 are eliminated. Note 2 of Table 16 is partly revised. “APPENDIX” is added.