R1RW0416D Series

4M High Speed SRAM (256-kword × 16-bit)

REJ03C0107-0100Z
Rev. 1.00
Mar.12.2004

Description

The R1RW0416D is a 4-Mbit high speed static RAM organized 256-kword × 16-bit. It has realized high speed access time by employing CMOS process (6-transistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. The R1RW0416D is packaged in 400-mil 44-pin SOJ and 400-mil 44-pin plastic TSOPII for high density surface mounting.

Features

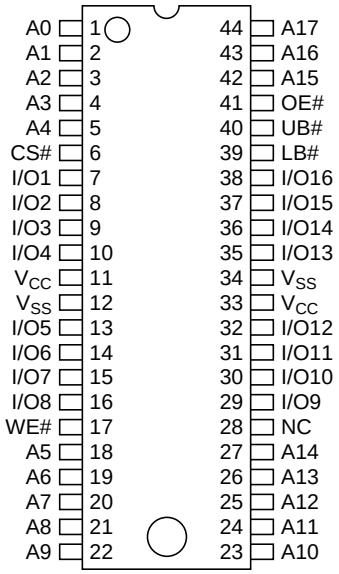
- Single 3.3 V supply: 3.3 V ± 0.3 V
- Access time: 12 ns (max)
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - — All inputs and outputs
- Operating current: 130 mA (max)
- TTL standby current: 40 mA (max)
- CMOS standby current: 5 mA (max)
  : 0.8 mA (max) (L-version)
- Data retention current: 0.4 mA (max) (L-version)
- Data retention voltage: 2.0 V (min) (L-version)
- Center V_{CC} and V_{SS} type pin out

Ordering Information

Type No.	Access time	Package
R1RW0416DGE-2PR	12 ns	400-mil 44-pin plastic SOJ (44P0K)
R1RW0416DGE-2LR	12 ns	
R1RW0416DSB-2PR	12 ns	400-mil 44-pin plastic TSOPII (44P3W-H)
R1RW0416DSB-2LR	12 ns	

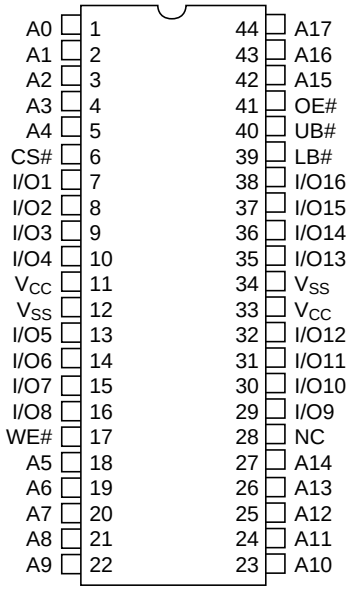
Pin Arrangement

44-pin SOJ



(Top View)

44-pin TSOP

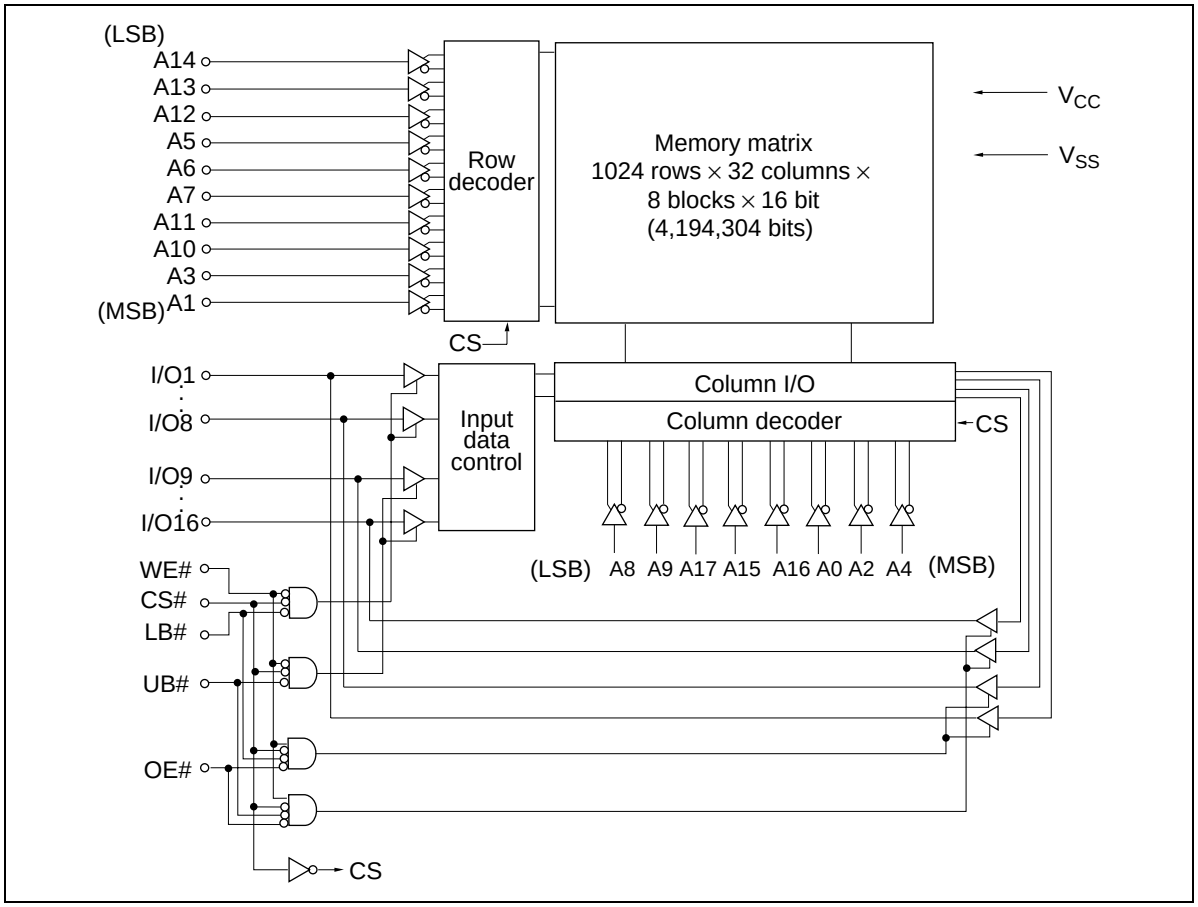


(Top View)

Pin Description

Pin name	Function
A0 to A17	Address input
I/O1 to I/O16	Data input/output
CS#	Chip select
OE#	Output enable
WE#	Write enable
UB#	Upper byte select
LB#	Lower byte select
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Operation Table

CS#	OE#	WE#	LB#	UB#	Mode	V_{CC} current	I/O1–I/O8	I/O9–I/O16	Ref. cycle
H	×	×	×	×	Standby	I_{SB}, I_{SB1}	High-Z	High-Z	—
L	H	H	×	×	Output disable	I_{CC}	High-Z	High-Z	—
L	L	H	L	L	Read	I_{CC}	Output	Output	Read cycle
L	L	H	L	H	Lower byte read	I_{CC}	Output	High-Z	Read cycle
L	L	H	H	L	Upper byte read	I_{CC}	High-Z	Output	Read cycle
L	L	H	H	H	—	I_{CC}	High-Z	High-Z	—
L	×	L	L	L	Write	I_{CC}	Input	Input	Write cycle
L	×	L	L	H	Lower byte write	I_{CC}	Input	High-Z	Write cycle
L	×	L	H	L	Upper byte write	I_{CC}	High-Z	Input	Write cycle
L	×	L	H	H	—	I_{CC}	High-Z	High-Z	—

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Voltage on any pin relative to V_{SS}	V_T	–0.5*[1] to V_{CC} + 0.5*[2]	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Notes: 1. V_T (min) = –2.0 V for pulse width (under shoot) ≤ 6 ns.
2. V_T (max) = V_{CC} + 2.0 V for pulse width (over shoot) ≤ 6 ns.

Recommended DC Operating Conditions

(Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}*[3]	3.0	3.3	3.6	V
	V_{SS}*[4]	0	0	0	V
Input voltage	V_{IH}	2.0	—	V_{CC} + 0.5*[2]	V
	V_{IL}	–0.5*[1]	—	0.8	V

Notes: 1. V_{IL} (min) = –2.0 V for pulse width (under shoot) ≤ 6 ns.
2. V_{IH} (max) = V_{CC} + 2.0 V for pulse width (over shoot) ≤ 6 ns.
3. The supply voltage with all V_{CC} pins must be on the same level.
4. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	2	µA	V_{IN} = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	2	µA	V_{IN} = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	130	mA	Min cycle CS# = V_{IL}, I_{OUT} = 0 mA Other inputs = V_{IH}/V_{IL}
Standby power supply current	I_{SB}	—	40	mA	Min cycle, CS# = V_{IH}, Other inputs = V_{IH}/V_{IL}
	I_{SB1}	—	5	mA	f = 0 MHz V_{CC} ≥ CS# ≥ V_{CC} – 0.2 V, (1) 0 V ≤ V_{IN} ≤ 0.2 V or (2) V_{CC} ≥ V_{IN} ≥ V_{CC} – 0.2 V
		—*[1]	0.8*[1]	mA	
Output voltage	V_{OL}	—	0.4	V	I_{OL} = 8 mA
	V_{OH}	2.4	—	V	I_{OH} = –4 mA

Note: 1. This characteristics is guaranteed only for L-version.

Capacitance

(Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Max	Unit	Test conditions
Input capacitance*[1]	C_{IN}	—	6	pF	V_{IN} = 0 V
Input/output capacitance*[1]	$C_{I/O}$	—	8	pF	$V_{I/O}$ = 0 V

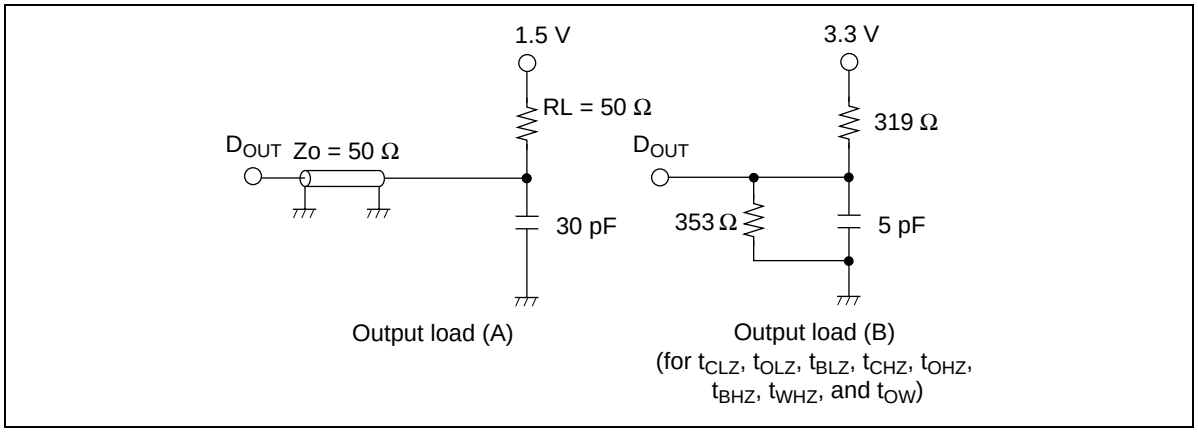
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



Read Cycle

		R1RW0416D			
		-2			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time	t_{RC}	12	—	ns	
Address access time	t_{AA}	—	12	ns	
Chip select access time	t_{ACS}	—	12	ns	
Output enable to output valid	t_{OE}	—	6	ns	
Byte select to output valid	t_{BA}	—	6	ns	
Output hold from address change	t_{OH}	3	—	ns	
Chip select to output in low-Z	t_{CLZ}	3	—	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	ns	1
Byte select to output in low-Z	t_{BLZ}	0	—	ns	1
Chip deselect to output in high-Z	t_{CHZ}	—	6	ns	1
Output disable to output in high-Z	t_{OHZ}	—	6	ns	1
Byte deselect to output in high-Z	t_{BHZ}	—	6	ns	1

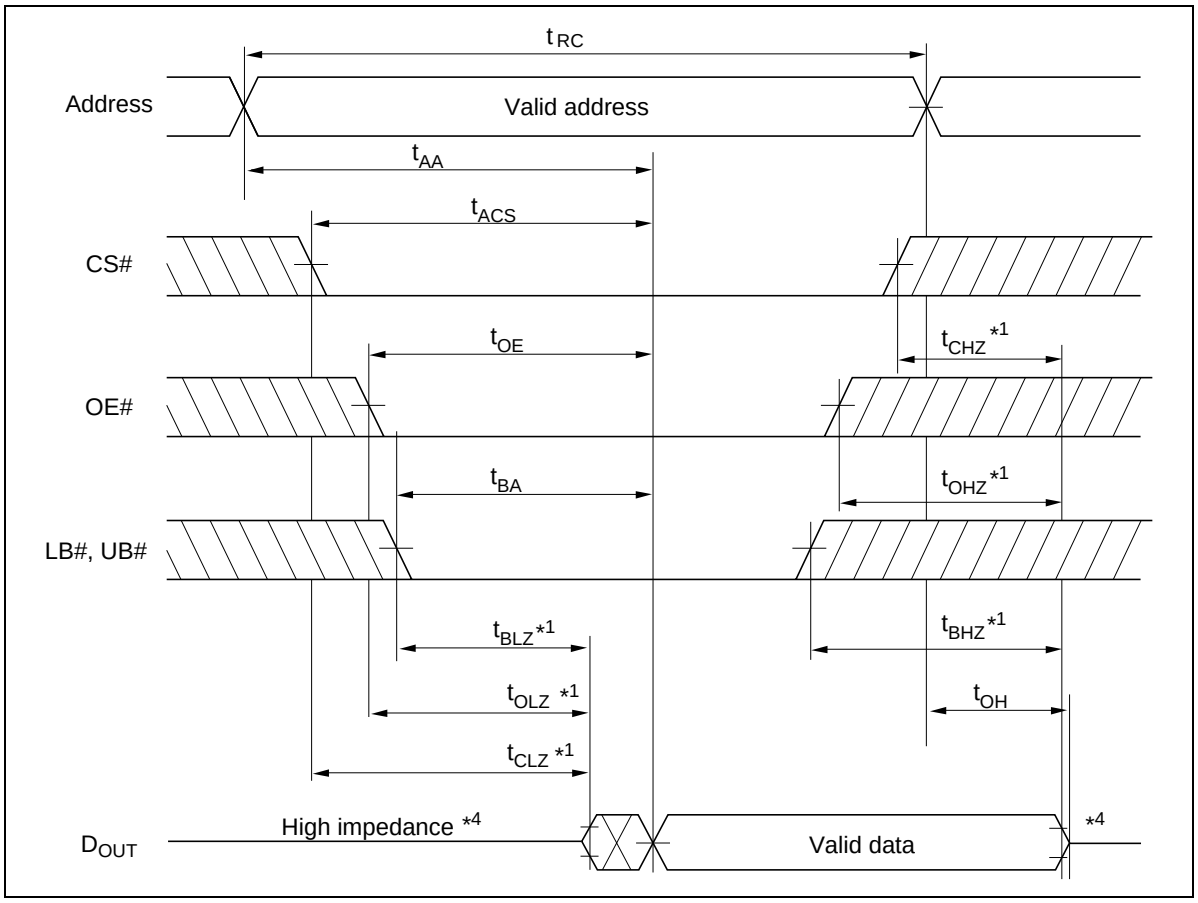
Write Cycle

		R1RW0416D			
		-2			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	12	—	ns	
Address valid to end of write	t_{AW}	8	—	ns	
Chip select to end of write	t_{CW}	8	—	ns	8
Write pulse width	t_{WP}	8	—	ns	7
Byte select to end of write	t_{BW}	8	—	ns	
Address setup time	t_{AS}	0	—	ns	5
Write recovery time	t_{WR}	0	—	ns	6
Data to write time overlap	t_{DW}	6	—	ns	
Data hold from write time	t_{DH}	0	—	ns	
Write disable to output in low-Z	t_{OW}	3	—	ns	1
Output disable to output in high-Z	t_{OHZ}	—	6	ns	1
Write enable to output in high-Z	t_{WHZ}	—	6	ns	1

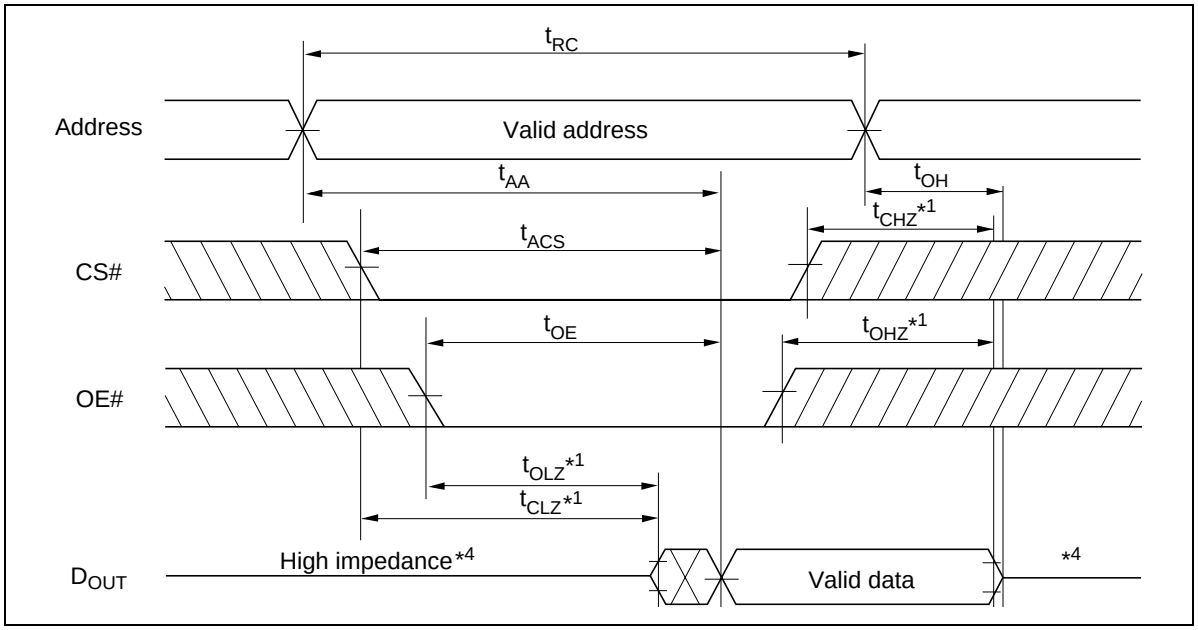
Notes:
1. Transition is measured ±200 mV from steady voltage with output load (B). This parameter is sampled and not 100% tested.
2. If the CS# or LB# or UB# low transition occurs simultaneously with the WE# low transition or after the WE# transition, output remains a high impedance state.
3. WE# and/or CS# must be high during address transition time.
4. If CS#, OE#, LB# and UB# are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
5. t_{AS} is measured from the latest address transition to the latest of CS#, WE#, LB# or UB# going low.
6. t_{WR} is measured from the earliest of CS#, WE#, LB# or UB# going high to the first address transition.
7. A write occurs during the overlap of a low CS#, a low WE# and a low LB# or a low UB# (t_{WP}). A write begins at the latest transition among CS# going low, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS# going high, WE# going high and LB# going high or UB# going high.
8. t_{CW} is measured from the later of CS# going low to the end of write.

Timing Waveforms

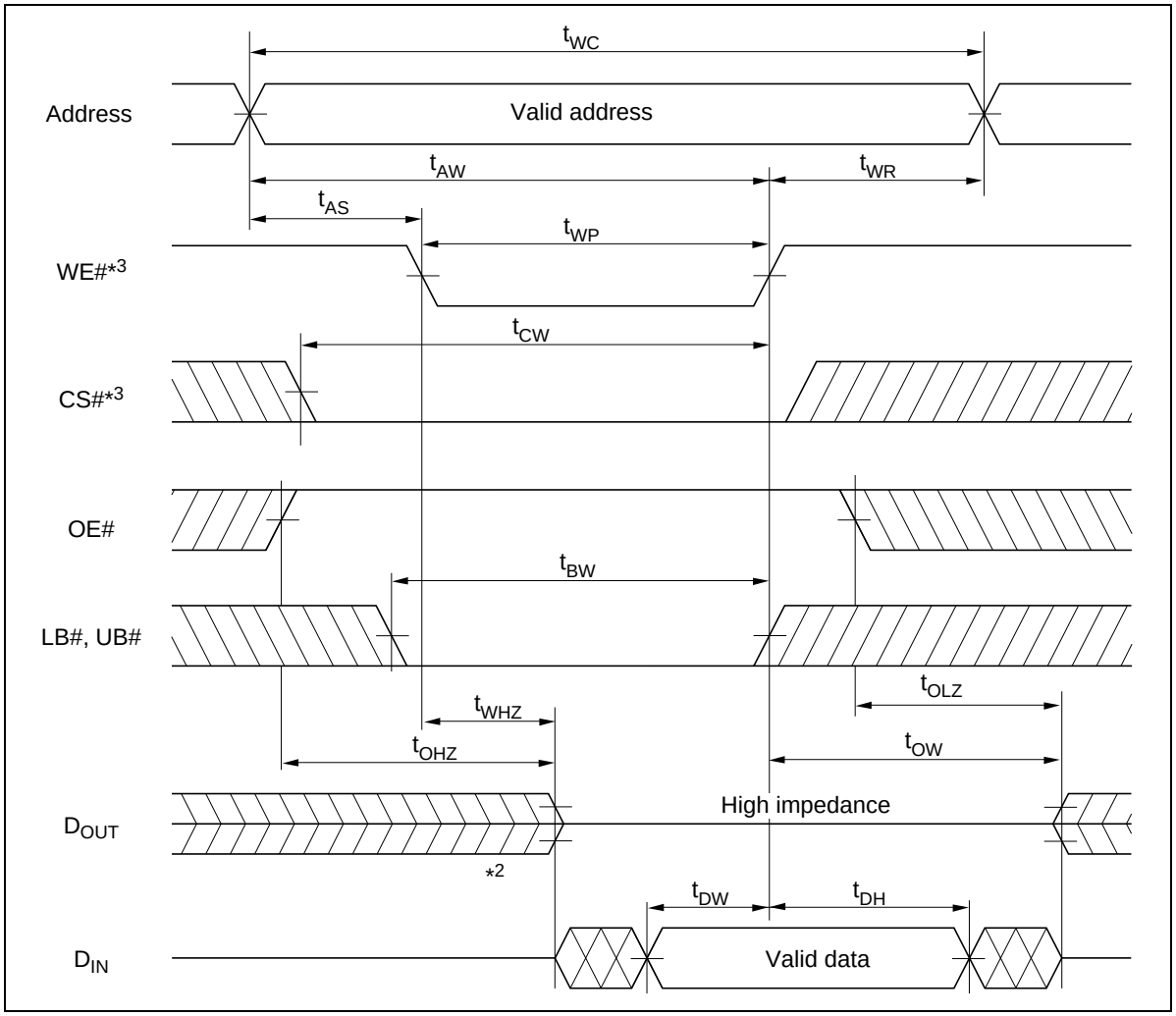
Read Timing Waveform (1) (WE# = V_{IH})



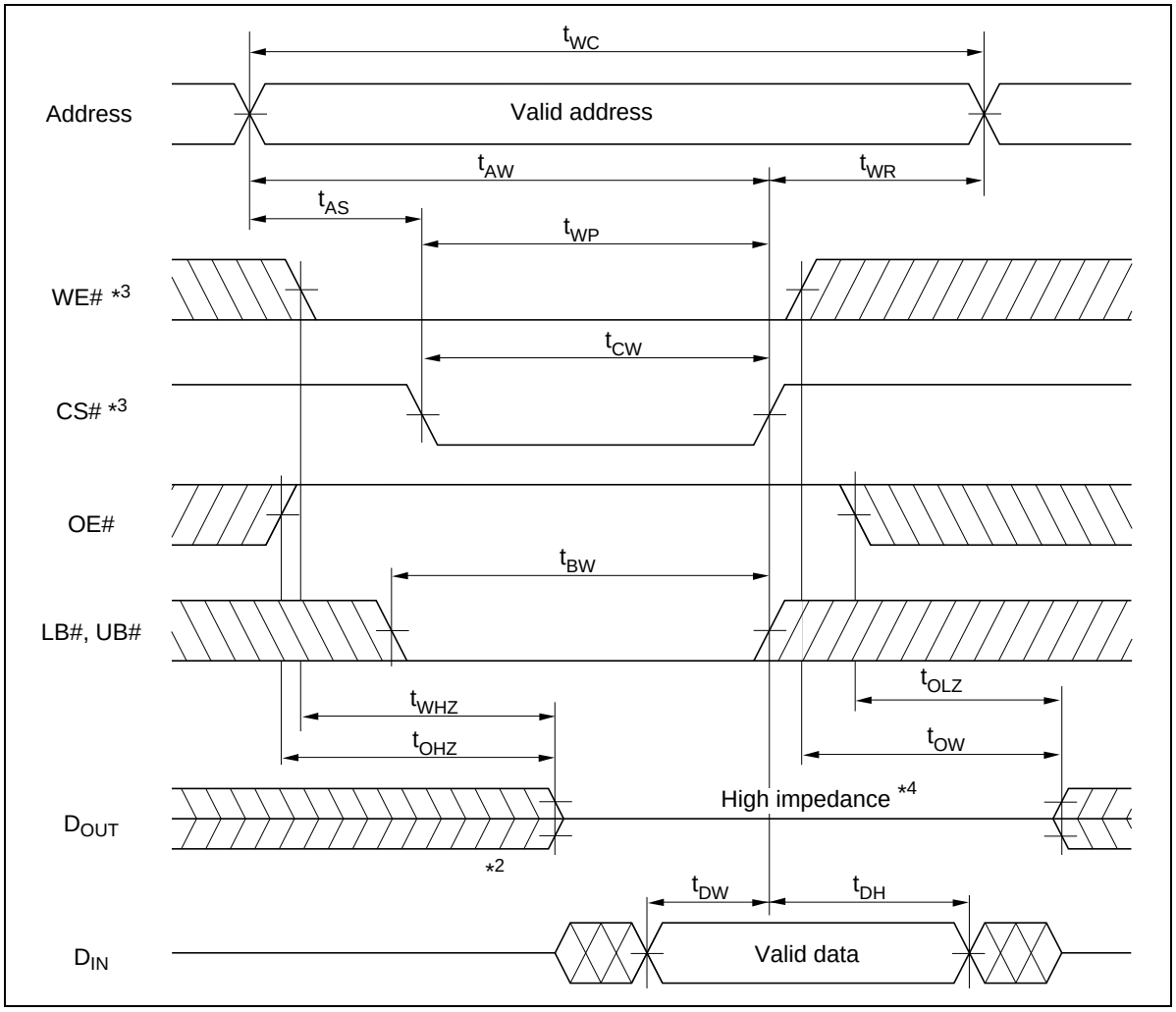
Read Timing Waveform (2) (WE# = V_{IH}, LB# = V_{IL}, UB# = V_{IL})



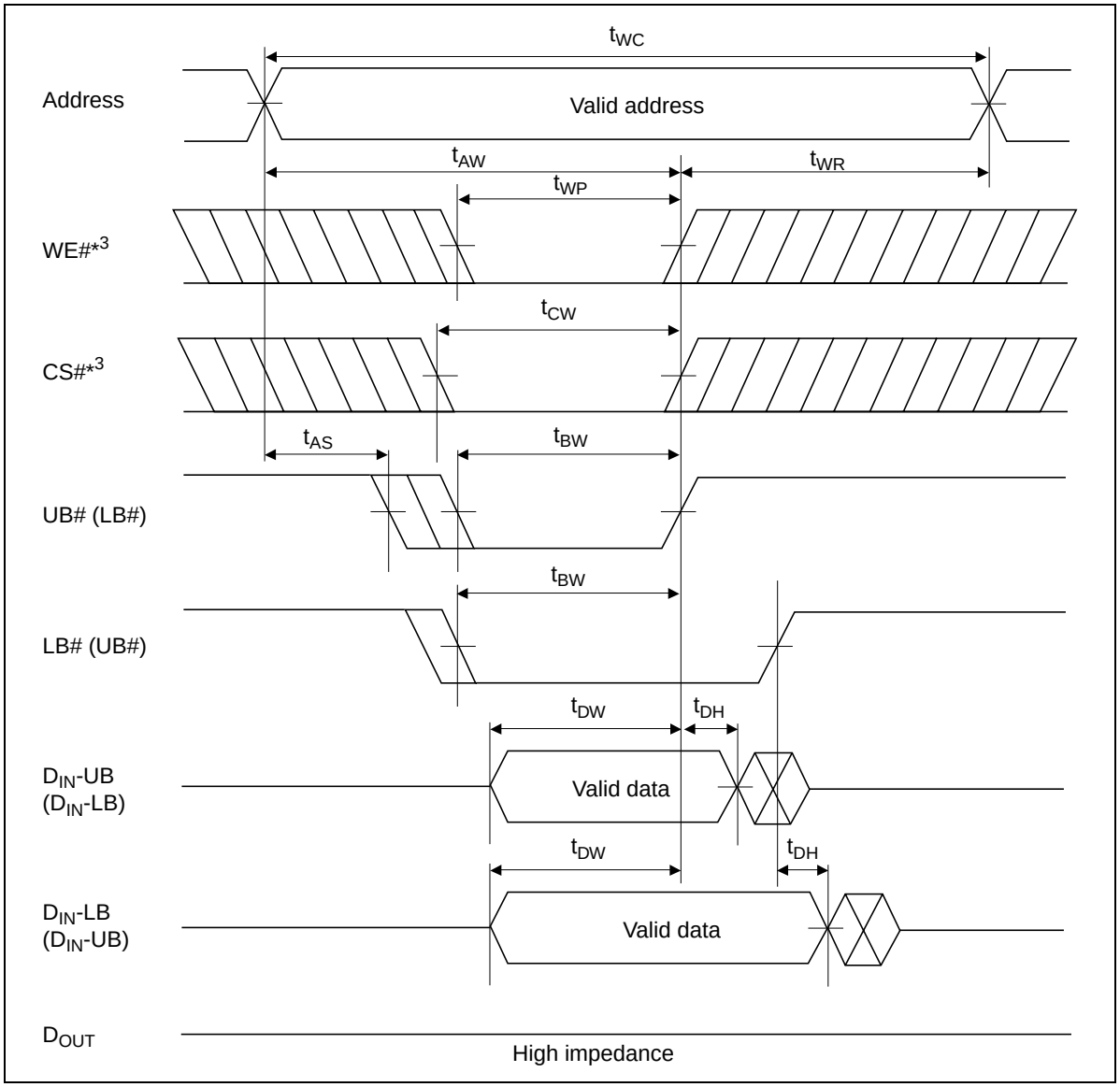
Write Timing Waveform (1) (WE# Controlled)



Write Timing Waveform (2) (CS# Controlled)



Write Timing Waveform (3) (LB#, UB# Controlled, OE# = V_{IH})



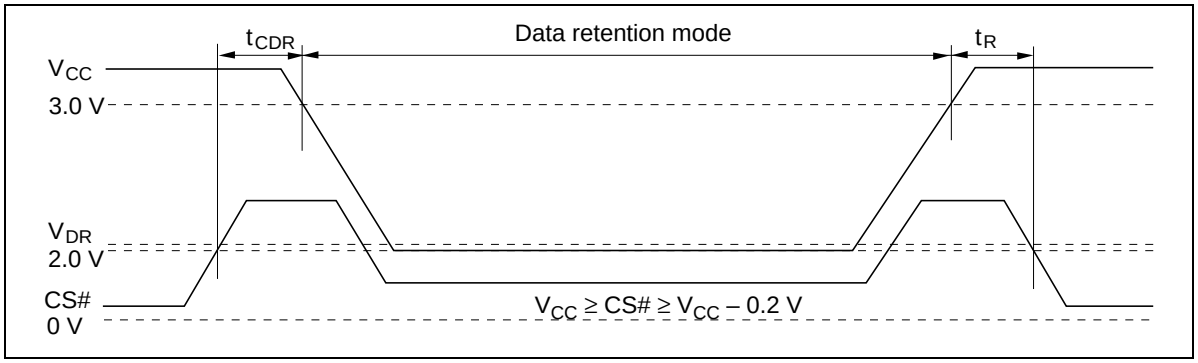
Low V_{CC} Data Retention Characteristics

(Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	V	$V_{CC} \geq CS\# \geq V_{CC} - 0.2$ V, (1) 0 V ≤ V_{IN} ≤ 0.2 V or (2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2$ V
Data retention current	I_{CCDR}	—	400	µA	V_{CC} = 3 V $V_{CC} \geq CS\# \geq V_{CC} - 0.2$ V, (1) 0 V ≤ V_{IN} ≤ 0.2 V or (2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2$ V
Chip deselect to data retention time	t_{CDR}	0	—	ns	See retention waveform
Operation recovery time	t_R	5	—	ms	

Low V_{CC} Data Retention Timing Waveform



Rev.	Date	Contents of Modification	
		Page	**Description**
0.01	Sep. 30, 2003	—	Initial issue
1.00	Mar.12.2004	—	Deletion of Preliminary

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