

# M64611FP

# DIGITAL SERVO MOTOR CONTROL FOR RADIO CONTROL

REJ03F0017-0100Z Rev.1.00 Aug.26.2003

#### **Description**

The M64611FP is a semiconductor integrated circuit of the BiCMOS structure for servo motor control for the radio control application.

#### **Features**

- A quick response and a powerful holding torque
- Simple settings of dead band, pulse stretcher, boost time addition, and max duty.

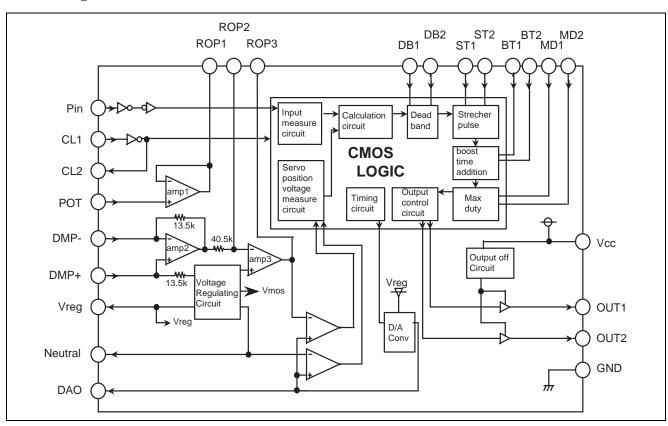
#### **Application**

• Digital proportional system for radio control

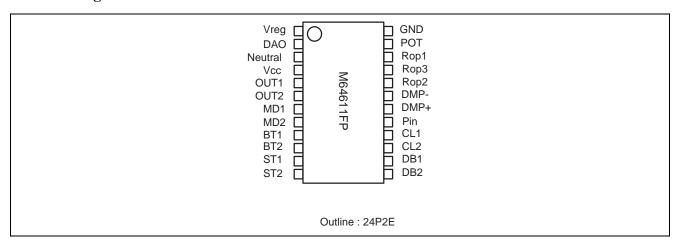
#### **Recommended operating condition**

• Supply voltage range: 4 to 9 V

#### **Block diagram**



# **Pin Arrangement**



# **Pin Description**

Pin No.	Symbol	Function	Notes
1	Vreg	Regulated voltage output	Connect a capacitor for the stabilization between Vreg and GND
2	DAO	D/A converter output	Connect the capacitor for the filter of 100 – 1000pF between DAO and GND.
3	Neutral	Neutral voltage output	Make it open usually.
			Connect a capacitor for the stabilization between Neutral and GND if Neutral voltage is unstable.
4	Vcc	Supply voltage	Connect the Electrolytic condenser more than 10 μF and
	OUT4	Outrot win 4	the ceramics condenser more than 0.1 μF.
5	OUT1	Output pin 1	Connect to the external driver IC for servo drive.
6	OUT2	Output pin 2	
7	MD1	Max. duty input 1	Refer to the following input table.
8	MD2	Max. duty input 2	When it is "H" : OPEN
9	BT1	Boost input 1	When it is "L" : GND
10	BT2	Boost input 2	
11	ST1	Stretcher input 1	
12	ST2	Stretcher input 2	
13	DB2	Dead Band input 2	
14	DB1	Dead Band input 1	
15	CL2	Oscillation terminal 2	Connect to resonator between CL1 and CL2.
16	CL1	Oscillation terminal 1	
17	Pin	Receiving pulse input	
18	DMP+	Damping resistor input+	Connect to the damping resistor of 100 k $\Omega$ -1 M $\Omega$ .
19	DMP-	Damping resistor input-	
20	ROP2	Gain Adjustment Resistor 2	Connect to the resistances for adjusting Gain.
21	ROP3	Gain Adjustment Resistor 3	
22	ROP1	Gain Adjustment Resistor 1	
23	POT	Servo position voltage input	Connect the potentiometer.
24	GND	GND	

# **Input Table**

<Dead Band >

Inp	ut	
DB1	DB2	Set value
L	L	4tosc
Н	L	6tosc
L	Н	9tosc
Н	Н	13tosc

<max< td=""><td>Duty</td><td>&gt;</td></max<>	Duty	>

In	put	
MD1	MD2	Set value
L	L	about 97%
Н	L	about 94%
L	Н	about 88%
Н	Н	about 82%

<Boost>

Inp	ut	
BT1	BT2	Set value
L	L	12x64xtosc
н	L	28x64xtosc
L	Η	64x64xtosc
Н	Н	116x64xtosc

#### <Stretcher Gain >

Inp	ut	
ST1	ST2	Set value
L	L	x 1
I	┙	x 2
┙	Η	x 4
I	Н	x 8

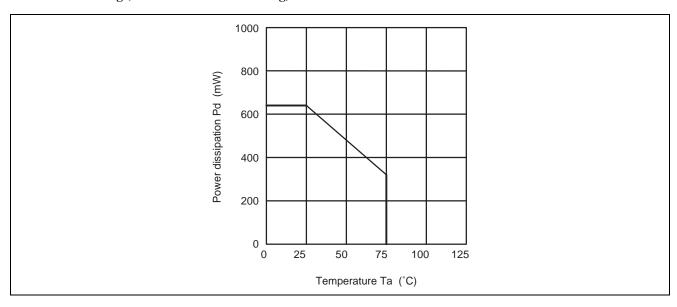
Note: tosc: oscillation period of resonator

# **Absolute Maximum Ratings**

 $(Ta = -20 \text{ to } 75^{\circ}\text{C}, \text{ unless otherwise noted})$ 

Symbol	Parameter	<b>Test Conditions</b>	Ratings	Unit	
Vcc	Supply voltage		-0.3 to +9.0	V	
lo	Output current	OUT1, OUT2	−5 to +5	mA	
pd	Power dissipation	Ta = 25°C	630	mW	
Topr	Operating temperature		-20 to +75	°C	
Tstg	Storage temperature		-40 to 125	°C	

#### **Thermal Derating (Absolute Maximum Rating)**



# **Recommended operating conditions**

 $(Ta = -20 \text{ to } +75^{\circ}C)$ 

Symbol	Parameter	Conditions	Ratings	Unit	
V <sub>CC</sub>	Supply voltage		4.0 to 9.0	V	
$V_{INPin}$	Pin input voltage		0 to Vcc	V	
V <sub>INPOT</sub>	POT input voltage		0.2 to 2.0	V	
I <sub>OVreg</sub>	Vreg output current		-2 to 0	mA	
V <sub>OROP3</sub>	ROP3 output voltage rage		0.2 to 2.0	V	

# **Electrical Characteristics**

 $(V_{CC} = 5V, Ta = 25^{\circ}C, unless otherwise noted)$ 

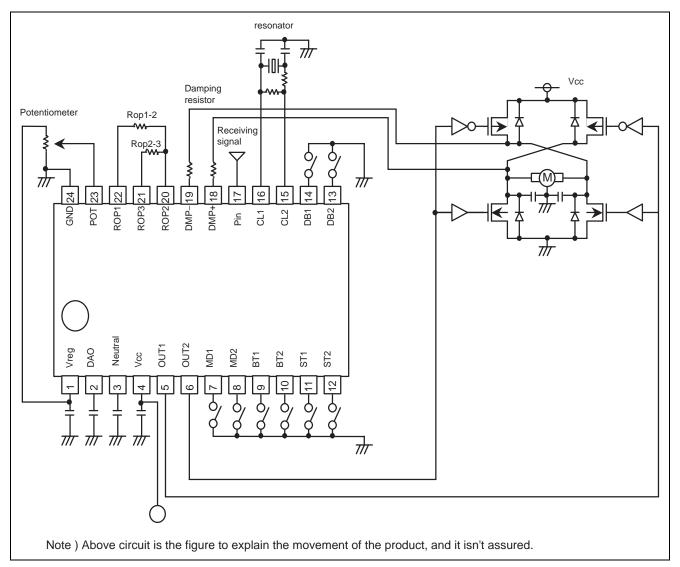
Symbol	Parameters	Test conditions	Measure Pin	Limits			Unit
				Min	Тур	Max	=
I <sub>CC1</sub>	Supply current 1	Vcc1 = 9 V	Vcc	_	19	28	mA
		OUT 1 and OUT2 are OFF.					
I <sub>CC2</sub>	Supply current 2	Vcc1 = 5 V	Vcc	_	15	21	mA
		OUT 1 and OUT2 are OFF.					
V <sub>OFF</sub>	Output voltage		Vcc	2.80	3.02	3.30	V
V <sub>ON</sub>	Output voltage		Vcc	2.93	3.15	3.43	V
V <sub>reg1</sub>	Regulated voltage 1	lo = 0 μA	Vreg	2.02	2.15	2.28	V
$V_{reg2}$	Regulated voltage 2	lo = -2 mA	Vreg	2.00	2.14	2.27	V
dV <sub>reg</sub>	Supply Voltage	Vreg1 standard. lo = 0 μA	Vreg	_	0.11	0.25	% / V
	dependence of Vreg	Vcc = 4 to 9 (V)					
V <sub>Neutral</sub>	Natural Voltage	V <sub>Neutral</sub> = 0.6 Vreg	Natural	1.21	1.29	1.37	V
I <sub>OH</sub>	"H" Output current	Vo = 0.7 V	OUT1	-2.4	-1.54	-1.1	mA
			OUT2				
V <sub>OL</sub>	"L" Output voltage	lo = 1 mA	OUT1	0.02	0.1	0.3	mV
			OUT2				
V <sub>OF1</sub>	amp 1offset voltage	POT = 1.1 V	Rop1	-10	1	10	mV
I <sub>IN amp1</sub>	amp 1input current	POT = 0.2 V	POT	-1	0.3	0	μΑ
V <sub>OH amp1</sub>	"H" output voltage	lo = -250 μA, POT = 2 V	Rop1	1.97	2.00	2.02	V
V <sub>OL amp1</sub>	"L" output voltage	lo = 250 μA, POT = 0.2 V	Rop1	0.18	0.20	0.23	V
G <sub>V1ROP3</sub>	Voltage gain 1	Damping resistors = 300 K $\Omega$	Rop3	-41	-37.5	-35	dB
	(from amp2 to amp3)	Rop2 to $3 = 12 \text{ K}\Omega$					
		DMP- = 5 V, DMP+ = 0 V					
G <sub>V2ROP3</sub>	Voltage gain 2	Damping resistors = 300 K $\Omega$	Rop3	<u>41</u>	-37.5	-35	dB
	(from amp2 to amp3)	Rop2 to $3 = 12 \text{ K}\Omega$					
		DMP-=5 V, DMP+=5 V					
$V_{IHPin}$	"H" intput voltage of		Pin	1.5	_	Vcc	V
	Pin						

# **Timing Requirement Conditions**

(Vcc = 5 V,  $Ta = 25^{\circ}\text{C}$ , unless otherwise noted)

Symbol	Parameters	Conditions	(,,,,	Limits	,		Unit
				Min	Тур.	Max	<del>-</del>
f <sub>CLK</sub>	Clock frequency			_	4.915	_	MHz
T <sub>wh (Pin)</sub>	Pin "H" pulse width	f <sub>CLK</sub> = 4.915 MHz		782	_	2187	μS

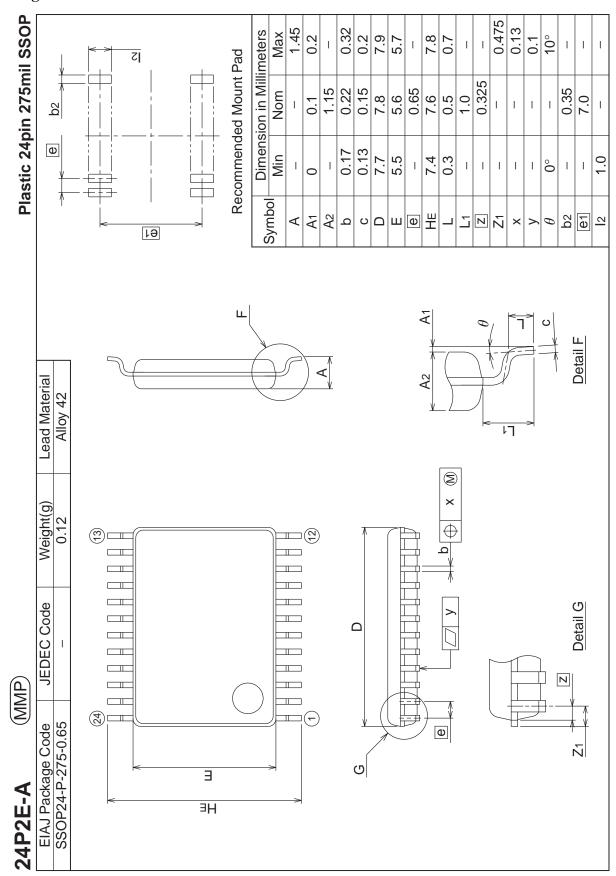
#### **Application Example**



Notes: Be careful of handing because 1 to 4 pin and 17, 23 pin break easily to other pins.

Renesas Technology corp. doesn't assume that responsibility when damage if to originate in the description mistake of these data arises to the customer though the information mentioned in these data was examined carefully to expect accuracy.

# **Package Dimension**



Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

The party in a survival circula designs; and the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.

2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.

3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.

The information described here may contain technical inaccuracies or typographical errors.

Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss resident product product of the responsibility of the information of the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).

4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.

5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances i

- use.

  6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.

  7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.

  Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.

  8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



**RENESAS SALES OFFICES** 

http://www.renesas.com

Renesas Technology America, Inc. 450 Holger Way, San Jose, CA 95134-1368, U.S.A Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH Dornacher Str. 3, D-85622 Feldkirchen, Germany Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd. 7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd. FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd. 26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632 Tel: <65> 6213-0200, Fax: <65> 6278-8001

L			