RENESAS HAF1004(L), HAF1004(S)

Silicon P Channel MOS FET Series Power Switching

REJ03G0028-0500Z (Previous ADE-208-629B (Z)) Rev.5.00 2003.04.29

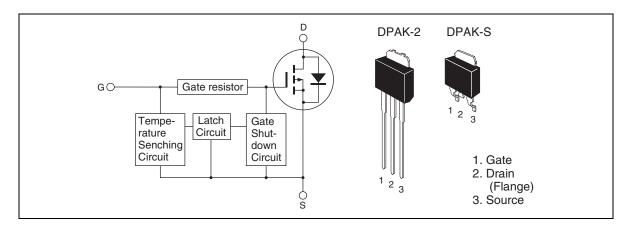
Description

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Logic level operation to (-4 to -6 V Gate drive)
- High endurance capability against to the shut-down circuit
- Built-in the over temperature shut-down circuit
- Latch type shut down operation (need 0 voltage recovery)

Outline



Absolute Maximum Ratings

 $(Ta = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	-60	V
Gate to source voltage	V _{GSS}	–16	V
Gate to source voltage	V _{GSS}	2.5	V
Drain current	I _D	-5	А
Drain peak current	I _{D (pulse)} Note1	-10	А
Body-drain diode reverse drain current	I _{DR}	-5	А
Cannel dissipation	Pch Note2	20	W
Cannel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. $PW \le 0\mu s$, duty cycle $\le 1\%$

2. Value at Ta = 25°C

Typical Operation Characteristics

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Input voltage	V _{IH}	-3.5	_	_	V	
	V _{IL}	_	_	-1.2	V	
Input current (Gate non shut down)	I _{IH1}		_	-100	μA	Vi = -8 V, V _{DS} = 0
	I _{IH2}	_	_	-50	μΑ	Vi = -3.5 V, V _{DS} = 0
	IIL	_	_	–1	μΑ	Vi = -1.2 V, V _{DS} = 0
Input current (Gate shut down)	I _{IH(sd)1}	_	-0.8		mA	Vi = -8 V, V _{DS} = 0
	I _{IH(sd)2}	—	-0.35	_	mA	Vi = -3.5 V, V _{DS} = 0
Shut down temperature	Tsd		175	_	°C	Cannel temperature
Gate operation voltage	Vop	-3.5	_	–12	V	

Electrical Characteristics

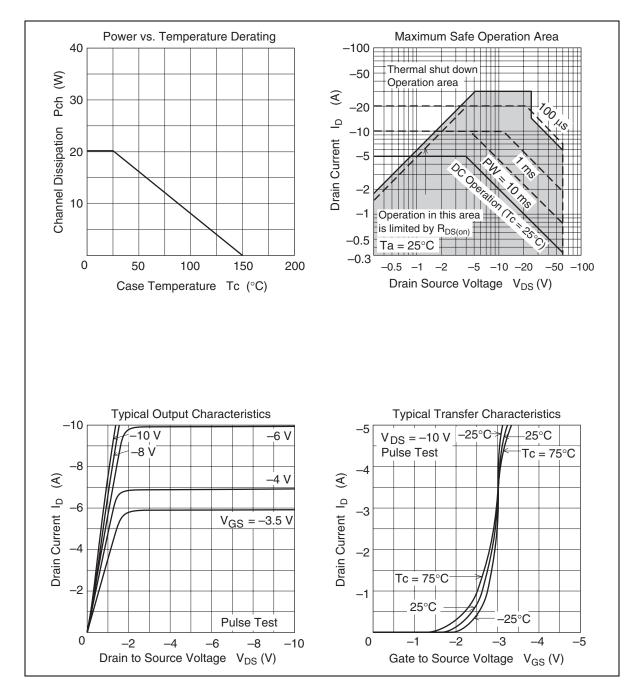
 $(Ta = 25^{\circ}C)$

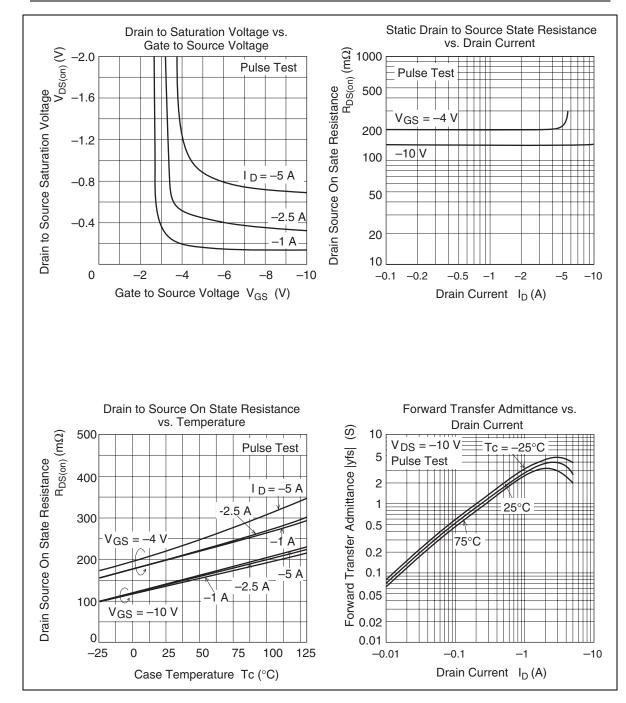
Item	Symbol	Vin	Тур	Max	Unit	Test Conditions	
Drain current	I _{D1}	4		_	А	V_{GS} = -3.5 V, V_{DS} = -2 V	
Drain current	I _{D2}	_		-10	mA	V_{GS} = -1.2 V, V_{DS} = -2 V	
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60		_	V	I _D = -10 mA, V _{GS} =0	
Gate to source breakdown voltage	$V_{(BR)GSS}$	-16		—	V	I _G = -800 μA, V _{DS} =0	
Gate to source breakdown voltage	$V_{(BR)GSS}$	2.5		—	V	I _G = 100 μA, V _{DS} =0	
Gate to source leak current	I _{GSS1}	_	_	-100	μA	V _{GS} = -8 V, V _{DS} =0	
	I _{GSS2}	_	_	-50	μA	V_{GS} = -3.5 V, V_{DS} =0	
	I _{GSS3}	_	_	–1	μA	V _{GS} = -1.2 V, V _{DS} =0	
	I _{GSS4}	_		100	μA	V _{GS} = 2.4 V, V _{DS} =0	
Input current (shut down)	I _{GS(OP)1}	_	-0.8	_	mA	V _{GS} = -8 V, V _{DS} =0	
	I _{GS(OP)2}	_	-0.35	—	mA	V_{GS} = -3.5 V, V_{DS} =0	
Zero gate voltage drain current	I _{DSS}	_		-10	μA	V_{DS} = -60 V, V_{GS} = 0	
Gate to source cut off voltage	$V_{GS(off)}$	-1.1		-2.25	V	V_{DS} = -10 V, I _D = -1 mA	
Forward transfer admittance	y _{fs}	2	4	—	S	I_D =–2.5 A, V_{DS} =–10 V ^{Note3}	
Static drain to source on state resistance	R _{DS(on)}	_	140	200	mΩ	$I_D = -2.5 \text{ A}, V_{GS} = -10 \text{ V}^{\text{Note3}}$	
Static drain to source on state resistance	R _{DS(on)}	_	200	340	mΩ	I_D = -2.5 A, V_{GS} = -4 V ^{Note3}	
Output capacitance	Coss	_	326	_	pF	V_{DS} = -10 V, V_{GS} =0, f = 1 MHz	
Turn-on delay time	t _{d(on)}	_	2	_	μs	$V_{GS} = -5 V, I_D = -2.5 A,$ $= R_L = 12 \Omega$	
Rise time	t _r	_	7.6	—	μs		
Turn off delay time	t _{d(off)}	_	3.2		μs		
Fall time	t _f	_	3.2	—	μs		
Body-drain diode forward voltage	V_{DF}	_	-0.9	—	V	$I_{F} = -5A, V_{GS} = 0$	
Body-drain diode reverse recovery time	t _{rr}	_	77	_	ns	$I_F = -5 \text{ A}, V_{GS} = 0$ diF/dt = 50 A/ μ s	
Over lord shut down	t _{os1}	_	8.4	_	ms	V_{GS} = -5 V, V_{DD} = -16 V	
operation time note4	t _{os2}	—	2.4	—	ms	V_{GS} = -5 V, V_{DD} = -24 V	

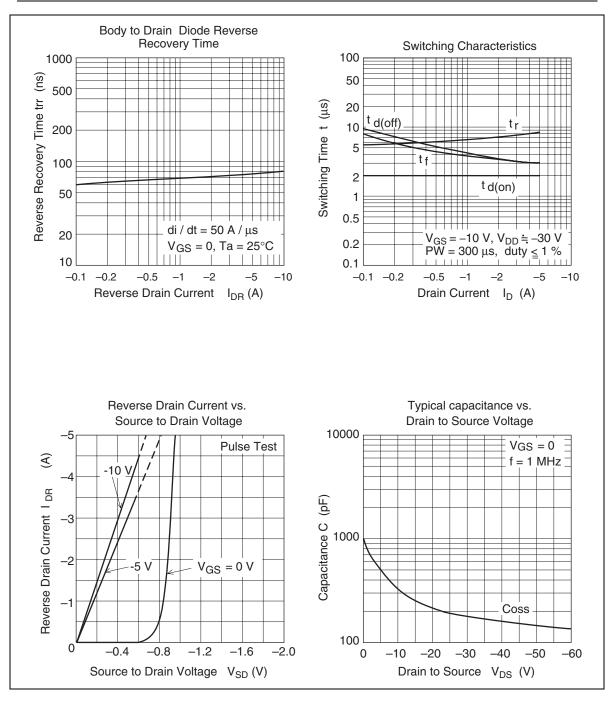
Notes: 3. Pulse test

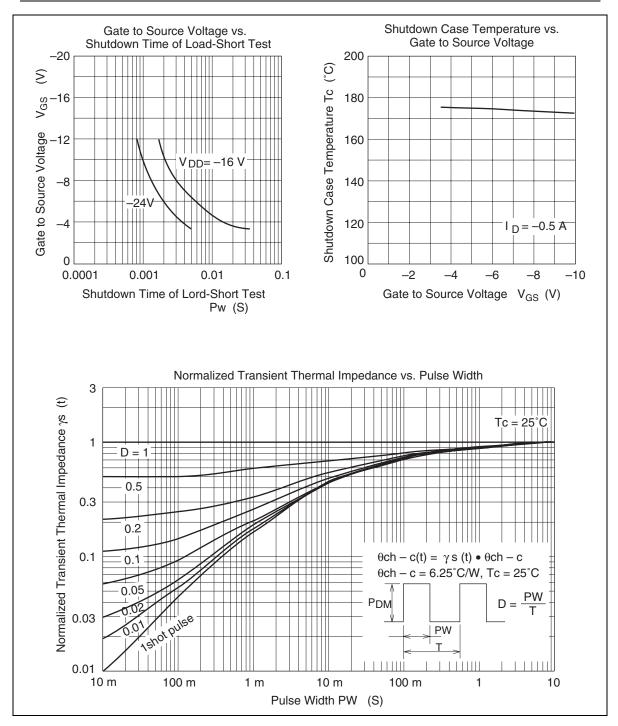
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Main Characteristics

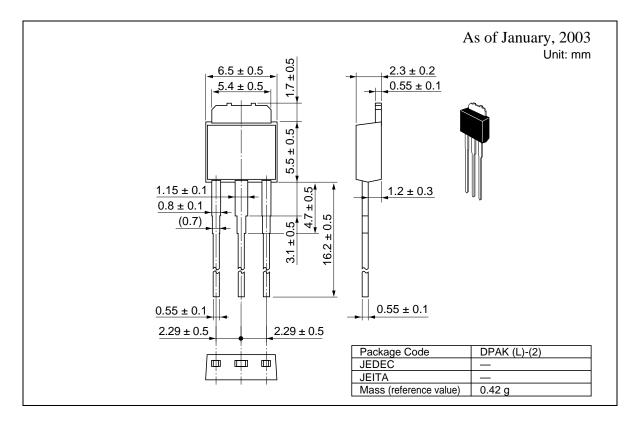


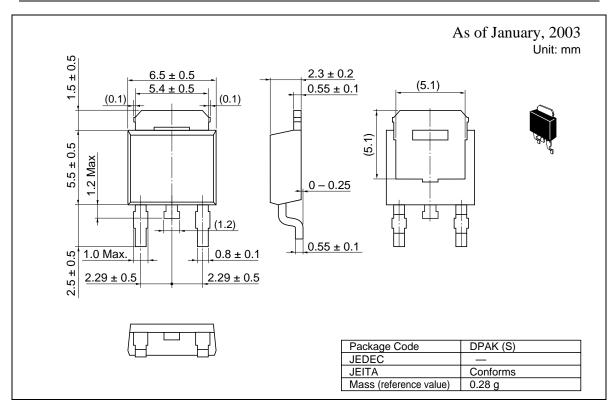






Package Dimensions





Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

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