

R1LV0416CBG-I Series

Wide Temperature Range Version
4M SRAM (256-kword × 16-bit)

REJ03C0259-0001
Preliminary
Rev.0.01
Jan.11.2005

Description

The R1LV0416CBG-I is a 4-Mbit static RAM organized 256-kword × 16-bit. The R1LV0416C-I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). The R1LV0416CBG-I Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has packaged in 48-pin CSP (0.75 mm ball pitch).

Features

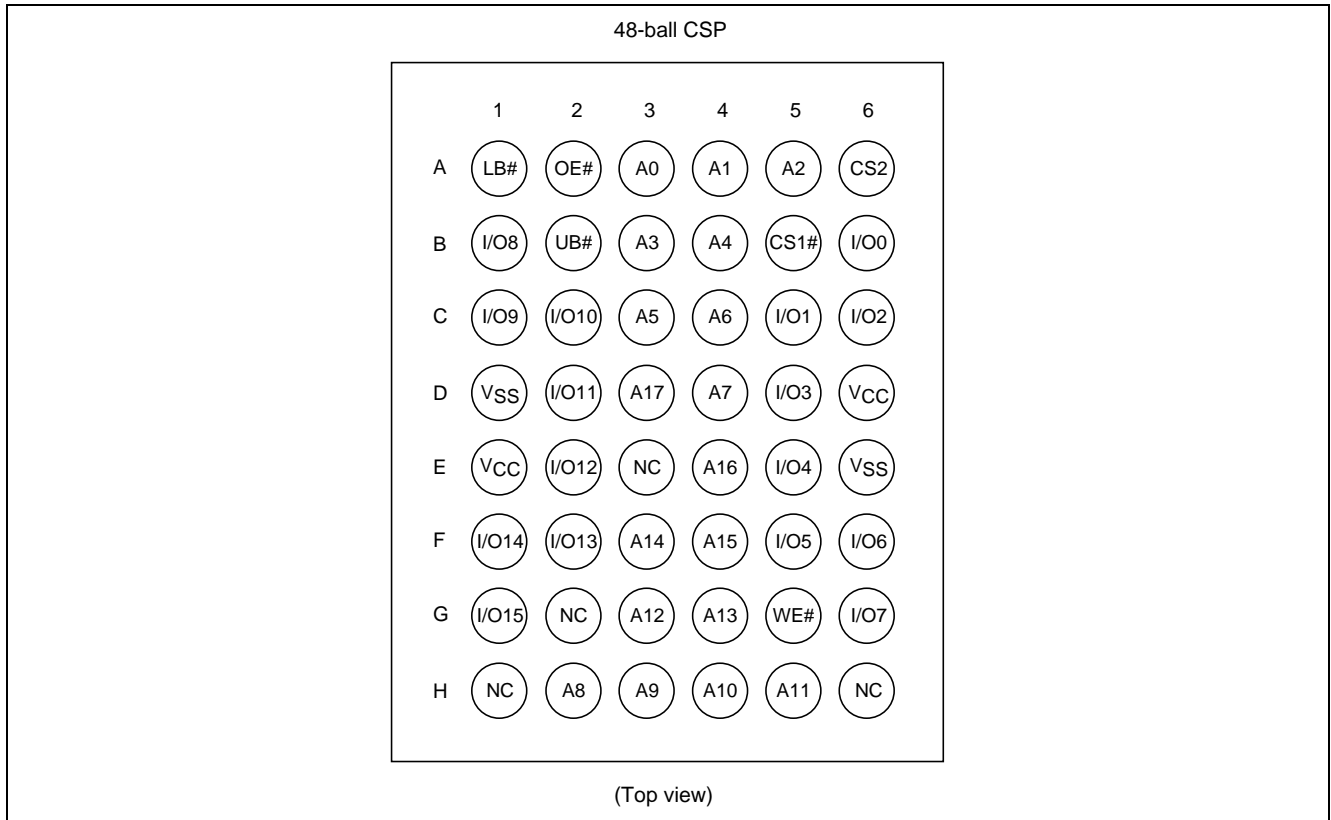
- Single 2.5 V and 3.0 V supply: 2.2 V to 3.6 V
- Fast access time: 55/70 ns (max)
- Power dissipation:
 - Active: 5.0 mW/MHz (typ) ($V_{CC} = 2.5$ V)
: 6.0 mW/MHz (typ) ($V_{CC} = 3.0$ V)
 - Standby: 1.25 μ W (typ) ($V_{CC} = 2.5$ V)
: 1.5 μ W (typ) ($V_{CC} = 3.0$ V)
- Completely static memory.
 - No clock or timing strobe required
- Access and cycle times are equal.
- Common data input and output.
 - Three state output
- Battery backup operation.
 - 2 chip selection for battery backup
- Temperature range: -40 to +85°C

Ordering Information

Type No.	Access time	Package
R1LV0416CBG-5SI	55 ns	48-ball CSP with 0.75 mm ball pitch (48FHH)
R1LV0416CBG-7LI	70 ns	

Preliminary: The specifications of this device are subject to change without notice. Please contact your nearest Renesas Technology's Sales Dept. regarding specifications.

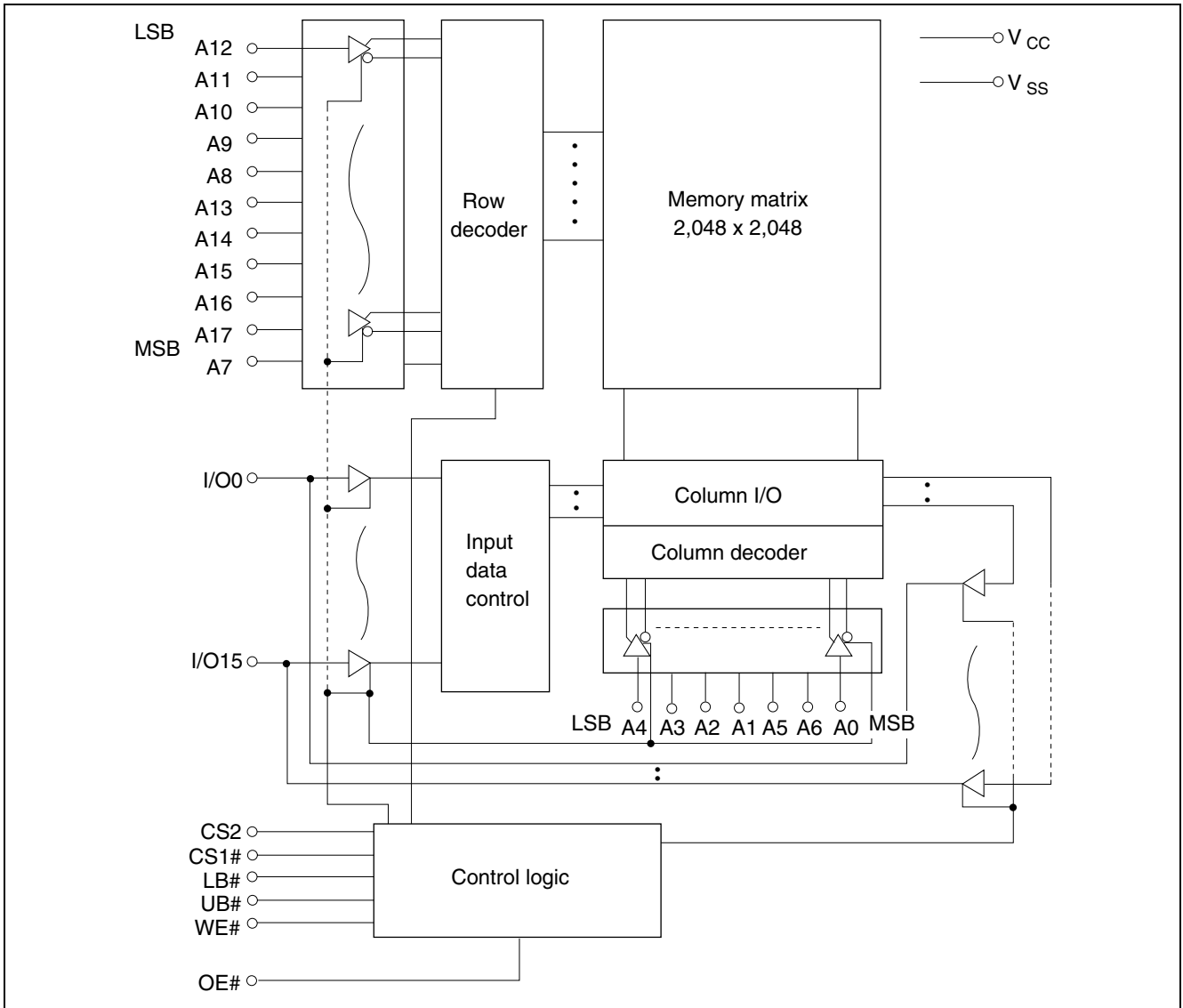
Pin Arrangement



Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
CS1# ($\overline{CS1}$)	Chip select 1
CS2	Chip select 2
WE# (\overline{WE})	Write enable
OE# (\overline{OE})	Output enable
LB# (\overline{LB})	Lower byte select
UB# (\overline{UB})	Upper byte select
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Block Diagram



Operation Table

CS1#	CS2	WE#	OE#	UB#	LB#	I/O0 to I/O7	I/O8 to I/O15	Operation
H	x	x	x	x	x	High-Z	High-Z	Standby
x	L	x	x	x	x	High-Z	High-Z	Standby
x	x	x	x	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	x	L	L	Din	Din	Write
L	H	L	x	H	L	Din	High-Z	Lower byte write
L	H	L	x	L	H	High-Z	Din	Upper byte write
L	H	H	H	x	x	High-Z	High-Z	Output disable

Note: H: V_{IH} , L: V_{IL} , x: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5* ¹ to $V_{CC} + 0.3$ * ²	V
Power dissipation	P_T	0.7	W
Operating temperature	T_{opr}	-40 to +85	°C
Storage temperature range	T_{stg}	-65 to +150	°C
Storage temperature range under bias	T_{bias}	-40 to +85	°C

Notes: 1. V_T min: -3.0 V for pulse half-width \leq 30 ns.

2. Maximum voltage is +4.6 V.

DC Operating Conditions

($T_a = -40$ to +85°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply voltage		V_{CC}	2.2	2.5/3.0	3.6	V	
		V_{SS}	0	0	0	V	
Input high voltage	$V_{CC} = 2.2$ V to 2.7 V	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	
	$V_{CC} = 2.7$ V to 3.6 V	V_{IH}	2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	$V_{CC} = 2.2$ V to 2.7 V	V_{IL}	-0.2	—	0.4	V	1
	$V_{CC} = 2.7$ V to 3.6 V	V_{IL}	-0.3	—	0.6	V	1

Note: 1. V_{IL} min: -3.0 V for pulse half-width \leq 30 ns.

DC Characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current			$ I_{LI} $	—	—	1	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current			$ I_{LO} $	—	—	1	μA	CS1# = V_{IH} or CS2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL} or LB# = UB# = V_{IH} , $V_{I/O} = V_{SS}$ to V_{CC}
Operating current			I_{CC}	—	5* ¹	20	mA	CS1# = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL} , $I_{I/O} = 0$ mA
Average operating current			I_{CC1}	—	8* ¹	25	mA	Min. cycle, duty = 100%, $I_{I/O} = 0$ mA, CS1# = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL}
			I_{CC2}	—	2* ¹	5	mA	Cycle time = 1 μs , duty = 100%, $I_{I/O} = 0$ mA, CS1# ≤ 0.2 V, CS2 $\geq V_{CC} - 0.2$ V $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby current			I_{SB}	—	0.1* ¹	0.3	mA	CS2 = V_{IL}
Standby current	-5SI	to +85°C	I_{SB1}	—	—	10	μA	$V_{in} \geq 0$ V (1) $0 \text{ V} \leq \text{CS2} \leq 0.2 \text{ V}$ or (2) CS1# $\geq V_{CC} - 0.2$ V, CS2 $\geq V_{CC} - 0.2$ V or (3) LB# = UB# $\geq V_{CC} - 0.2$ V, CS2 $\geq V_{CC} - 0.2$ V, CS1# ≤ 0.2 V
		to +70°C	I_{SB1}	—	—	8	μA	
		to +40°C	I_{SB1}	—	0.7* ²	3	μA	
		to +25°C	I_{SB1}	—	0.5* ¹	2.5	μA	
	-7LI	to +85°C	I_{SB1}	—	—	20	μA	
		to +70°C	I_{SB1}	—	—	16	μA	
		to +40°C	I_{SB1}	—	0.7* ²	10	μA	
Output high voltage	$V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$		V_{OH}	2.0	—	—	V	$I_{OH} = -0.5$ mA
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		V_{OH}	2.4	—	—	V	$I_{OH} = -1$ mA
	$V_{CC} = 2.2 \text{ V to } 3.6 \text{ V}$		V_{OH2}	$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100$ μA
Output low voltage	$V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$		V_{OL}	—	—	0.4	V	$I_{OL} = 0.5$ mA
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		V_{OL}	—	—	0.4	V	$I_{OL} = 2$ mA
	$V_{CC} = 2.2 \text{ V to } 3.6 \text{ V}$		V_{OL2}	—	—	0.2	V	$I_{OL} = 100$ μA

Notes: 1. Typical values are at $V_{CC} = 3.0$ V, $T_a = +25^\circ\text{C}$ and specified loading, and not guaranteed.

2. Typical values are at $V_{CC} = 3.0$ V, $T_a = +40^\circ\text{C}$ and specified loading, and not guaranteed.

Capacitance

($T_a = +25^\circ\text{C}$, $f = 1.0$ MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	8	pF	$V_{in} = 0$ V	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0$ V	1

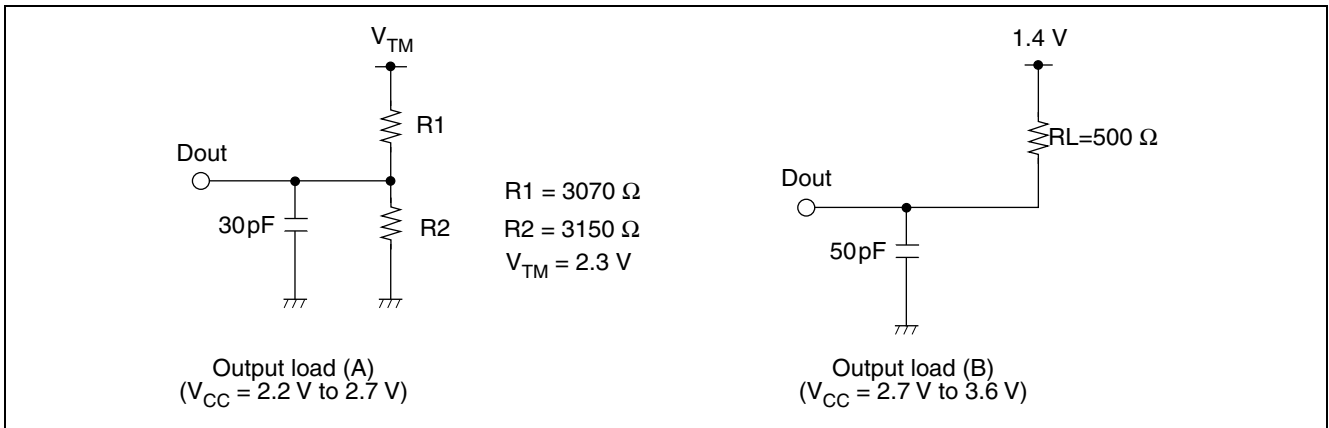
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.2$ V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: $V_{IL} = 0.4$ V, $V_{IH} = 2.2$ V ($V_{CC} = 2.2$ V to 2.7 V)
: $V_{IL} = 0.4$ V, $V_{IH} = 2.4$ V ($V_{CC} = 2.7$ V to 3.6 V)
- Input rise and fall time: 5 ns
- Input/output timing reference levels: 1.1 V ($V_{CC} = 2.2$ V to 2.7 V)
: 1.4 V ($V_{CC} = 2.7$ V to 3.6 V)
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	R1LV0416CBG-I				Unit	Notes
		-5SI		-7LI			
		Min	Max	Min	Max		
Read cycle time	t_{RC}	55	—	70	—	ns	
Address access time	t_{AA}	—	55	—	70	ns	
Chip select access time	t_{ACS1}	—	55	—	70	ns	
	t_{ACS2}	—	55	—	70	ns	
Output enable to output valid	t_{OE}	—	35	—	40	ns	
Output hold from address change	t_{OH}	10	—	10	—	ns	
LB#, UB# access time	t_{BA}	—	55	—	70	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	10	—	ns	2, 3
	t_{CLZ2}	10	—	10	—	ns	2, 3
LB#, UB# disable to low-Z	t_{BLZ}	5	—	5	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	0	25	ns	1, 2, 3
	t_{CHZ2}	0	20	0	25	ns	1, 2, 3
LB#, UB# disable to high-Z	t_{BHZ}	0	20	0	25	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1, 2, 3

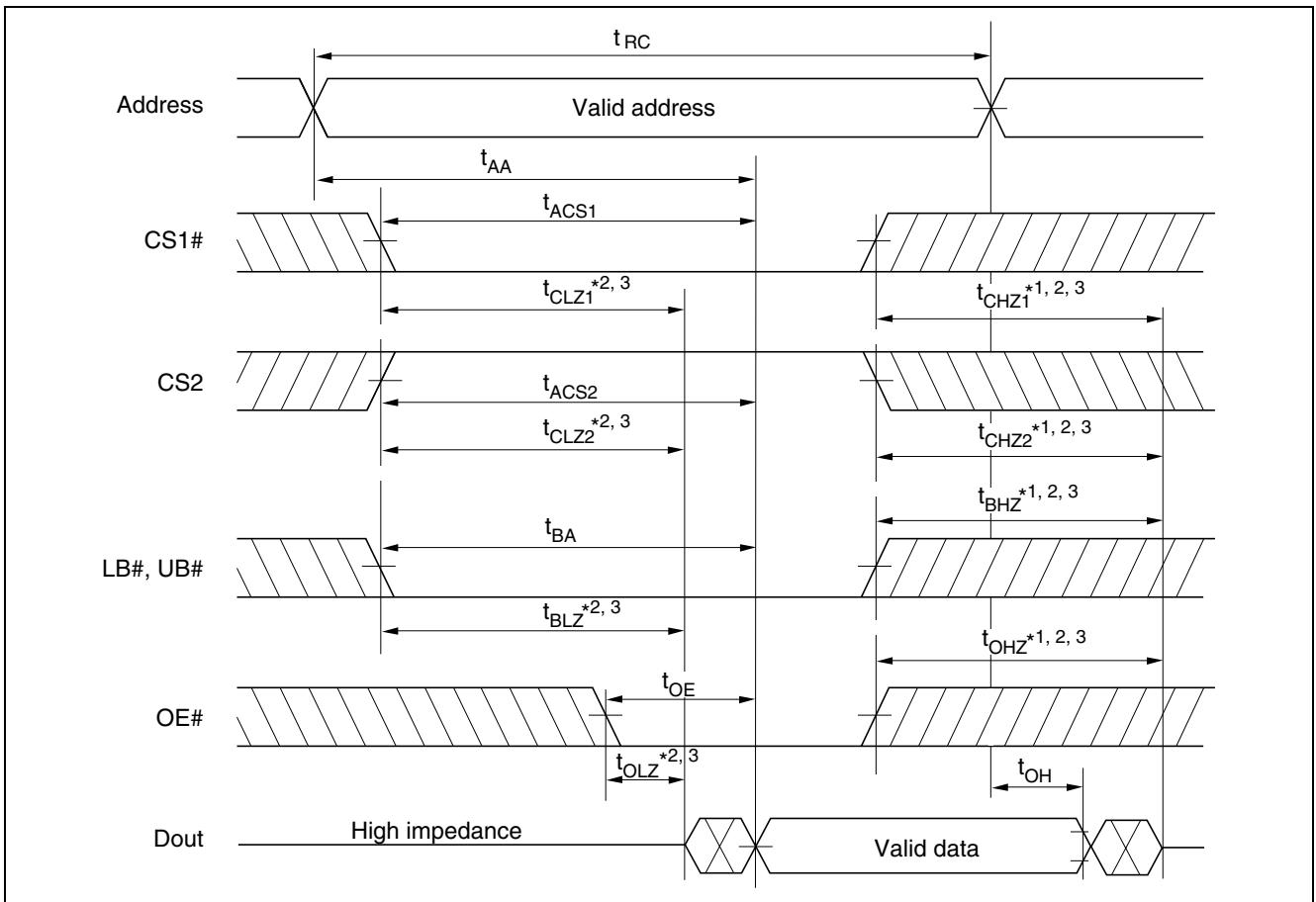
Write Cycle

Parameter	Symbol	R1LV0416CBG-I				Unit	Notes
		-5SI		-7LI			
		Min	Max	Min	Max		
Write cycle time	t_{WC}	55	—	70	—	ns	
Address valid to end of write	t_{AW}	50	—	60	—	ns	
Chip selection to end of write	t_{CW}	50	—	60	—	ns	5
Write pulse width	t_{WP}	40	—	50	—	ns	4
LB#, UB# valid to end of write	t_{BW}	50	—	55	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	6
Write recovery time	t_{WR}	0	—	0	—	ns	7
Data to write time overlap	t_{DW}	25	—	30	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1, 2, 3
Write to output in high-Z	t_{WHZ}	0	20	0	25	ns	1, 2

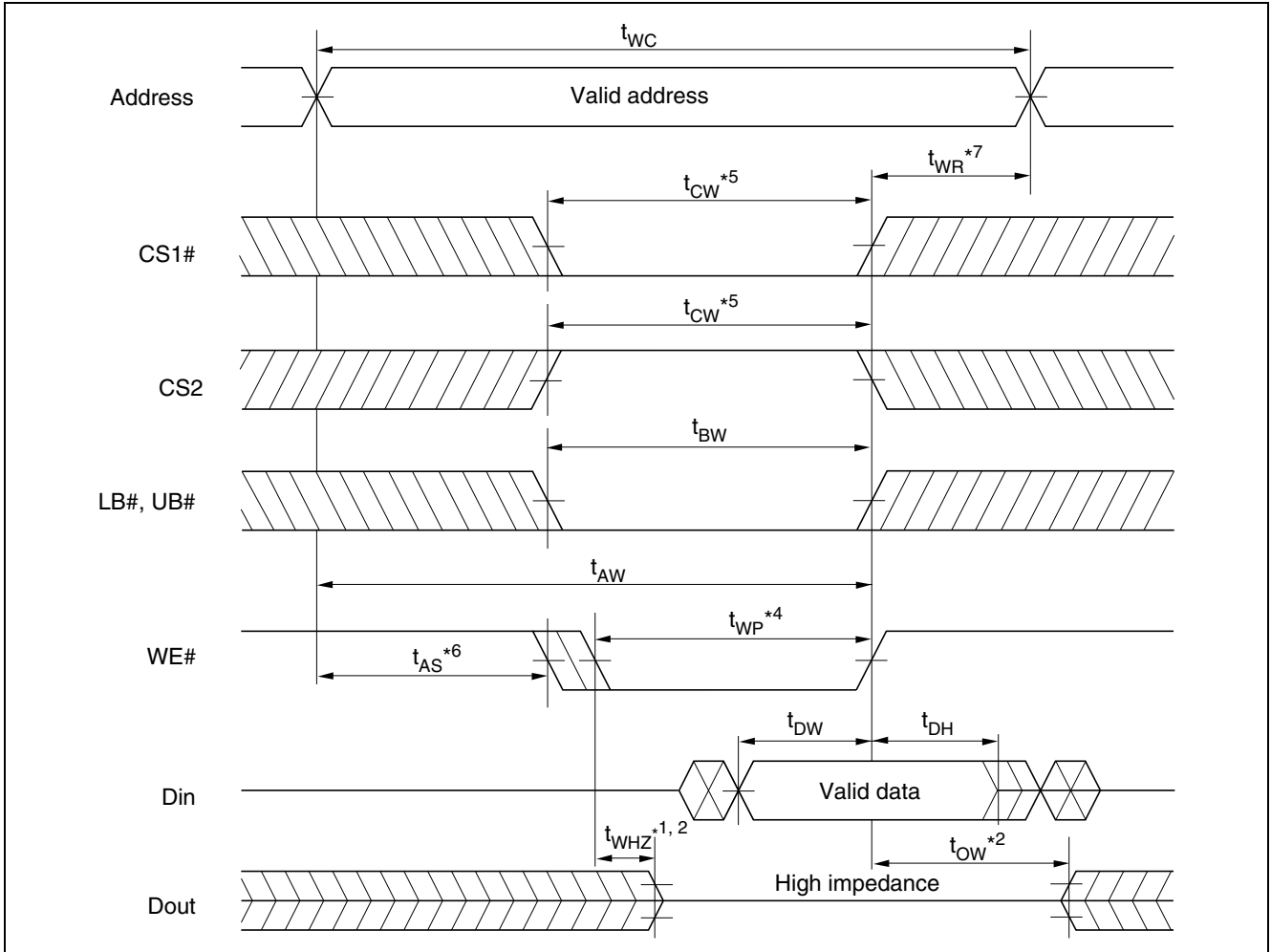
- Notes:
1. t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 2. This parameter is sampled and not 100% tested.
 3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.
 5. t_{CW} is measured from the later of CS1# going low or CS2 going high to the end of write.
 6. t_{AS} is measured from the address valid to the beginning of write.
 7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

Timing Waveform

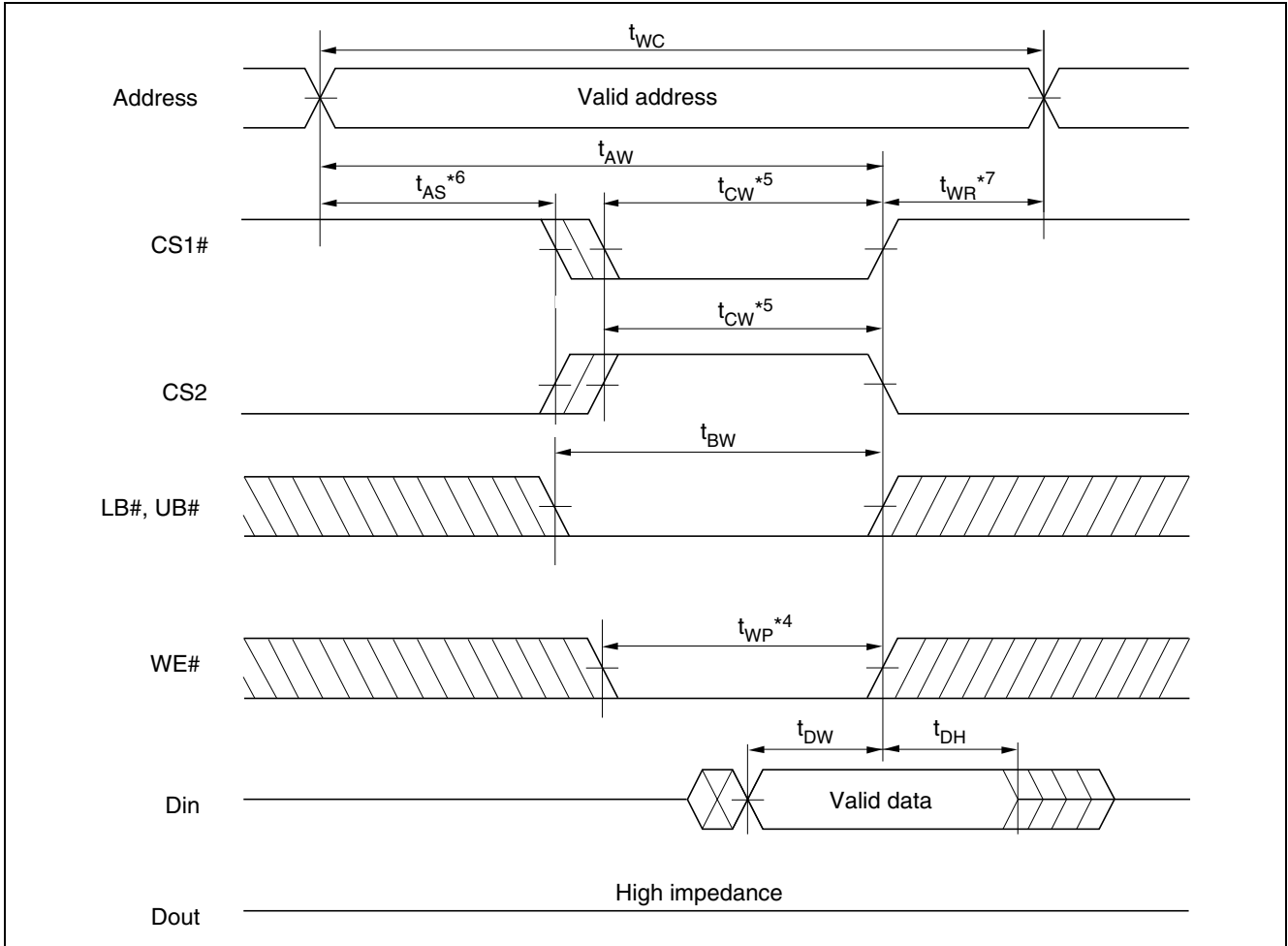
Read Timing Waveform (WE# = V_{IH})



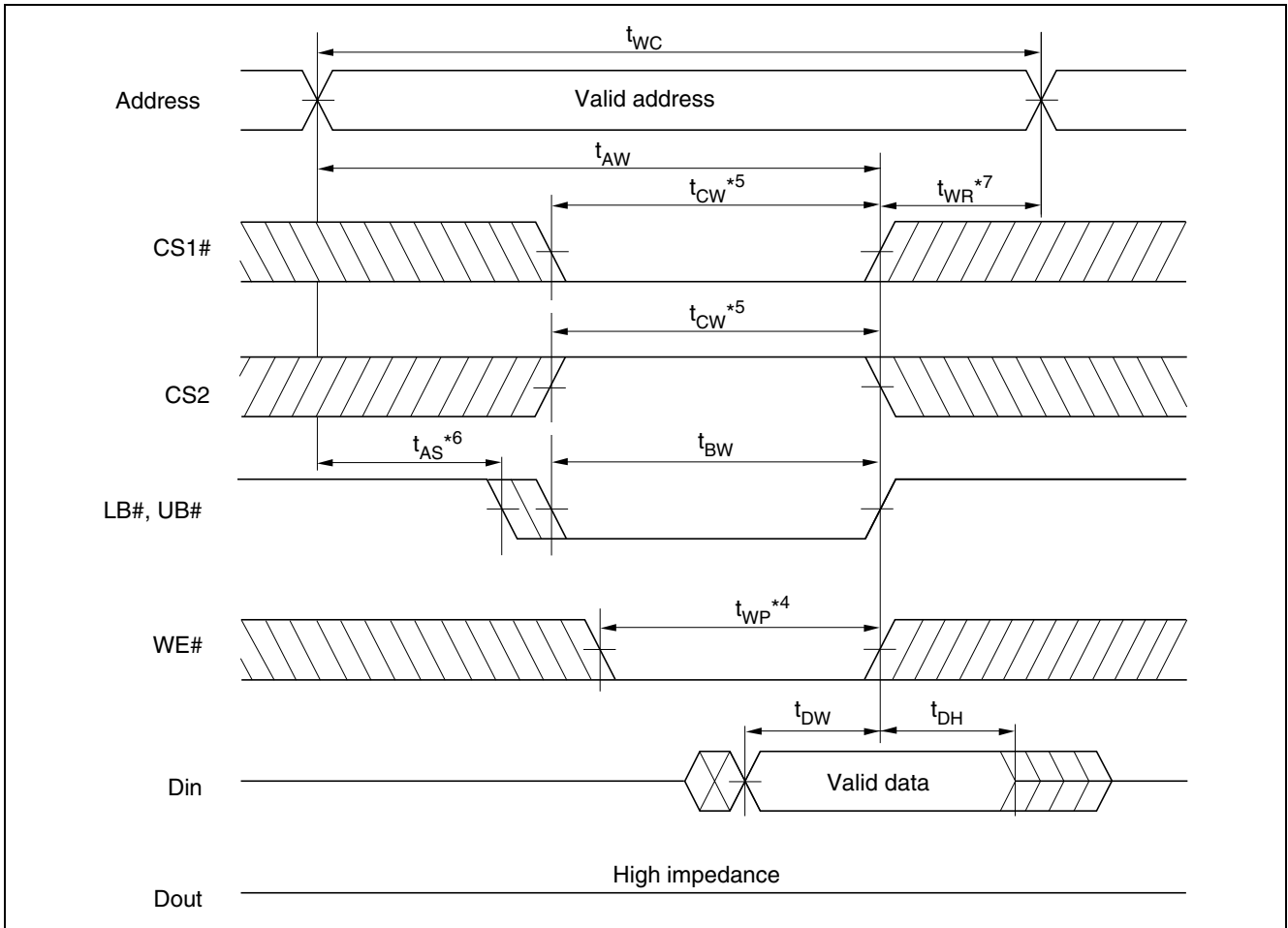
Write Timing Waveform (1) (WE# Clock)



Write Timing Waveform (2) (CS# Clock, OE# = V_{IH})



Write Timing Waveform (3) (LB#, UB# Clock, OE# = V_{IH})



Low V_{CC} Data Retention Characteristics

(Ta = -40 to +85°C)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions* ³
V_{CC} for data retention			V_{DR}	2.0	—	—	V	$V_{in} \geq 0V$ (1) $0V \leq CS2 \leq 0.2V$ or (2) $CS2 \geq V_{CC} - 0.2V$, $CS1\# \geq V_{CC} - 0.2V$ or (3) $LB\# = UB\# \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$, $CS1\# \leq 0.2V$
Data retention current	-5SI	to +85°C	I_{CCDR}	—	—	10	μA	$V_{CC} = 3.0V$, $V_{in} \geq 0V$ (1) $0V \leq CS2 \leq 0.2V$ or (2) $CS2 \geq V_{CC} - 0.2V$, $CS1\# \geq V_{CC} - 0.2V$ or (3) $LB\# = UB\# \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$, $CS1\# \leq 0.2V$
		to +70°C	I_{CCDR}	—	—	8	μA	
		to +40°C	I_{CCDR}	—	0.7* ²	3	μA	
		to +25°C	I_{CCDR}	—	0.5* ¹	2.5	μA	
	-7LI	to +85°C	I_{CCDR}	—	—	20	μA	
		to +70°C	I_{CCDR}	—	—	16	μA	
		to +40°C	I_{CCDR}	—	0.7* ²	10	μA	
		to +25°C	I_{CCDR}	—	0.5* ¹	10	μA	
Chip deselect to data retention time			t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time			t_R	t_{RC} * ⁴	—	—	ns	

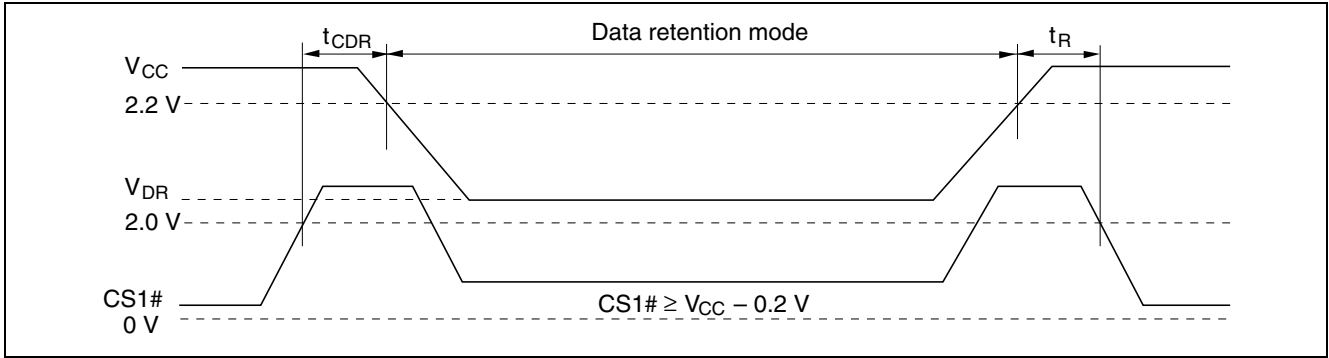
Notes: 1. Typical values are at $V_{CC} = 3.0V$, $T_a = +25^\circ C$ and specified loading, and not guaranteed.

2. Typical values are at $V_{CC} = 3.0V$, $T_a = +40^\circ C$ and specified loading, and not guaranteed.

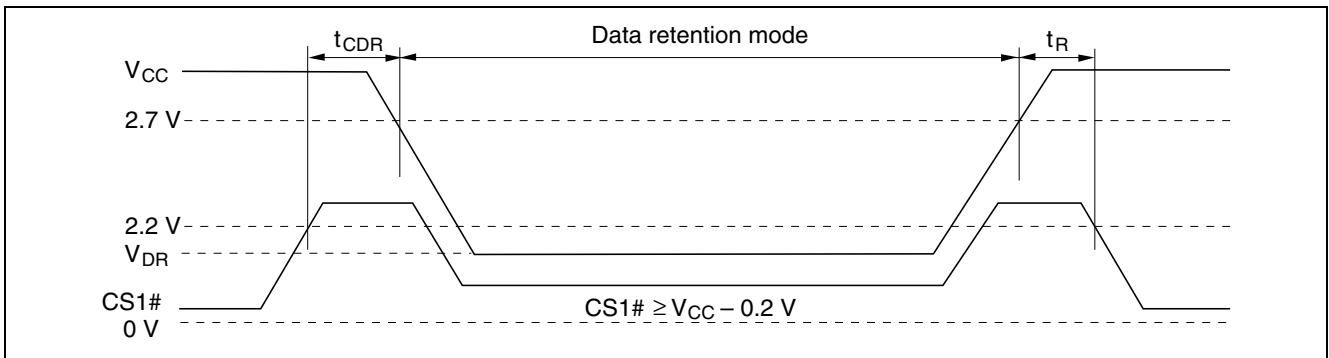
3. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB#, UB# buffer and Din buffer. If CS2 controls data retention mode, V_{in} levels (address, WE#, OE#, CS1#, LB#, UB#, I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be $CS2 \geq V_{CC} - 0.2V$ or $0V \leq CS2 \leq 0.2V$. The other input levels (address, WE#, OE#, LB#, UB#, I/O) can be in the high impedance state.

4. t_{RC} = read cycle time.

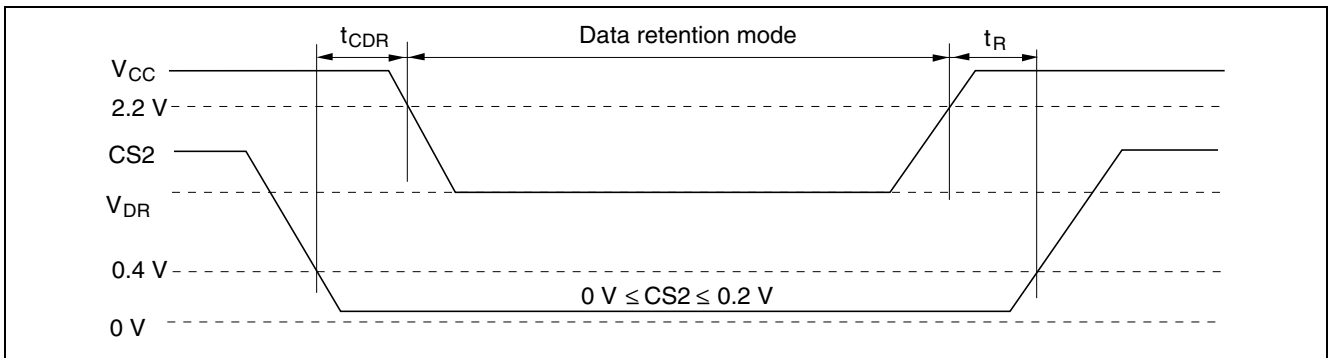
Low V_{CC} Data Retention Timing Waveform (1) (CS1# Controlled) ($V_{CC} = 2.2\text{ V to } 2.7\text{ V}$)



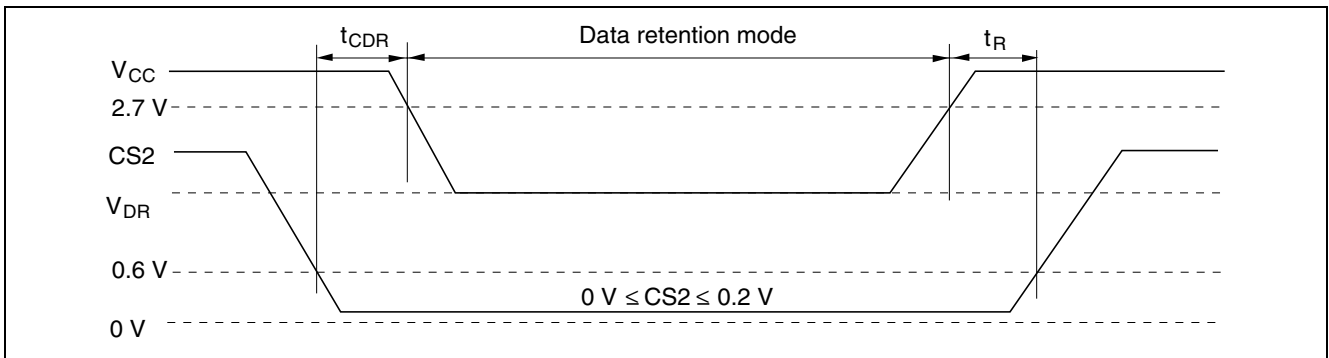
Low V_{CC} Data Retention Timing Waveform (2) (CS1# Controlled) ($V_{CC} = 2.7\text{ V to } 3.6\text{ V}$)



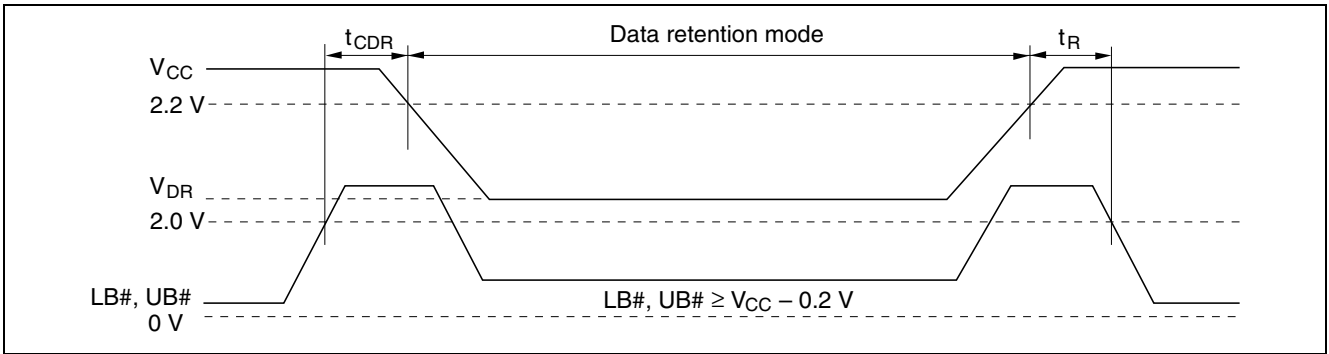
Low V_{CC} Data Retention Timing Waveform (3) (CS2 Controlled) ($V_{CC} = 2.2\text{ V to } 2.7\text{ V}$)



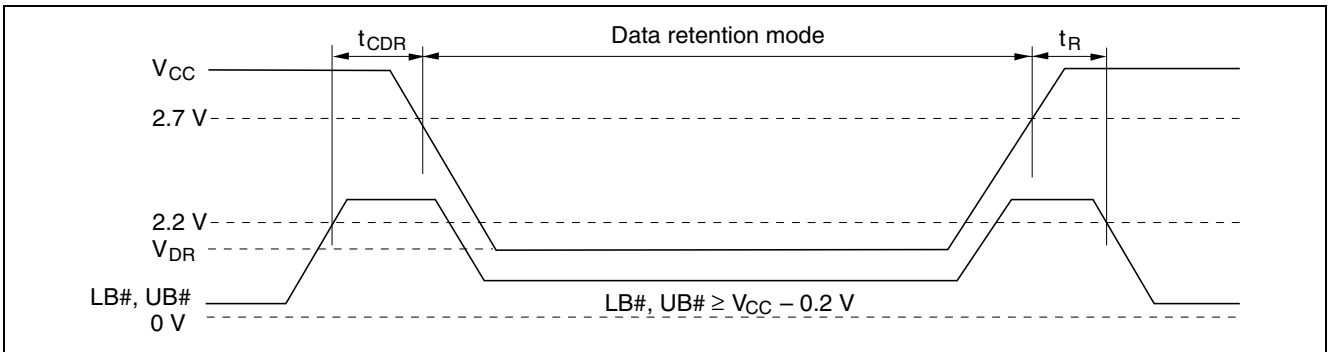
Low V_{CC} Data Retention Timing Waveform (4) (CS2 Controlled) ($V_{CC} = 2.7\text{ V to } 3.6\text{ V}$)



Low V_{CC} Data Retention Timing Waveform (5) (LB#, UB# Controlled) ($V_{CC} = 2.2\text{ V to }2.7\text{ V}$)



Low V_{CC} Data Retention Timing Waveform (6) (LB#, UB# Controlled) ($V_{CC} = 2.7\text{ V to }3.6\text{ V}$)



Revision History	R1LV0416CBG-I Series
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Rev.	Date	Contents of Modification	
		Page	Description
0.01	Jan.11.2005	—	Initial issue

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