HA16150T/P

High-Speed Current Mode Push-Pull PWM Control IC

REJ03F0146-0200
(Previous: ADE-204-071A)
Rev.2.00
Jun 15, 2005

Description

The HA16150 is a high-speed current mode PWM control IC with push-pull dual outputs, suitable for high-reliability, high-efficiency, high-mounting-density isolated DC-DC converter and high-output AC-DC converter control.

The HA16150 can be used in various applications, including push-pull converters and half-bridge, double-forward, and single-forward applications.

The HA16150 incorporates 180-degree phase-inverted push-pull dual outputs, and directly drives a power MOS FET. Operation at a maximum of 1 MHz is possible on an oscillator reference frequency.

The package lineup comprises an ultra-thin surface-mount TSSOP-16 suitable for slim communication system modules, and a general-purpose insertion DILP-6 suitable for characteristics evaluation.

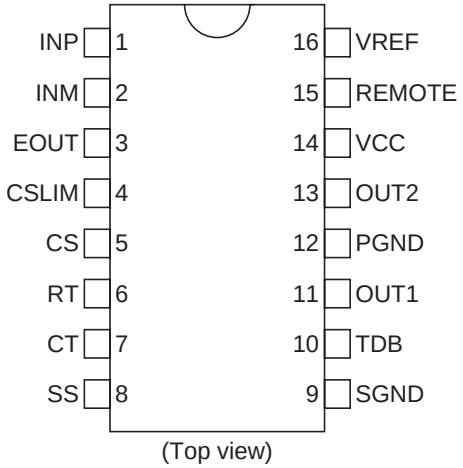
Features

<Maximum Ratings>
- Supply voltage Vcc: 20 V
- Peak output current Ipk-out: ±1.0 A
- Operating junction temperature Tjopr: –40°C to +125°C

<Electrical Characteristics>
- VREF output voltage VREF: 5.0 V ± 1%
- UVLO start threshold VH: 9.3 V ± 0.7 V
- UVLO shutdown threshold VL: 8.3 V ± 0.7 V
- Operating current Icc: 4 mA typ.
- Standby current Is: 150 µA typ.

<Functions>
- Soft start (one external timing capacitance)
- Remote on/off control
- Independent dead band time adjustment
- Current limiter adjustment (set drooping characteristic adjustment)
- Push-pull/single-end output switching
- Package lineup: TSSOP-16/DILP-16

Pin Arrangement

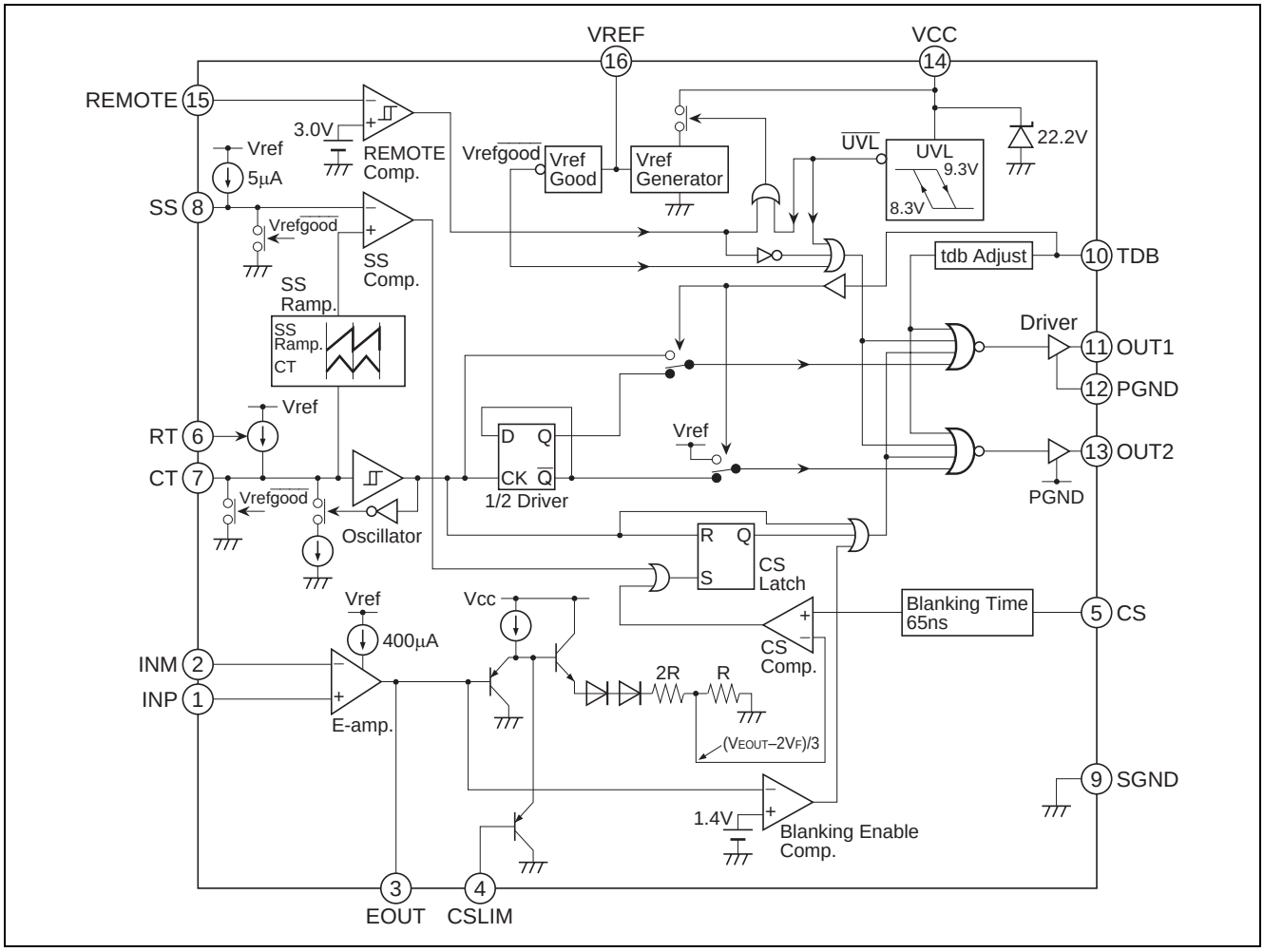


(Top view)

Pin Functions

Pin No.	Pin Name	Pin Functions
1	INP	Error amplifier non-inverted (+) input
2	INM	Error amplifier inverted (–) input
3	EOUT	Error amplifier output
4	CSLIM	Current limiter level adjustment
5	CS	Current sense signal input
6	RT	Operating frequency setting resistance connection
7	CT	Operating frequency setting capacitance connection
8	SS	Soft start time setting timing capacitance connection
9	SGND	Small signal system ground
10	TDB	Dead band time setting timing capacitance connection
11	OUT1	Power MOS FET driver output 1
12	PGND	Power system ground
13	OUT2	Power MOS FET driver output 2
14	VCC	Supply voltage
15	REMOTE	Remote on/off control
16	VREF	Reference voltage

Block Diagram



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Power supply voltage	Vcc	20	V	
OUT1 output current (peak)	Ipk-out1	±1.0	A	3
OUT2 output current (peak)	Ipk-out2	±1.0	A	3
OUT1 output current (DC)	Idc-out1	±0.1	A	
OUT2 output current (DC)	Idc-out2	±0.1	A	
OUT1 output voltage	Vout1	–0.3 to Vcc	V	
OUT2 output voltage	Vout2	–0.3 to Vcc	V	
INM pin voltage	Vinm	–0.3 to Vcc	V	
REMOTE pin voltage	Vremote	–0.3 to Vcc	V	
REMOTE pin current	Iremote	+0.2	mA	
INP pin voltage	Vinp	–0.3 to Vcc	V	
SS pin voltage	Vss	–0.3 to Vref	V	
RT pin voltage	Vrt	–0.3 to Vref	V	
RT pin current	Irt	–0.2	mA	
CT pin voltage	Vct	–0.3 to Vref	V	
CSLIM pin voltage	Vcslim	–0.3 to Vref	V	
EOUT pin voltage	Veout	–0.3 to Vref	V	
VREF pin voltage	Vref	–0.3 to Vref	V	
TDB pin voltage	Vtdb	–0.3 to Vref	V	
CS pin voltage	Vcs	–0.3 to Vref	V	
Operating junction temperature	Tj-opr	–40 to +125	°C	4
Storage temperature	Tstg	–55 to +150	°C	

Notes: 1. Rated voltages are with reference to the GND (SGND, PGND) pin.
2. For rated currents, inflow to the IC is indicated by (+), and outflow by (–).
3. Shows the transient current when driving a capacitive load.
4. HA16150T (TSSOP): θja = 250°C/W
This value is based on actual measurements on a 110% wiring density glass epoxy circuit board (55 mm × 45 mm × 1.6 mm).
HA16150P (DILP): θja = 124°C/W

Electrical Characteristics

(Ta = 25°C, Vcc = 12 V, Fosc = 100 kHz)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	Start threshold	VH	8.6	9.3	10.0	V	
	Shutdown threshold	VL	7.6	8.3	9.0	V	
	UVLO hysteresis	dV_{UVL}	0.7	1.0	1.3	V	
	Start-up current	Is	100	150	250	µA	Vcc = 8V
	Operating current	Icc	–	4	6	mA	Vinm = 1.0V, Vinp = 1.25V, Vcs = 0V
	Vcc zenner shunt voltage	Vz	21.2	22.2	23.2	V	Icc = 10mA
	Vz temperature stability	dVz/dTa	–	4.5	–	mV/°C	Icc = 10mA *1
VREF	Output voltage	Vref	4.95	5.0	5.05	V	Iref = –1mA
	Line regulation	Vref-line	–	5	20	mV	Vcc = 11V to 18V
	Load regulation	Vref-load	–	5	20	mV	Iref = –1mA to –20mA
	Temperature stability	dVref/dTa	–	80	–	ppm/°C	Ta = –40 to 125°C
Oscillator	Oscillator frequency	fosc	88	100	112	kHz	Measured at OUT1 and OUT2 RT = 27kΩ, CT = 1000pF
	Temperature stability	dfosc/dTa	–	±0.1	–	%/°C	Ta = –40 to 125°C *1
PWM Comparator	High voltage	Vth	–	3.0	–	V	DC *1
	Low voltage	Vtl	–	2.0	–	V	DC *1
	Differential voltage	dVt	–	1.0	–	V	DC *1
Error amplifier	Input bias current	Ifb	–1	–	+1	µA	
	Open loop gain	Av	–	70	–	dB	f = 1.0kHz *1
	EOUT sink current	Isnk-eout	–	3.0	–	mA	Veout = 1.1V *1
	EOUT source current	Isrc-eout	–	–0.4	–	mA	Veout = 3.0V *1
	Low voltage	Vol-eout	–	0.8	1.1	V	EOUT : Open
	High voltage	Voh-eout	4.7	5.0	–	V	EOUT : Open
Current sense	Voltage gain	Avcs	2.85	3.00	3.15	V/V	
	Delay to output	td-cs	–	150	230	ns	
	Leading edge blanking time	tbl	–	65	–	ns	*1
	Leading edge blanking disable voltage	Vbl-off	1.3	1.4	1.5	V	Measured pin : EOUT
Remote	On threshold voltage	Von	1.40	–	–	V	*1
	Off threshold voltage	Voff	–	–	3.00	V	*1
	Sink current	Iremote	60	90	120	µA	Vremote = 4V
Soft start	Source current	Iss	–7.0	–5.0	–3.0	µA	Vss = 1V

Note: 1. Reference values for design.

Electrical Characteristics (cont.)

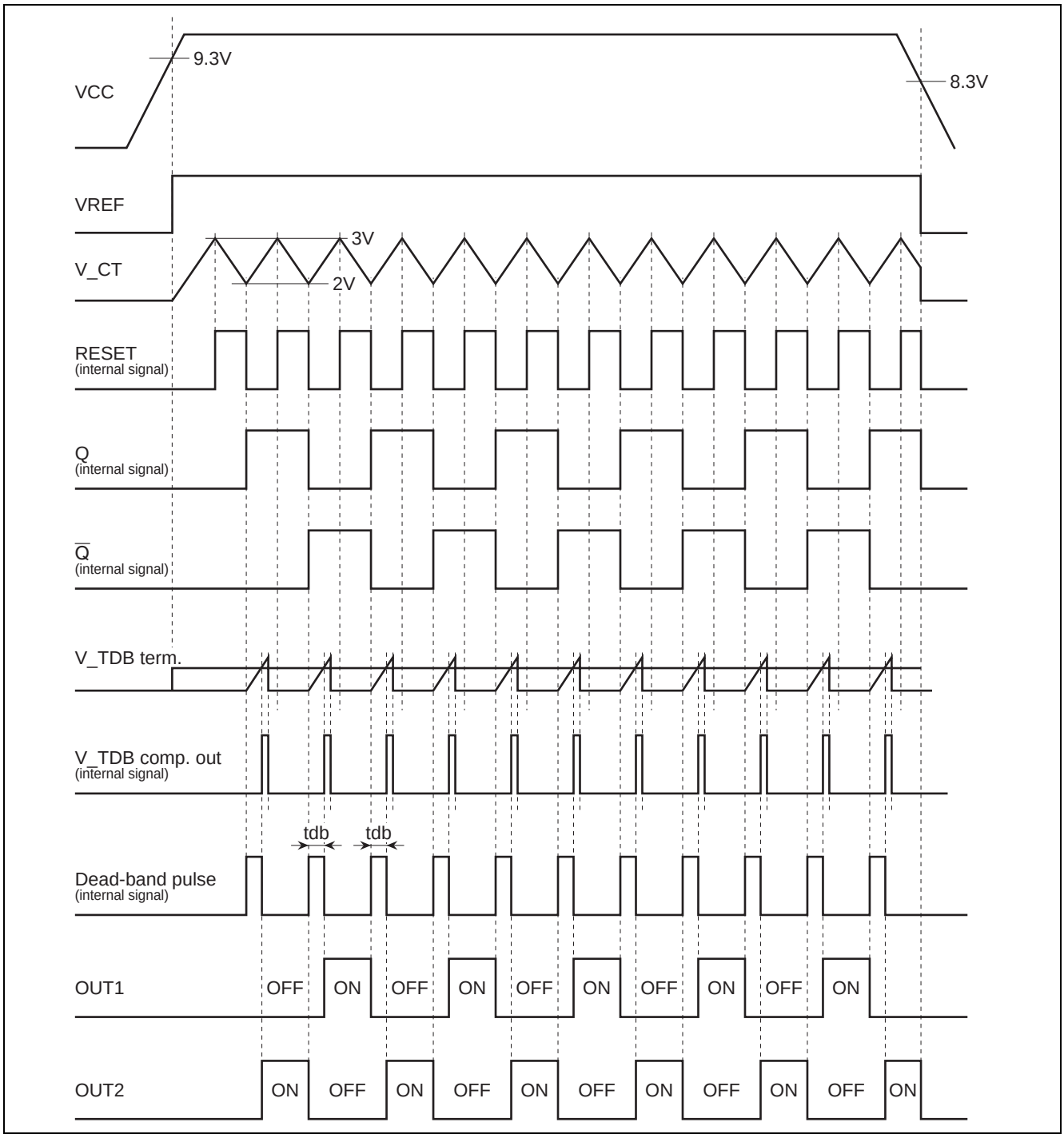
(Ta = 25°C, Vcc = 12 V, Fosc = 100 kHz)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
OUT1	Minimum duty cycle	Dmin-out1	–	–	0	%	Veout = 0V
	Maximum duty cycle	Dmax-out1	48	49	–	%	TDB : OPEN
	Rise time	tr-out1	–	30	65	ns	CL = 1000pF
	Fall time	tf-out1	–	30	65	ns	CL = 1000pF
	Low voltage	Vol1-out1	–	0.05	0.2	V	Iout = 20mA
		Vol2-out1	–	0.5	2.0	V	Iout = 200mA (pulse)
	High voltage	Voh1-out1	11.5	11.9	–	V	Iout = –20mA
		Voh2-out1	10.0	11.0	–	V	Iout = –200mA (pulse)
OUT2	Minimum duty cycle	Dmin-out2	–	–	0	%	Veout = 0V
	Maximum duty cycle	Dmax-out2	48	49	–	%	TDB : OPEN
	Rise time	tr-out2	–	30	65	ns	CL = 1000pF
	Fall time	tf-out2	–	30	65	ns	CL = 1000pF
	Low voltage	Vol1-out2	–	0.05	0.2	V	Iout = 20mA
		Vol2-out2	–	0.5	2.0	V	Iout = 200mA (pulse)
	High voltage	Voh1-out2	11.5	11.9	–	V	Iout = –20mA
		Voh2-out2	10.0	11.0	–	V	Iout = –200mA (pulse)
Dead-band time	Dead-band time	tdb0	–	60	–	ns	TDB : OPEN *1
		tdb	–	140	–	ns	Ctdb = 47pF *1

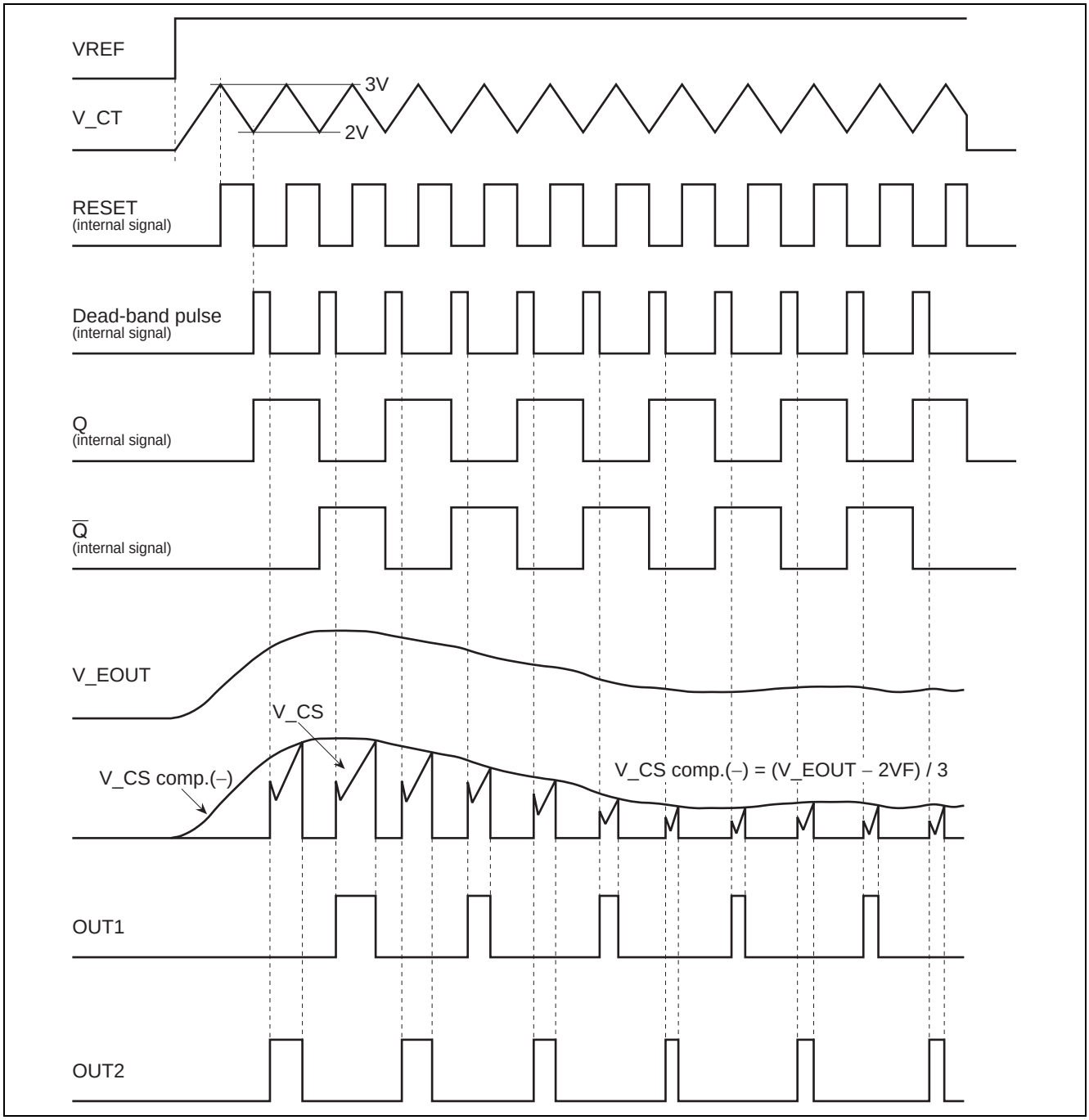
Note: 1. Reference values for design.

Timing Diagram

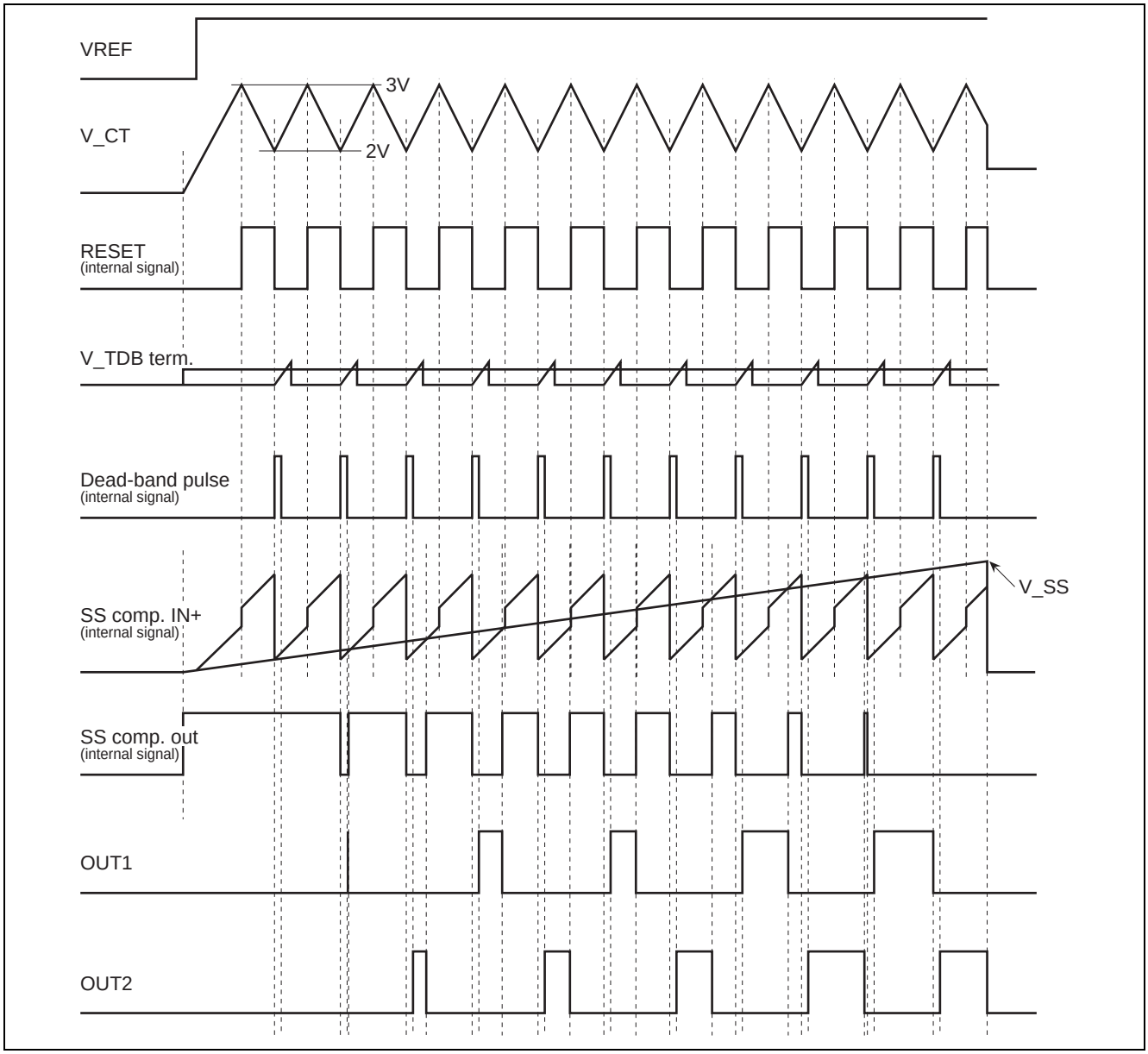
1. Start-up Timing



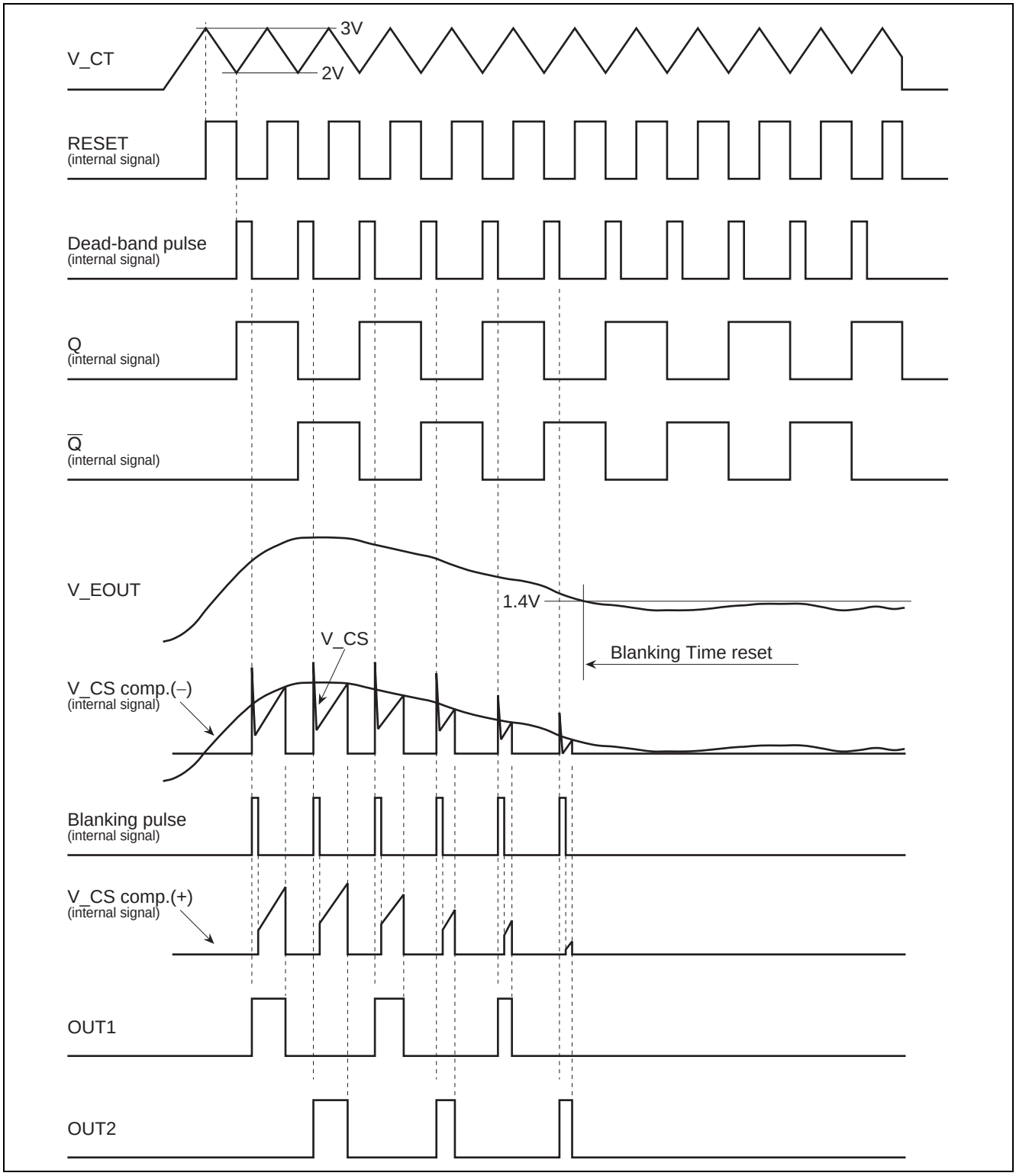
2. Current Sense



3. Soft Start

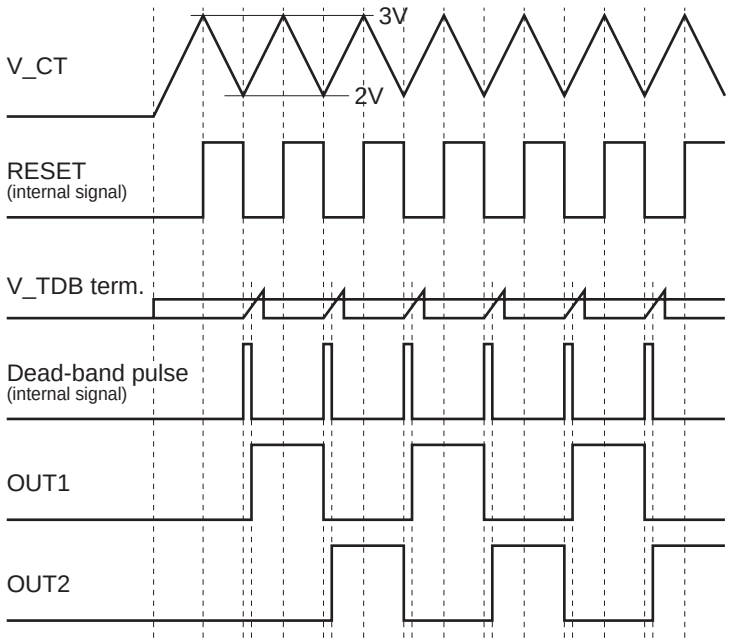

VREF
3V
V_CT
2V
RESET
(internal signal)
V_TDB term.
Dead-band pulse
(internal signal)
SS comp. IN+
(internal signal)
V_SS
SS comp. out
(internal signal)
OUT1
OUT2

4. Leading Edge Blanking

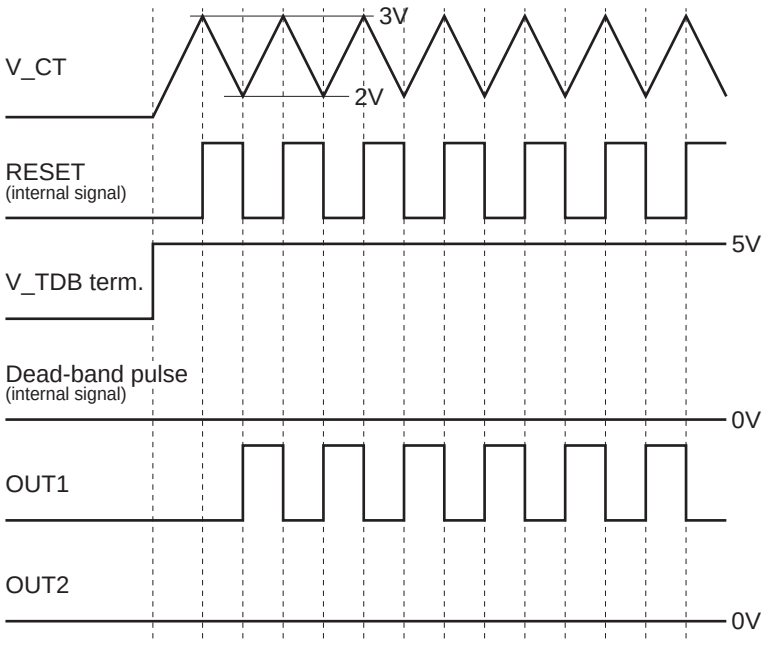


5. Push-Pull/Single-End Switching

(1) Push-pull operation: Leave the TDB pin open or connect a capacitance to GND



(2) Single-end operation: Perform pull-up connection of the TDB pin to the VREF pin



Functional Description

1. UVL Circuit

The UVL circuit monitors the Vcc voltage and halts operation of the IC in the event of a low voltage.

The voltage for detecting Vcc has a hysteresis characteristic, with 9.3 V as the start threshold and 8.3 V as the shutdown threshold.

When the IC has been halted by the UVL circuit, control is performed to fix driver circuit output low, halt VREF output and the oscillator, and reset the soft start circuit.

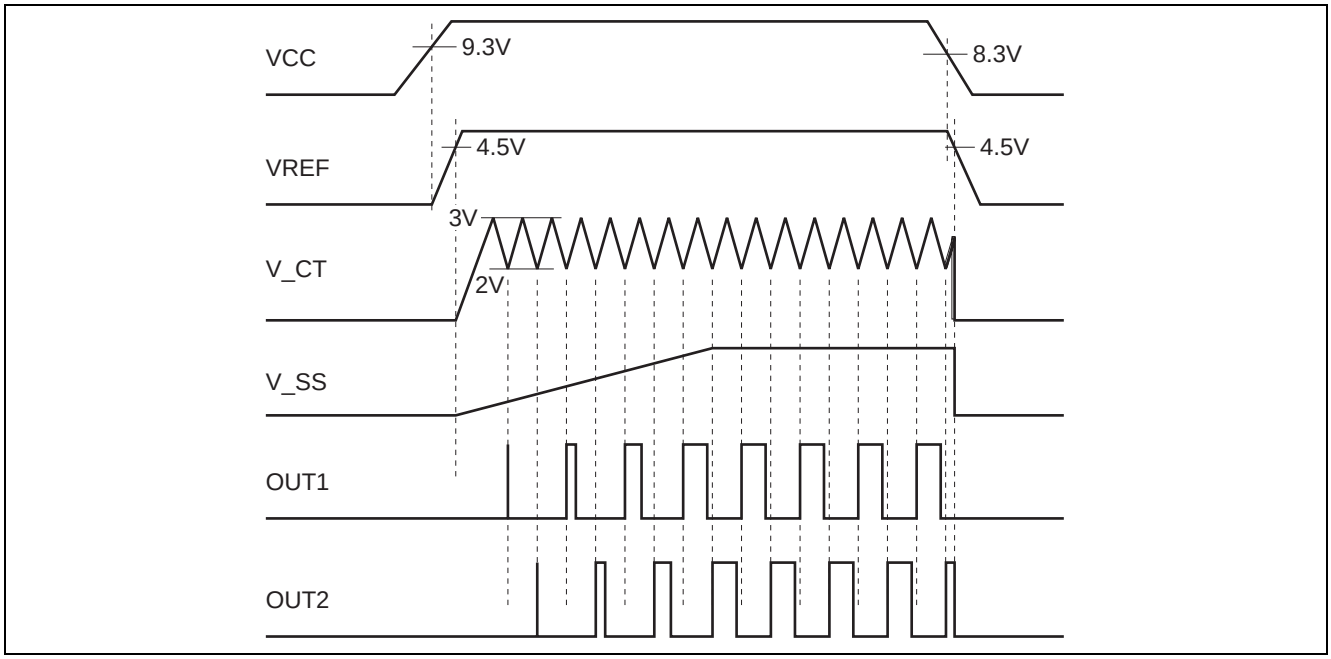


Figure 1

2. Remote ON/OFF Circuit

A remote on/off control function is incorporated, enabling the IC to be halted without cutting the supply voltage by pulling the REMOTE pin up to 3.0 V or higher.

This function halts VREF output and driver output.

At this time the IC enters Remote-OFF mode and IC current dissipation can be decreased. This function can thus be used for power management, etc.

When remote off control is performed, the soft start circuit is also reset, and therefore a soft start is effected when restarting, preventing overshoot.

If the remote on/off control function is not used, the REMOTE pin should be permanently pulled down to GND with a resistance of about 100 kΩ.

3. Soft Start Circuit

This function gradually increases the pulse width of the OUT pin from 0% duty at start-up to prevent a sudden increase in the pulse width that may cause problems such as transient stress on external parts or overshoot of the secondary-side output voltage.

The soft start time can easily be set with a single external capacitance.

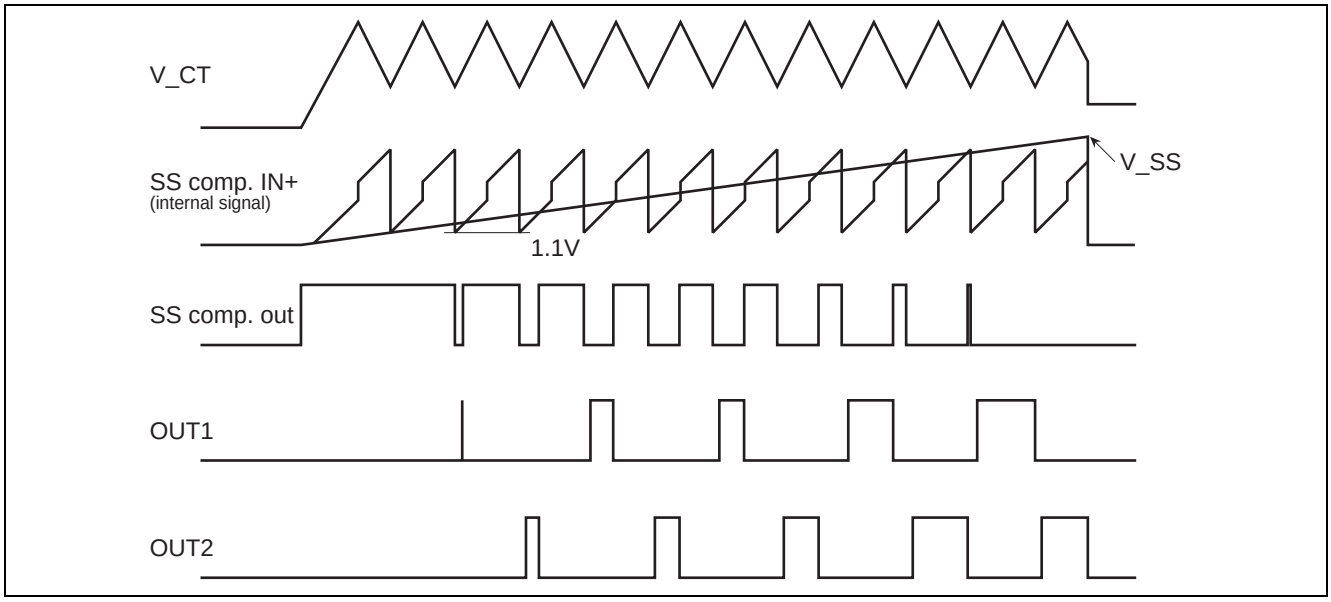


Figure 2

Soft start time tss is determined by SS pin connection capacitance Css and an internal constant, and can be estimated using the equation shown below.

Soft start time tss is the time until the first pulse is output to the driver output OUT pin after VREF starts up following UVLO release.

This is equivalent to the time until the SS pin voltage reaches IC-internal SS comparator reference voltage VTL (1.1 V), and can be calculated using the approximate equation shown below.

Soft start time tss when Css is 1000pF is given by the following equation.

$$tss = \frac{Css \times VTL}{Iss} = \frac{1000\ [pF] \times 1.1\ [V]}{5\ [\mu A]}$$
$$\approx 220\ [\mu s]$$

* Iss: SS pin source current, 5 μA typ.

4. Dead Band Generation Circuit

"Dead band" refers to the time when both push-pull dual outputs are off.

By setting the dead band time arbitrarily, it is possible to configure a system in which the dual outputs are never on simultaneously with respect to input and load variations.

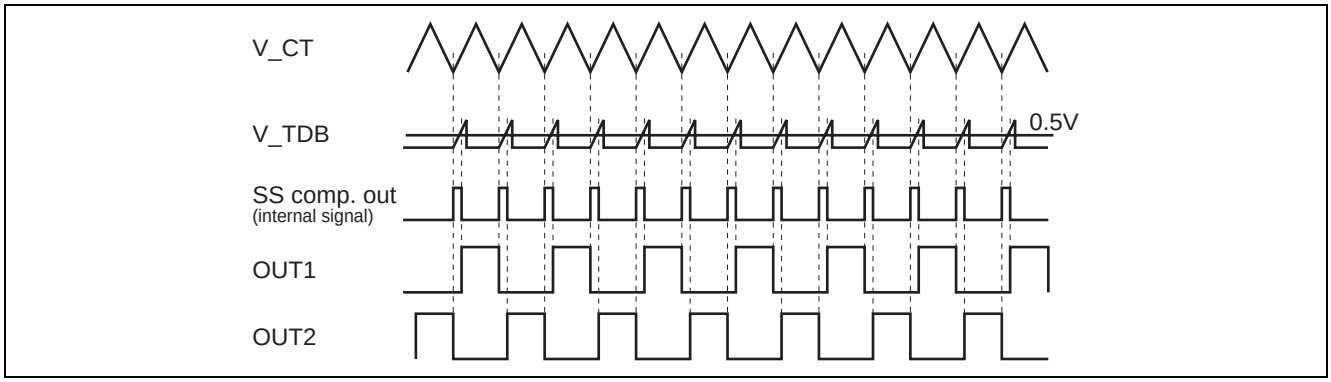


Figure 3

Dead band time tdb is determined by TDB pin connection capacitance Cdb and an internal constant, and can be estimated using the equation shown below.

Even when the TDB pin is open, the dead band time does not become zero due to floating capacitance of the IC package, etc. This dead band time is designated tdb0.

Dead band time tdb when Cdb is 47 pF is given by the following equation.

$$tdb = tdb0 + \frac{Cdb \times Vth}{Idb} = tdb0 + \frac{47\ [pF] \times 0.5\ [V]}{300\ [\mu A]}$$

$$= 60\ [ns] + 78\ [ns]$$

$$= 138\ [ns]$$

* Idb: TDB pin source current, 300 μA typ.
* Vth: IC-internal TDB comparator reference voltage

5. Operating Frequency

The operating frequency is adjusted by means of CT and RT.

Adjustment examples are shown in the graph below. This graph shows driver output operating frequencies. The reference operating frequency generated at the CT pin is twice the driver output frequency.

The driver output operating frequency can be estimated using the approximate equation shown below.

This is only an approximate equation, and the higher the frequency, the greater will be the degree of error of the approximate equation due to the effects of CT pin voltage overshoot, undershoot and so forth.

When the operating frequency is adjusted, it is essential to confirm operation using the actual system.

$$fosc = \frac{8}{3 \times CT \times RT} = \frac{8}{3 \times C6 \times R7}$$

$$= \frac{8}{3 \times 470\ [pF] \times 27\ [k\Omega]}$$

$$= 210\ [kHz]$$

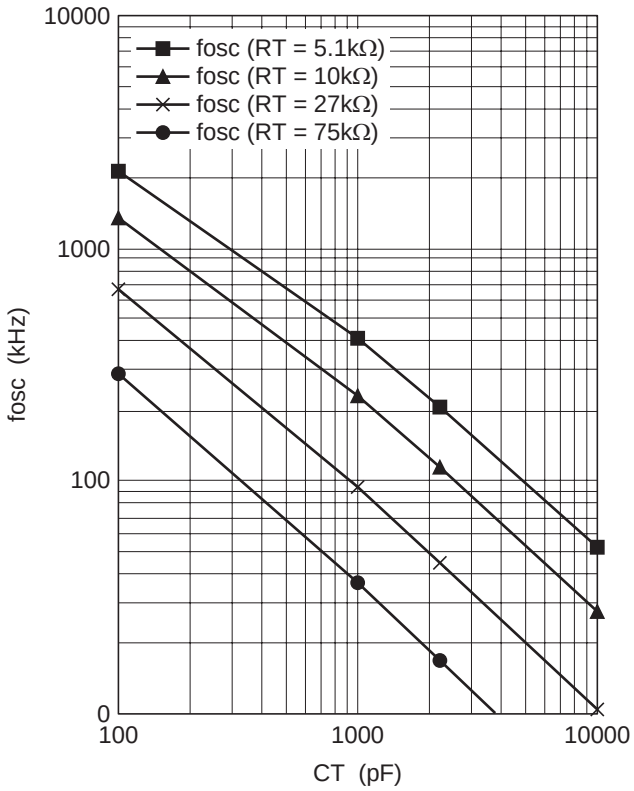


Figure 4

6. Current Limiter Level

The drooping characteristic of the power supply output can be adjusted by adjusting the CSLIM pin voltage.

For example, the drooping characteristic can easily be adjusted, as shown in the figure below, by setting VREF to a divided value with resistances R1 and R2 and connecting adjustment resistance Rx in parallel to R2.

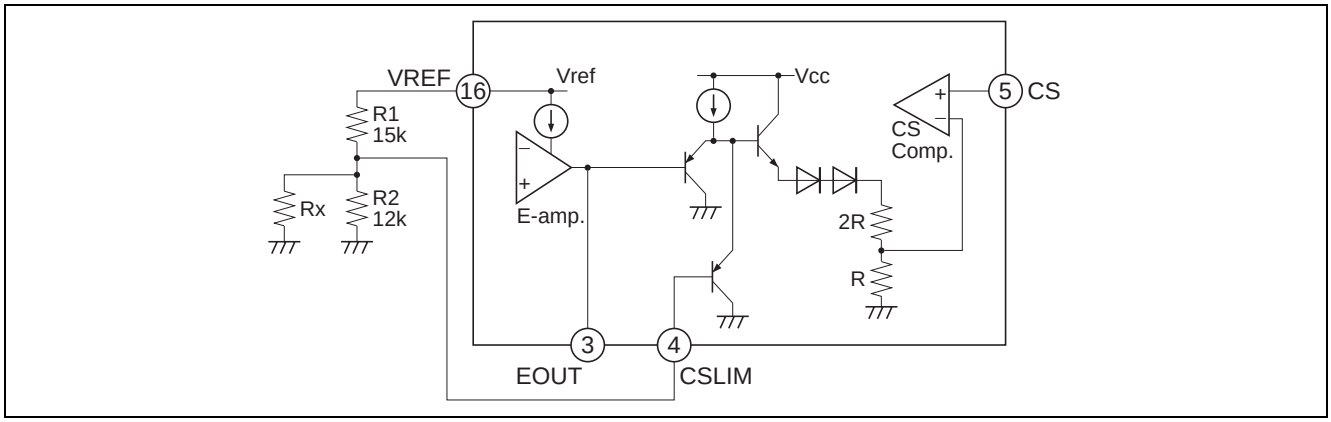


Figure 5 CSLIM Peripheral Circuit

The graph below shows examples of power supply output drooping characteristic adjustment in a push-pull converter.

As shown in this graph, the point at which the power supply output current limit begins to be applied can be adjusted by adjustment of the CSLIM pin voltage.

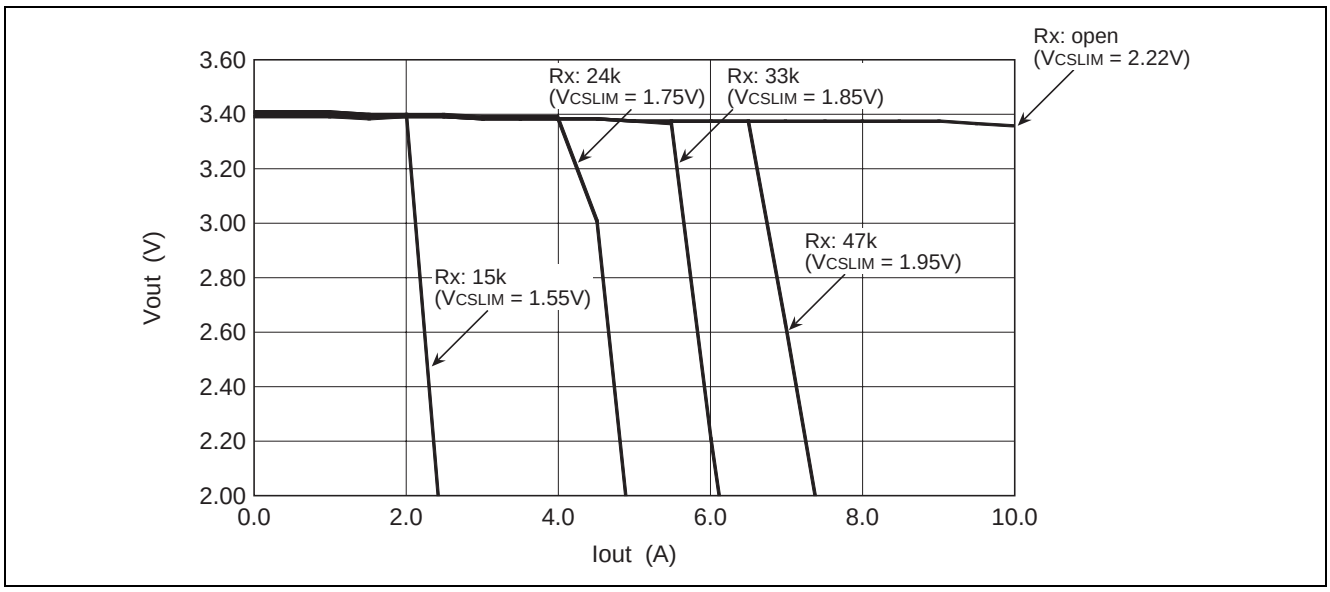
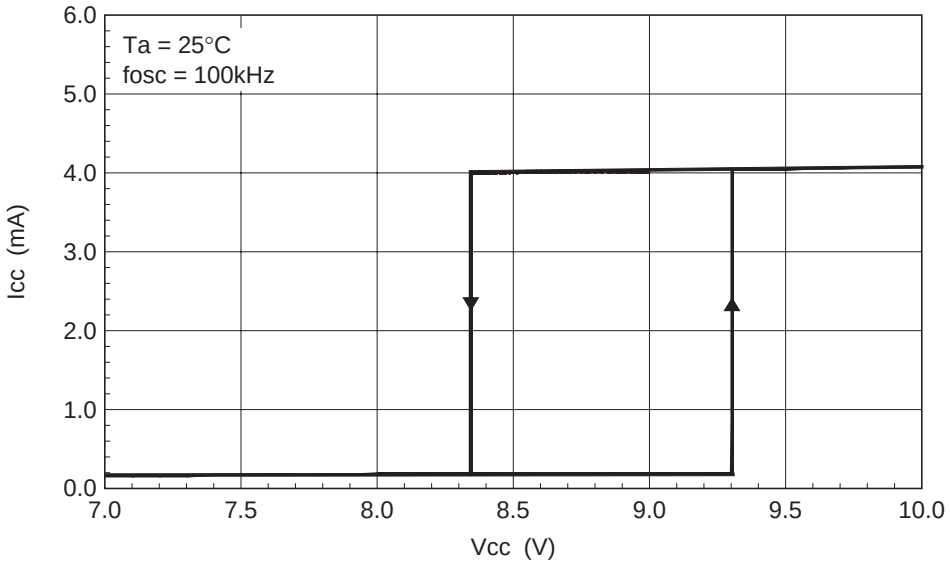


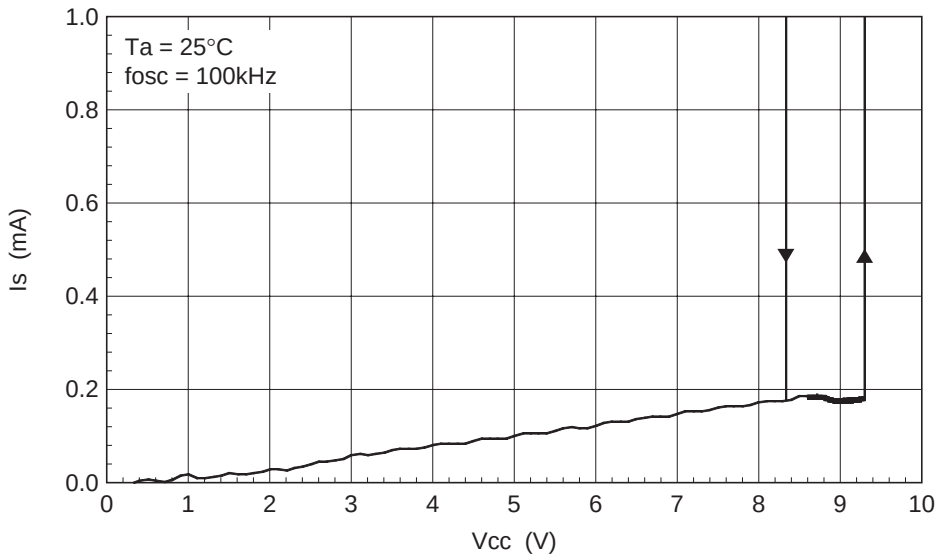
Figure 6 Adjustment of Power Supply Output Drooping Characteristic

Characteristic Curves

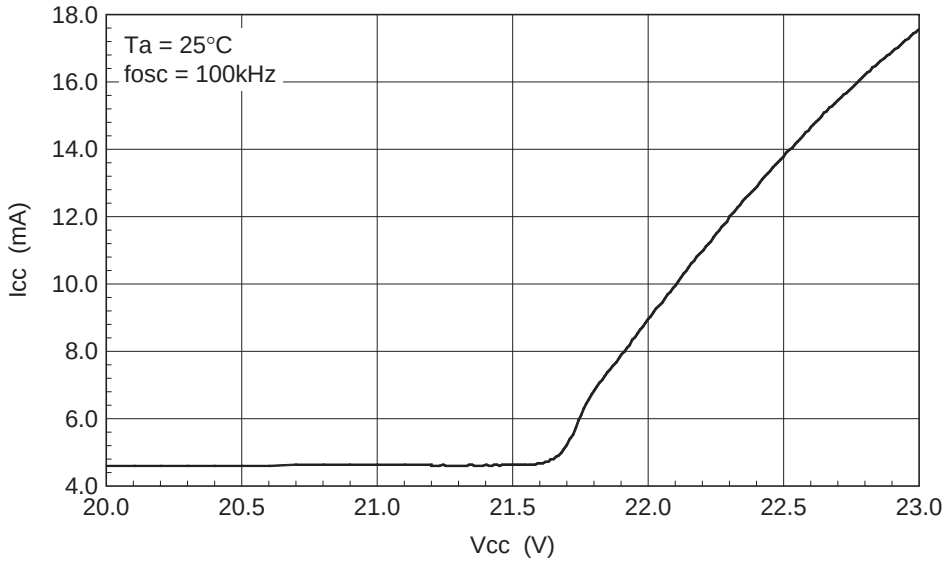
Power Supply Current vs. Power Supply Voltage Characteristics



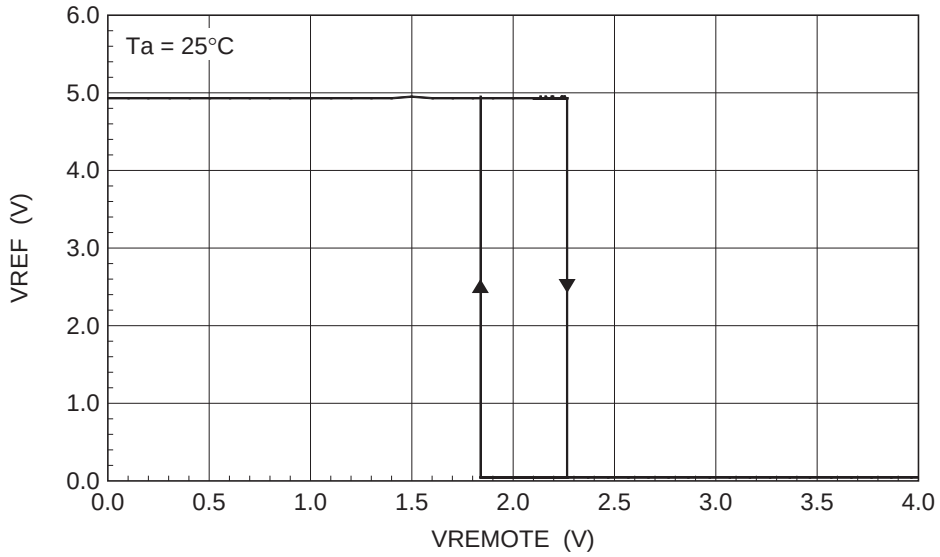
Standby Current vs. Power Supply Voltage Characteristics



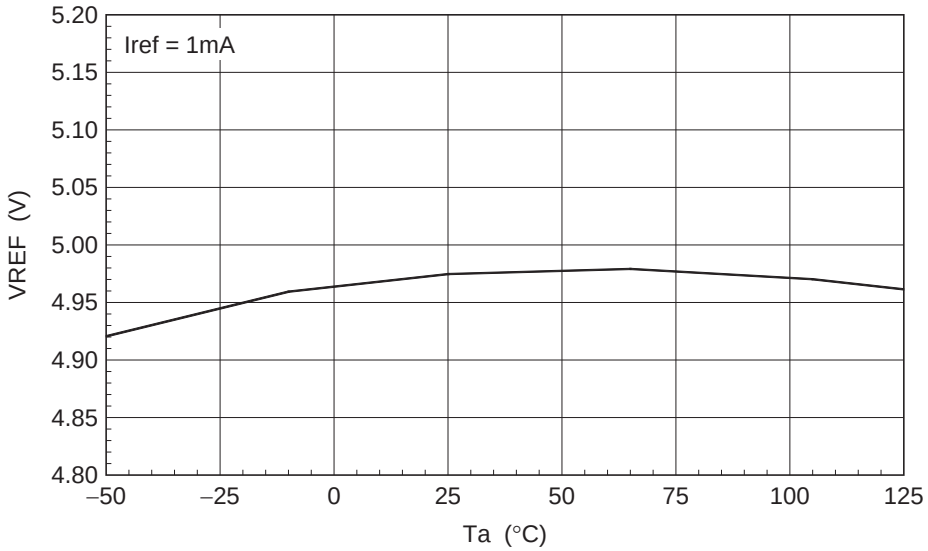
Power Supply Current vs. Power Supply Voltage (Clamp Zener Voltage) Characteristics



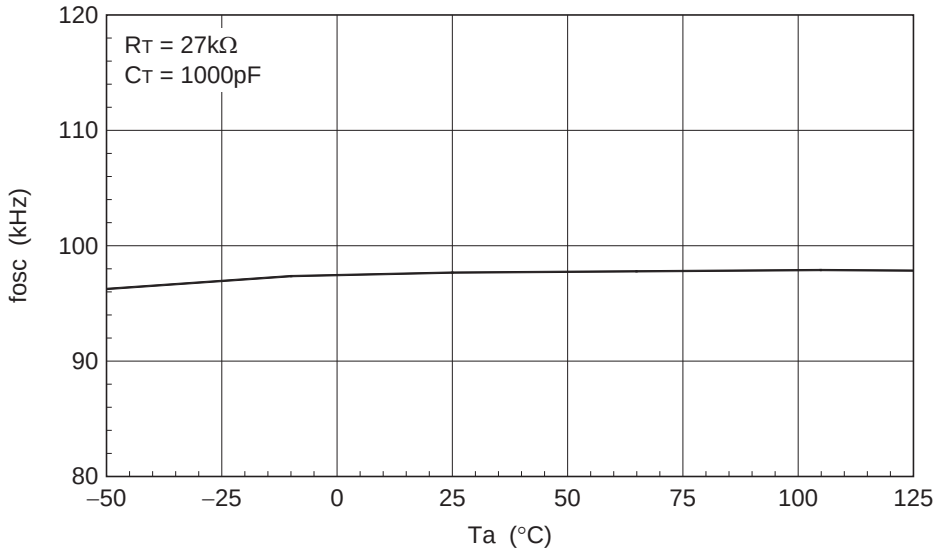
VREF Output Voltage vs. REMOTE Pin Voltage Characteristics



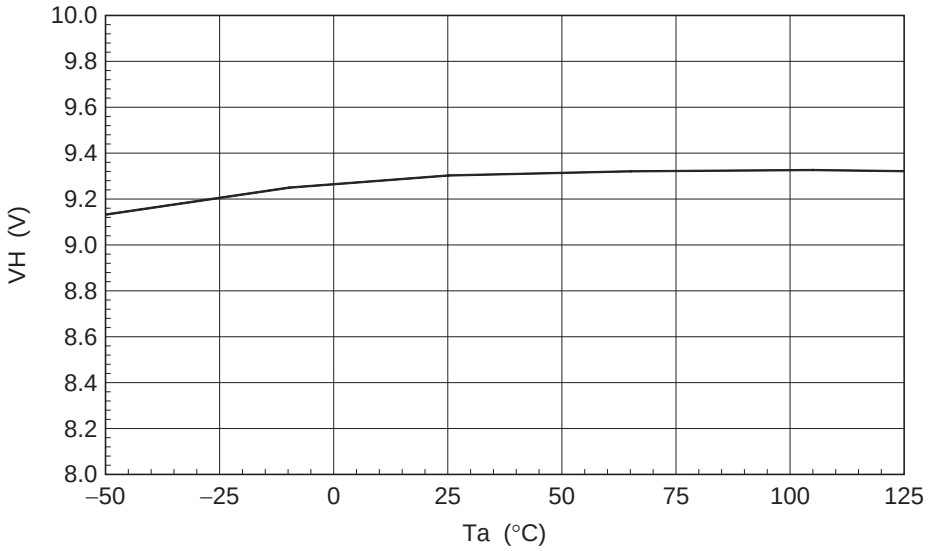
VREF Output Voltage vs. Ambient Temperature Characteristics



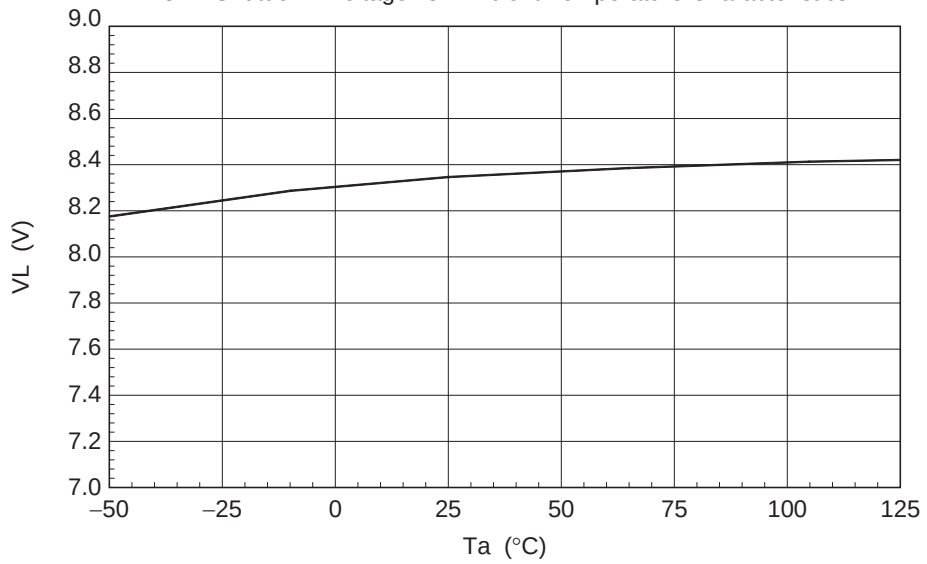
Operating Frequency vs. Ambient Temperature Characteristics



UVL Start-up Voltage vs. Ambient Temperature Characteristics

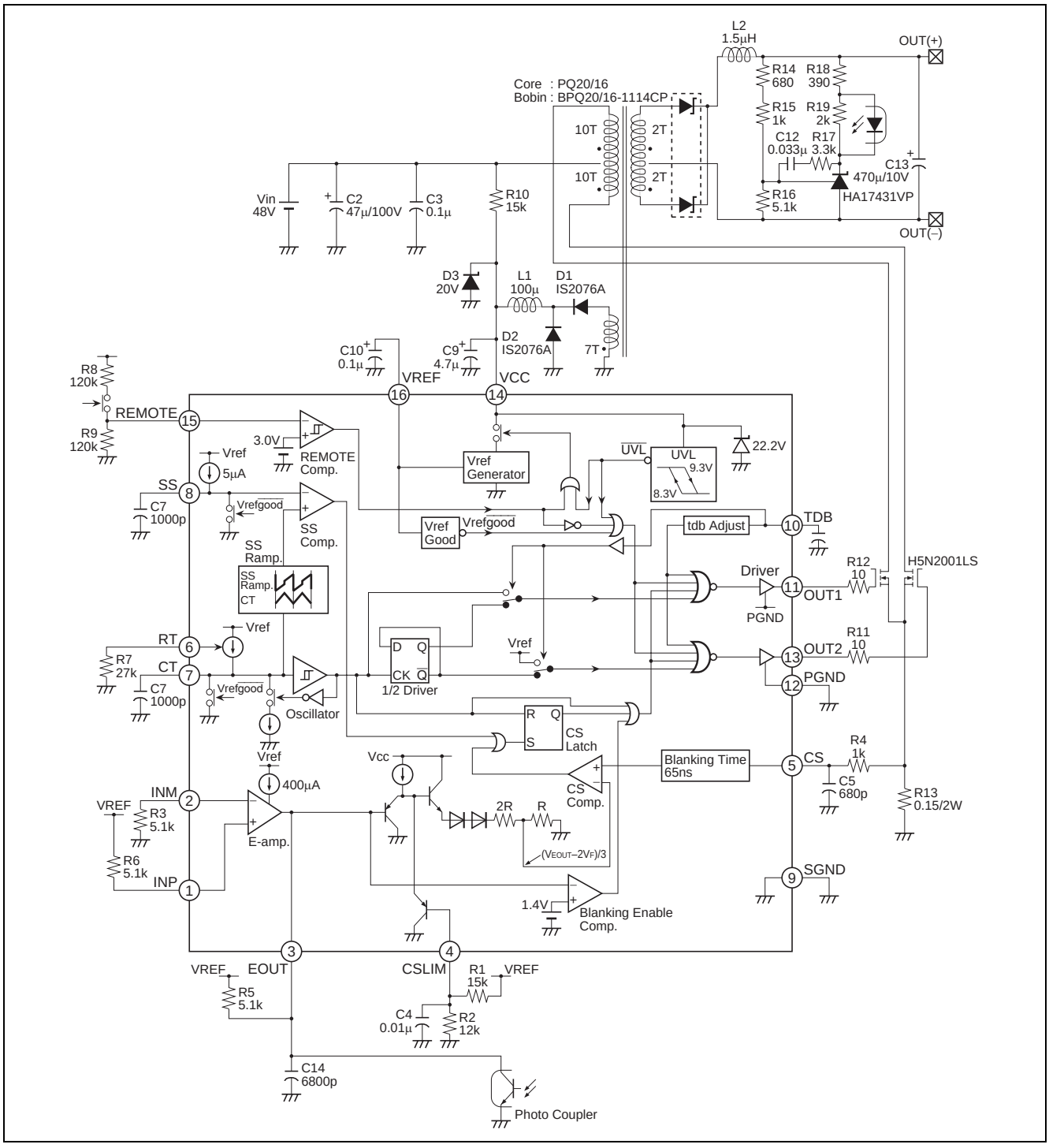


UVL Shutdown Voltage vs. Ambient Temperature Characteristics



ApplicationCircuit Example

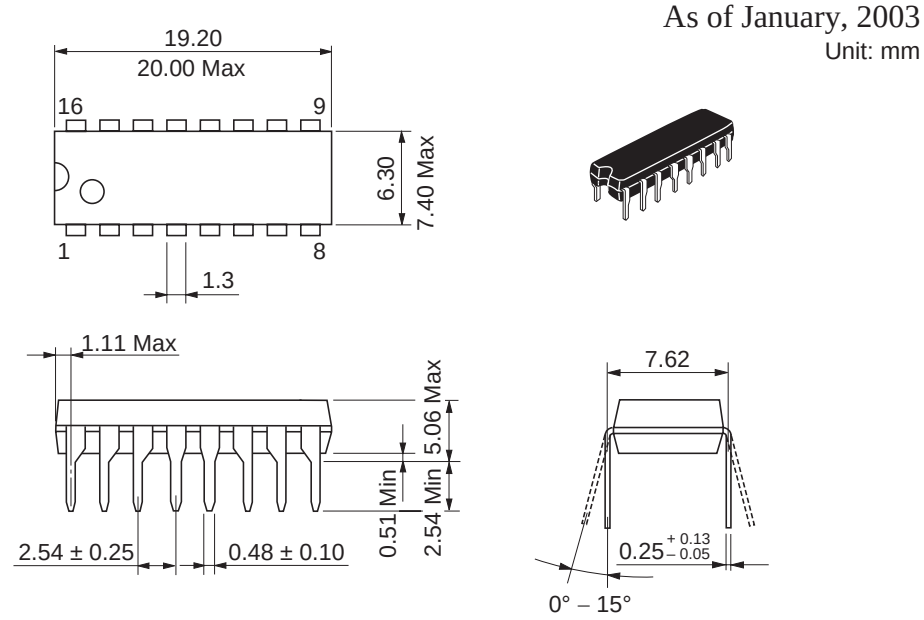
The following diagram shows a sample application circuit for a push-pull converter with a 48 V input voltage, 3.3 V output voltage, and 10 A output current.



Package Dimensions

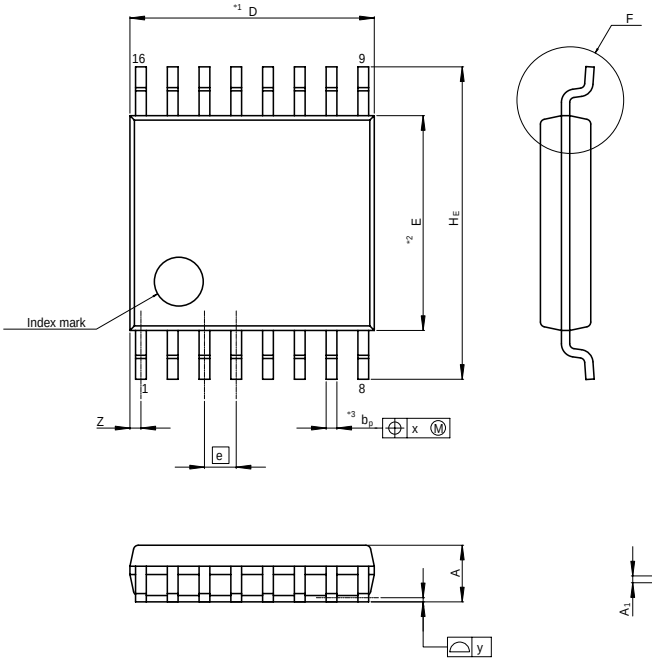
As of January, 2003

Unit: mm

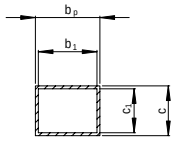


Package Code	DP-16
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	1.07 g

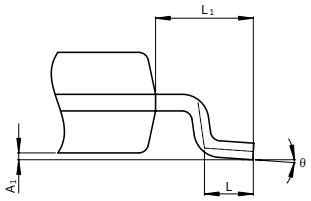
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP16-4.4x5-0.65	PTSP0016JB-B	TTP-16DA	0.05g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.00	5.30
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.22	0.30
b_1	—	0.20	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.65
L	0.40	0.50	0.60
L_1	—	1.0	—

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