

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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# H7N0308LD, H7N0308LS, H7N0308LM

Silicon N Channel MOS FET  
High Speed Power Switching

**RENESAS**

ADE-208-1535C (Z)

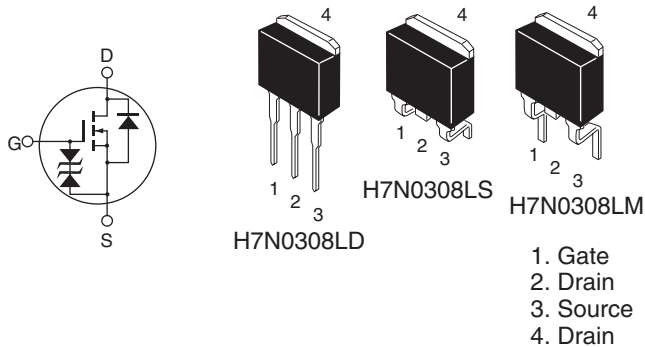
4th. Edition  
Aug. 2002

## Features

- Low on-resistance  
 $R_{DS(on)} = 3.8 \text{ m}\Omega$  typ.
- Low drive current
- 4.5 V gate drive device can be driven from 5 V source

## Outline

LDPAK



**Absolute Maximum Ratings**

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	30	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	70	A
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	280	A
Body-drain diode reverse drain current	$I_{DR}$	70	A
Channel dissipation	$P_{ch}$ <sup>Note 2</sup>	100	W
Channel to case thermal impedance	$\theta_{ch-c}$	1.25	°C/W
Channel to ambient thermal impedance	$\theta_{ch-a}$	89	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1 \%$ 

2. Value at Tc = 25°C

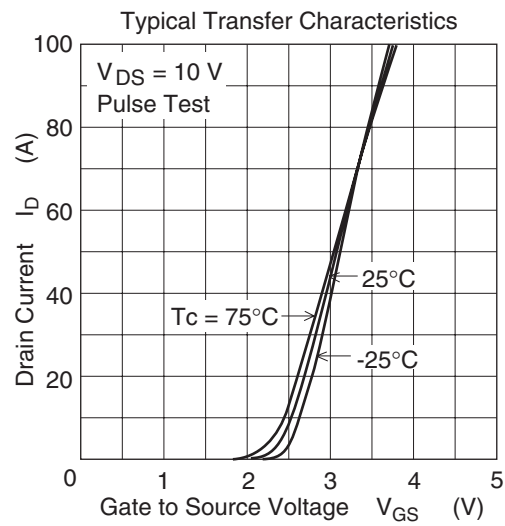
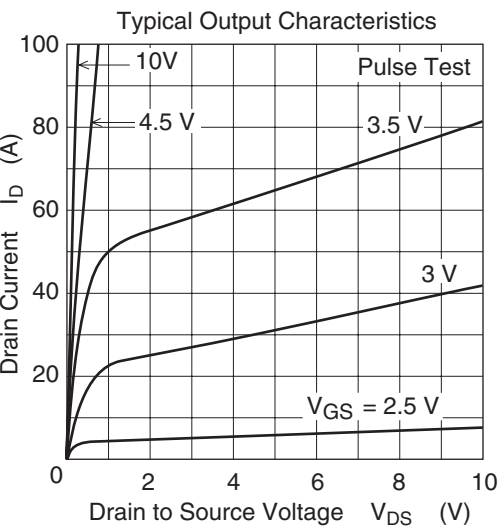
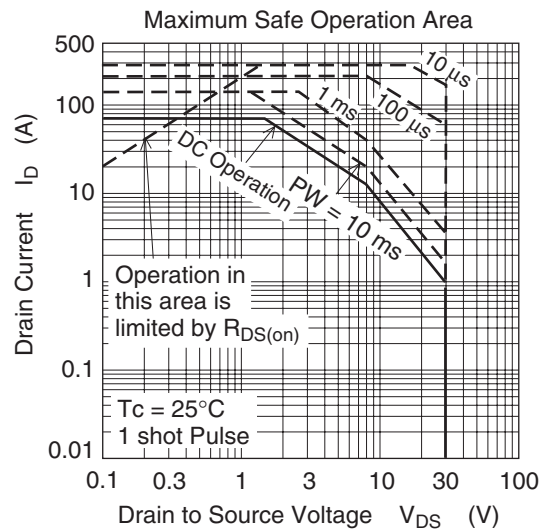
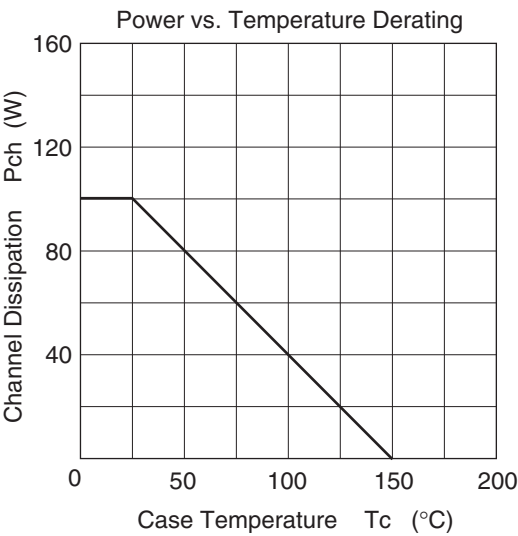
## Electrical Characteristics

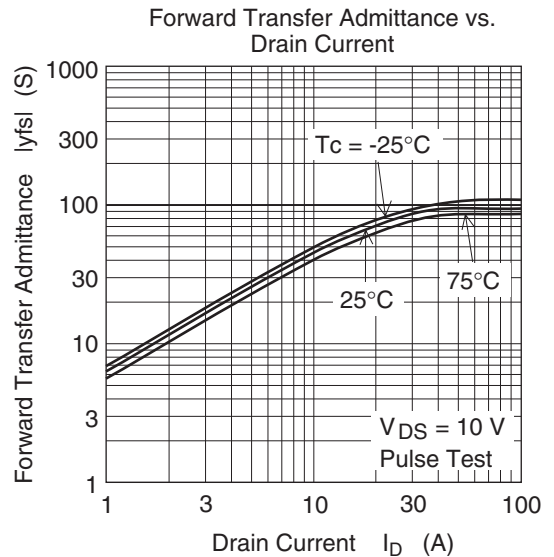
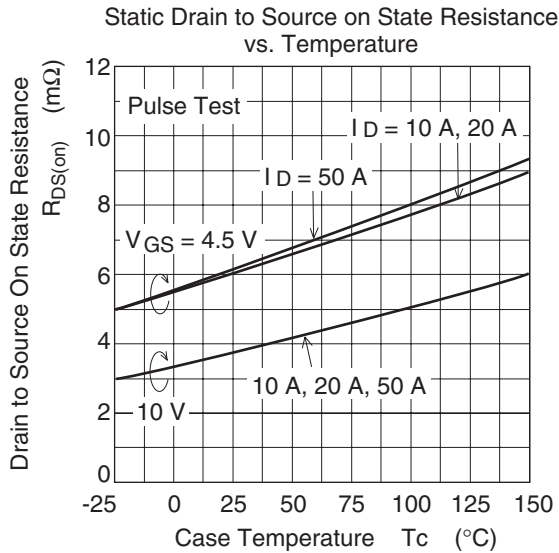
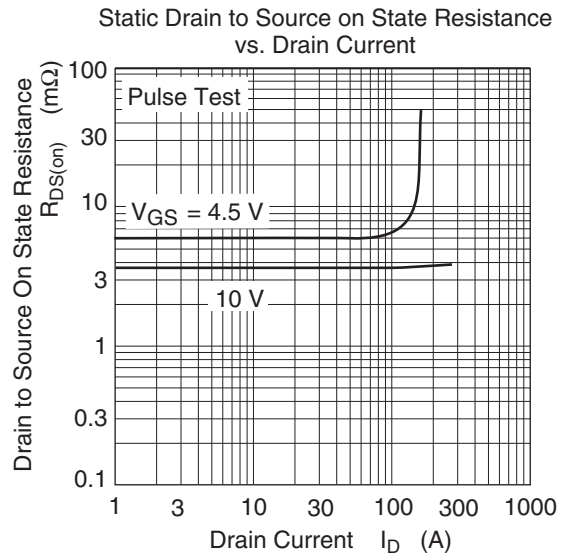
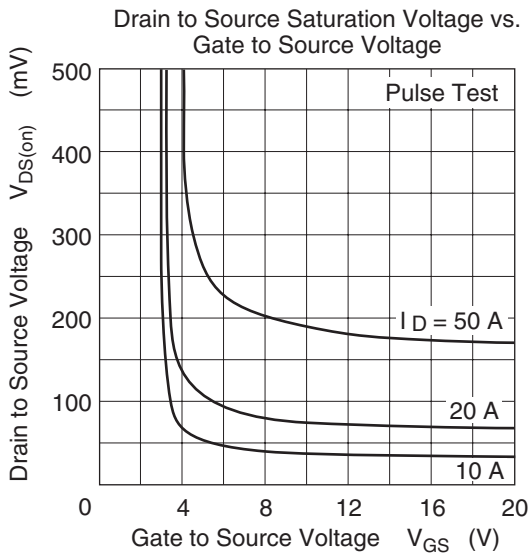
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—		$I_G = \pm 100 \text{ }\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu\text{A}$	$V_{DS} = 30 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1 \text{ mA}$ , $V_{DS} = 10 \text{ V}$ <sup>Note 1</sup>
Static drain to source on state resistance	$R_{DS(on)}$	—	3.8	4.8	$\text{m}\Omega$	$I_D = 35 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note 1</sup>
		—	6.0	8.5	$\text{m}\Omega$	$I_D = 35 \text{ A}$ , $V_{GS} = 4.5 \text{ V}$ <sup>Note 1</sup>
Forward transfer admittance	$ y_{fs} $	54	90	—	S	$I_D = 35 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note 1</sup>
Input capacitance	$C_{iss}$	—	3350	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	840	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	480	—	pF	$f = 1 \text{ MHz}$
Total gate charge	$Q_g$	—	52	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	$Q_{gs}$	—	11	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	10	—	nc	$I_D = 70 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	$V_{GS} = 10 \text{ V}$ , $I_D = 35 \text{ A}$
Rise time	$t_r$	—	370	—	ns	$R_L = 0.29 \text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	—	80	—	ns	$R_g = 4.7 \text{ }\Omega$
Fall time	$t_f$	—	27	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.93	—	V	$I_F = 70 \text{ A}$ , $V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	60	—	ns	$I_F = 70 \text{ A}$ , $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

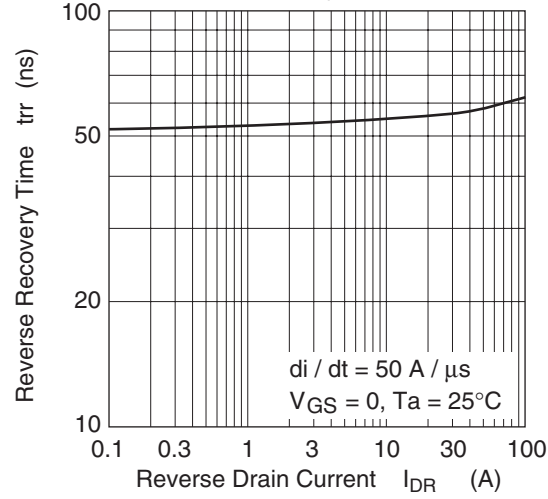
Notes: 1. Pulse test

Main Characteristics

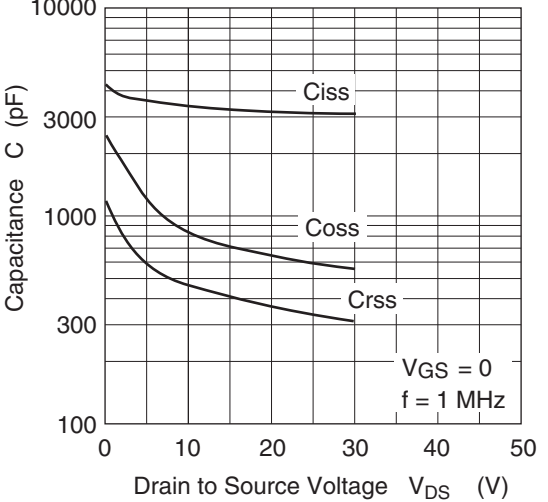




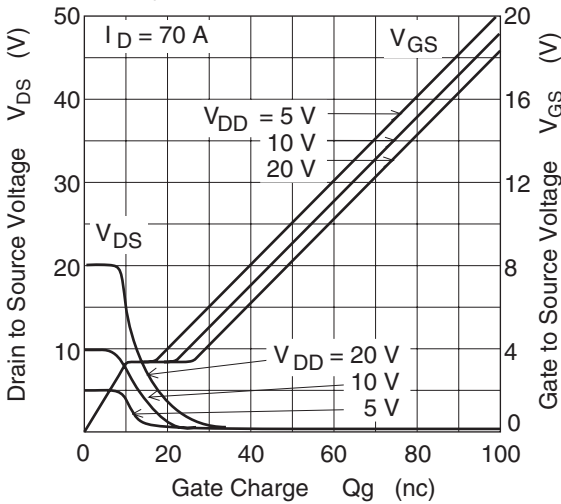
Body-Drain Diode Reverse Recovery Time



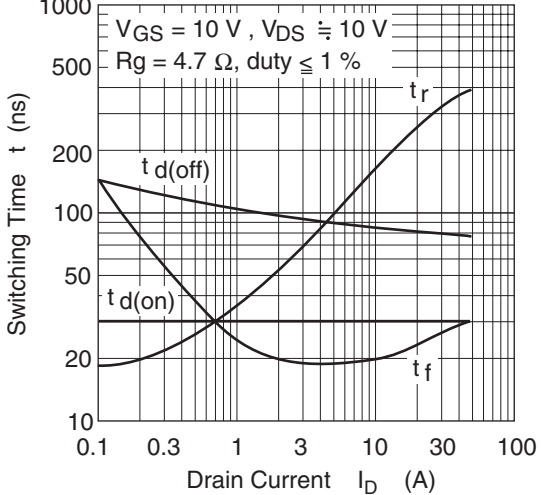
Typical Capacitance vs. Drain to Source Voltage



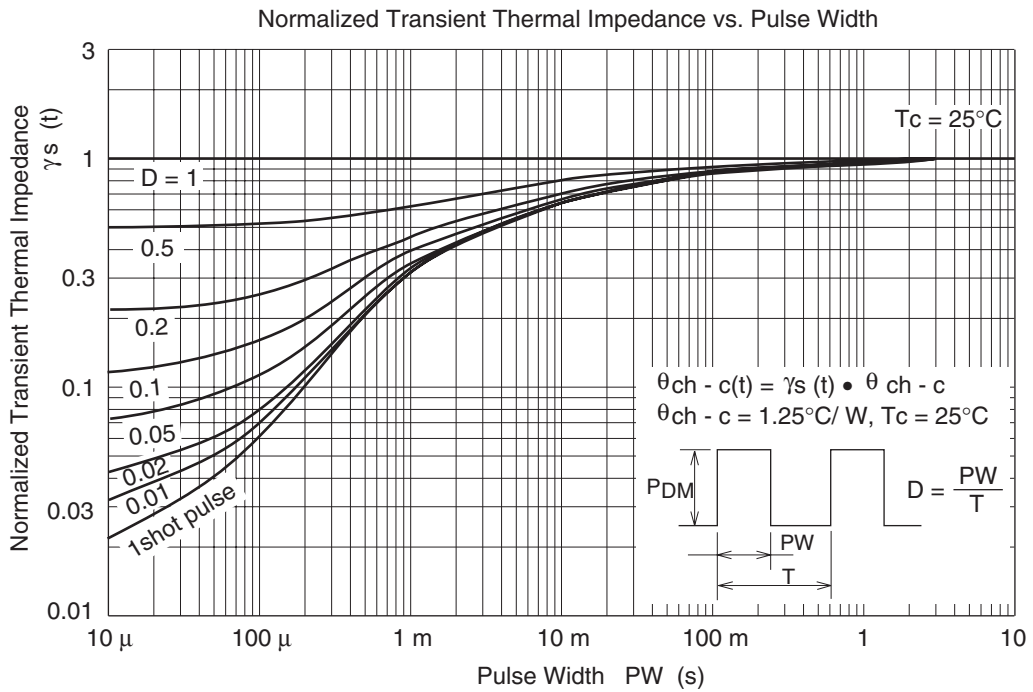
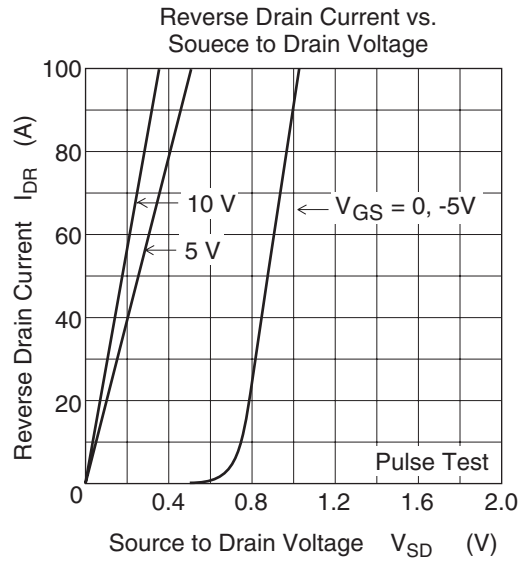
Dynamic Input Characteristics



Switching Characteristics



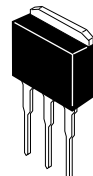
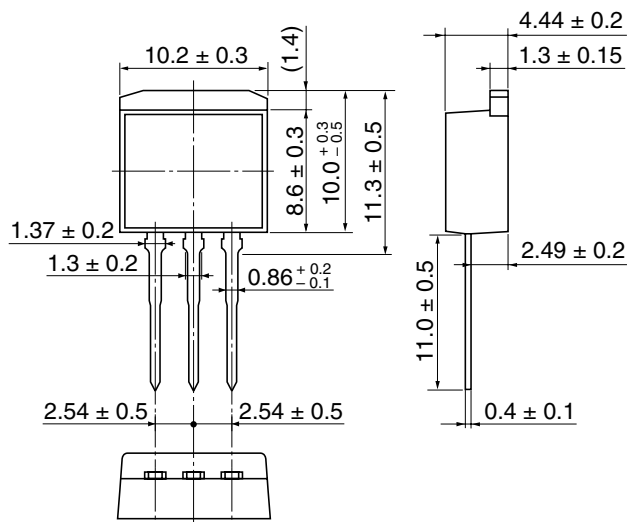




Package Dimensions

• H7N0308LD

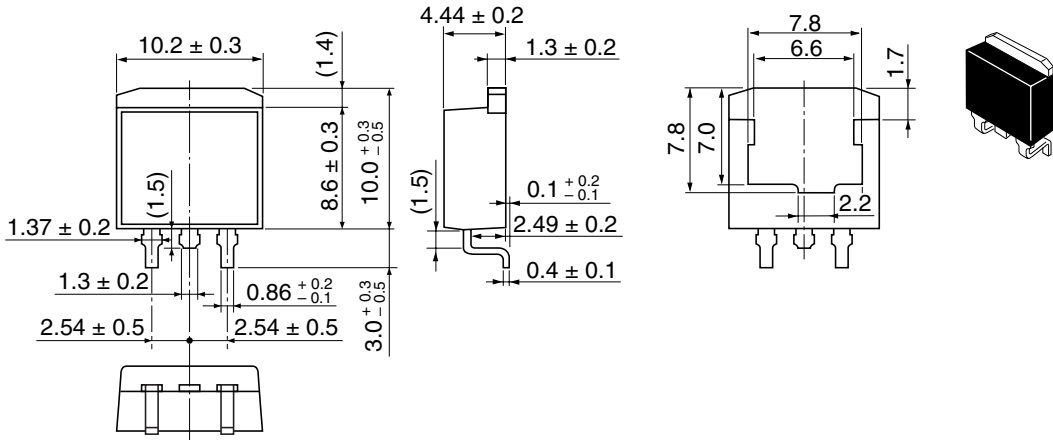
Unit: mm



Hitachi Code	LDPAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.4 g

• H7N0308LS

Unit: mm

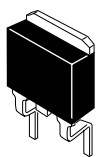
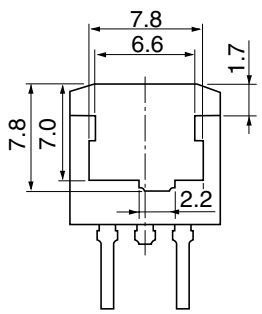
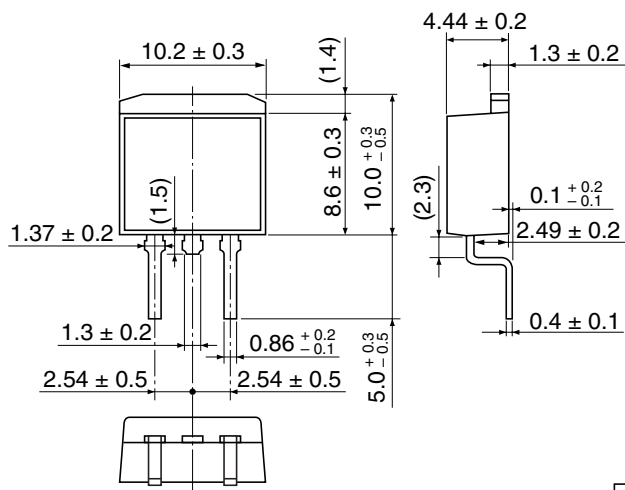


Hitachi Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.3 g

H7N0308LD, H7N0308LS, H7N0308LM

• H7N0308LM

Unit: mm



Hitachi Code	LDBAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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