

To all our customers

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## **Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.**

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The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

# MITSUBISHI MICROCOMPUTERS

# M35045-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

## DESCRIPTION

The M35045-XXXSP/FP is a TV screen display control IC. It uses a silicon gate CMOS process and is housed in a 20-pin shrink DIP package (M35045-XXXSP) or a 20-pin shrink SOP package (M35045-XXXFP).

For M35045-001SP/FP that is a standard ROM version of M35045-XXXSP/FP respectively, the character pattern is also mentioned.

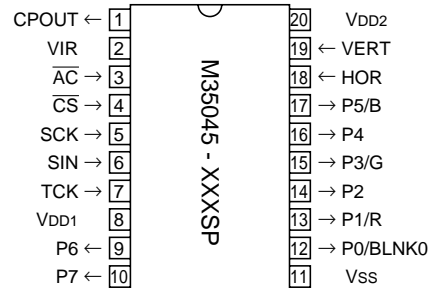
## FEATURES

- Screen composition ..... 24 columns × 12 lines
- Number of characters displayed ..... 288 (Max.)
- Character composition ..... 12 × 18 dot matrix
- Characters available ..... 256 characters
- Character sizes available ..... 4 (horizontal) × 4 (vertical)
- Display locations available
  - Horizontal direction ..... 1000 locations
  - Vertical direction ..... 1023 locations
- Blinking ..... Character units
  - Cycle : division of vertical synchronization signal into 64 or 32
  - Duty : 25%, 50%, or 75%
- Data input ..... By the 16-bit serial input function
- Coloring
  - Character color ..... Character unit
  - Background coloring ..... Character unit
  - Matrix-outline (shadow) coloring ..... 8 colors (RGB output)
    - Specified by register
  - Border coloring ..... 8 colors (RGB output)
    - Specified by register
  - Raster coloring ..... 8 colors (RGB output)
    - Specified by register
- Blanking
  - Blanking off
  - Character size blanking
  - Border size blanking
  - Matrix-outline blanking
  - All blanking (all raster area)
- Output ports
  - 4 shared output ports (toggled between RGB output)
  - 4 dedicated output ports
- Display RAM erase function
- Display input frequency range ..... Fosc = 30MHz-80MHz

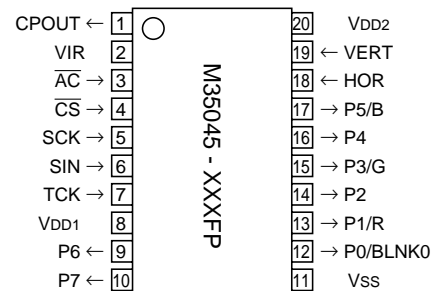
## APPLICATION

Monitor

## PIN CONFIGURATION (TOP VIEW)



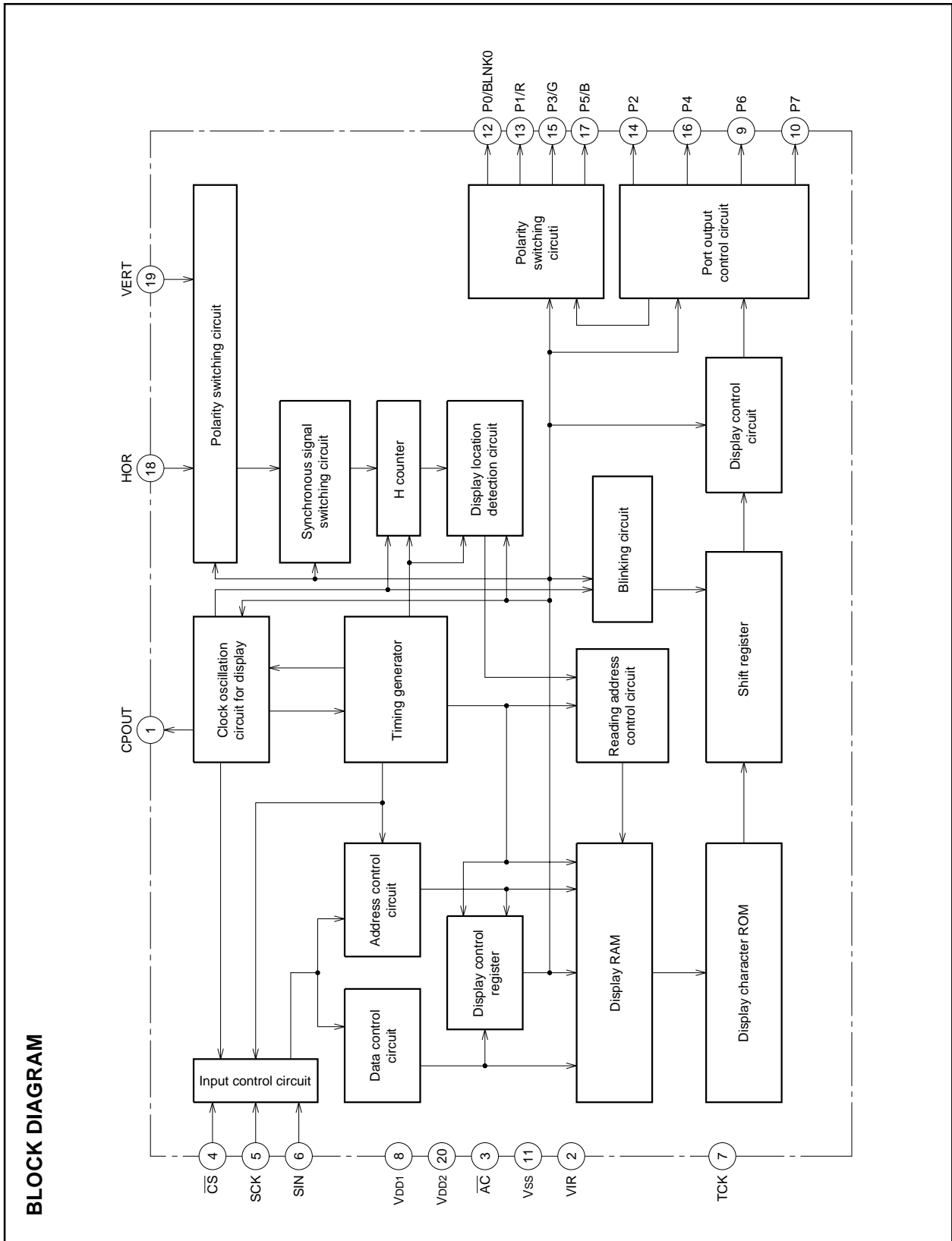
### Outline 20P4B



### Outline 20P2Q-A

**PIN DESCRIPTION**

Pin Number	Symbol	Pin name	Input/Output	Function
1	CPOUT	Phase difference	Output	<p>Connect loop filter to this pin.</p> <p>*1 Use at 1% precision *2 Use at 10% precision</p>
2	VIR	Frequency control	–	Connect to GND.
3	AC	Auto-clear input	Input	When "L", this pin resets the internal IC circuit. Hysteresis input. Includes built-in pull-up resistor.
4	$\overline{\text{CS}}$	Chip select input	Input	This is the chip select pin, and when serial data transmission is being carried out, it goes to "L". Hysteresis input. Includes built-in pull-up resistor.
5	SCK	Serial clock input	Input	When CS pin is "L", SIN serial data is taken in when SCK rises. Hysteresis input. Built-in pull-up resistor is included.
6	SIN	Serial data input	Input	This is the pin for serial input of data and addresses for the display control register and the display data memory. Hysteresis input. Includes built-in pull-up resistor.
7	TCK	Test clock	Input	Input for test. Please connect to GND using circuit earthing pin.
8	VDD1	Power pin	–	Please connect to +5V with the power pin.
9	P6	Port P6 output	Output	This is the output port. Port data is set by PTD6.
10	P7	Port P7 output	Output	This is the output port. Port data is set by PTD7.
11	VSS	Earthing pin	–	Please connect to GND using circuit earthing pin.
12	P0/BLNK0	Port P0 output	Output	This pin can be toggled between port pin output and BLNK0 signal output.
13	P1/R	Port P1 output	Output	This pin can be toggled between port pin output and R signal output.
14	P2	Port P2 output	Output	This is the output port. Port data is set by PTD2.
15	P3/G	Port P3 output	Output	This pin can be toggled between port pin output and G signal output.
16	P4	Port P4 output	Output	This is the output port. Port data is set by PTD4.
17	P5/B	Port P5 output	Output	This pin can be toggled between port pin output and B signal output.
18	HOR	Horizontal synchronization signal input	Input	This pin inputs the horizontal synchronization signal. Hysteresis input.
19	VERT	Vertical synchronization signal input	Input	This pin inputs the vertical synchronization signal. Hysteresis input.
20	VDD2	Power pin	–	Please connect to +5V with the power pin.



**MEMORY CONSTITUTION**

Address 000<sub>16</sub> to 11F<sub>16</sub> are assigned to the display RAM, address 120<sub>16</sub> to 128<sub>16</sub> are assigned to the display control registers. The internal circuit is reset and all display control registers (address 120<sub>16</sub> to 128<sub>16</sub>) are set to "0" and display RAM (address 000<sub>16</sub> to 11F<sub>16</sub>) are set to "FF<sub>16</sub>" when the AC pin level is "L".  
Memory constitution is shown in Figure 1.

**SCREEN CONSTITUTION**

The screen lines and rows are determined from each address of the display RAM. The screen constitution is shown in Figure 2.

	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
000 <sub>16</sub>	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
⋮	⋮	Background coloring			Blinking	Character color			Character code							
11F <sub>16</sub>	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
120 <sub>16</sub>	0	0	DIVS2	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
121 <sub>16</sub>	0	0	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
122 <sub>16</sub>	0	0	SPACE2	SPACE1	SPACE0	TEST9	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
123 <sub>16</sub>	0	0	TEST3	TEST2	TEST1	TEST0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
124 <sub>16</sub>	0	0	TEST5	TEST4	DSP11	DSP10	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
125 <sub>16</sub>	0	0	VSZ1H1	VSZ1H0	VSZ1L1	VSZ1L0	V1SZ1	V1SZ0	LIN9	LIN8	LIN7	LIN6	LIN5	LIN4	LIN3	LIN2
126 <sub>16</sub>	0	0	VSZ2H1	VSZ2H0	VSZ2L1	VSZ2L0	V18SZ1	V18SZ0	LIN17	LIN16	LIN15	LIN14	LIN13	LIN12	LIN11	LIN10
127 <sub>16</sub>	0	0	HSZ21	HSZ20	HSZ11	HSZ10	BETA14	TEST8	TEST7	TEST6	FB	FG	FR	RB	RG	RR
128 <sub>16</sub>	0	0	BLINK2	BLINK1	BLINK0	DSPON	STOP	RAMERS	SYAD	BLK1	BLK0	POLH	POLV	VMASK	B/F	BCOL

Fig. 1 Memory constitution

Row Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	000 <sub>16</sub>	001 <sub>16</sub>	002 <sub>16</sub>	003 <sub>16</sub>	004 <sub>16</sub>	005 <sub>16</sub>	006 <sub>16</sub>	007 <sub>16</sub>	008 <sub>16</sub>	009 <sub>16</sub>	00A <sub>16</sub>	00B <sub>16</sub>	00C <sub>16</sub>	00D <sub>16</sub>	00E <sub>16</sub>	00F <sub>16</sub>	010 <sub>16</sub>	011 <sub>16</sub>	012 <sub>16</sub>	013 <sub>16</sub>	014 <sub>16</sub>	015 <sub>16</sub>	016 <sub>16</sub>	017 <sub>16</sub>
2	018 <sub>16</sub>	019 <sub>16</sub>	01A <sub>16</sub>	01B <sub>16</sub>	01C <sub>16</sub>	01D <sub>16</sub>	01E <sub>16</sub>	01F <sub>16</sub>	020 <sub>16</sub>	021 <sub>16</sub>	022 <sub>16</sub>	023 <sub>16</sub>	024 <sub>16</sub>	025 <sub>16</sub>	026 <sub>16</sub>	027 <sub>16</sub>	028 <sub>16</sub>	029 <sub>16</sub>	02A <sub>16</sub>	02B <sub>16</sub>	02C <sub>16</sub>	02D <sub>16</sub>	02E <sub>16</sub>	02F <sub>16</sub>
3	030 <sub>16</sub>	031 <sub>16</sub>	032 <sub>16</sub>	033 <sub>16</sub>	034 <sub>16</sub>	035 <sub>16</sub>	036 <sub>16</sub>	037 <sub>16</sub>	038 <sub>16</sub>	039 <sub>16</sub>	03A <sub>16</sub>	03B <sub>16</sub>	03C <sub>16</sub>	03D <sub>16</sub>	03E <sub>16</sub>	03F <sub>16</sub>	040 <sub>16</sub>	041 <sub>16</sub>	042 <sub>16</sub>	043 <sub>16</sub>	044 <sub>16</sub>	045 <sub>16</sub>	046 <sub>16</sub>	047 <sub>16</sub>
4	048 <sub>16</sub>	049 <sub>16</sub>	04A <sub>16</sub>	04B <sub>16</sub>	04C <sub>16</sub>	04D <sub>16</sub>	04E <sub>16</sub>	04F <sub>16</sub>	050 <sub>16</sub>	051 <sub>16</sub>	052 <sub>16</sub>	053 <sub>16</sub>	054 <sub>16</sub>	055 <sub>16</sub>	056 <sub>16</sub>	057 <sub>16</sub>	058 <sub>16</sub>	059 <sub>16</sub>	05A <sub>16</sub>	05B <sub>16</sub>	05C <sub>16</sub>	05D <sub>16</sub>	05E <sub>16</sub>	05F <sub>16</sub>
5	060 <sub>16</sub>	061 <sub>16</sub>	062 <sub>16</sub>	063 <sub>16</sub>	064 <sub>16</sub>	065 <sub>16</sub>	066 <sub>16</sub>	067 <sub>16</sub>	068 <sub>16</sub>	069 <sub>16</sub>	06A <sub>16</sub>	06B <sub>16</sub>	06C <sub>16</sub>	06D <sub>16</sub>	06E <sub>16</sub>	06F <sub>16</sub>	070 <sub>16</sub>	071 <sub>16</sub>	072 <sub>16</sub>	073 <sub>16</sub>	074 <sub>16</sub>	075 <sub>16</sub>	076 <sub>16</sub>	077 <sub>16</sub>
6	078 <sub>16</sub>	079 <sub>16</sub>	07A <sub>16</sub>	07B <sub>16</sub>	07C <sub>16</sub>	07D <sub>16</sub>	07E <sub>16</sub>	07F <sub>16</sub>	080 <sub>16</sub>	081 <sub>16</sub>	082 <sub>16</sub>	083 <sub>16</sub>	084 <sub>16</sub>	085 <sub>16</sub>	086 <sub>16</sub>	087 <sub>16</sub>	088 <sub>16</sub>	089 <sub>16</sub>	08A <sub>16</sub>	08B <sub>16</sub>	08C <sub>16</sub>	08D <sub>16</sub>	08E <sub>16</sub>	08F <sub>16</sub>
7	090 <sub>16</sub>	091 <sub>16</sub>	092 <sub>16</sub>	093 <sub>16</sub>	094 <sub>16</sub>	095 <sub>16</sub>	096 <sub>16</sub>	097 <sub>16</sub>	098 <sub>16</sub>	099 <sub>16</sub>	09A <sub>16</sub>	09B <sub>16</sub>	09C <sub>16</sub>	09D <sub>16</sub>	09E <sub>16</sub>	09F <sub>16</sub>	0A0 <sub>16</sub>	0A1 <sub>16</sub>	0A2 <sub>16</sub>	0A3 <sub>16</sub>	0A4 <sub>16</sub>	0A5 <sub>16</sub>	0A6 <sub>16</sub>	0A7 <sub>16</sub>
8	0A8 <sub>16</sub>	0A9 <sub>16</sub>	0AA <sub>16</sub>	0AB <sub>16</sub>	0AC <sub>16</sub>	0AD <sub>16</sub>	0AE <sub>16</sub>	0AF <sub>16</sub>	0B0 <sub>16</sub>	0B1 <sub>16</sub>	0B2 <sub>16</sub>	0B3 <sub>16</sub>	0B4 <sub>16</sub>	0B5 <sub>16</sub>	0B6 <sub>16</sub>	0B7 <sub>16</sub>	0B8 <sub>16</sub>	0B9 <sub>16</sub>	0BA <sub>16</sub>	0BB <sub>16</sub>	0BC <sub>16</sub>	0BD <sub>16</sub>	0BE <sub>16</sub>	0BF <sub>16</sub>
9	0C0 <sub>16</sub>	0C1 <sub>16</sub>	0C2 <sub>16</sub>	0C3 <sub>16</sub>	0C4 <sub>16</sub>	0C5 <sub>16</sub>	0C6 <sub>16</sub>	0C7 <sub>16</sub>	0C8 <sub>16</sub>	0C9 <sub>16</sub>	0CA <sub>16</sub>	0CB <sub>16</sub>	0CC <sub>16</sub>	0CD <sub>16</sub>	0CE <sub>16</sub>	0CF <sub>16</sub>	0D0 <sub>16</sub>	0D1 <sub>16</sub>	0D2 <sub>16</sub>	0D3 <sub>16</sub>	0D4 <sub>16</sub>	0D5 <sub>16</sub>	0D6 <sub>16</sub>	0D7 <sub>16</sub>
10	0D8 <sub>16</sub>	0D9 <sub>16</sub>	0DA <sub>16</sub>	0DB <sub>16</sub>	0DC <sub>16</sub>	0DD <sub>16</sub>	0DE <sub>16</sub>	0DF <sub>16</sub>	0E0 <sub>16</sub>	0E1 <sub>16</sub>	0E2 <sub>16</sub>	0E3 <sub>16</sub>	0E4 <sub>16</sub>	0E5 <sub>16</sub>	0E6 <sub>16</sub>	0E7 <sub>16</sub>	0E8 <sub>16</sub>	0E9 <sub>16</sub>	0EA <sub>16</sub>	0EB <sub>16</sub>	0EC <sub>16</sub>	0ED <sub>16</sub>	0EE <sub>16</sub>	0EF <sub>16</sub>
11	0F0 <sub>16</sub>	0F1 <sub>16</sub>	0F2 <sub>16</sub>	0F3 <sub>16</sub>	0F4 <sub>16</sub>	0F5 <sub>16</sub>	0F6 <sub>16</sub>	0F7 <sub>16</sub>	0F8 <sub>16</sub>	0F9 <sub>16</sub>	0FA <sub>16</sub>	0FB <sub>16</sub>	0FC <sub>16</sub>	0FD <sub>16</sub>	0FE <sub>16</sub>	0FF <sub>16</sub>	100 <sub>16</sub>	101 <sub>16</sub>	102 <sub>16</sub>	103 <sub>16</sub>	104 <sub>16</sub>	105 <sub>16</sub>	106 <sub>16</sub>	107 <sub>16</sub>
12	108 <sub>16</sub>	109 <sub>16</sub>	10A <sub>16</sub>	10B <sub>16</sub>	10C <sub>16</sub>	10D <sub>16</sub>	10E <sub>16</sub>	10F <sub>16</sub>	110 <sub>16</sub>	111 <sub>16</sub>	112 <sub>16</sub>	113 <sub>16</sub>	114 <sub>16</sub>	115 <sub>16</sub>	116 <sub>16</sub>	117 <sub>16</sub>	118 <sub>16</sub>	119 <sub>16</sub>	11A <sub>16</sub>	11B <sub>16</sub>	11C <sub>16</sub>	11D <sub>16</sub>	11E <sub>16</sub>	11F <sub>16</sub>

\* The hexadecimal numbers in the boxes show the display RAM address.

Fig. 2 Screen constitution

**REGISTERS DESCRIPTION**

(1) Address 120<sub>16</sub>

DA	Register	Contents		Remarks																
		Status	Function																	
0	DIV0	○	Set multiply value (frequency value) of horizontal synchronous frequency.	Display frequency is computed as shown below.  $F_{OSC} = f_H \times N1$ Fosc [MHz] : Display frequency fH [kHz] : Horizontal synchronous signal frequency to HOR pin. N1 : Shown left  Set display frequency Fosc to within 30MHz to 80MHz range. When display frequency Fosc, set frequency value N2 in association with DIVS0 and DIVS1.																
		1																		
1	DIV1	○	$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1: frequency value																	
		1																		
2	DIV2	○			$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1: frequency value															
		1																		
3	DIV3	○				$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1: frequency value														
		1																		
4	DIV4	○					$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1: frequency value													
		1																		
5	DIV5	○						$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1: frequency value												
		1																		
6	DIV6	○							$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1: frequency value											
		1																		
7	DIV7	○								$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1: frequency value										
		1																		
8	DIV8	○		$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1: frequency value																
		1																		
9	DIV9	○	$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1: frequency value																	
		1																		
A	DIV10	○			$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1: frequency value															
		1																		
B	DIVS0	○				Set frequency value N2					Set frequency value N2 in association with display frequency range.									
		1										<table border="1"> <thead> <tr> <th>DIVS</th> <th>Frequency value N2</th> </tr> </thead> <tbody> <tr> <td>1 0</td> <td>Division into 2</td> </tr> <tr> <td>0 0</td> <td>Division into 2</td> </tr> <tr> <td>0 1</td> <td>Division into 3</td> </tr> <tr> <td>1 0</td> <td>Division into 4</td> </tr> <tr> <td>1 1</td> <td>Do not set</td> </tr> </tbody> </table>	DIVS	Frequency value N2	1 0	Division into 2	0 0	Division into 2	0 1	Division into 3
DIVS	Frequency value N2																			
1 0	Division into 2																			
0 0	Division into 2																			
0 1	Division into 3																			
1 0	Division into 4																			
1 1	Do not set																			
C	DIVS1	○				Set frequency value N2	<table border="1"> <thead> <tr> <th>Display frequency</th> <th>Frequency value N2</th> </tr> </thead> <tbody> <tr> <td>55 ~ 80</td> <td>Division into 2</td> </tr> <tr> <td>40 ~ 55</td> <td>Division into 3</td> </tr> <tr> <td>30 ~ 40</td> <td>Division into 4</td> </tr> </tbody> </table>	Display frequency	Frequency value N2	55 ~ 80		Division into 2	40 ~ 55	Division into 3	30 ~ 40	Division into 4				
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1	<table border="1"> <thead> <tr> <th>Display frequency</th> <th>Frequency value N2</th> </tr> </thead> <tbody> <tr> <td>55 ~ 80</td> <td>Division into 2</td> </tr> <tr> <td>40 ~ 55</td> <td>Division into 3</td> </tr> <tr> <td>30 ~ 40</td> <td>Division into 4</td> </tr> </tbody> </table>	Display frequency	Frequency value N2	55 ~ 80		Division into 2		40 ~ 55	Division into 3	30 ~ 40		Division into 4								
Display frequency	Frequency value N2																			
55 ~ 80	Division into 2																			
40 ~ 55	Division into 3																			
30 ~ 40	Division into 4																			
D	DIVS2	○	It should be fixed to "0".	<table border="1"> <thead> <tr> <th>Display frequency</th> <th>Frequency value N2</th> </tr> </thead> <tbody> <tr> <td>55 ~ 80</td> <td>Division into 2</td> </tr> <tr> <td>40 ~ 55</td> <td>Division into 3</td> </tr> <tr> <td>30 ~ 40</td> <td>Division into 4</td> </tr> </tbody> </table>	Display frequency	Frequency value N2		55 ~ 80	Division into 2	40 ~ 55	Division into 3	30 ~ 40	Division into 4							
		Display frequency	Frequency value N2																	
55 ~ 80	Division into 2																			
40 ~ 55	Division into 3																			
30 ~ 40	Division into 4																			
1	Can not be used.																			

Note: The mark ○ around the status value means the reset status by the "L" level is input to AC pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) Address 121<sub>16</sub>

DA	Register	Contents		Remarks	
		Status	Function		
0	PTC0	0	P0 output (port P0). Port data is set by PTD0.	BLNK0 outputs blanking signal. Blanking status is determined by BLK0, BLK1, and DSP0 to DSP11 settings.	
		1	BLNK0 output. Polarity is set by PTD0.		
1	PTC1	0	P1 output (port P1). Port data is set by PTD1.		
		1	R signal output. Polarity is set by PTD1.		
2	PTC2	0	P2 output (port P2). Port data is set by PTD2.		
		1	Do not set.		
3	PTC3	0	P3 output (port P3). Port data is set by PTD3.		
		1	G signal output. Polarity is set by PTD3.		
4	PTC4	0	P4 output (port P4). Port data is set by PTD4.		
		1	Do not set.		
5	PTC5	0	P5 output (port P5). Port data is set by PTD5.		
		1	B signal output. Polarity is set by PTD5.		
6	PTD0	0	"L" output (P0 output) or negative polarity output (BLNK0 output).		P0 pin data control.
		1	"H" output (P0 output) or positive polarity output (BLNK0 output).		
7	PTD1	0	"L" output (P1 output) or negative polarity output (R signal output).		P1 pin data control.
		1	"H" output (P1 output) or positive polarity output (R signal output).		
8	PTD2	0	"L" output (P2 output).	P2 pin exclusive port output state control.	
		1	"H" output (P2 output).		
9	PTD3	0	"L" output (P3 output) or negative polarity output (G signal output).	P3 pin data control.	
		1	"H" output (P3 output) or positive polarity output (G signal output).		
A	PTD4	0	"L" output (P2 output).	P4 pin exclusive port output state control.	
		1	"H" output (P2 output).		
B	PTD5	0	"L" output (P5 output) or negative polarity output (B signal output).	P5 pin data control.	
		1	"H" output (P5 output) or positive polarity output (B signal output).		
C	PTD6	0	"L" output (P6 output).	P6 pin exclusive port output state control.	
		1	"H" output (P6 output).		
D	PTD7	0	"L" output (P7 output).	P7 pin exclusive port output state control.	
		1	"H" output (P7 output).		

MITSUBISHI MICROCOMPUTERS  
**M35045-XXXSP/FP**

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(3) Address 122<sub>16</sub>

DA	Register	Contents			Remarks																																													
		Status	Function																																															
0	HP0 (LSB)	○	If HS is the horizontal display start location,		Horizontal display start location is specified using the 10 bits from HP9 to HP0. Note: HP9 to 0 = (0000000002) and (0000010112) setting is forbidden																																													
		1	$HS = T \times \left( \sum_{n=0}^9 2^n HP_n + N \right).$																																															
1	HP1	○	T: The cycle of display frequency																																															
		1	<table border="1" style="display: inline-table; vertical-align: middle;"> <thead> <tr> <th>HSZ11</th> <th>HSZ10</th> <th rowspan="2">N</th> </tr> <tr> <th>HSZ21</th> <th>HSZ20</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>6</td> </tr> <tr> <td>0</td> <td>1</td> <td>7</td> </tr> <tr> <td>1</td> <td>0</td> <td>8</td> </tr> <tr> <td>1</td> <td>1</td> <td>9</td> </tr> </tbody> </table>	HSZ11		HSZ10	N	HSZ21	HSZ20	0	0	6	0	1	7	1	0	8	1	1	9																													
HSZ11	HSZ10	N																																																
HSZ21	HSZ20																																																	
0	0	6																																																
0	1	7																																																
1	0	8																																																
1	1	9																																																
2	HP2	○	1000 settings are possible.																																															
		1																																																
3	HP3	○			1000 settings are possible.																																													
		1																																																
4	HP4	○					1000 settings are possible.																																											
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5	HP5	○							1000 settings are possible.																																									
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6	HP6	○									1000 settings are possible.																																							
		1																																																
7	HP7	○	1000 settings are possible.																																															
		1																																																
8	HP8	○			1000 settings are possible.																																													
		1																																																
9	HP9 (MSB)	○					1000 settings are possible.																																											
		1																																																
A	TEST9	○							It should be fixed to "0".				Leave one line worth of space in the vertical direction. For example, 6 [S] 6 indicates two sets of 6 lines with a line of spaces between lines 6 and 7. A line is 18 × N horizontal scan lines. N is determined by the character size in the vertical direction as follows: ×1 N = 1    ×2 N = 2 ×3 N = 3    ×4 N = 4																																					
		1							Can not be used.																																									
B	SPACE0	○							<table border="1" style="display: inline-table; vertical-align: middle;"> <thead> <tr> <th colspan="3">SPACE</th> <th rowspan="2">Number of Lines and Space ([S] represents space)</th> </tr> <tr> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>12</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1 [S] 10 [S] 1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>2 [S] 8 [S] 2</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>3 [S] 6 [S] 3</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>4 [S] 4 [S] 4</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>5 [S] 2 [S] 5</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>6 [S] 6</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>6 [S] [S] 6</td> </tr> </tbody> </table>	SPACE				Number of Lines and Space ([S] represents space)	2	1	0	0	0	0	12	0	0	1	1 [S] 10 [S] 1	0	1	0	2 [S] 8 [S] 2	0	1	1	3 [S] 6 [S] 3	1	0	0	4 [S] 4 [S] 4	1	0	1	5 [S] 2 [S] 5	1	1	0	6 [S] 6	1	1	1	6 [S] [S] 6	[S] represents one line worth of spaces.
		SPACE							Number of Lines and Space ([S] represents space)																																									
2	1	0																																																
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0	0	1	1 [S] 10 [S] 1																																															
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1	1	0	6 [S] 6																																															
1	1	1	6 [S] [S] 6																																															
1																																																		
C	SPACE1	○																																																
		1																																																
D	SPACE2	○																																																
		1																																																



(4) Address 123<sub>16</sub>

DA	Register	Contents		Remarks							
		Status	Function								
0	VP0 (LSB)	0	If VS is the vertical display start location,	The vertical start location is specified using the 10 bits from VP9 to VP0. VP9 to VP0 = (0000000002) setting is forbidden. Note 1: In case of B/F register is "0".							
		1	$VS = H \times (\sum_{n=0}^9 2^n VP_n)$ .								
1	VP1	0	H: Cycle with the horizontal synchronizing pulse 1023 settings are possible.								
		1									
2	VP2	0	<p>The diagram shows a vertical synchronizing pulse (VERT) and a horizontal synchronizing pulse (HOR). Within the VERT pulse, there is a horizontal pulse (HP) and a vertical pulse (VP). The intersection of HP and VP defines the 'Character displaying area'.</p>								
		1									
3	VP3	0									
		1									
4	VP4	0									
		1									
5	VP5	0									
		1									
6	VP6	0									
		1									
7	VP7	0									
		1									
8	VP8	0									
		1									
9	VP9 (MSB)	0									
		1									
A	TEST0	0	It should be fixed to "0".								
		1	Can not be used.								
B	TEST1	0	It should be fixed to "0".								
		1	Can not be used.								
C	TEST2	0	It should be fixed to "0".								
		1	Can not be used.								
D	TEST3	0	It should be fixed to "0".								
		1	Can not be used.								

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(5) Address 124<sub>16</sub>

DA	Register	Contents		Remarks
		Status	Function	
0	DSP0	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 1.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
1	DSP1	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 2.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
2	DSP2	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 3.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
3	DSP3	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 4.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
4	DSP4	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 5.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
5	DSP5	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 6.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
6	DSP6	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 7.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
7	DSP7	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 8.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
8	DSP8	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 9.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
9	DSP9	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 10.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
A	DSP10	0	Blanking is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 11.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
B	DSP11	0	Blanking is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 12.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
C	TEST4	0	It should be fixed to "0".	
		1	Can not be used.	
D	TEST5	0	It should be fixed to "0".	
		1	Can not be used.	

Note: Refer to DISPLAY FORM1.

(6) Address 125<sub>16</sub>

DA	Register	Contents		Remarks												
		Status	Function													
0	LIN2	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 2nd line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
1	LIN3	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 3rd line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
2	LIN4	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 4th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
3	LIN5	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 5th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
4	LIN6	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 6th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
5	LIN7	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 7th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
6	LIN8	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 8th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
7	LIN9	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 9th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
8	V1SZ0	○	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction for the 1st line. (display monitor 1 ~ 12 line)												
		1	<table border="1"> <thead> <tr> <th>V1SZ1</th> <th>V1SZ0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>		V1SZ1	V1SZ0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
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0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
A	VSZ1L0	○	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor 1 line) at "0" state in register LIN2 ~ LIN17.												
		1	<table border="1"> <thead> <tr> <th>VSZ1L1</th> <th>VSZ1L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>		VSZ1L1	VSZ1L0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
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1	1	4H/dot														
C	VSZ1H0	○	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor 1 line) at "1" state in register LIN2 ~ LIN17.												
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MITSUBISHI MICROCOMPUTERS  
M35045-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(7) Address 126<sub>16</sub>

DA	Register	Contents		Remarks												
		Status	Function													
0	LIN10	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 10th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
1	LIN11	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 11th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
2	LIN12	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 12th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
3	LIN13	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 13th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
4	LIN14	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 14th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
5	LIN15	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 15th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
6	LIN16	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 16th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
7	LIN17	○	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 17th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
8	V18SZ0	○	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction for the 18th line. (display monitor 1 ~ 12 line)												
		1	<table border="1"> <thead> <tr> <th>V18SZ1</th> <th>V18SZ0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>		V18SZ1	V18SZ0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
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0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
A	VSZ2L0	○	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor for 2 ~ 12 line) at "0" state in register LIN2 ~ LIN17.												
		1	<table border="1"> <thead> <tr> <th>VSZ2L1</th> <th>VSZ2L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>		VSZ2L1	VSZ2L0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
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1	1	4H/dot														
B	VSZ2L1	○														
		1	<table border="1"> <thead> <tr> <th>VSZ2L1</th> <th>VSZ2L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>		VSZ2L1	VSZ2L0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
VSZ2L1	VSZ2L0	Vertical direction size														
0	0	1H/dot														
0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
C	VSZ2H0	○	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor for 2 ~ 12 line) at "1" state in register LIN2 ~ LIN17.												
		1	<table border="1"> <thead> <tr> <th>VSZ2H1</th> <th>VSZ2H0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>		VSZ2H1	VSZ2H0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
VSZ2H1	VSZ2H0	Vertical direction size														
0	0	1H/dot														
0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
D	VSZ2H1	○														
		1	<table border="1"> <thead> <tr> <th>VSZ2H1</th> <th>VSZ2H0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>		VSZ2H1	VSZ2H0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
VSZ2H1	VSZ2H0	Vertical direction size														
0	0	1H/dot														
0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														

MITSUBISHI MICROCOMPUTERS  
M35045-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(8) Address 127<sub>16</sub>

DA	Register	Contents				Remarks		
		Status	Function					
0	RR	○	RB	RG	RR	Color	Sets the color of all blankings.	
		1	0	0	0	Black		
1	RG	○	0	0	1	Red		
			0	1	0	Green		
		1	0	1	1	Yellow		
			1	0	0	Blue		
2	RB	○	1	0	1	Magenta		
			1	1	0	Cyan		
3	FR	○	1	1	1	White		
			1	1	1	White		
4	FG	○	BB	BG	BR	Color	Sets the blanking color of the Border size, or the shadow size.	
			1	0	0	Black		
5	FB	○	0	0	1	Red		
			0	1	0	Green		
		1	0	1	1	Yellow		
			1	0	0	Blue		
6	TEST6	○	1	0	1	Magenta		
			1	1	0	Cyan		
7	TEST7	○	1	1	1	White		
			1	1	1	White		
8	TEST8	○	It should be fixed to "0".					
			Can not be used.					
9	BETA14	○	Matrix-outline display (12 × 18 dot)				Set this register to the character font set by display RAM BR, BG and BB.	
			Matrix-outline display (14 × 18 dot)					
A	HSZ10	○	T: Display frequency cycle				Character size setting in the vertical direction for the first line.	
			1	HSZ11	HSZ10	Vertical direction size		
B	HSZ11	○	0	0	1T/dot			
			0	1	2T/dot			
		1	1	0	3T/dot			
			1	1	4T/dot			
C	HSZ20	○	T: Display frequency cycle					Character size setting in the vertical direction for the 2nd line to 12th line.
			1	VSZ21	HSZ20	Vertical direction size		
D	HSZ21	○	0	0	1T/dot			
			0	1	2T/dot			
		1	1	0	3T/dot			
			1	1	4T/dot			

**MITSUBISHI MICROCOMPUTERS**  
**M35045-XXXSP/FP**

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(9) Address 128<sub>16</sub>

DA	Register	Contents		Remarks																		
		Status	Function																			
0	BCOL	0	Blanking of BLK0, BLK1	Sets all raster blanking																		
		1	All raster blanking																			
1	B/F	0	Synchronize with the leading edge of horizontal synchronization.	Synchronize with the front porch or back porch of the horizontal synchronization signal.																		
		1	Synchronize with the trailing edge of horizontal synchronization.																			
2	VMASK	0	Do not mask by VERT input signal	This register has or do not have mask at phase comparison operating.																		
		1	Mask by VERT input signal																			
3	POLV	0	VERT pin polarity is negative electrode	Set VERT pin polarity.																		
		1	VERT pin polarity is positive electrode																			
4	POLH	0	HOR pin polarity is negative electrode	Set HOR pin polarity.																		
		1	HOR pin polarity is positive electrode																			
5	BLK0	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <thead> <tr> <th colspan="2">BLK</th> <th rowspan="2">Blanking mode</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>Matrix-outline size</td> </tr> <tr> <td>0</td> <td>1</td> <td>Character size</td> </tr> <tr> <td>1</td> <td>0</td> <td>Border size</td> </tr> <tr> <td>1</td> <td>1</td> <td>Matrix-outline size</td> </tr> </tbody> </table>	BLK		Blanking mode	1	0		0	0	Matrix-outline size	0	1	Character size	1	0	Border size	1	1	Matrix-outline size	Set blanking mode. (Note 1) An example of blanking mode at BCOL = "0", DSPn = "0" (n = 0 ~ 11) shown left.
		BLK		Blanking mode																		
1	0																					
0	0	Matrix-outline size																				
0	1	Character size																				
1	0	Border size																				
1	1	Matrix-outline size																				
1																						
6	BLK1	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <thead> <tr> <th colspan="2">BLK</th> <th rowspan="2">Blanking mode</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>Matrix-outline size</td> </tr> <tr> <td>0</td> <td>1</td> <td>Character size</td> </tr> <tr> <td>1</td> <td>0</td> <td>Border size</td> </tr> <tr> <td>1</td> <td>1</td> <td>Matrix-outline size</td> </tr> </tbody> </table>	BLK		Blanking mode	1	0		0	0	Matrix-outline size	0	1	Character size	1	0	Border size	1	1	Matrix-outline size	
		BLK		Blanking mode																		
1	0																					
0	0	Matrix-outline size																				
0	1	Character size																				
1	0	Border size																				
1	1	Matrix-outline size																				
1																						
7	SYAD	0	Border display of character	(Note 2)																		
		1	Shadow display of character																			
8	RAMERS	0	RAM not erased	There is no need to reset because there is no register for this bit.																		
		1	RAM erased																			
9	STOP	0	Oscillation of clock for display	R, G, B and BLNK0 output can be altered.																		
		1	Stop the oscillation of clock for display																			
A	DSPON	0	Display OFF	Display can be altered.																		
		1	Display ON																			
B	BLINK0	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <thead> <tr> <th colspan="2">BLINK</th> <th rowspan="2">Duty</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>Blinking OFF</td> </tr> <tr> <td>0</td> <td>1</td> <td>25%</td> </tr> <tr> <td>1</td> <td>0</td> <td>50%</td> </tr> <tr> <td>1</td> <td>1</td> <td>75%</td> </tr> </tbody> </table>	BLINK		Duty	1	0		0	0	Blinking OFF	0	1	25%	1	0	50%	1	1	75%	Blinking duty ratio can be altered.
		BLINK		Duty																		
1	0																					
0	0	Blinking OFF																				
0	1	25%																				
1	0	50%																				
1	1	75%																				
1																						
C	BLINK1	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <thead> <tr> <th colspan="2">BLINK</th> <th rowspan="2">Duty</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>Blinking OFF</td> </tr> <tr> <td>0</td> <td>1</td> <td>25%</td> </tr> <tr> <td>1</td> <td>0</td> <td>50%</td> </tr> <tr> <td>1</td> <td>1</td> <td>75%</td> </tr> </tbody> </table>	BLINK		Duty	1	0		0	0	Blinking OFF	0	1	25%	1	0	50%	1	1	75%	
		BLINK		Duty																		
1	0																					
0	0	Blinking OFF																				
0	1	25%																				
1	0	50%																				
1	1	75%																				
1																						
D	BLINK2	0	Divided into 64 of vertical synchronous signal	Blinking frequency can be altered.																		
		1	Divided into 32 of vertical synchronous signal																			

Notes 1: Refer to DISPLAY FORM 1  
2: Refer to DISPLAY FORM 3

**DISPLAY FORM1**

Table 1 shows display form of blanking.

**Table 1. Display mode**

BCOL	Standard blanking		When the all of registers DSPn (Note 2) are set to "0"	When some of registers DSPi are set to "1"		BLNK0 output
	BLK1	BLK0		DSPn = 0	DSPn = 1	
0	0	0	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline display color set: display RAM (Note 3)	DSPn = "0" line } Matrix-outline size DSPn = "1" line }
	0	1	Character	Character	Border display color set: display RAM (Note 3)	DSPn = "0" line → Character size DSPn = "1" line → Border size
	1	0	Border display color set: display RAM (Note 3)	Border display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	DSPn = "0" line → Border size DSPn = "1" line → Matrix-outline size
	1	1	Matrix-outline display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	Character	DSPn = "0" line → Matrix-outline size DSPn = "1" line → Character size
1 (Note 1)	0	0	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline display color set: display RAM (Note 3)	All blanking size
	0	1	Character	Character	Border display color set: display RAM (Note 3)	
	1	0	Border display color set: display RAM (Note 3)	Border display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	
	1	1	Matrix-outline display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	Character	

Notes 1: Color setting of raster area is set by register RR, RG and RB.

2: DSPn (n = 0 ~ 11)

3: Set by BR, BG and BB of display RAM.

4: Set border by register FR, FG and FB. Set matrix-outline by BR, BG and BB of display RAM.

## Display form 2

M35045-XXXSP has the following four display forms.

- (1) Character size  
: Blanking same as the character size.
- (2) Border size  
: Blanking the background as a size from character.
- (3) Matrix-outline size  
: Blanking the background 12 × 18 dot.  
When set register BETA14 to "1", setting of blanking the background 14 × 18 dot is possible.
- (4) All blanking size  
: When set register BCOL to "1", all raster area is blanking.

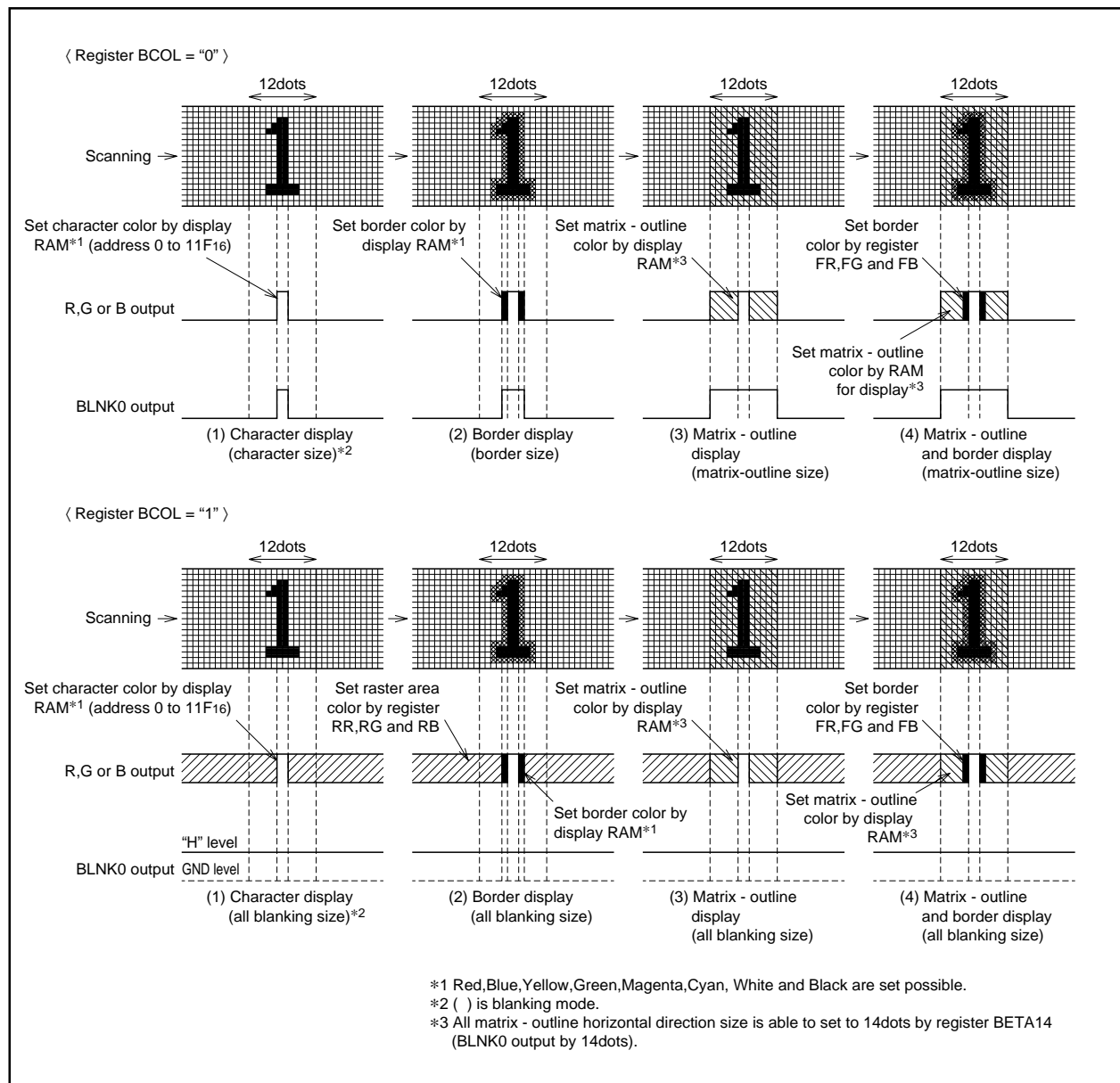


Fig. 3 Display form



### Display form 3

When border display mode, if set SYAD = "0" to "1", it change to shadow display mode.

Border and shadow display are shown below.

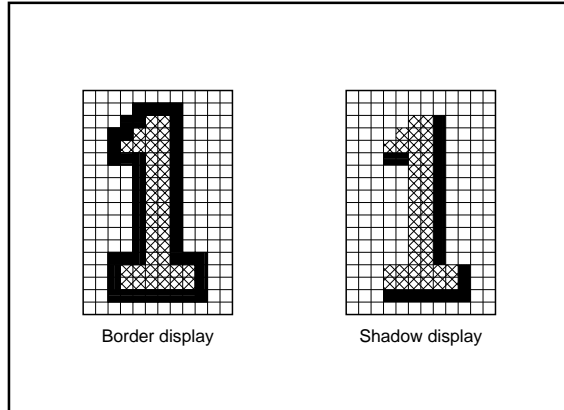


Fig. 4 Border and shadow display

Set shadow display color by display RAM or register FR, FG and FB.

**DATA INPUT EXAMPLE**

Data of display RAM and display control registers can be set by the serial input function. Example of data setting is shown in Figure 5.

		DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Addition
		200 msec hold																System set-up
1	address 120 <sub>16</sub>	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	Address set
2	data 120 <sub>16</sub>	0	0	0	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	Setting frequency dividing value (Note 1)
3	data 121 <sub>16</sub>	0	0	PTD7	PTD6	1	PTD4	1	PTD2	1	1	1	0	1	0	1	1	Output setting
4	data 122 <sub>16</sub>	0	0	0	0	0	0	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display location setting
5	data 123 <sub>16</sub>	0	0	0	0	0	0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display location setting
6	data 124 <sub>16</sub>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Display form setting
7	data 125 <sub>16</sub>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
8	data 126 <sub>16</sub>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
9	data 127 <sub>16</sub>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Color, character size setting
10	data 128 <sub>16</sub>	0	0	0	0	0	0	0	1	0	1	1	POLH	POLV	0	0	0	Display OFF, display form (Note 2)
		200 msec hold																
11	data 000 <sub>16</sub>	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0	Character setting
12	⋮	⋮	Character background color			Blinking	Character color			Character code								
⋮	⋮	⋮																
297	⋮	⋮																
298	data 11F <sub>16</sub>	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0	
299	address 128 <sub>16</sub>	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	Address setting
300	data 128 <sub>16</sub>	0	0	0	0	0	1	0	0	0	1	1	POLH	POLV	0	0	0	Display ON, display form (Note 2)

Notes 1: Input horizontal synchronous signal to HOR pin.  
2: Matrix-outline display in this data.

Fig. 5 Example of data setting by the serial input function

**SERIAL DATA INPUT TIMING**

- (1) Serial data should be input with the LSB first.
- (2) The address consists of 16 bits.
- (3) The data consists of 16 bits.
- (4) The 16 bits in the SCK after the CS signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits.

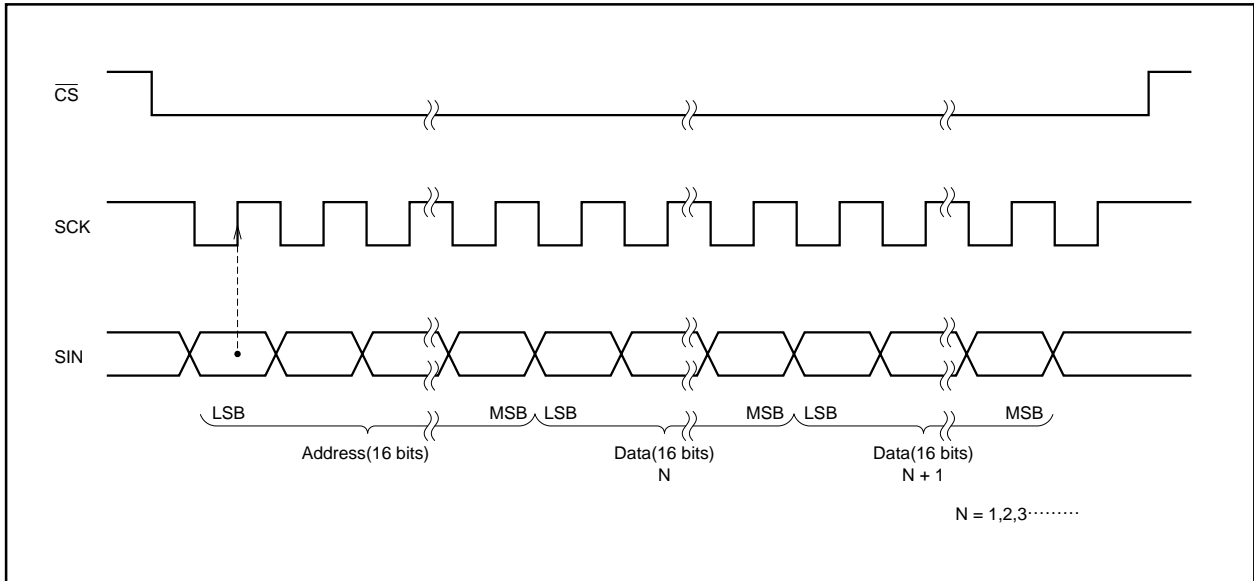


Fig. 6 Serial input timing

### CHARACTER FONT

Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

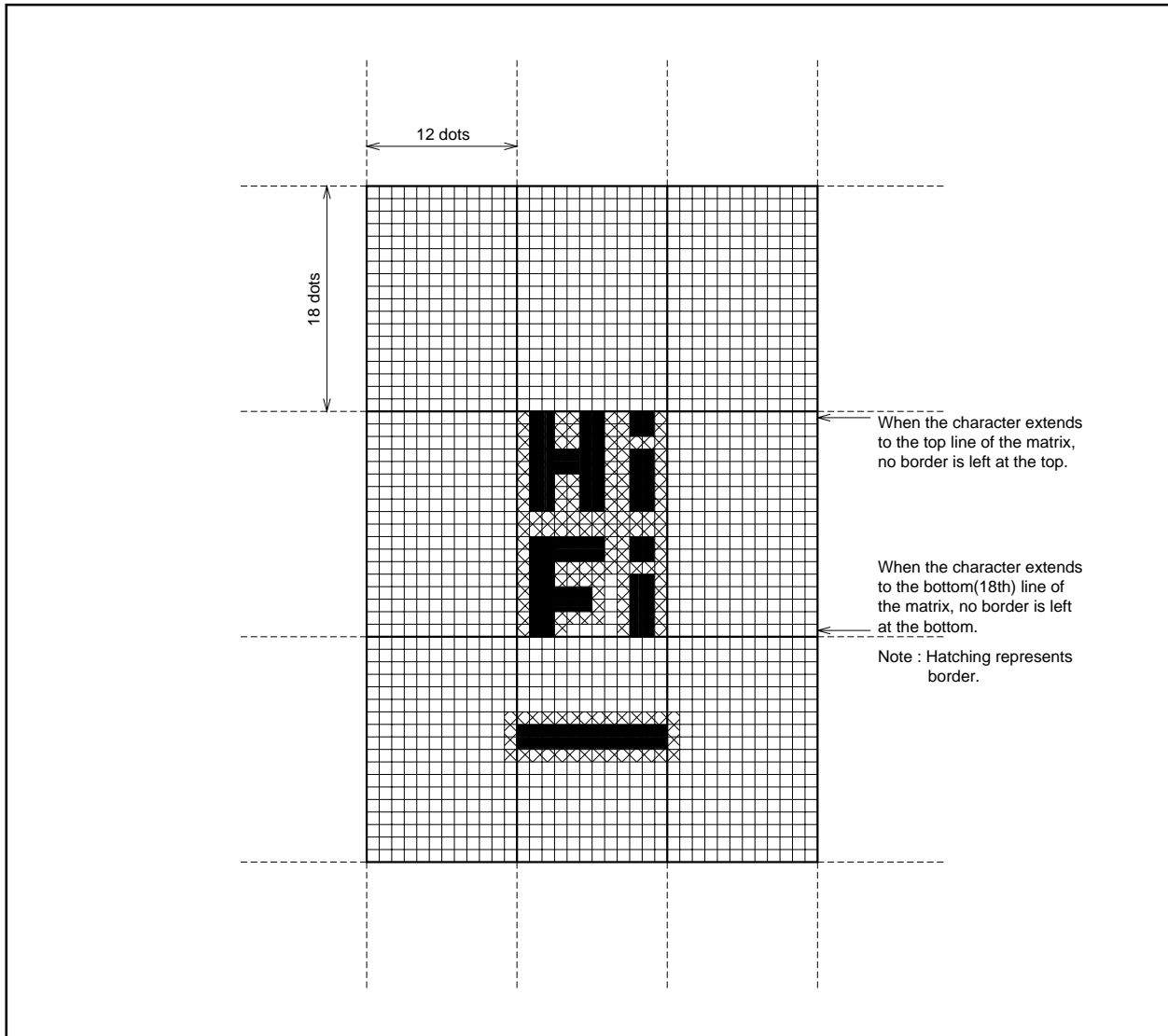
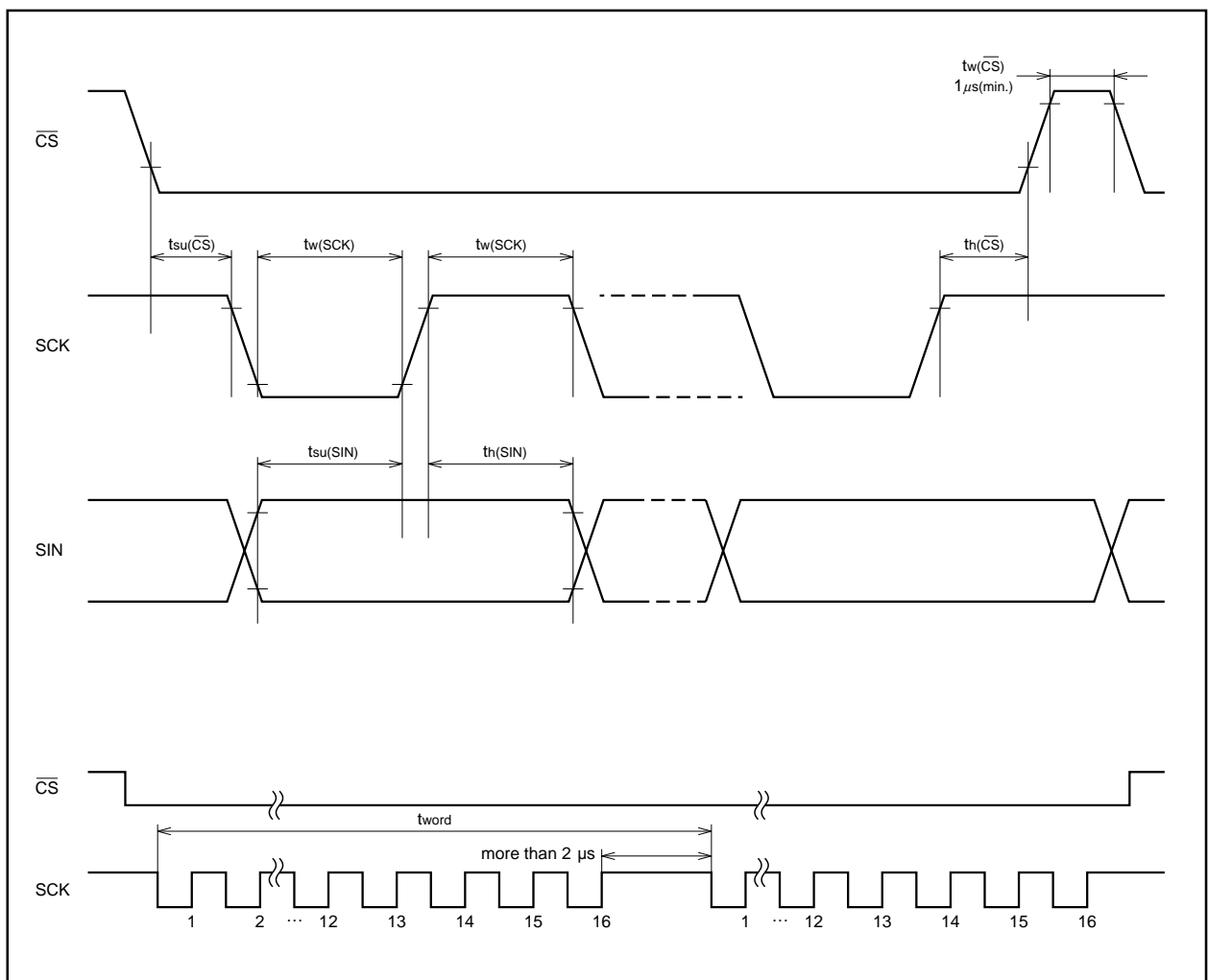


Fig. 7 Example for displaying a continuous pattern after combining characters in the horizontal or vertical direction

Character code FF<sub>16</sub> is fixed as a blank without background.  
Therefore, you cannot register a character font in this code.

**TIMING REQUIREMENTS** ( $T_a = -20^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 5 \pm 0.25\text{V}$ , unless otherwise noted)

Symbol	Parameter	Limits			Unit	Remarks
		Min.	Typ.	Max.		
$t_w(\text{SCK})$	SCK width	200	—	—	ns	See Figure 8
$t_{su}(\overline{\text{CS}})$	$\overline{\text{CS}}$ setup time	200	—	—	ns	
$t_h(\overline{\text{CS}})$	$\overline{\text{CS}}$ hold time	2	—	—	$\mu\text{s}$	
$t_{su}(\text{SIN})$	SIN setup time	200	—	—	ns	
$t_h(\text{SIN})$	SIN hold time	200	—	—	ns	
$t_{\text{word}}$	1 word writing time	10	—	—	$\mu\text{s}$	



**Fig. 8** Serial input timing requirements

EXAMPLE OF THE M35045-XXXSP/FP CLOCK PERIPHERAL CIRCUIT

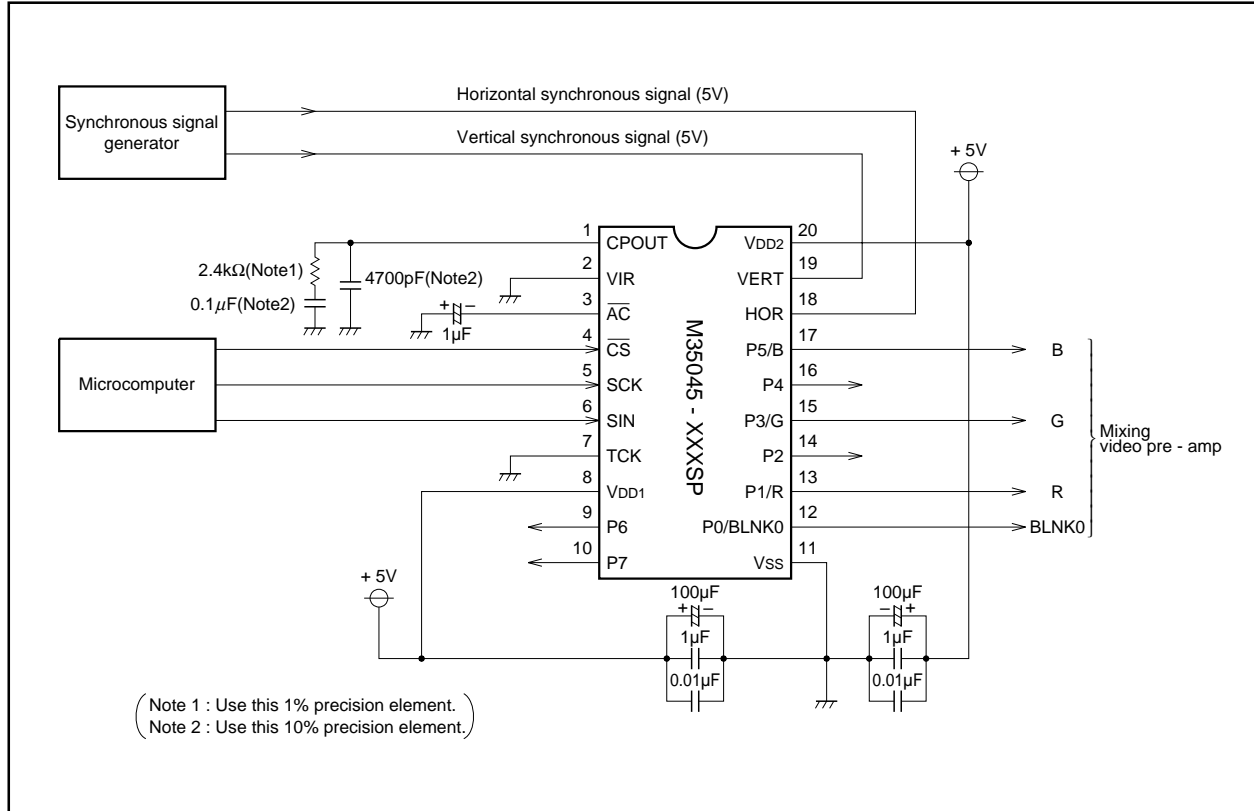


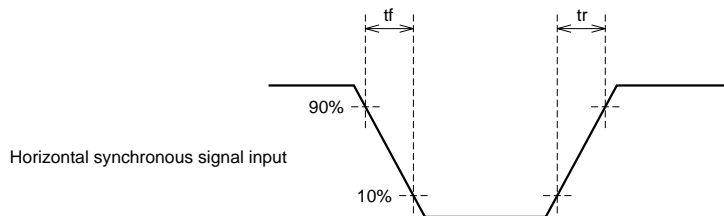
Fig. 9 Example of the M35045-XXXSP peripheral circuit (M35045-XXXFP peripheral circuit is same as that of M35045-XXXSP)

**Note for waveform timing of the horizontal signals to the HOR pin.**

Set horizontal synchronous signal edge\* waveform timing to under 5ns and input to HOR pin.

Set only the side which set by B/F register waveform timing under 5ns and input to HOR pin.

\*: Set front porch edge or back porch edge by B/F register.



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
VDD	Supply voltage	With respect to VSS.	-0.3 to +6.0	V
Vi	Input voltage		VSS -0.3 < Vi < VDD +0.3	V
Vo	Output voltage		VSS < Vo < VDD	V
Pd	Power dissipation	Ta = 25°C	300	mW
Topr	Operating temperature		-20 to +85	°C
Tstg	Storage temperature		-40 to +125	°C

**RECOMMENDED OPERATING CONDITIONS** (VDD = 5V, Ta = -20 to +85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
VDD	Supply voltage	4.75	5.0	5.25	V
VIH	"H" level input voltage SIN, SCK, CS, AC HOR, VERT	0.8VDD	VDD	VDD	V
VIL	"L" level input voltage SIN, SCK, CS, AC HOR, VERT	0	0	0.2VDD	V
FOSC	Oscillating frequency for display	30.0	—	80.0	MHz

**ELECTRICAL CHARACTERISTICS** (VDD = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
VDD	Supply voltage		Ta = -20 to +85°C	4.75	5.0	5.25	V
IDD	Supply current		VDD = 5.25V	—	30	50	mA
VOH	"H" level output voltage	P0 ~ P7	VDD = 4.75V, IOH = 0.4mA	3.5	—	—	V
		CPOUT	VDD = 4.75V, IOH = 0.05mA				
VOL	"L" level output voltage	P0 ~ P7	VDD = 4.75V, IOL = 0.4mA	—	—	0.4	V
		CPOUT	VDD = 4.75V, IOL = 0.05mA				
RI	Pull-up resistance SCK, AC, CS, SIN		VDD = 5.0V	10	30	100	kΩ

**Note for Supplying Power**

Timing of power supplying to AC pin

The internal circuit of M35045-XXXSP/FP is reset when the level of the auto clear input pin  $\overline{AC}$  is "L". This pin is hysteresis input with the pull-up resistor. The timing about power supplying of AC pin is shown in Figure 10.

Timing of power supplying to  $V_{DD1}$  and  $V_{DD2}$ .

Supply power to  $V_{DD1}$  and  $V_{DD2}$  at the same time.

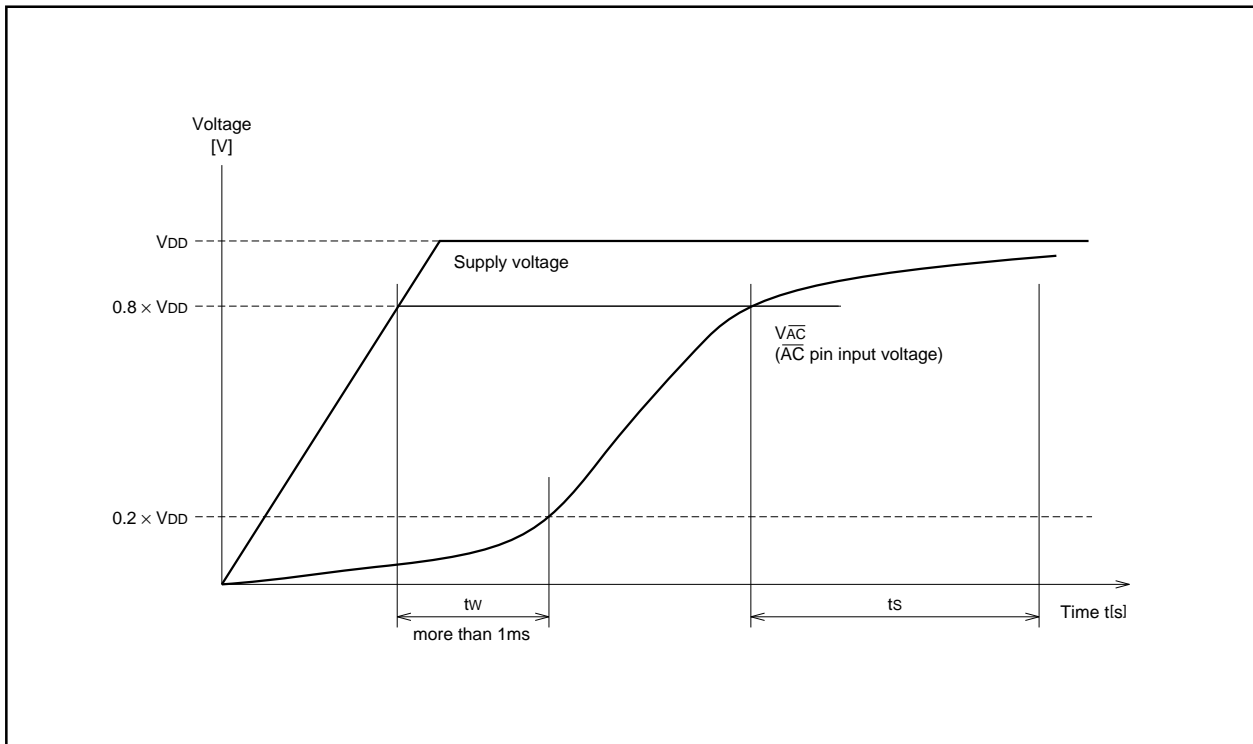


Fig. 10 Timing of power supplying to  $\overline{AC}$  pin

After supplying the power ( $V_{DD}$  and  $V_{SS}$ ) to M35045-XXXSP/FP and the supply voltage becomes more than  $0.8 \times V_{DD}$ , it needs to keep  $V_{IL}$  time;  $t_w$  of the AC pin for more than 1ms.

Start inputting from microcomputer after AC pin supply voltage becomes more than  $0.8 \times V_{DD}$  and keeping 200ms wait time.

**PRECAUTION FOR USE**

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor ( $\approx 0.1\mu F$ ) directly between the  $V_{DD1}$  pin and  $V_{SS}$  pin, and the  $V_{DD2}$  pin and  $V_{SS}$  pin using a heavy wire.

**DATA REQUIRED FOR MASK ROM ORDERING**

Please send the following data for mask orders.

- (1) M35045-XXXSP/FP mask ROM order confirmation form
- (2) 20P4B mask specification form
- (3) ROM data (EPROM 3 sets)
- (4) Floppy disks containing the character font generating program + character data



**STANDARD ROM TYPE : M35045-002SP/FP**

M35045-002SP/FP is a standard ROM type of M35045-XXXSP/FP.  
The character patterns are fixed to the contents of Figure 11 to 16.

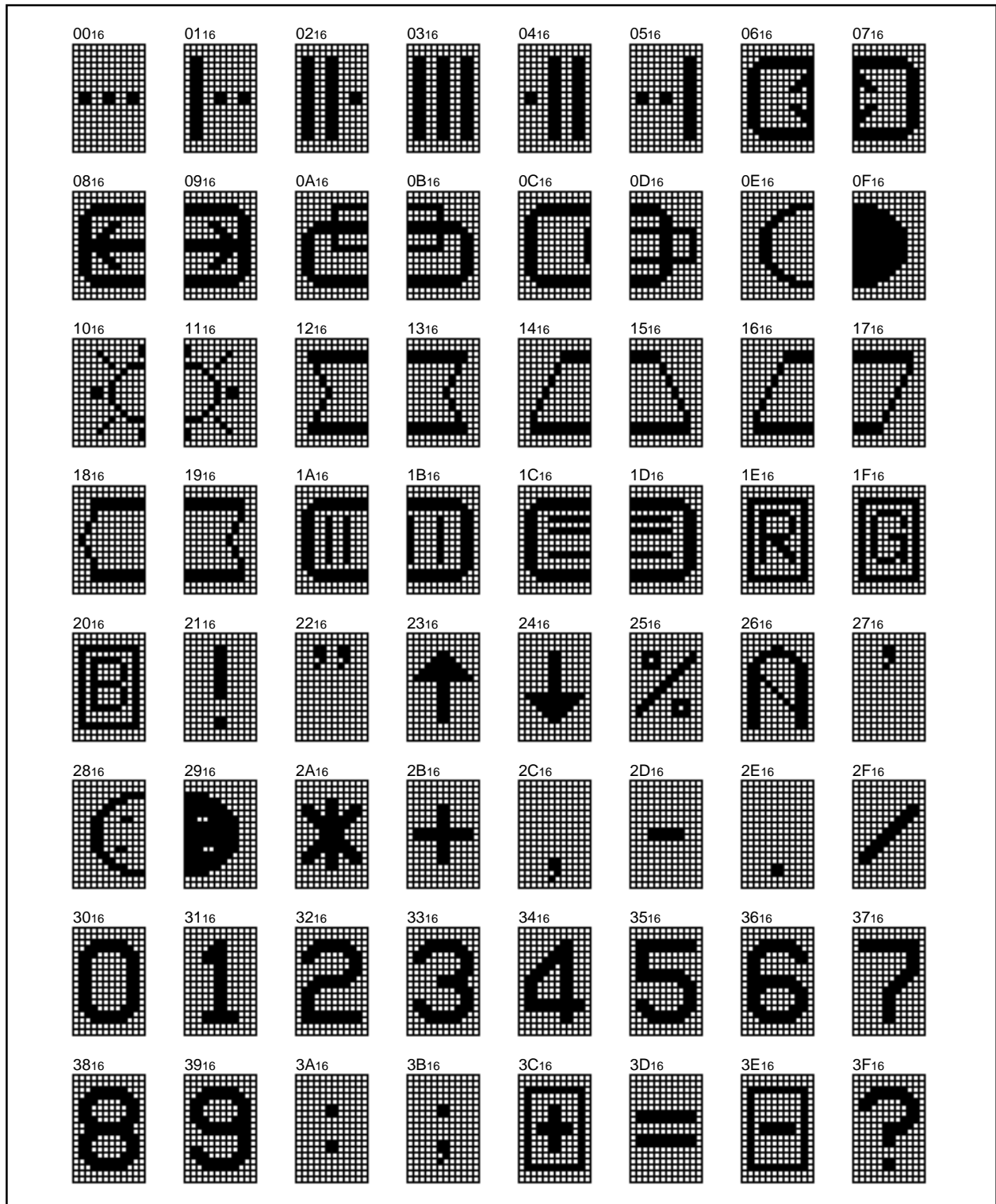


Fig. 11 M35045-002SP/FP character patterns (1)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

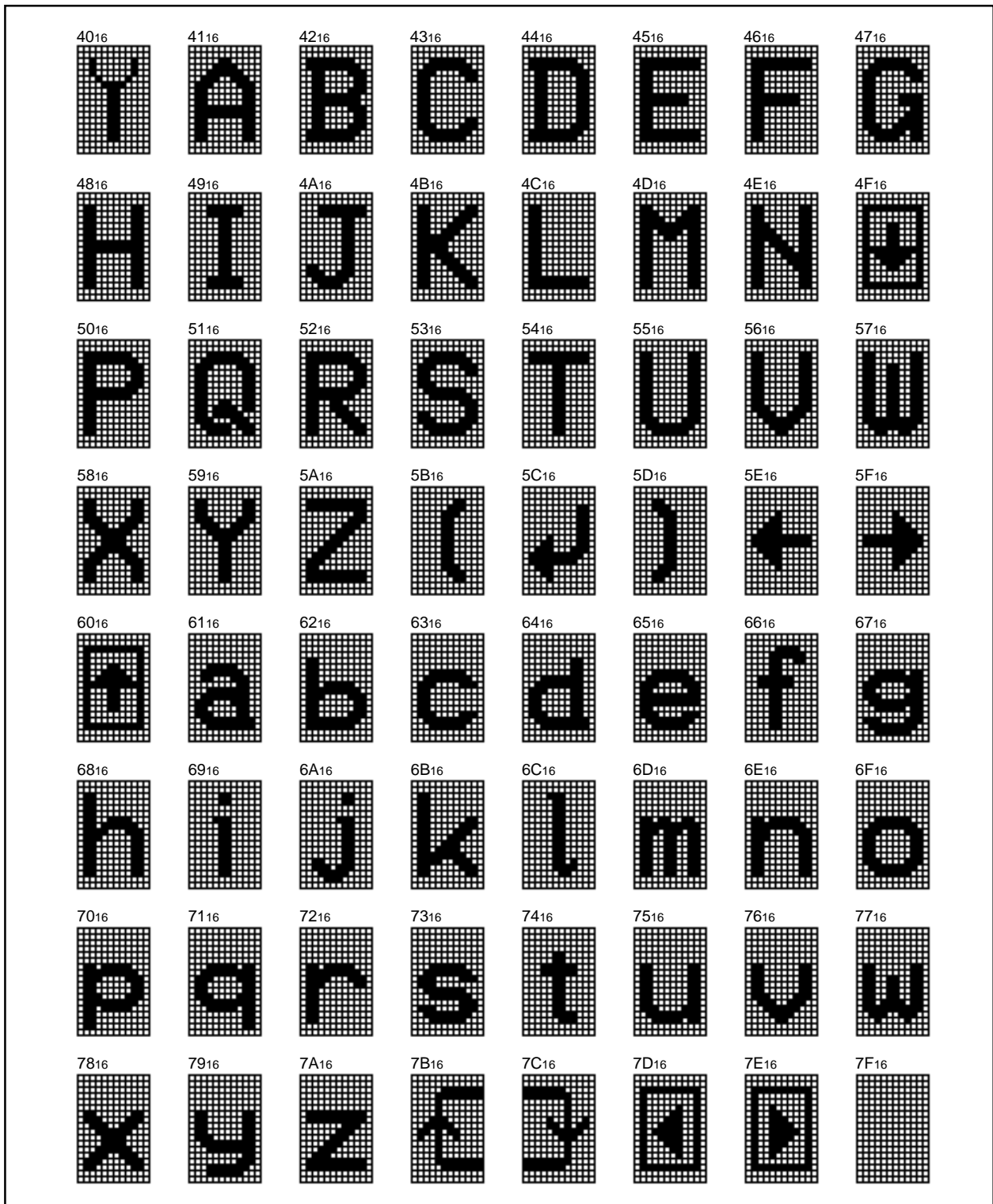


Fig. 12 M35045-002SP/FP character patterns (2)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

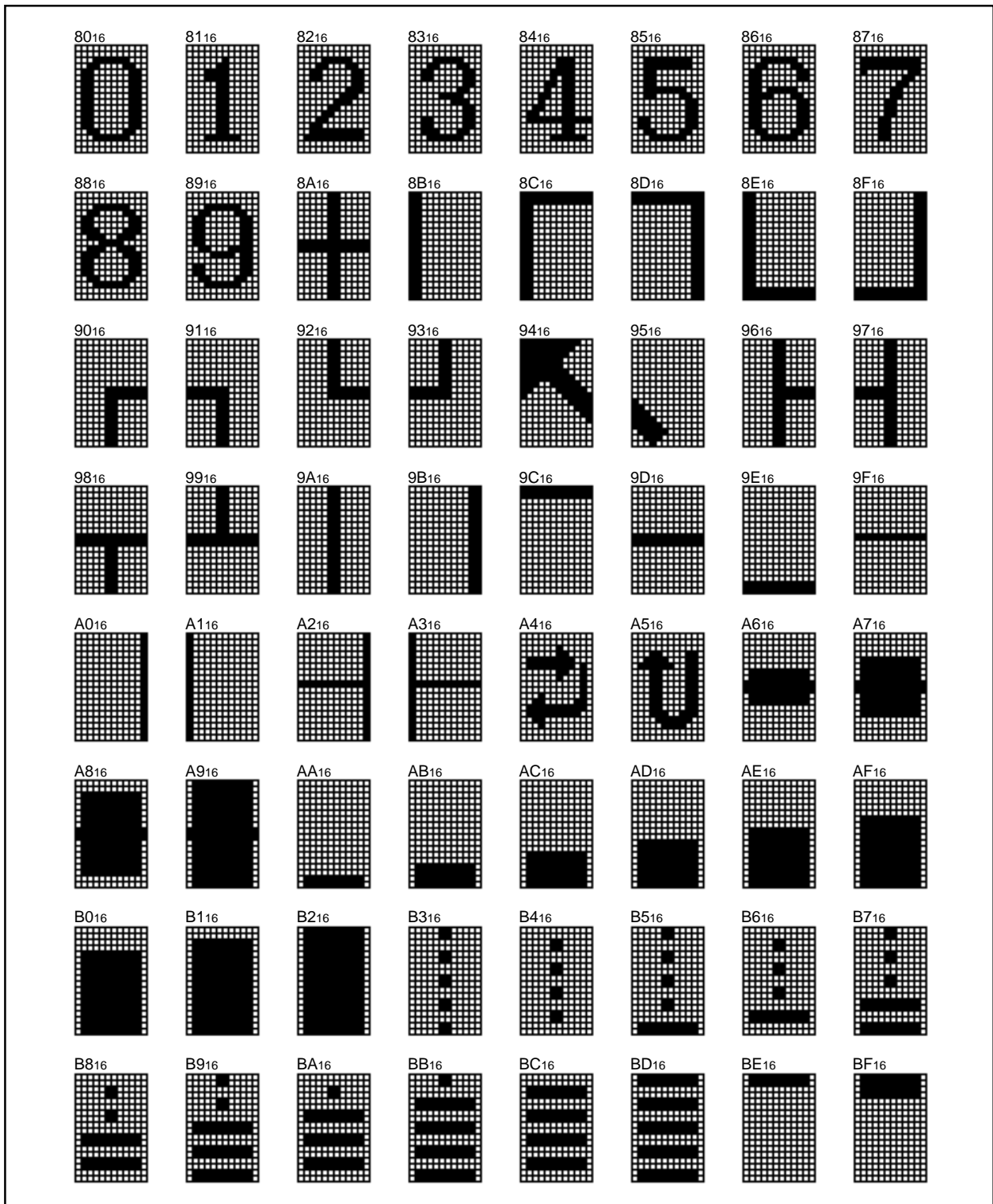


Fig. 13. M35045-002SP/FP character patterns (3)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

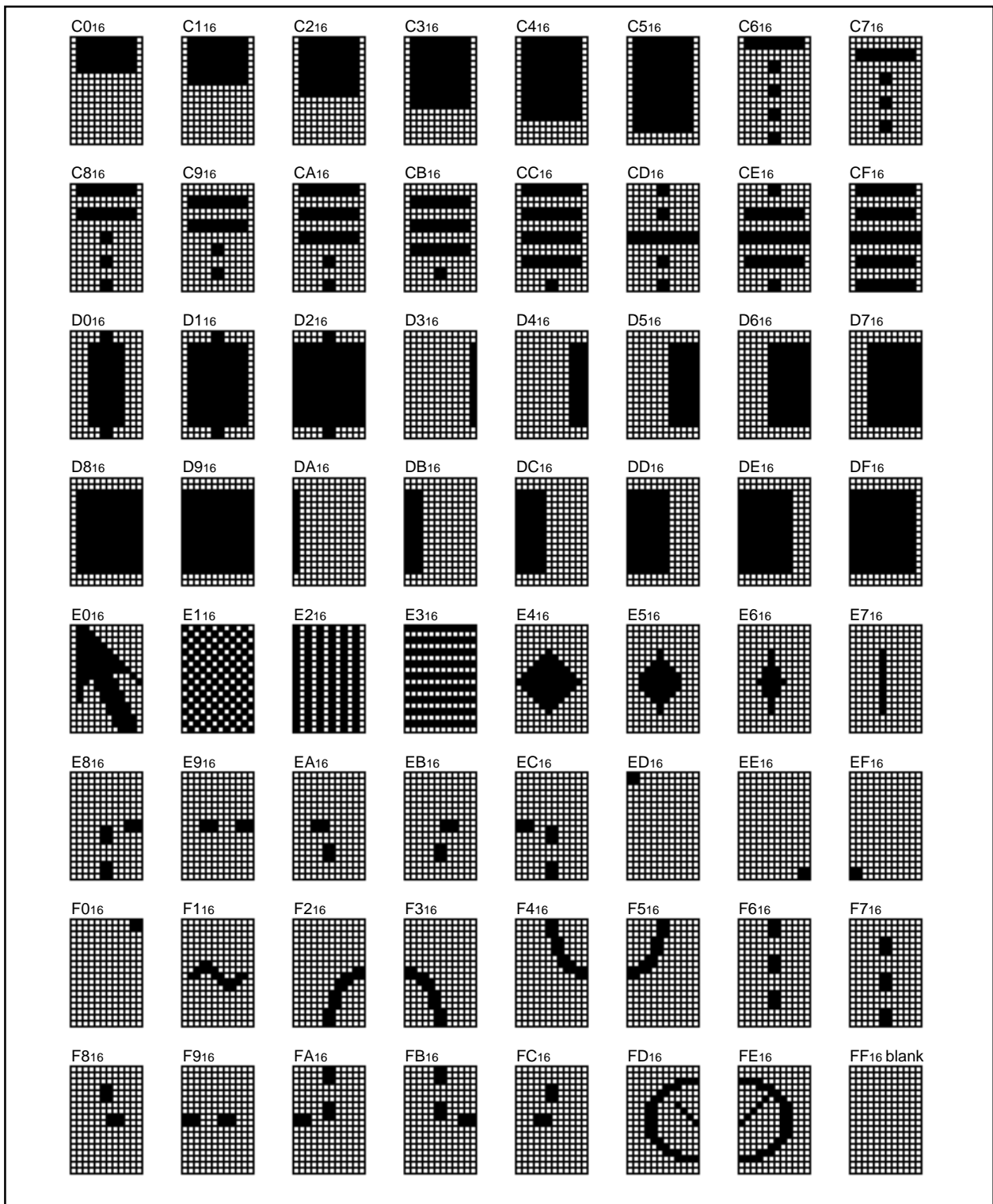
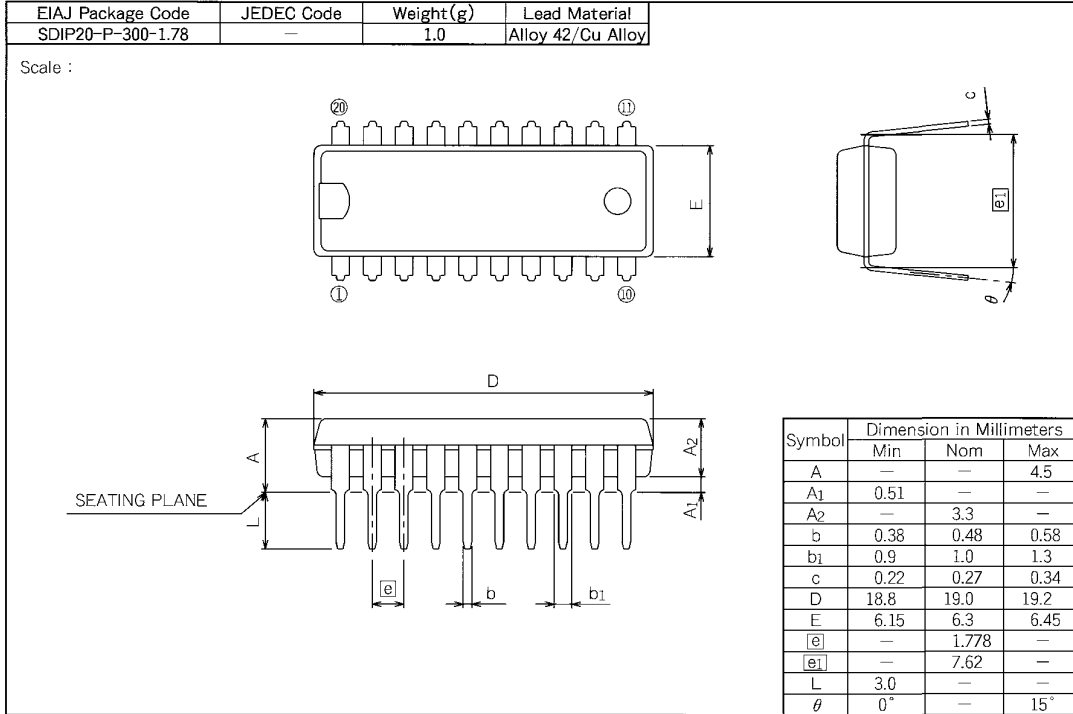


Fig. 14 M35045-002SP/FP character patterns (4)

**PACKAGE OUTLINE**

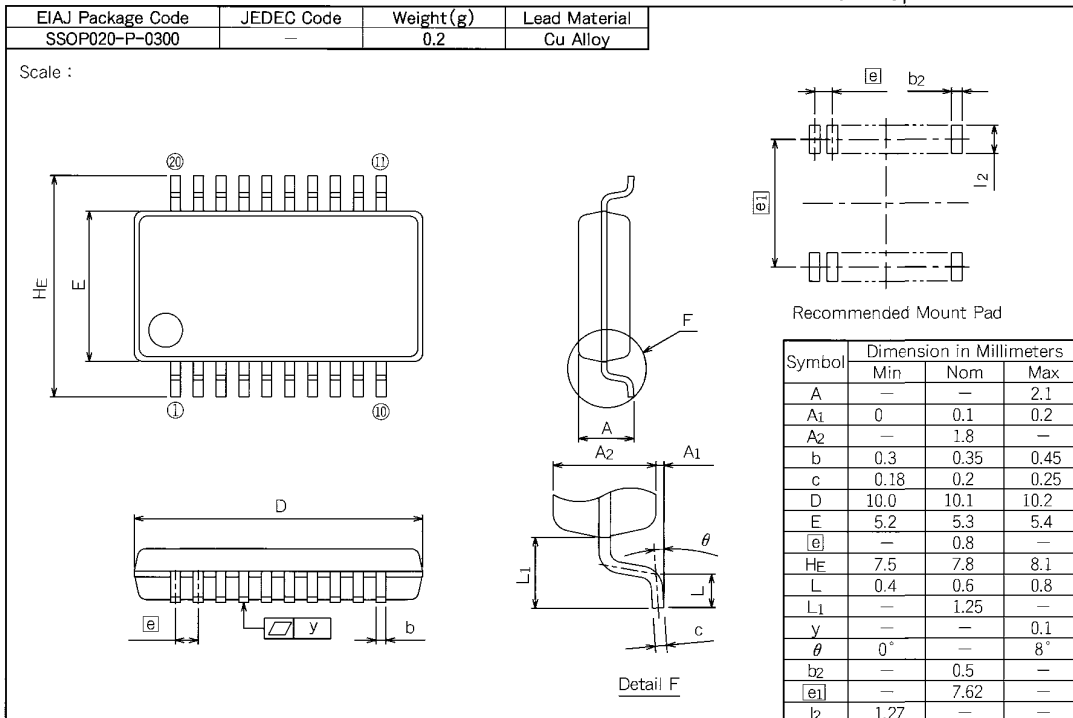
**20P4B**

Plastic 20pin 300mil SDIP



**20P2Q-A**

Plastic 20pin 300mil SSOP



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REVISION DESCRIPTION LIST

M35045-XXXSP/FP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	9706
1.1	Delete Mask ROM ORDER CONFIRMATION FORM and MASK SPECIFICATION FORM	0008