# HM628127H/HM629127H Series

**131072-word × 8/9-bit High Speed CMOS Static RAM**

The HM628127H/HM629127H is an asynchronous high speed static RAM organized as 131,072-word × 8/9-bit. It realizes high speed access time (20/25 ns) with employing 0.8 µm CMOS process and high speed circuit designing technology.

It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system.

The HM628127H/HM629127H is packaged in 400-mil 32/36-pin SOJ for high density surface mounting.

## Features

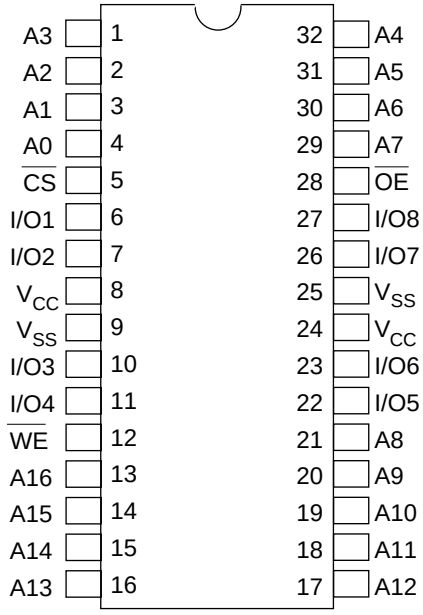
- Single 5 V supply: 5 V ± 10%
- Access time 20/25 ns (max)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - All inputs and outputs
- 400-mil 32/36-pin SOJ package
- Center $V_{CC}$ and $V_{SS}$ type pinout

## Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HM628127HJP-20 | 20 ns | 400-mil 32-pin plastic SOJ (CP-32DB) |
| HM628127HJP-25 | 25 ns | |
| HM628127HLJP-20 | 20 ns | |
| HM628127HLJP-25 | 25 ns | |
| HM629127HJP-20 | 20 ns | 400-mil 36-pin Plastic SOJ (CP-36D) |
| HM629127HJP-25 | 25 ns | |
| HM629127HLJP-20 | 20 ns | |
| HM629127HLJP-25 | 25 ns | |

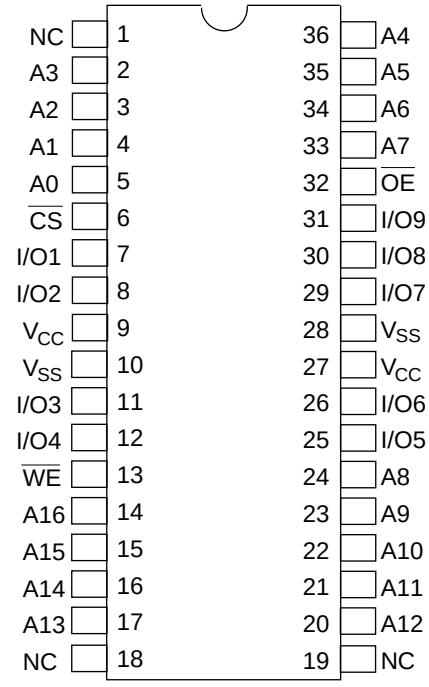
## Pin Arrangement

HM628127H Series




(Top View)

HM629127H Series



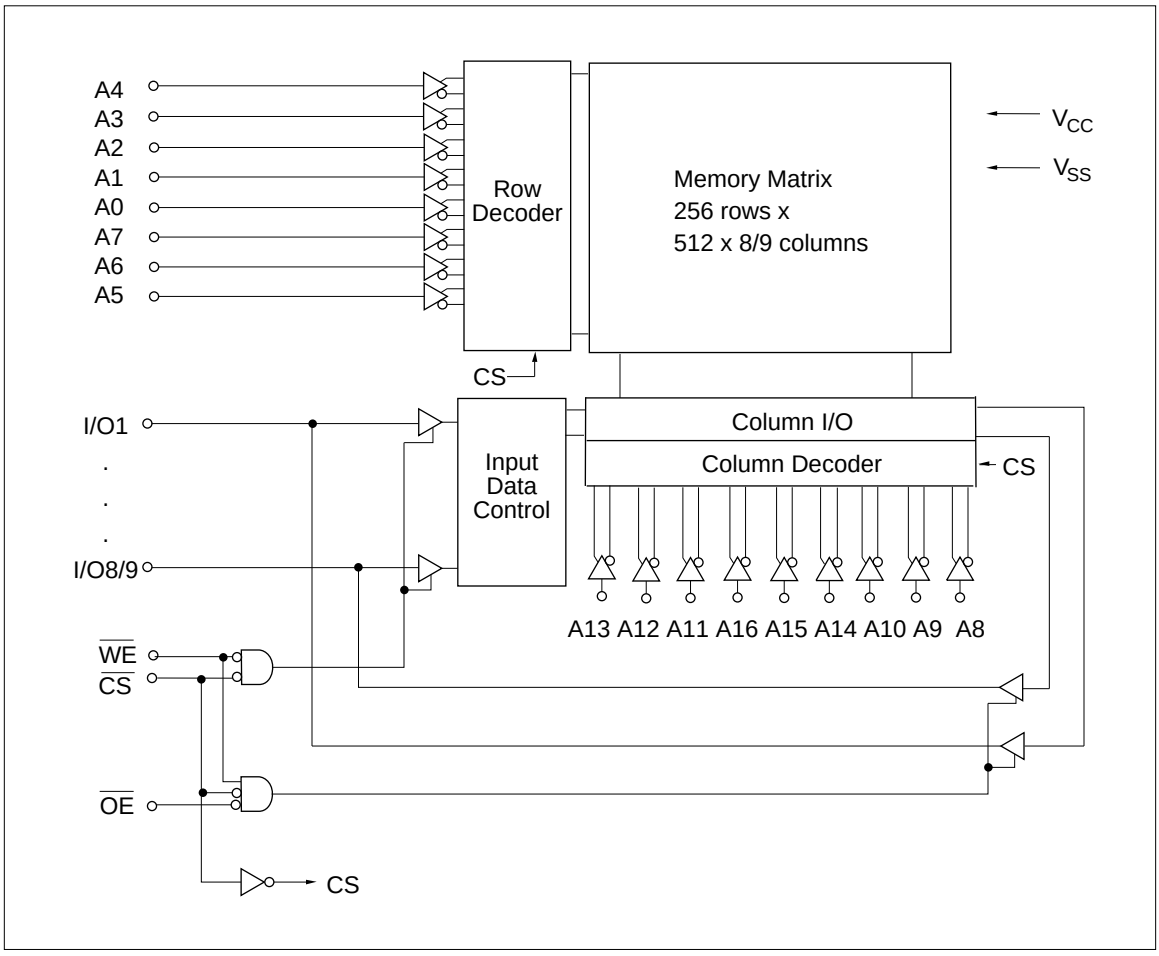

(Top View)

## Pin Description

**Pin name**

| HM628127H | HM629127H | Function |
|---|---|---|
| A0 – A16 | A0 – A16 | Address |
| I/O1 – I/O8 | I/O1 – I/O9 | Data input/output |
| $\overline{CS}$ | $\overline{CS}$ | Chip select |
| $\overline{WE}$ | $\overline{WE}$ | Write enable |
| $\overline{OE}$ | $\overline{OE}$ | Output enable |
| $V_{CC}$ | $V_{CC}$ | Power supply |
| $V_{SS}$ | $V_{SS}$ | Ground |
| — | NC | No connection |

## Block Diagram




## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage relative to $V_{SS}$ | $V_{CC}$ | –0.5 to +7.0 | V |
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | –0.5 *1 to $V_{CC}$ + 0.5 | V |
| Power dissipation | $P_T$ | 1.0*2 / 1.5*3 | W |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | –55 to +125 | °C |
| Storage temperature under bias | Tbias | –10 to +85 | °C |

Note: 1. –2.5 V for pulse width (under shoot) ≤ 10 ns
2. at still air condition
3. at air flow ≥ 1.0 m/s

## Function Table

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | $V_{CC}$ current | I/O | Ref. cycle |
|---|---|---|---|---|---|
| H | X | X | $I_{SB}$, $I_{SB1}$ | High-Z | — |
| L | H | H | $I_{CC}$ | High-Z | — |
| L | L | H | $I_{CC}$ | Output | Read cycle |
| L | X | L | $I_{CC}$ | Input | Write cycle |

Note: X: H or L

## Recommended DC Operating Conditions (Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage*2 | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$ | 0 | 0 | 0 | V |
| Input voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$ + 0.5 | V |
| | $V_{IL}$ | –0.5 *1 | — | 0.8 | V |

Note: 1. –2.0 V for pulse width (under shoot) ≤ 10 ns
2. The supply voltage with all $V_{CC}$ pins must be on the same level.
The supply voltage with all $V_{SS}$ pins must be on the same level.

## DC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V)

| Parameter | Symbol | Min | Typ*1 | Max | Unit | Test conditions | Notes |
|---|---|---|---|---|---|---|---|
| Input leakage current | $\|I_{LI}\|$ | — | — | 2 | µA | Vin = $V_{SS}$ to $V_{CC}$ | |
| Output leakage current | $\|I_{LO}\|$ | — | — | 2 | µA | $V_{I/O}$ = $V_{SS}$ to $V_{CC}$ | |
| Operating power supply current | $I_{CC}$ | — | 130 | 180 | mA | 20 ns cycle, $\overline{CS}$ = $V_{IL}$, Iout = 0 mA | |
| | | — | 100 | 160 | mA | 25 ns cycle, Other inputs = $V_{IH}$/$V_{IL}$ | |
| Standby power supply current | $I_{SB}$ | — | 50 | 90 | mA | 20 ns cycle, $\overline{CS}$ = $V_{IH}$, Other inputs | |
| | | — | 40 | 85 | mA | 25 ns cycle, = $V_{IH}$/$V_{IL}$ | |
| Standby power supply current (1) | $I_{SB1}$ | — | — | 2 | mA | $V_{CC}$ ≥ $\overline{CS}$ ≥ $V_{CC}$ – 0.2 V, 0 V ≤ Vin ≤ 0.2 V or $V_{CC}$ ≥ Vin ≥ $V_{CC}$ – 0.2 V | |
| | | — | — | 0.2 | mA | | L-version |
| Output voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 8 mA | |
| | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = –4 mA | |

Note: 1. Typical values are at $V_{CC}$ = 5.0 V, Ta = +25°C and specified loading.

## Capacitance (Ta = 25°C, f = 1.0 MHz)*1

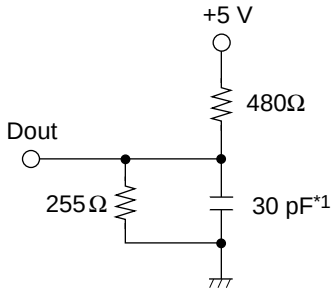
| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input capacitance | Cin | — | — | 6 | pF | Vin = 0 V |
| Input/output capacitance | $C_{I/O}$ | — | — | 8 | pF | $V_{I/O}$ = 0 V |

Note: 1. This parameter is sampled and not 100% tested.

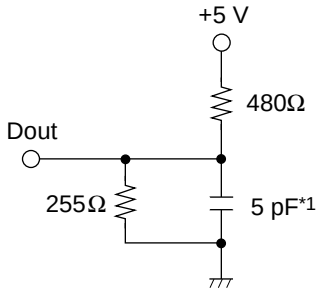
## AC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%, unless otherwise noted.)

### Test Conditions

- Input pulse levels: $V_{SS}$ to 3.0 V
- Input rise and fall times: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures




Output load (A)



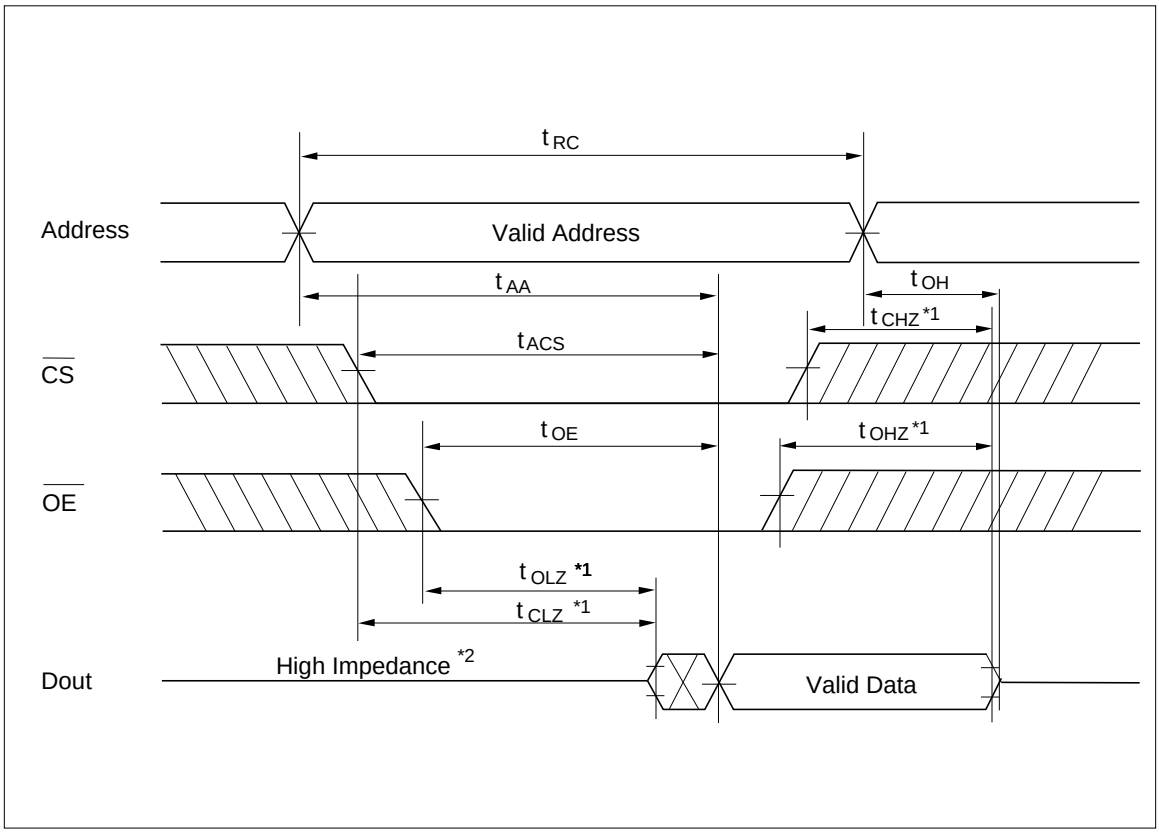

Output load (B)
(for $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{WHZ}$, and $t_{OW}$)

Note: 1. Including scope and jig

### Read Cycle

| | | HM628127H/HM629127H | | | | |
|---|---|---|---|---|---|---|
| | | -20 | | -25 | | |
| Parameter | Symbol | Min | Max | Min | Max | Unit |
| Read cycle time | $t_{RC}$ | 20 | — | 25 | — | ns |
| Address access time | $t_{AA}$ | — | 20 | — | 25 | ns |
| Chip select access time | $t_{ACS}$ | — | 20 | — | 25 | ns |
| Output enable to output valid | $t_{OE}$ | — | 10 | — | 12 | ns |
| Output hold from address change | $t_{OH}$ | 5 | — | 5 | — | ns |
| Chip select to output in low-Z | $t_{CLZ}$ | 3 | — | 3 | — | ns |
| Output enable to output in low-Z | $t_{OLZ}$ | 1 | — | 1 | — | ns |
| Chip deselect to output in high-Z | $t_{CHZ}$ | — | 7 | — | 7 | ns |
| Output disable to output in high-Z | $t_{OHZ}$ | — | 7 | — | 7 | ns |

**Read Timing Waveform*3**

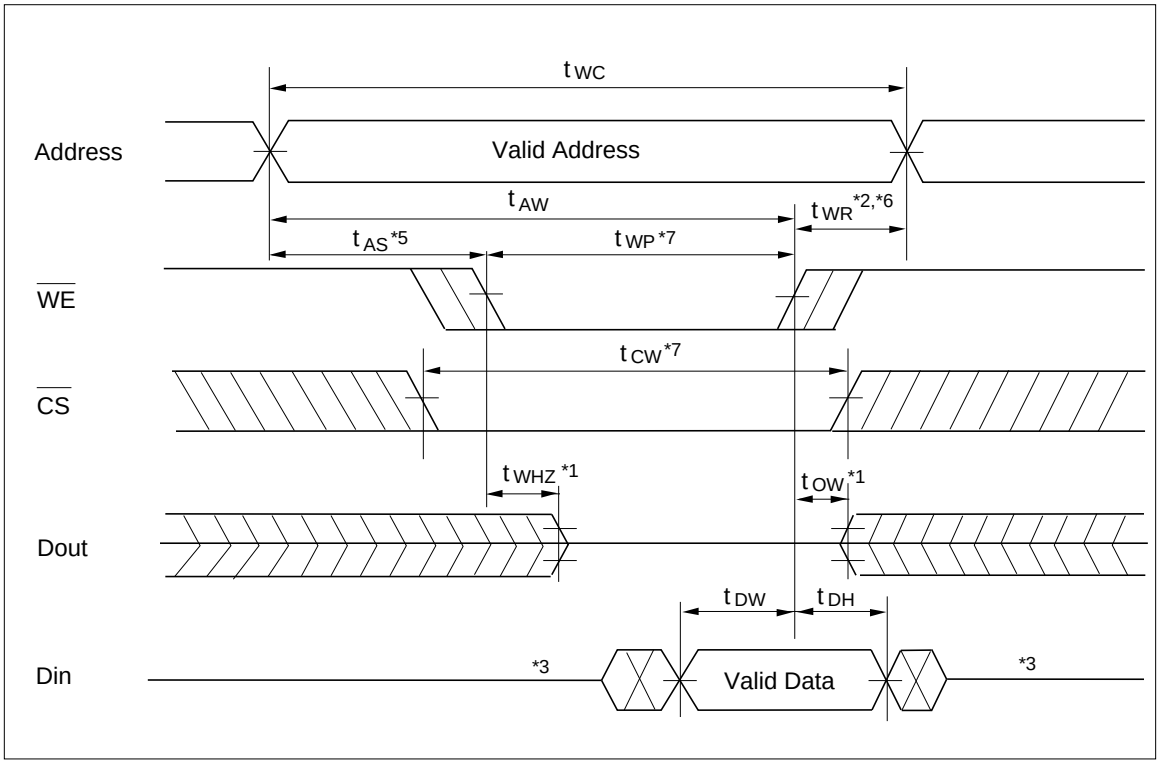



Notes: 1. Transition is measured ±200 mV from steady state's voltage with Load (B). This parameter is sampled and not 100% tested.
2. When $\overline{CS}$ and $\overline{OE}$ are low, Dout is low impedance.
3. $\overline{WE}$ is high for read cycle.

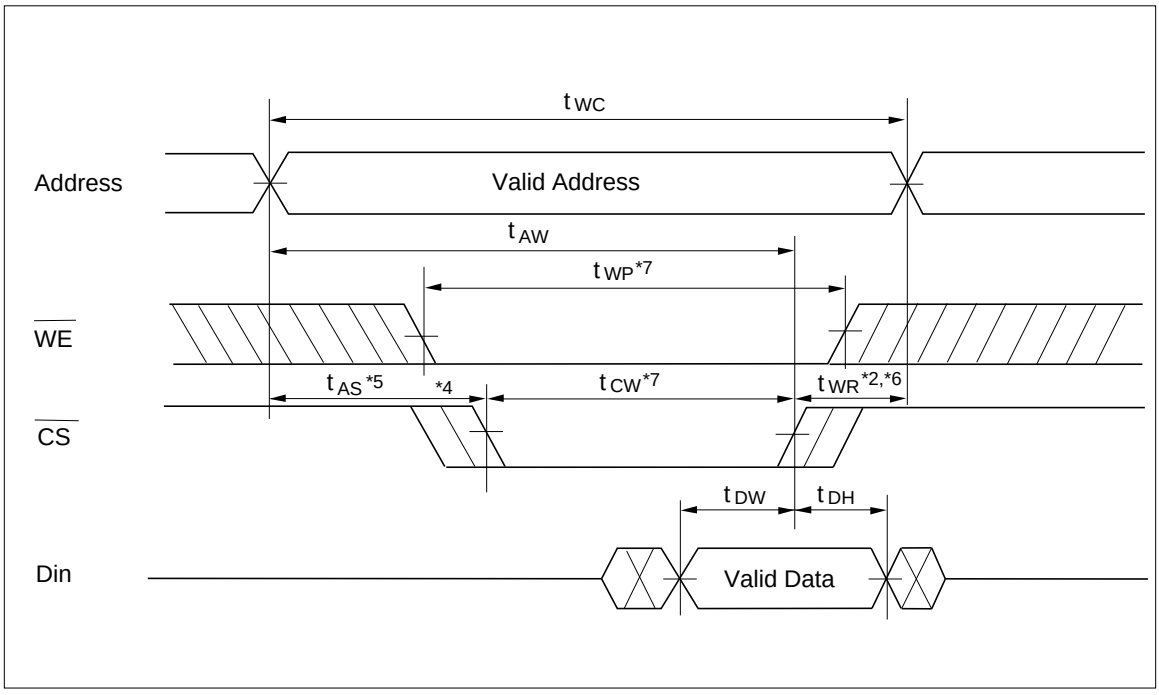
### Write Cycle

| | | HM628127H/HM629127H | | | | |
|---|---|---|---|---|---|---|
| | | -20 | | -25 | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Write cycle time | $t_{WC}$ | 20 | — | 25 | — | ns |
| Address valid to end of write | $t_{AW}$ | 15 | — | 20 | — | ns |
| Chip select to end of write | $t_{CW}$ | 12 | — | 12 | — | ns |
| Write pulse width | $t_{WP}$ | 12 | — | 12 | — | ns |
| Address setup time | $t_{AS}$ | 0 | — | 0 | — | ns |
| Write recovery time | $t_{WR}$ | 0 | — | 0 | — | ns |
| Data to write time overlap | $t_{DW}$ | 10 | — | 10 | — | ns |
| Data hold from write time | $t_{DH}$ | 0 | — | 0 | — | ns |
| Write disable to output in low-Z | $t_{OW}$ | 3 | — | 3 | — | ns |
| Write enable to output in high-Z | $t_{WHZ}$ | — | 7 | — | 7 | ns |

### Write Timing Waveform (1) ($\overline{WE}$ Controlled)



**Write Timing Waveform (2) ($\overline{CS}$ Controlled)**




Notes:
1. Transition is measured ±200 mV from high impedance state's voltage with Load (B). This parameter is sampeld and not 100% tested.
2. $\overline{WE}$ must be high during transition except when the device is disabled with $\overline{CS}$.
3. If $\overline{CS}$ and $\overline{OE}$ are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
4. If the $\overline{CS}$ low transition occurs s.imultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.
5. $t_{AS}$ is from the latest address change to the latest transition (High to Low) of $\overline{WE}$ or $\overline{CS}$.
6. $t_{WR}$ is from the first transition (Low to High) of $\overline{WE}$ or $\overline{CS}$ to the first address transition.
7. A write occurs during the overlap of a low $\overline{WE}$ and a low $\overline{CS}$.

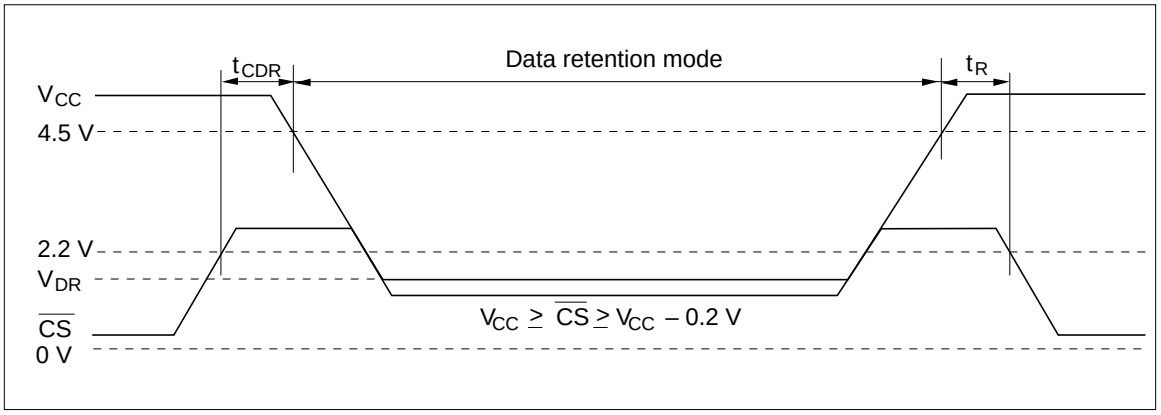
## Low $V_{CC}$ Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| $V_{CC}$ for data retention | $V_{DR}$ | 2.0 | — | — | V | $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, $V_{CC} \geq Vin \geq V_{CC} - 0.2$ V or $0 V \leq Vin \leq 0.2$ V |
| Data retention current | $I_{CCDR}$ | — | 2 | 80*1 | µA | |
| Chip deselect to data retention time | $t_{CDR}$ | 0 | — | — | ns | |
| Operation recovery time | $t_R$ | 5 | — | — | ms | |

Note: 1. $V_{CC}$ = 3.0 V

### Low $V_{CC}$ Data Retention Timing Waveform



# HM628127HB Series

**Preliminary**

**131072-word × 8-bit High Speed CMOS Static RAM**

HITACHI

**Rev. 0.0**

The HM628127HB is an asyncronous high speed static RAM organized as 128-kword × 8-bit. It realize high speed access time (15/20/25 ns) with employing 0.8 µm shrink CMOS process and high speed circuit designing technology.
It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system.
The HM628127HB is packaged in 400-mil 32-pin SOJ for high density surface mounting.

## Features

- Single 5 V supply: 5 V ± 10%
- Access time 15/20/25 ns (max)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - All inputs and outputs
- 400-mil 32-pin SOJ package
- Center $V_{CC}$ and $V_{SS}$ type pinout

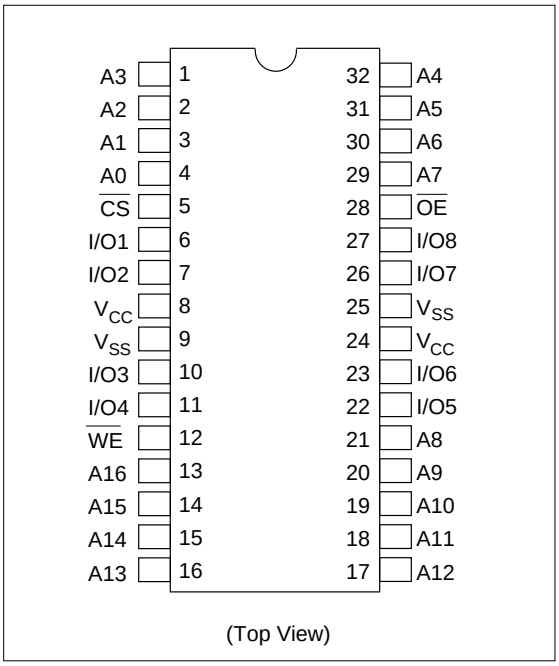
## Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HM628127HBJP-15 | 15 ns | 400-mil 32-pin plastic SOJ (CP-32DB) |
| HM628127HBJP-20 | 20 ns | |
| HM628127HBJP-25 | 25 ns | |
| HM628127HBLJP-15 | 15 ns | |
| HM628127HBLJP-20 | 20 ns | |
| HM628127HBLJP-25 | 25 ns | |

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Hitachi semiconductor

## Pin Arrangement



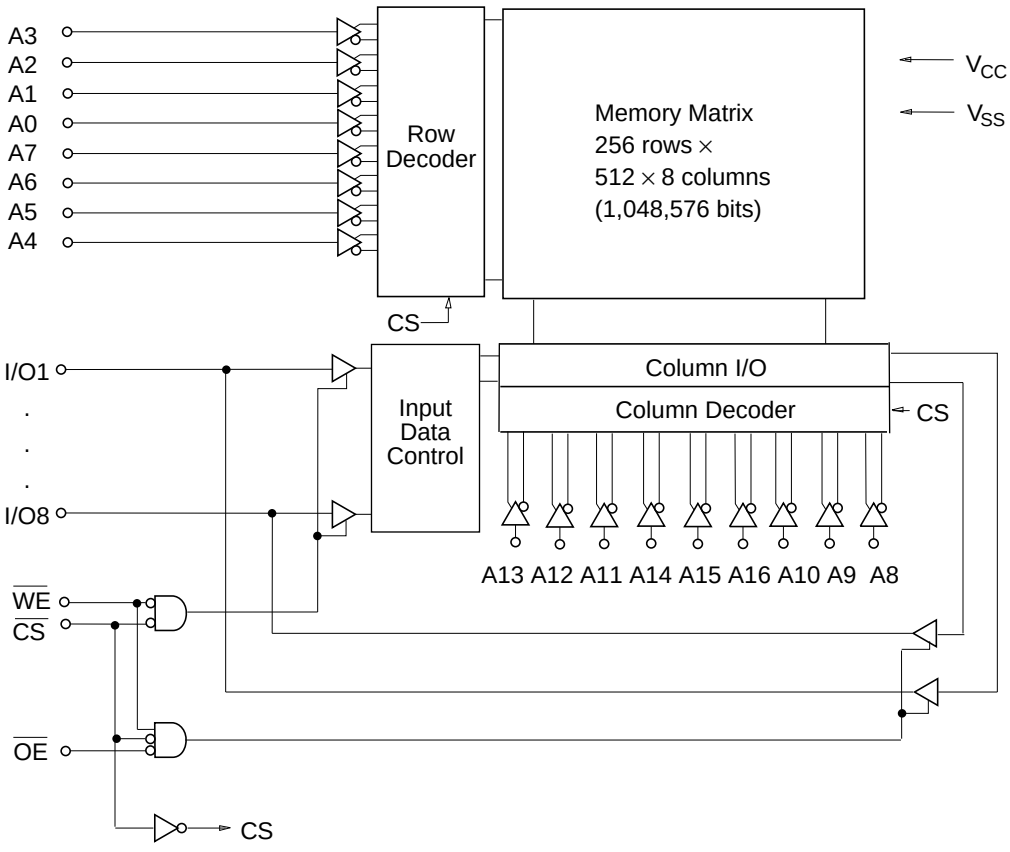

(Top View)

## Pin Description

| Pin name | Function |
|---|---|
| A0 to A16 | Address |
| I/O1 to I/O8 | Input/output |
| $\overline{CS}$ | Chip select |
| $\overline{OE}$ | Output enable |
| $\overline{WE}$ | Write enable |
| $V_{CC}$ | Power supply |
| $V_{SS}$ | Ground |

ADE-203-350(Z)

## Block Diagram



## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage relative to $V_{SS}$ | $V_{CC}$ | –0.5 to +7.0 | V |
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | –0.5 *1 to $V_{CC}$+0.5 | V |
| Power dissipation | $P_T$ | 1.0*2 / 1.5*3 | W |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | –55 to +125 | °C |
| Storage temperature under bias | Tbias | –10 to +85 | °C |

Note: 1. –2.5 V for pulse width (under shoot) ≤ 10 ns
2. at still air condition
3. at air flow ≥ 1.0 m/s

## Function Table

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | $V_{CC}$ current | I/O | Ref. cycle |
|---|---|---|---|---|---|
| H | X | X | $I_{SB}$, $I_{SB1}$ | High-Z | — |
| L | H | H | $I_{CC}$ | High-Z | — |
| L | L | H | $I_{CC}$ | Output | Read cycle |
| L | X | L | $I_{CC}$ | Input | Write cycle |

Note: 1. X: H or L

## Recommended DC Operating Conditions (Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage*2 | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$ | 0 | 0 | 0 | V |
| Input voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$+0.5 | V |
| | $V_{IL}$ | –0.5 *1 | — | 0.8 | V |

Note: 1. –2.0 V for pulse width (under shoot) ≤ 10 ns
2. The supply voltage with all $V_{CC}$ pins must be on the same level.
The supply voltage with all $V_{SS}$ pins must be on the same level.

## DC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ±10%, $V_{SS}$ = 0 V)

| Parameter | Symbol | Min | Typ*1 | Max | Unit | Test conditions | Notes |
|---|---|---|---|---|---|---|---|
| Input leakage current | $\|I_{LI}\|$ | — | — | 2 | µA | Vin = $V_{SS}$ to $V_{CC}$ | |
| Output leakage current | $\|I_{LO}\|$ | — | — | 2 | µA | $V_{I/O}$ = $V_{SS}$ to $V_{CC}$ | 1 |
| Operating power supply current | $I_{CC}$ | — | 120 | 180 | mA | 15 ns cycle, $\overline{CS}$ = $V_{IL}$, Iout = 0 mA, Other inputs = $V_{IH}$/$V_{IL}$ | |
| | | — | 100 | 150 | mA | 20 ns cycle | |
| | | — | 85 | 130 | mA | 25 ns cycle | |
| Standby power supply current | $I_{SB}$ | — | 55 | 100 | mA | 15 ns cycle, $\overline{CS}$ = $V_{IH}$, Other inputs = $V_{IH}$/$V_{IL}$ | |
| | | — | 45 | 80 | mA | 20 ns cycle | |
| | | — | 40 | 70 | mA | 25 ns cycle | |
| Standby power supply current (1) | $I_{SB1}$ | — | — | 2 | mA | $V_{CC} \geq \overline{CS} \geq V_{CC}$ – 0.2 V, 0 V ≤ Vin ≤ 0.2 V or $V_{CC} \geq$ Vin ≥ $V_{CC}$ – 0.2 V | |
| | | — | — | 0.2 | mA | | L-version |
| Output voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 8 mA | |
| | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = –4 mA | |

Note: 1. Typical values are at $V_{CC}$ = 5.0 V, Ta = +25°C and specified loading.

## Capacitance (Ta = 25°C, f = 1.0 MHz)*1

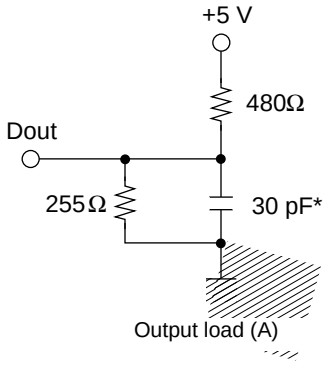
| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input capacitance | Cin | — | — | 6 | pF | Vin = 0 V |
| Input/output capacitance | $C_{I/O}$ | — | — | 8 | pF | $V_{I/O}$ = 0 V |

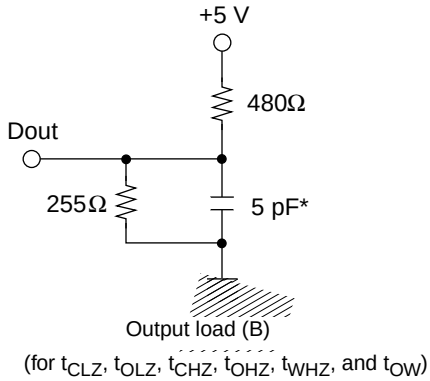
Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%, unless otherwise noted.)

### Test Conditions

- Input pulse levels: $V_{SS}$ to 3.0 V
- Input rise and fall times: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures

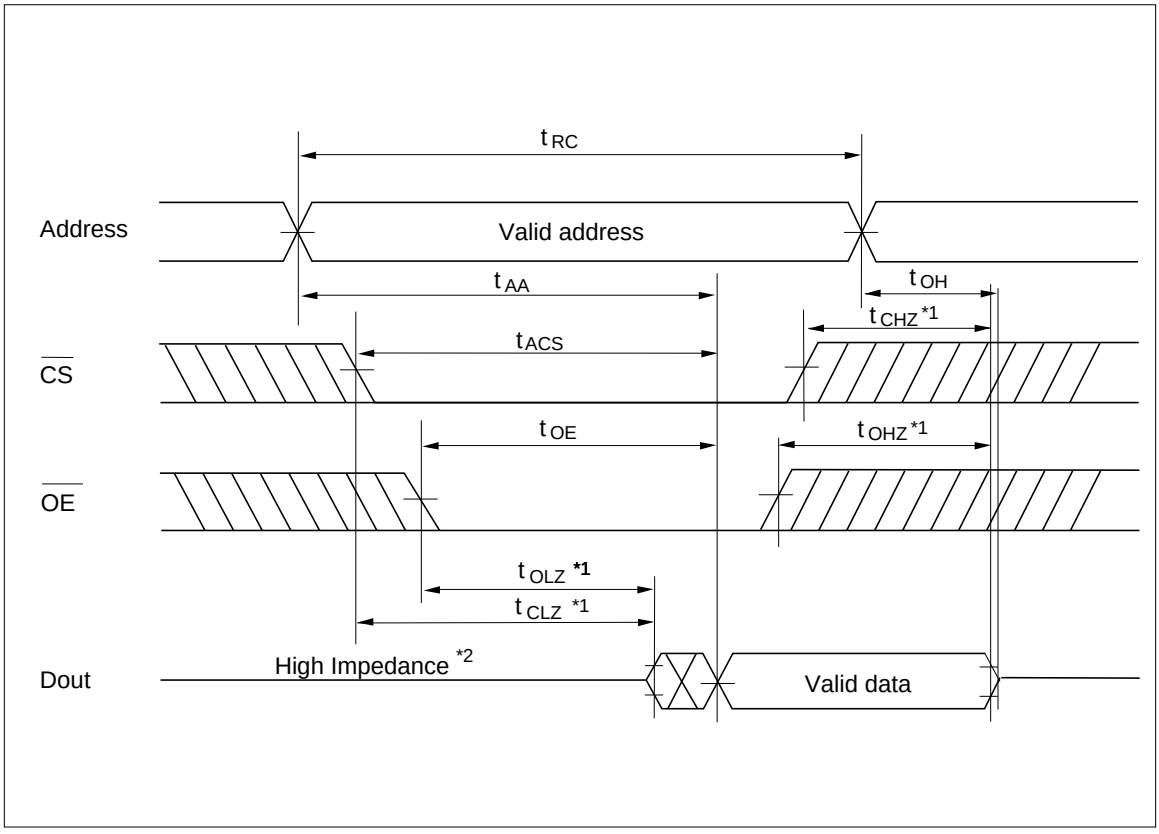



### Read Cycle

| | | HM628127HB | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | -15 | | -20 | | -25 | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit |
| Read cycle time | $t_{RC}$ | 15 | — | 20 | — | 25 | — | ns |
| Address access time | $t_{AA}$ | — | 15 | — | 20 | — | 25 | ns |
| Chip select access time | $t_{ACS}$ | — | 15 | — | 20 | — | 25 | ns |
| Output enable to output valid | $t_{OE}$ | — | 8 | — | 10 | — | 12 | ns |
| Output hold from address change | $t_{OH}$ | 5 | — | 5 | — | 5 | — | ns |
| Chip select to output in low-Z | $t_{CLZ}$ | 3 | — | 3 | — | 3 | — | ns |
| Output enable to output in low-Z | $t_{OLZ}$ | 1 | — | 1 | — | 1 | — | ns |
| Chip deselect to output in high-Z | $t_{CHZ}$ | — | 7 | — | 7 | — | 7 | ns |
| Output disable to output in high-Z | $t_{OHZ}$ | — | 7 | — | 7 | — | 7 | ns |

**Read Timing Waveform*3**

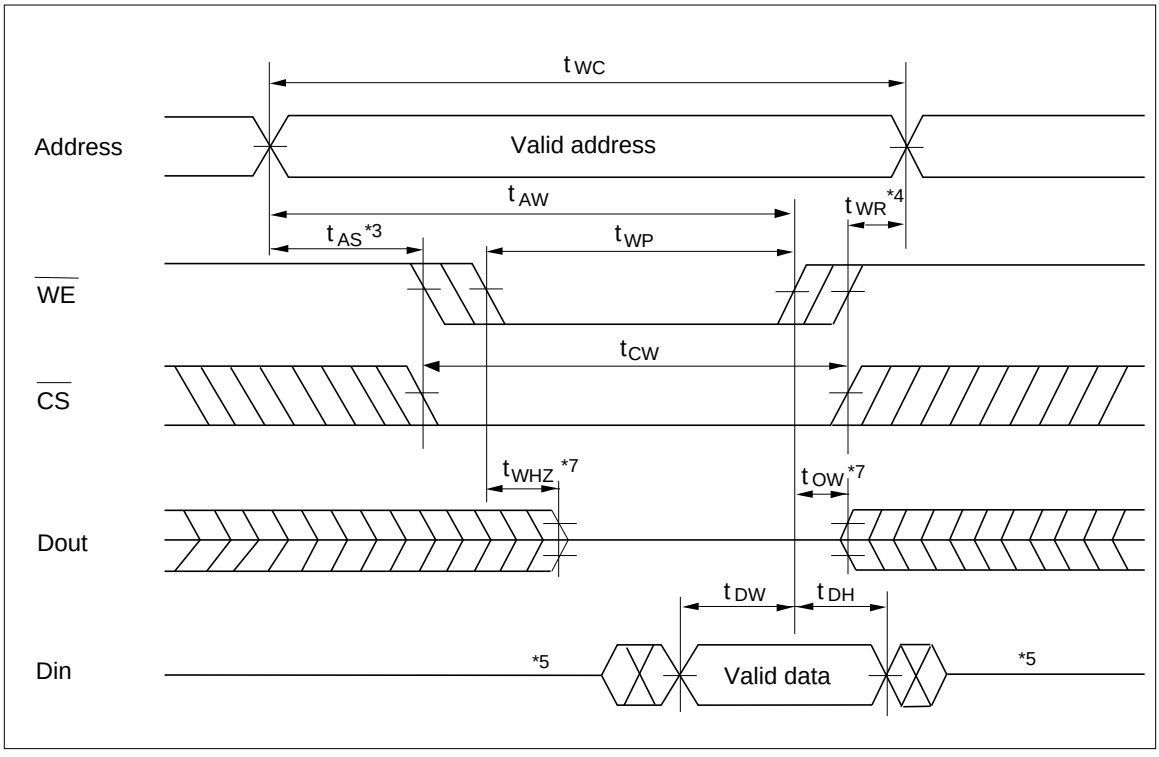



Notes: 1. Transition is measured ± 200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
2. When $\overline{CS}$ and $\overline{OE}$ are low, Dout is low impedance.
3. $\overline{WE}$ is high for read cycle.

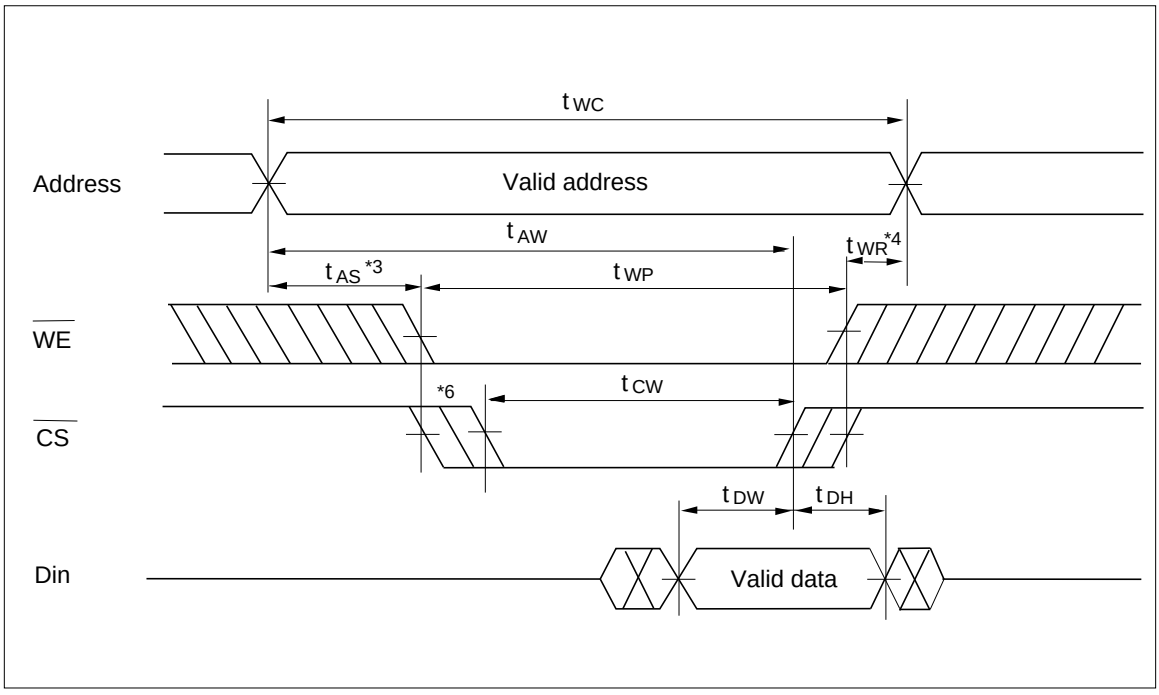
## Write Cycle

| | | HM628127HB | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | -15 | | -20 | | -25 | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit |
| Write cycle time | $t_{WC}$ | 15 | — | 20 | — | 25 | — | ns |
| Address valid to end of write | $t_{AW}$ | 12 | — | 15 | — | 15 | — | ns |
| Chip select to end of write | $t_{CW}$ | 10 | — | 12 | — | 12 | — | ns |
| Write pulse width | $t_{WP}$ | 10 | — | 12 | — | 12 | — | ns |
| Address setup time | $t_{AS}$ | 0 | — | 0 | — | 0 | — | ns |
| Write recovery time | $t_{WR}$ | 0 | — | 0 | — | 0 | — | ns |
| Data to write time overlap | $t_{DW}$ | 8 | — | 10 | — | 10 | — | ns |
| Data hold from write time | $t_{DH}$ | 0 | — | 0 | — | 0 | — | ns |
| Write disable to output in low-Z | $t_{OW}$ | 3 | — | 3 | — | 3 | — | ns |
| Write enable to output in high-Z | $t_{WHZ}$ | — | 7 | — | 7 | — | 7 | ns |

## Write Timing Waveform (1) ($\overline{WE}$ Controlled)



**Write Timing Waveform (2) ($\overline{CS}$ Controlled)**




Notes:
1. A write occurs during the overlap of low $\overline{CS}$ and low $\overline{WE}$.
2. $\overline{WE}$ must be high during address transition except when the device is disabled with $\overline{CS}$.
3. $t_{AS}$ is measured from the latest address transition to the later of $\overline{CS}$ or $\overline{WE}$ going low.
4. $t_{WR}$ is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the first address transition.
5. If $\overline{CS}$ and $\overline{OE}$ are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.
7. Transition is measured ±200 mV from high impedance state's voltage with Load (B). This parameter is sampled and not 100% tested.

## Low $V_{CC}$ Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| $V_{CC}$ for data retention | $V_{DR}$ | 2.0 | — | — | V | $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, $V_{CC} \geq Vin \geq V_{CC} - 0.2$ V or $0\ V \leq Vin \leq 0.2\ V$ |
| Data retention current | $I_{CCDR}$ | — | 2 | 80*1 | µA | |
| Chip deselect to data retention time | $t_{CDR}$ | 0 | — | — | ns | |
| Operation recovery time | $t_R$ | 5 | — | — | ms | |

Note: 1. $V_{CC}$ = 3.0 V

### Low $V_{CC}$ Data Retention Timing Waveform