

HD74ALVCH162832

1-to-4 Address Register / Driver with 3-state Outputs

HITACHI

ADE-205-215B (Z)
3rd. Edition
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Description

This 1-bit to 4-bit address register / driver is designed for 2.3 V to 3.6 V V_{CC} operation.

The device is ideal for use in applications in which a single address bus is driving four separate memory locations. The HD74ALVCH162832 can be used as a buffer or a register, depending on the logic level of the select (\overline{SEL}) input.

When \overline{SEL} is a logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output enable (\overline{OE}) inputs. Each \overline{OE} controls two groups of seven outputs.

When \overline{SEL} is a logic low, the device is in the register mode. The register is an edge triggered D-type flip flop. On the positive transition of the clock (CLK) input, data at the A inputs is stored in the internal registers. \overline{OE} controls operate the same as in the buffer mode.

When \overline{OE} is a logic low, the outputs are in a normal logic state (high or low logic level). When \overline{OE} is a logic high, the outputs are in the high impedance state.

Neither \overline{SEL} nor \overline{OE} affect the internal operation of the flip flops. Old data can be retained or new data can be entered while the outputs are in the high impedance state.

To ensure the high impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level. All outputs, which are designed to sink up to 12 mA, include 26 Ω resistors to reduce overshoot and undershoot.

Features

- $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$
- Typical V_{OL} ground bounce $< 0.8 \text{ V}$ ($@V_{CC} = 3.3 \text{ V, } T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.0 \text{ V}$ ($@V_{CC} = 3.3 \text{ V, } T_a = 25^\circ\text{C}$)
- High output current $\pm 24 \text{ mA}$ ($@V_{CC} = 3.0 \text{ V}$)
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors
- All outputs have equivalent 26 Ω series resistors, so no external resistors are required

Function Table

Inputs				Output Y
\overline{OE}	\overline{SEL}	CLK	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

H : High level

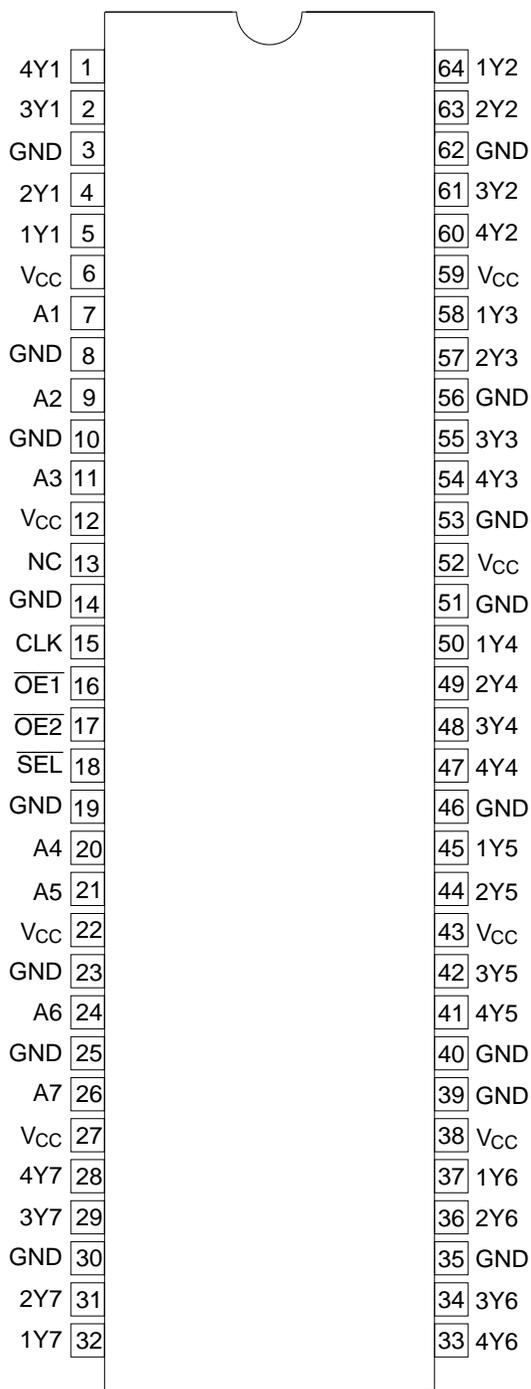
L : Low level

X : Immaterial

Z : High impedance

↑ : Low to high transition

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	-0.5 to 4.6	V	
Input voltage ^{*1}	V_I	-0.5 to 4.6	V	
Output voltage ^{*1,2}	V_O	-0.5 to $V_{CC} + 0.5$	V	
Input clamp current	I_{IK}	-50	mA	$V_I < 0$
Output clamp current	I_{OK}	± 50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	± 50	mA	$V_O = 0$ to V_{CC}
V_{CC} , GND current / pin	I_{CC} or I_{GND}	± 100	mA	
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) ^{*3}	P_T	1	W	TSSOP
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

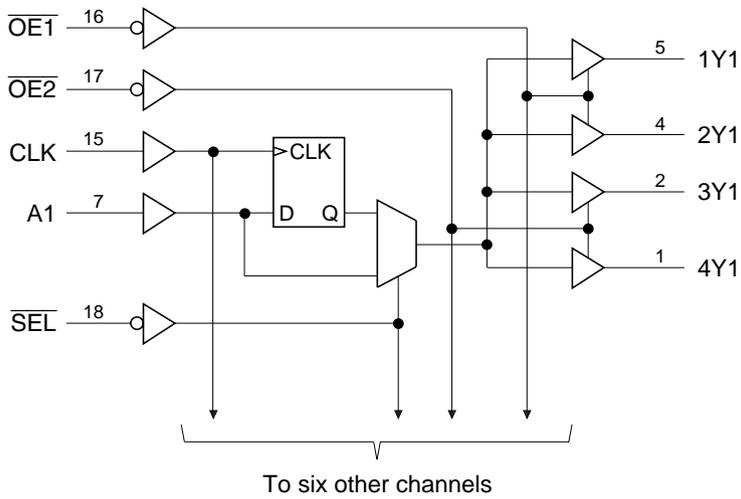
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	2.3	3.6	V	
Input voltage	V_I	0	V_{CC}	V	
Output voltage	V_O	0	V_{CC}	V	
High level output current	I_{OH}	—	-6	mA	$V_{CC} = 2.3\text{ V}$
		—	-8		$V_{CC} = 2.7\text{ V}$
		—	-12		$V_{CC} = 3.0\text{ V}$
Low level output current	I_{OL}	—	6	mA	$V_{CC} = 2.3\text{ V}$
		—	8		$V_{CC} = 2.7\text{ V}$
		—	12		$V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	T_a	-40	85	$^\circ\text{C}$	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



Electrical Characteristics (Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V) ^{*1}	Min	Max	Unit	Test Conditions			
Input voltage	V _{IH}	2.3 to 2.7	1.7	—	V				
		2.7 to 3.6	2.0	—					
	V _{IL}	2.3 to 2.7	—	0.7					
		2.7 to 3.6	—	0.8					
Output voltage	V _{OH}	2.3 to 3.6	V _{CC} -0.2	—	V	I _{OH} = -100 μA			
		2.3	1.9	—		I _{OH} = -4 mA, V _{IH} = 1.7 V			
		2.3	1.7	—		I _{OH} = -6 mA, V _{IH} = 1.7 V			
		2.7	2.0	—		I _{OH} = -8 mA, V _{IH} = 2.0 V			
		3.0	2.4	—		I _{OH} = -6 mA, V _{IH} = 2.0 V			
		3.0	2.0	—		I _{OH} = -12 mA, V _{IH} = 2.0 V			
	V _{OL}	2.3 to 3.6	—	0.2		I _{OL} = 100 μA			
		2.3	—	0.4		I _{OL} = 4 mA, V _{IL} = 0.7 V			
		2.3	—	0.55		I _{OL} = 6 mA, V _{IL} = 0.7 V			
		2.7	—	0.6		I _{OL} = 8 mA, V _{IL} = 0.8 V			
		3.0	—	0.55		I _{OL} = 6 mA, V _{IL} = 0.8 V			
		3.0	—	0.8		I _{OL} = 12 mA, V _{IL} = 0.8 V			
		Input current	I _{IN}	3.6		—	±5	μA	V _{IN} = V _{CC} or GND
				2.3		45	—		V _{IN} = 0.7 V
2.3	-45			—	V _{IN} = 1.7 V				
3.0	75			—	V _{IN} = 0.8 V				
3.0	-75			—	V _{IN} = 2.0 V				
3.6	—			±500	V _{IN} = 0 to 3.6 V ^{*2}				
Off state output current	I _{OZ}	3.6	—	±10	μA	V _{OUT} = V _{CC} or GND			
Quiescent supply current	I _{CC}	3.6	—	40	μA	V _{IN} = V _{CC} or GND			
	ΔI _{CC}	3.0 to 3.6	—	750	μA	V _{IN} = one input at (V _{CC} -0.6) V, other inputs at V _{CC} or GND			

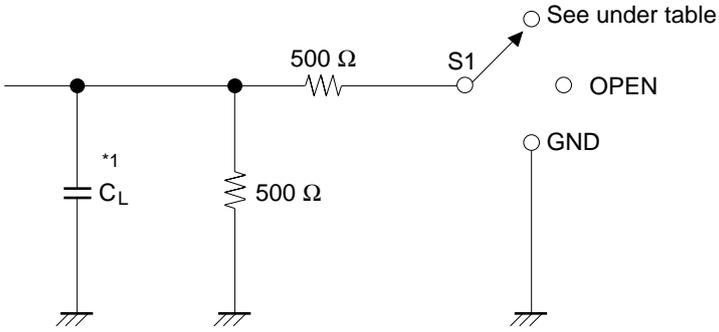
Notes: 1. For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

2. This is the bus hold maximum dynamic current required to switch the input from one state to another.

Switching Characteristics (Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f _{max}	2.5±0.2	150	—	—	MHz		
		2.7	150	—	—			
		3.3±0.3	150	—	—			
Propagation delay time	t _{PLH}	2.5±0.2	1.1	—	4.7	ns	A	Y
		2.7	—	—	4.8			
		3.3±0.3	1.5	—	4.3			
	t _{PHL}	2.5±0.2	1.0	—	5.3		CLK	Y
		2.7	—	—	5.3			
		3.3±0.3	1.4	—	4.7			
	t _{PHL}	2.5±0.2	1.1	—	6.0		SEL	Y
		2.7	—	—	6.2			
		3.3±0.3	1.5	—	4.8			
Output enable time	t _{ZH}	2.5±0.2	1.0	—	5.9	ns	OE	Y
		2.7	—	—	5.9			
		3.3±0.3	1.1	—	5.1			
t _{ZL}	2.5±0.2	1.4	—	6.3	ns	OE	Y	
	2.7	—	—	5.4				
	3.3±0.3	1.6	—	5.1				
Setup time	t _{su}	2.5±0.2	2.0	—	—	ns		
		2.7	2.0	—	—			
		3.3±0.3	1.6	—	—			
Hold time	t _h	2.5±0.2	0.7	—	—	ns		
		2.7	0.5	—	—			
		3.3±0.3	1.1	—	—			
Pulse width	t _w	2.5±0.2	3.3	—	—	ns		
		2.7	3.3	—	—			
		3.3±0.3	3.3	—	—			
Input capacitance	C _{IN}	3.3	—	4.5	—	pF	Control inputs	
		3.3	—	5.0	—		Data inputs	
Output capacitance	C _O	3.3	—	7.5	—	pF	Outputs	

Test Circuit

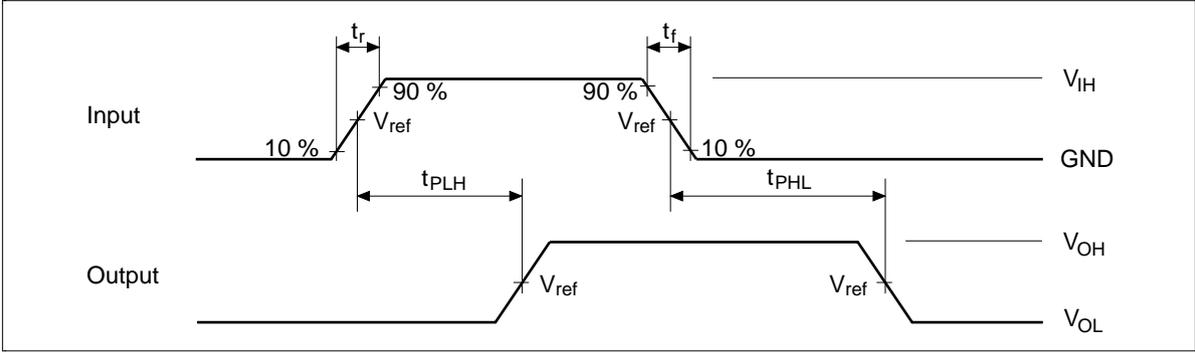


Load Circuit for Outputs

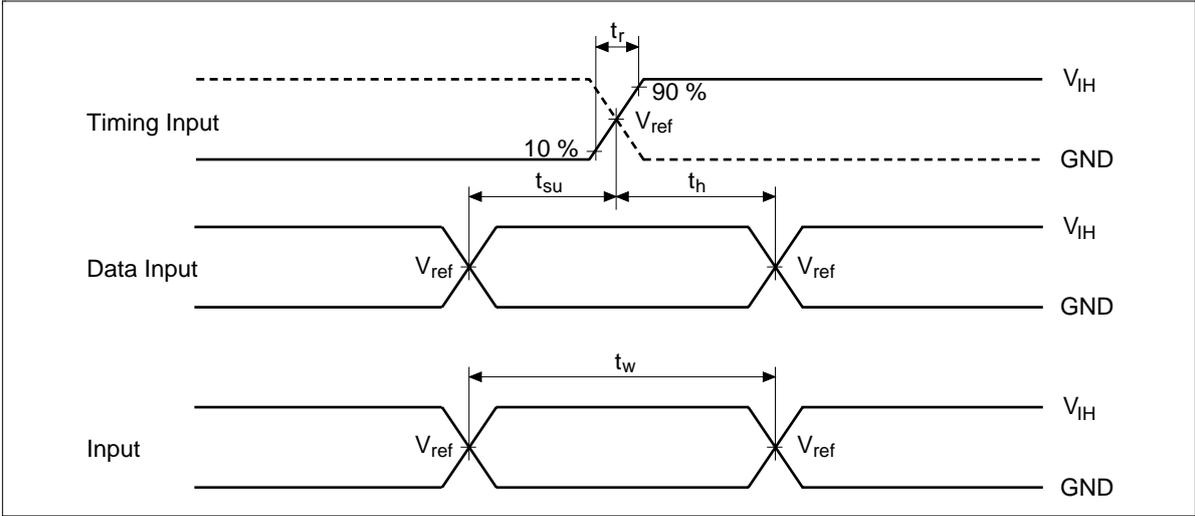
Symbol	$V_{CC}=2.5\pm 0.2V$	$V_{CC}=2.7V,$ $3.3\pm 0.3V$
t_{PLH}/t_{PHL}	OPEN	OPEN
$t_{su}/t_h/t_w$	OPEN	OPEN
t_{ZH}/t_{HZ}	GND	GND
t_{ZL}/t_{LZ}	$2 \times V_{CC}$	6.0 V
C_L	30 pF	50 pF

Note: 1. C_L includes probe and jig capacitance.

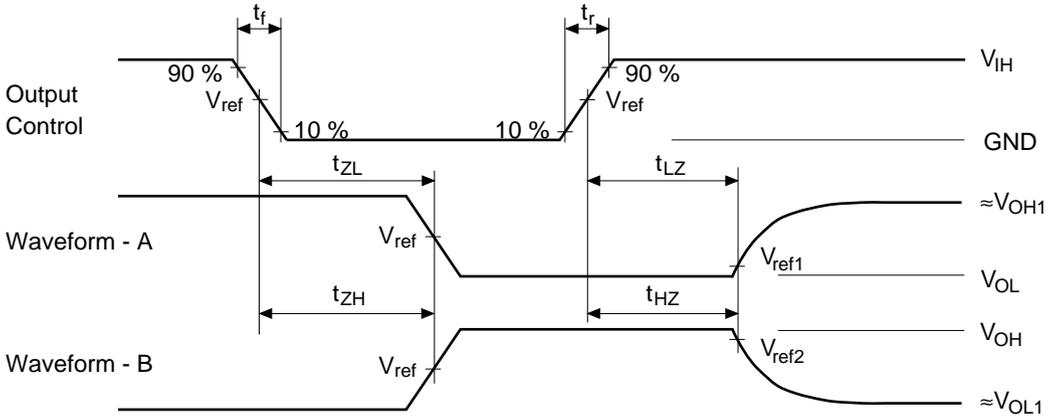
Waveforms – 1



Waveforms – 2



Waveforms – 3

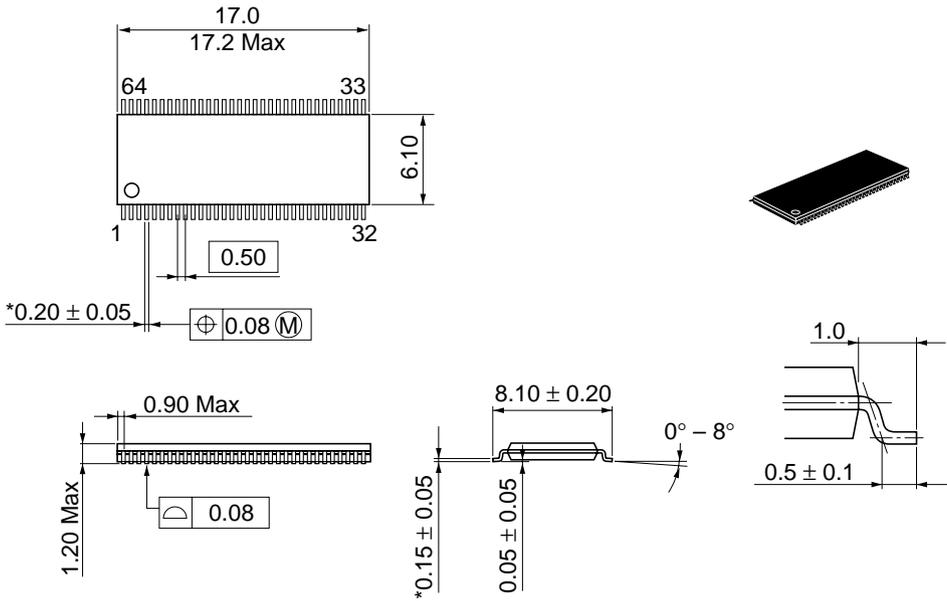


TEST	$V_{CC}=2.5\pm 0.2V$	$V_{CC}=2.7V, 3.3\pm 0.3V$
V_{IH}	V_{CC}	2.7 V
V_{ref}	$1/2 V_{CC}$	1.5 V
V_{ref1}	$V_{OL} + 0.15 V$	$V_{OL} + 0.3 V$
V_{ref2}	$V_{OH} - 0.15 V$	$V_{OH} - 0.3 V$
V_{OH1}	V_{CC}	3.0 V
V_{OL1}	GND	GND

- Notes:
1. All input pulses are supplied by generators having the following characteristics :
 $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 2.0 \text{ ns}$, $t_f \leq 2.0 \text{ ns}$. ($V_{CC} = 2.5\pm 0.2 \text{ V}$)
 $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$. ($V_{CC} = 2.7 \text{ V}, 3.3\pm 0.3 \text{ V}$)
 2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions

Unit : mm



*Pd plating

Hitachi Code	TTP-64D
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.47 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL North America : <http://semiconductor.hitachi.com/>
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher StraÙe 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel: <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : <http://www.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel: <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel : <852>-(2)-735-9218
Fax : <852>-(2)-730-0281
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