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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74AC125/HD74ACT125

Quad Buffer/Line Driver with 3-State Output

ADE-205-366 (Z)
1st. Edition
Sep. 2000

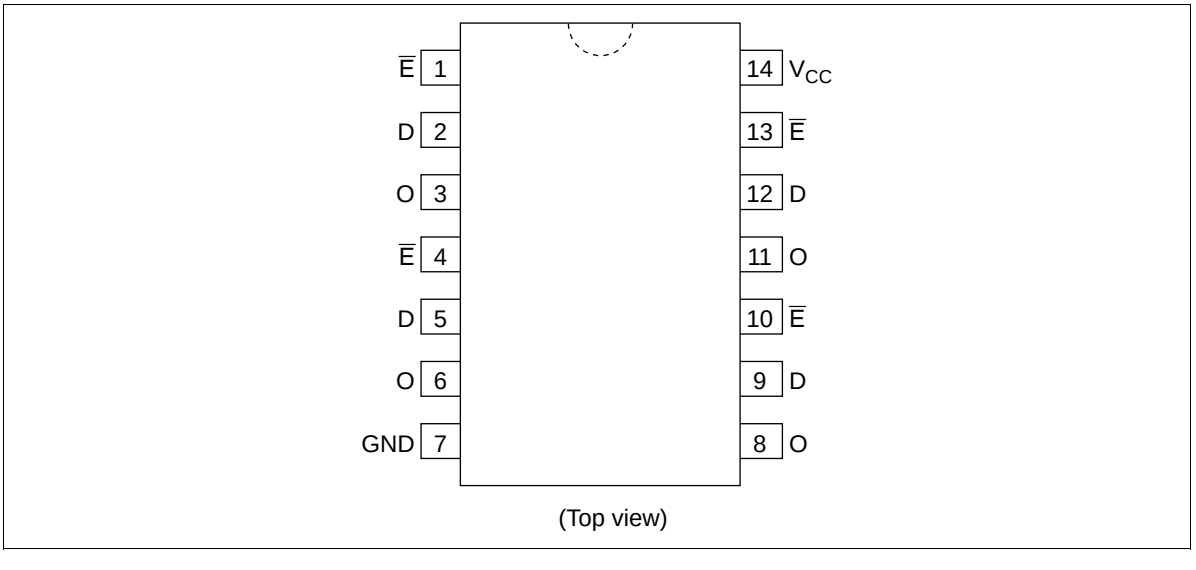
Description

The HD74AC125/HD74ACT125 is an quad buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

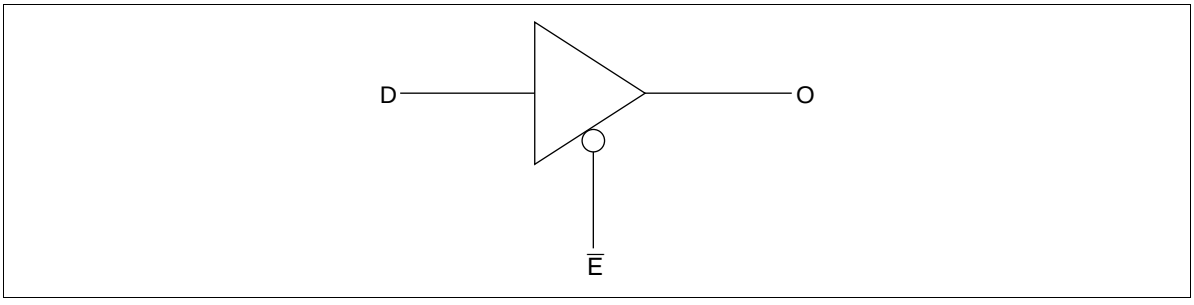
Features

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- HD74ACT125 has TTL-Compatible Inputs

Pin Arrangement



Logic Symbol



Pin Names

D	Data Inputs
$\overline{E}$	3-State Output Enable Inputs (Active Low)
O	Outputs

Truth Table

Inputs

$\overline{E}$	D	Output
L	L	L
L	H	H
H	X	Z

H : High Voltage Level
L : Low Voltage Level
X : Immaterial
Z : High Impedance

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	µA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = Worst case
Maximum quiescent supply current	I_{CC}	8.0	µA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = 25°C
Maximum I_{CC}/input (HD74ACT125)	I_{CCT}	1.5	mA	V_{IN} = V_{CC} – 2.1 V, V_{CC} = 5.5 V Ta = Worst case

AC Characteristics: HD74AC125

			Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		
Item	**Symbol**	**V_{CC} (V)*[1]**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**
Propagation delay	t_{PLH}	3.3	1.0	6.5	9.0	1.0	10.0	ns
		5.0	1.0	5.5	7.0	1.0	7.5	
Propagation delay	t_{PHL}	3.3	1.0	6.5	9.0	1.0	10.0	
		5.0	1.0	5.0	7.0	1.0	7.5	
Enable time	t_{ZH}	3.3	1.0	6.0	10.5	1.0	11.0	
		5.0	1.0	5.0	7.0	1.0	8.0	
Enable time	t_{ZL}	3.3	1.0	7.5	10.0	1.0	11.0	
		5.0	1.0	5.5	8.0	1.0	8.5	
Disable time	t_{HZ}	3.3	1.0	7.0	10.0	1.0	10.5	
		5.0	1.0	6.5	9.0	1.0	9.5	
Disable time	t_{LZ}	3.3	1.0	7.5	10.5	1.0	11.5	
		5.0	1.0	6.5	9.0	1.0	9.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT125

			Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		
Item	**Symbol**	**V_{CC} (V)*[1]**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**
Propagation delay	t_{PLH}	5.0	1.0	6.5	9.0	1.0	10.0	ns
Propagation delay	t_{PHL}	5.0	1.0	7.0	9.0	1.0	10.0	
Enable time	t_{ZH}	5.0	1.0	6.0	8.5	1.0	9.5	
Enable time	t_{ZL}	5.0	1.0	7.0	9.5	1.0	10.5	
Disable time	t_{HZ}	5.0	1.0	7.0	9.5	1.0	10.5	
Disable time	t_{LZ}	5.0	1.0	7.5	10.0	1.0	10.5	

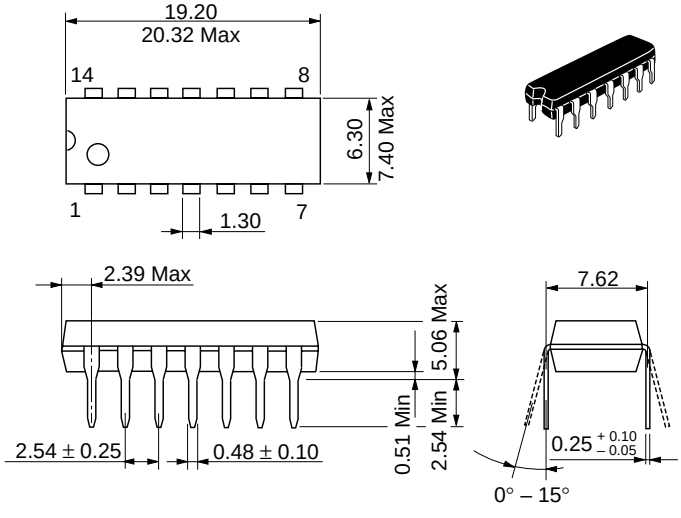
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	**Symbol**	**Typ**	**Unit**	**Condition**
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	45.0	pF	V_{CC} = 5.0 V

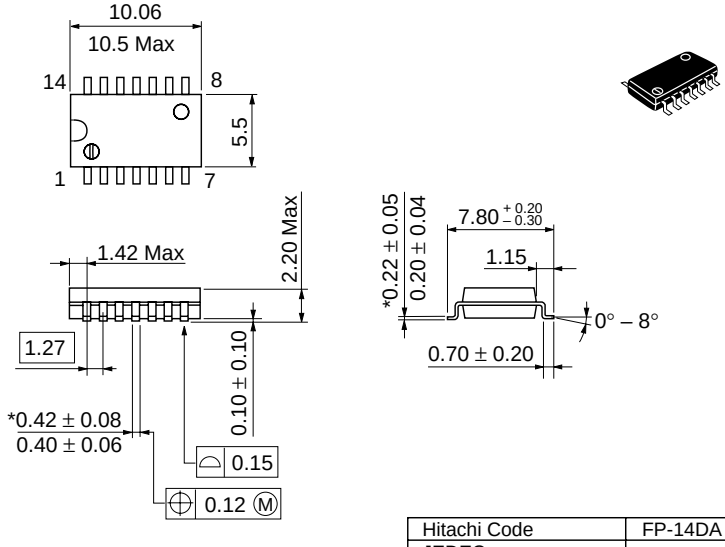
Package Dimensions

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.97 g

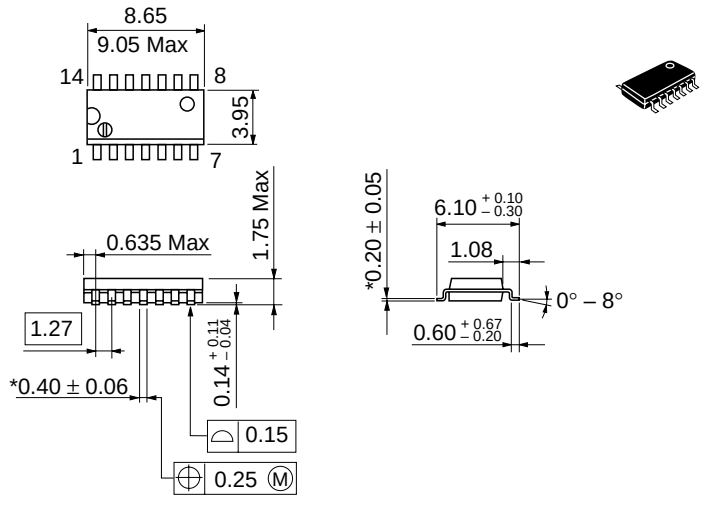
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.23 g

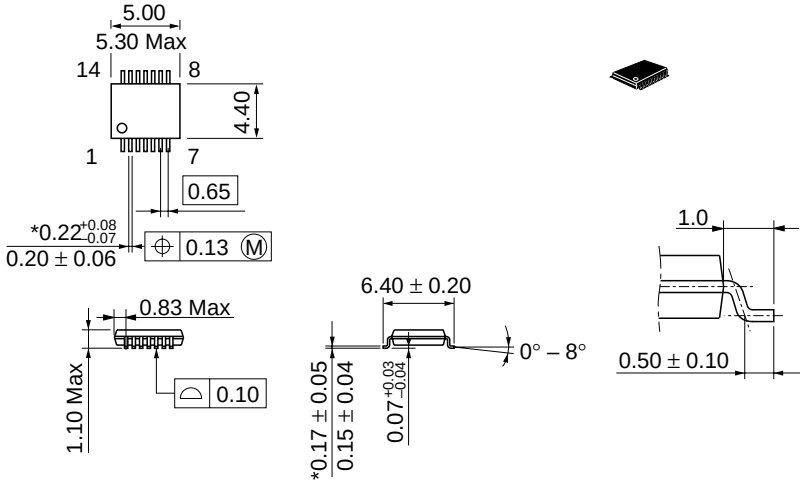
Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.13 g

*Pd plating

Unit: mm



Hitachi Code	TTP-14D
JEDEC	—
EIAJ	—
Mass (reference value)	0.05 g

*Dimension including the plating thickness
Base material dimension

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