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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HD74AC107/HD74ACT107

Dual JK Flip-Flop (with Separate Clear and Clock)

ADE-205-363 (Z)
1st. Edition
Sep. 2000

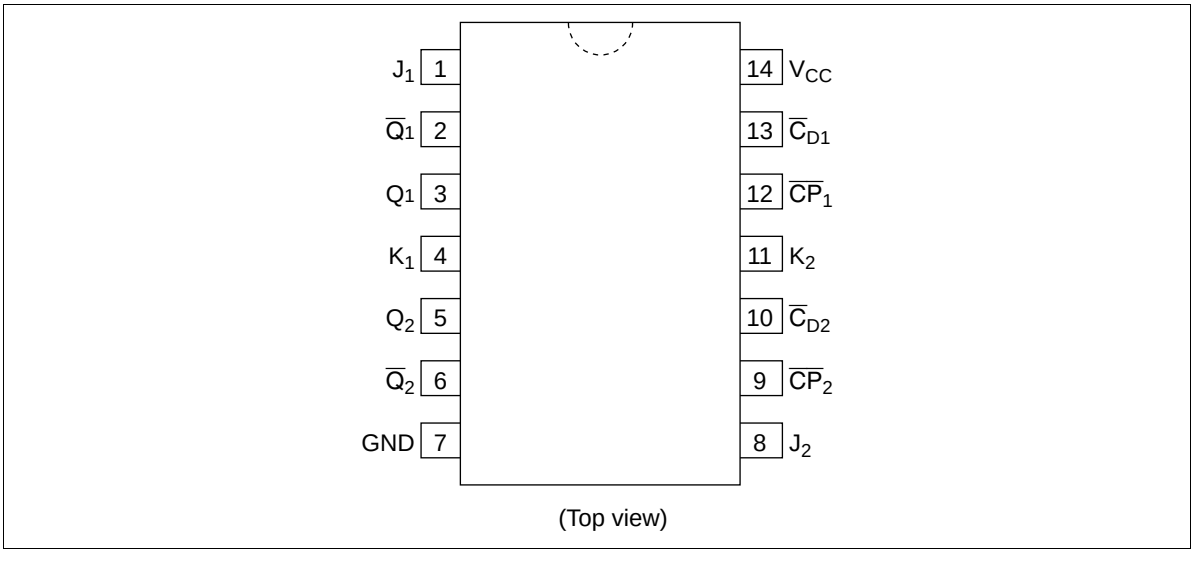
Description

The HD74AC107/HD74ACT107 dual JK master/slave flip-flops have a separate clock for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from J and K inputs to master; 3) disable J and K inputs; 4) transfer information from master to slave.

Features

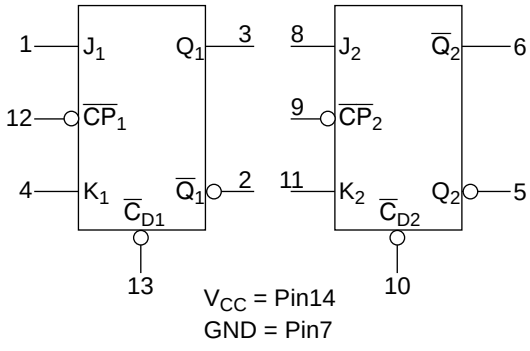
- Outputs Source/Sink 24 mA
- HD74ACT107 has TTL-Compatible Inputs

Pin Arrangement



(Top view)

Logic Symbol



Pin Names

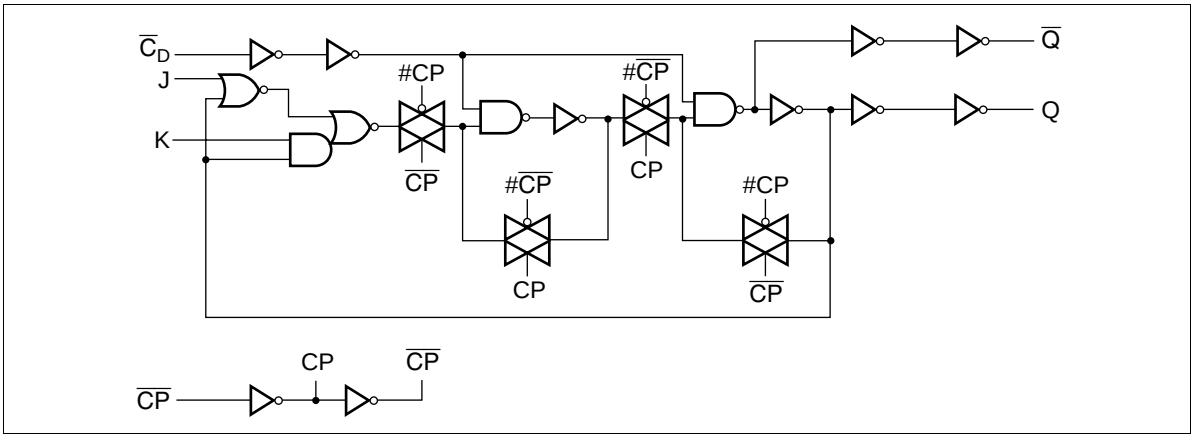
J_1, J_2, K_1, K_2	Data Inputs
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active Low)
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs

Truth Table

Inputs		**Outputs**
@ t_n		@ t_{n+1}
J	**K**	**Q**
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Q}$n

H : High Voltage Level
L : Low Voltage Level
t_n : Bit time before clock pulse.
t_{n+1} : Bit time after clock pulse.

Logic Diagram



DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	40	µA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = Worst case
Maximum quiescent supply current	I_{CC}	4.0	µA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = 25°C
Maximum additional I_{CC}/input (HD74ACT107)	I_{CCT}	1.5	mA	V_{IN} = V_{CC} – 2.1 V, V_{CC} = 5.5 V Ta = Worst case

AC Characteristics: HD74AC107

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF			Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock	f_{max}	3.3	125	—	—	100	—	MHz
frequency		5.0	150	—	—	125	—	
Propagation delay	t_{PLH}	3.3	1.0	9.5	13.0	1.0	14.0	ns
$\overline{C}_P$ to Q or $\overline{Q}$		5.0	1.0	7.5	10.0	1.0	11.0	
Propagation delay	t_{PHL}	3.3	1.0	10.0	13.5	1.0	14.5	ns
$\overline{C}_P$ to Q or $\overline{Q}$		5.0	1.0	8.0	10.5	1.0	11.5	
Propagation delay	t_{PLH}	3.3	1.0	9.5	13.0	1.0	14.0	ns
$\overline{C}_D$ to $\overline{Q}$		5.0	1.0	7.5	10.0	1.0	11.0	
Propagation delay	t_{PHL}	3.3	1.0	9.5	13.0	1.0	14.0	ns
$\overline{C}_D$ to $\overline{Q}$		5.0	1.0	7.5	10.0	1.0	11.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Operating Requirements: HD74AC107

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF	Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Typ	Guaranteed Minimum		
Setup time	t_{su}	3.3	3.0	5.5	6.0	ns
J or k to $\overline{C}_P$		5.0	2.0	4.0	4.5	
Hold time	t_h	3.3	–1.5	0.0	0.0	
$\overline{C}_P$ to J or k		5.0	–0.5	0.0	0.0	
Pulse width	t_w	3.3	2.0	5.5	7.0	
$\overline{C}_P$ or $\overline{C}_D$		5.0	2.0	4.5	5.0	
Recovery time	t_{rec}	3.3	1.5	3.0	3.0	
$\overline{C}_D$ to $\overline{C}_P$		5.0	1.0	3.0	3.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT107

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF			Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	5.0	100	—	—	80	—	MHz
Propagation delay $\overline{C_P}$ to Q or $\overline{Q}$	t_{PLH}	5.0	1.0	9.5	12.5	1.0	13.5	ns
Propagation delay $\overline{C_P}$ to Q or $\overline{Q}$	t_{PHL}	5.0	1.0	10.5	13.0	1.0	14.0	
Propagation delay $\overline{C_D}$ to $\overline{Q}$	t_{PLH}	5.0	1.0	8.5	11.0	1.0	12.0	
Propagation delay $\overline{C_D}$ to Q	t_{PHL}	5.0	1.0	8.5	11.0	1.0	12.0	

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Operating Requirements: HD74ACT107

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF	Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Typ	Guaranteed Minimum		
Setup time J or k to $\overline{C_P}$	t_{su}	5.0	2.5	7.0	8.0	ns
Hold time $\overline{C_P}$ to J or k	t_h	5.0	0.0	1.5	1.5	
Pulse width $\overline{C_P}$ or $\overline{C_D}$	t_w	5.0	4.5	7.0	8.0	
Recovery time $\overline{C_D}$ to $\overline{C_P}$	t_{rec}	5.0	—	3.0	3.0	

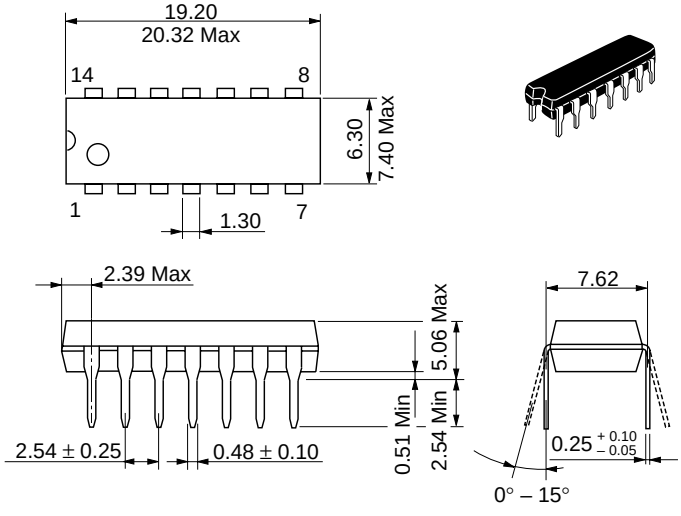
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	35.0	pF	V_{CC} = 5.0 V

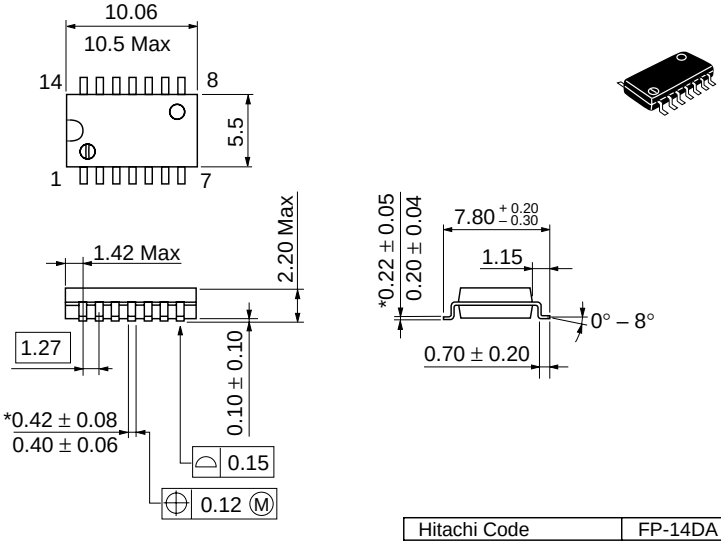
Package Dimensions

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.97 g

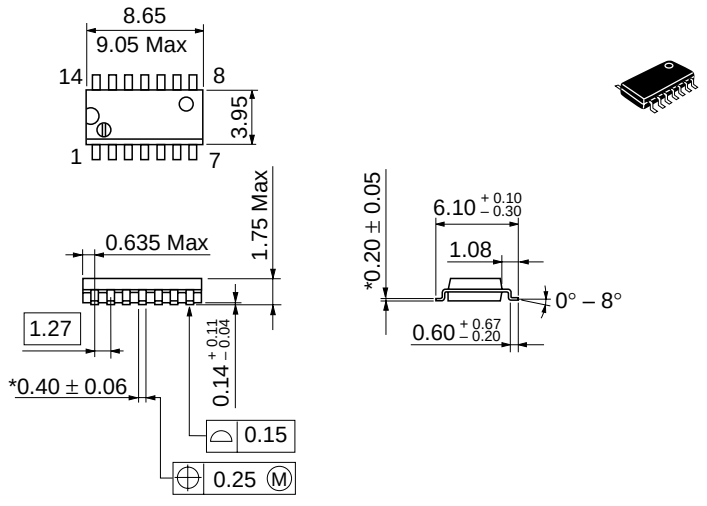
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.23 g

Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.13 g

*Pd plating

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