M64110WG

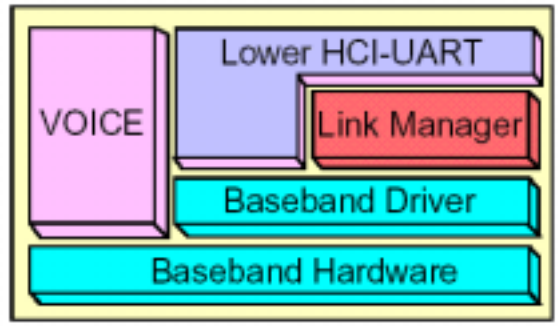
PRELIMINARY

REJ03F0002-0110Z
Rev.1.10
2003.05.20

BLUETOOTH BASEBAND LSI
(Under Development)

Description

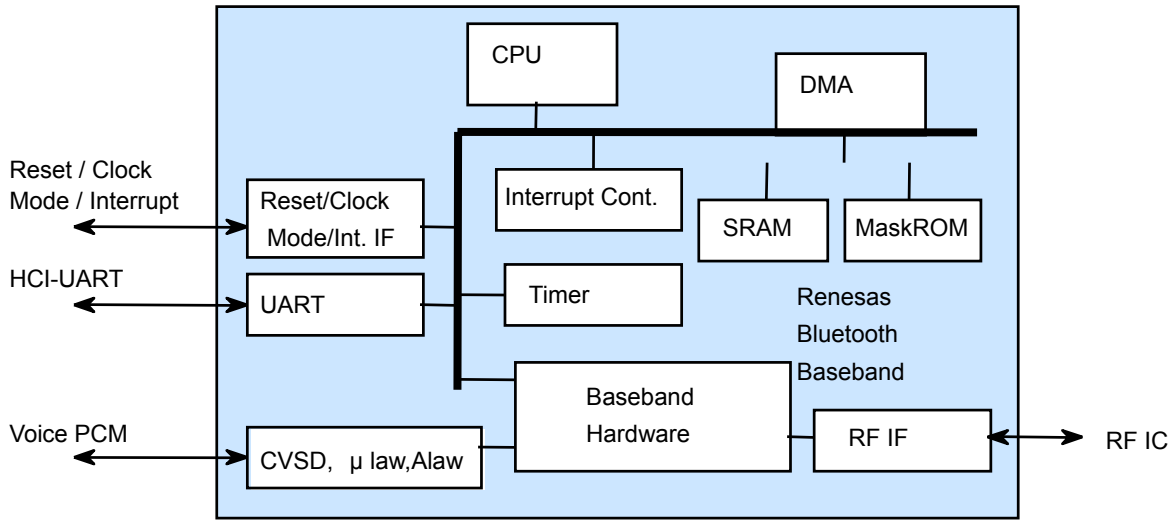
The Renesas Bluetooth Baseband provides the full functionality of HCI, Link Manager and Baseband, compliant with Bluetooth specification V1.1. ACL links support DM1, DH1, DM3, DH3, DM5, DH5 and AUX packets, whereas SCO links for voice channels support HV1, HV2, HV3 and DV packets. Flexible connections can be configured by switch of master slave role and piconet. The baseband operates at 16MHz and reduces power dissipation using low frequency oscillator at 32.768kHz in Sniff, Hold and Park modes. On the transceiver side the Renesas radio IC is supported.
The host interface is built based on HCI-UART and has some vendor-specific commands for selecting Radio IC type, 79-hop or 23-hop system, Write_BD_ADDR and so on.



Protocol Stack in Bluetooth Baseband

Features

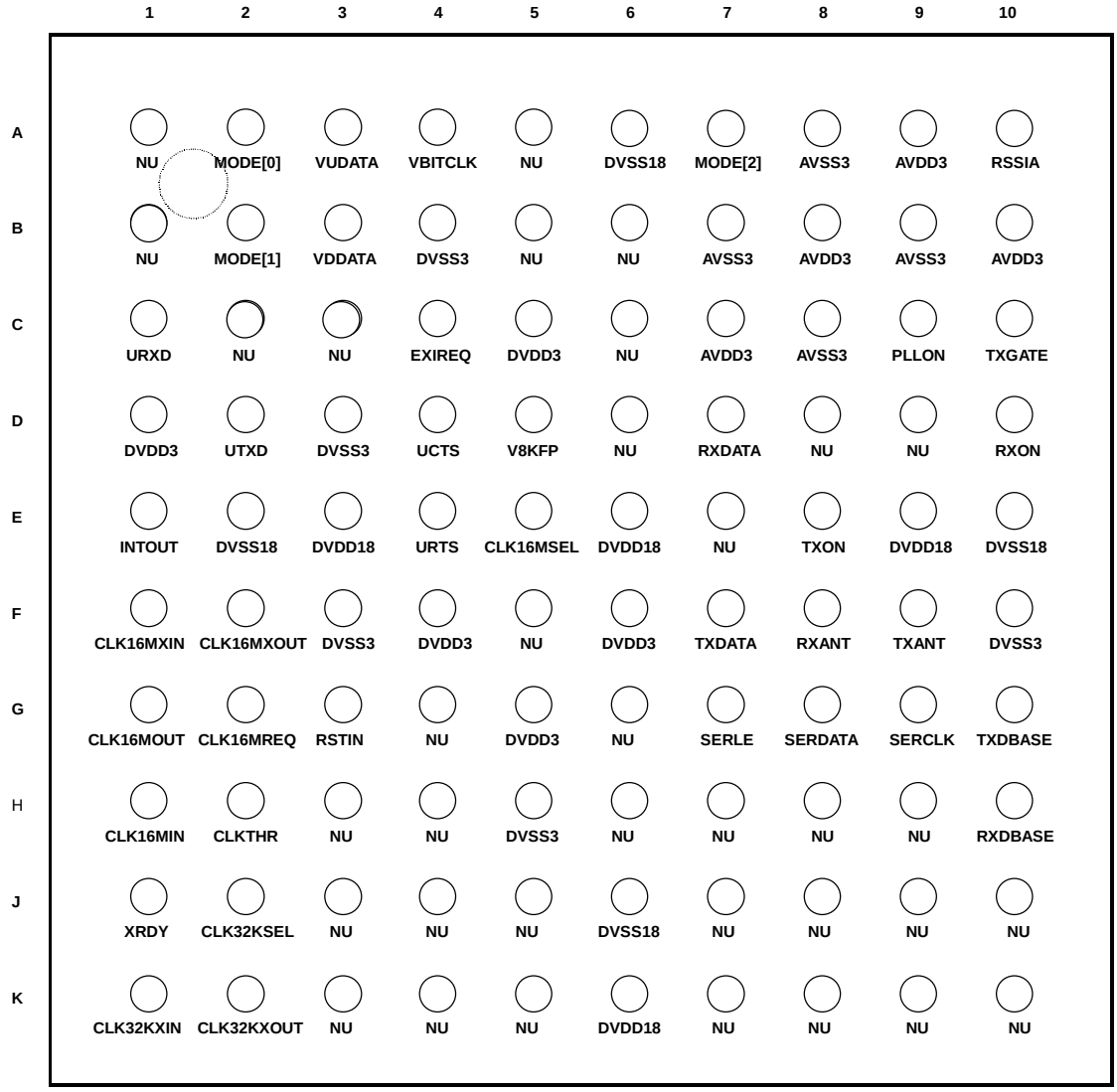
- Bluetooth V1.1 compliant
- HCI, Link Manager and Baseband functions
- Inquiry and Paging
- ACL link for command and data transfer
- SCO link for voice transfer (one channel)
- CRC, FEC, whitening and ARQ
- Authentication and Encryption
- Switch of master slave role
- Piconet (up to 7 devices)
- Sniff, Hold and Park mode operations
- Power control with low frequency oscillator at 32.768kHz
- Bluetooth test mode
- Radio interface for Renesas Radio IC
- Supports 79-hop and 23-hop systems
- 14-bit linear PCM interface for voice
- CVSD, µlaw and Alaw voice codecs
- Internal microprocessor running at 16MHz
- UART for HCI interface
- 100-pin FBGA 0.8mm ball pitch, 9mm x 9mm
- Operating Temperature Range -40 to 85 °C
- Digital supply voltage 1.8 to 2.0V for internal circuit
  Digital supply voltage 2.7 to 3.3V for I/O ports
  Analog supply voltage 2.7 to 3.3V



Functional Block Diagram

Device Pinout Diagram (100-pin FBGA)

Orientation from top of device



TOP VIEW

Pin Description for 100-pin FBGA

Pin Name for 100-pin		Type	Dir	Description
HCI-UART	UTXD	Dig	Out	Transmit data
	URXD	Dig	In	Receive data
	URTS	Dig	Out	Request to send
	UCTS	Dig	In	Clear to send
Voice	VBITCLK	Dig	In/Out	Voice bit clock
Interface	V8KFP	Dig	In/Out	Voice 8kHz frame pulse
	VDDATA	Dig	In	Voice downstream data
	VUDATA	Dig	Out	Voice upstream data
RF	TXDATA	Dig	Out	Transmit data
Interface	TXGATE	Dig	Out	Transmit gate
	RXDATA	Ana	In	Receive data
	PLLON	Dig	Out	PLL power on
	TXANT	Dig	Out	Transmitter antenna select
	TXON	Dig	Out	Transmitter power on
	RXANT	Dig	Out	Receiver antenna select
	RXON	Dig	Out	Receiver power on
	SERCLK	Dig	Out	Serial interface clock
	SERLE	Dig	Out	Serial interface control
	SERDATA	Dig	Out	Serial interface data in
	RSSIA	Ana	In	RSSI(Reserved)
	TXDBASE	Dig	Out	Transmit data for Baseband connection(for Test/Debug)
	RXDBASE	Dig	In	Receive data for Baseband connection(for Test/Debug)
Mode	MODE[2:0]	Dig	In	Mode select
Interrupt	EXIREQ	Dig	In	External interrupt request in
	INTOUT	Dig	Out	Interrupt out
Reset	RSTIN	Dig	In	External reset in
Clock	XRDY	Dig	In	Oscillator circuit ready
	CLKTHR	Dig	In	16MHz clock source select
	CLK16MSEL	Dig	In	16MHz clock source select(TCXO or Oscillator)
	CLK16MREQ	Dig	Out	External 16MHz clock request
	CLK16MIN	Dig	In	External 16MHz clock in
	CLK16MXIN	Xin	In	16MHz crystal in
	CLK16MXOUT	Xout	Out	16MHz crystal out
	CLK16MOUT	Dig	Out	External 16MHz clock out
	CLK32KSEL	Dig	In	32.768KHz clock source select
	CLK32KXIN	Xin	In	32.768kHz crystal in
	CLK32KXOUT	Xout	Out	32.768kHz crystal out

Pin Name for 100-pin		Type	Dir	Description
Power	DVDD3	VDD	-	Digital power supply for I/O ports
Ground	DVSS3	GND	-	Digital ground for I/O ports
	DVDD18	VDD	-	Digital power supply for internal logic
	DVSS18	GND	-	Digital ground for internal logic
	AVDD3	VDD	-	Analog Power Supply
	AVSS3	GND	-	Analog Ground

(Note1) NU pins should be opened.

Absolute Maximum Ratings

Symbol	Item	Condition	Rating	Unit
VDD3 (Note1)	Supply Voltage		-0.3 to 4.2	V
VDD18 (Note2)	Supply Voltage		-0.3 to 2.5	V
VI	Input Voltage	CLK16MIN	-0.3 to VDD18+0.3	V
VI	Input Voltage	Except CLK16MIN	-0.3 to VDD3+0.3	V
VO	Output Voltage		-0.3 to VDD3+0.3	V
Tstg	Storage Temperature		-55 to +125	°C

(Note1) DVDD3, AVDD3
(Note2) DVDD18

Recommended Operating Condition

Symbol	Item	Condition	Rating			Unit
			Min	Typ	Max	
VDD3 (Note1)	Supply Voltage		2.7	3.0	3.3	V
VDD18 (Note2)	Supply Voltage		1.8	1.9	2.0	V
VIH	'H' Level Input Voltage	Except CLK16MIN	0.7 x VDD3			V
VIL	'L' Level Input Voltage				0.8	V
Topr	Operating Temperature range		-40		85	°C

(Note1) DVDD3, AVDD3
(Note2) DVDD18

Electrical Characteristics (Unless otherwise stated: VDD3=2.7 to 3.3V,VDD18=1.8 to 2.0V,Topr=-40°C to +85°C)

Symbol	Item		Measurement Condition	Rating			Unit
				Min	Typ	Max	
VOH1	'H' Level Output Voltage	UTXD,URTS,VBITCLK V8KFP,VUDATA,PLLON TXGATE,TXON,RXON SERLE,SERCLK SERDATA,TXDBASE CLK16MREQ,INTOUT MODE[2:0] TESTOUT[11:0]	IOH=-1mA	VDD3-0.4			V
VOL1	'L' Level Output Voltage		IOL=+1mA			0.4	V
VOH2	'H' Level Output Voltage	CLK16MOUT	IOH=-2mA	VDD3-0.4			V
VOL2	'L' Level Output Voltage		IOL=+2mA			0.4	V
VOH3	'H' Level Output Voltage	TXDATA,TXANT,RXANT	IOH=-4mA	VDD3-0.4			V
VOL3	'L' Level Output Voltage		IOL=+4mA			0.4	V
IIH1	High State Input Current (Note 1)	URXD,UCTS,VBITCLK V8KFP,VDDATA,RSTIN XRDY,CLKTHR CLK16MSEL,INTOUT CLK32KSEL	VIH=VDD3			1	µA
IIL1	Low State Input Current (Note 1)		VIL=0V	-1			µA
IIH2	High State Input Current	EXIREQ	VIH=VDD3			1	µA
IIL2	Low State Input Current		VDD3=3V VIL=0V	-30	-15	-10	µA
IIH3	High State Input Current (Note 1)	RXDBASE, TSTMODE[5:1] TESTOUT[11:0]	VDD3=3V VIH=VDD3	10	15	30	µA
IIL3	Low State Input Current (Note 1)		VIH=0V	-1			µA

(Note 1) In/Out pins were measured with Output off.

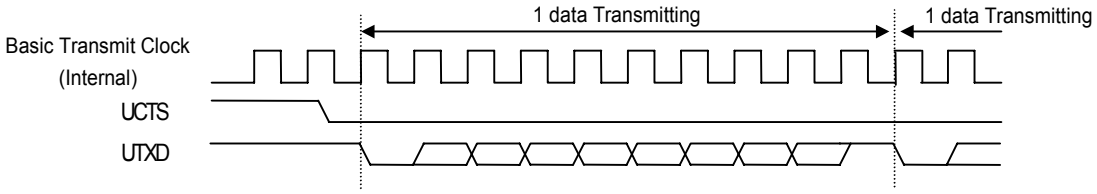
Timing Requirements (Unless otherwise stated: VDD3=2.7 to 3.3V,VDD18=1.8 to 2.0V)

Symbol	Item		Condition	Rating			Unit
				Min	Typ	Max	
$f_{CLK16MIN}$	16MHz Clock Input Frequency	CLK16MIN	Within +/-20ppm		16		MHz
$f_{CLK32KIN}$	32kHz Clock Input Frequency	CLK32XIN			32.768		kHz
f_{DUTY}	Clock Input Duty	CLK16MIN CLK32XIN		40		60	%
tr	Clock Input Rise Time	CLK16MIN				5	ns
tf	Clock Input Fall Time	CLK16MIN				5	ns
tw(RSTIN) (Note1)	Reset Input 'L' Pulse width	RSTIN		2			ms

(Note1) When power on, sufficient reset period is needed.

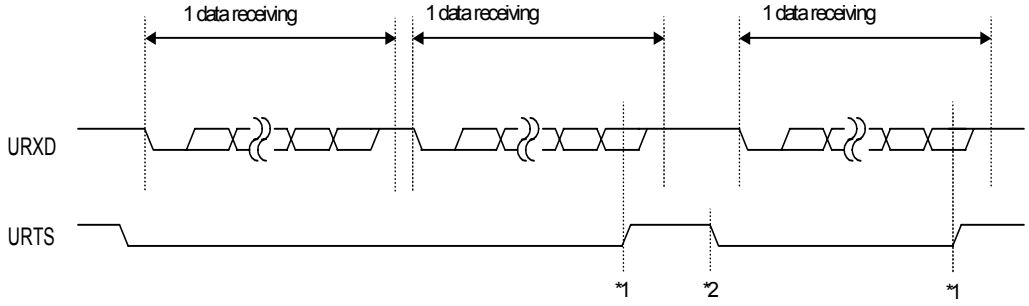
Example of UART Interface behavior

Transmit Timing



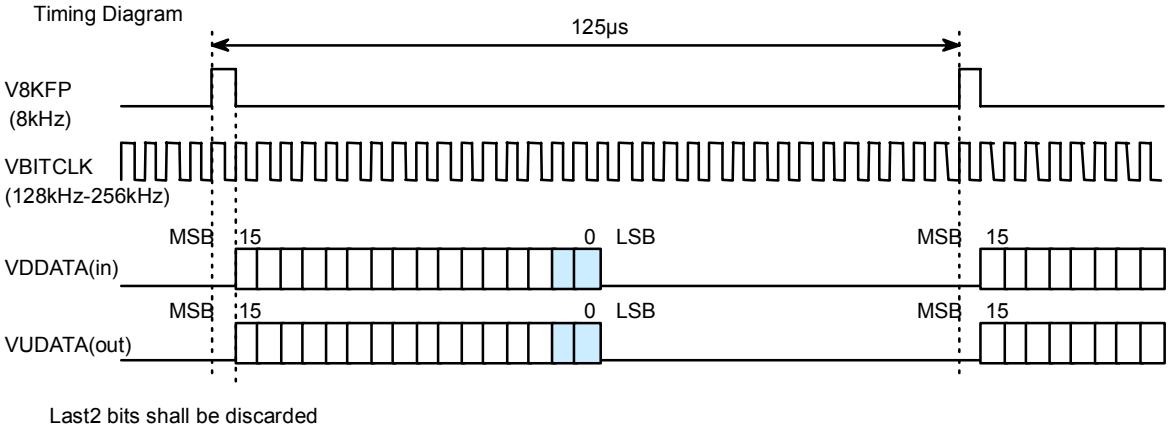
Notes)
- If the UCTS input pin changes to 'H' during the transmission of data byte and active UCTS function, the transmission stops after finishing the current transmission.
- Start and stop of transmission and UCTS function are executed by internal processing of Baseband.
- Basic clock is determined by the value set by internal baud rate.

Receive Timing



Notes)
- The above timing chart shows the status when 2 bytes data are received, 1 of 2 bytes received data is read, and then the next receiving are executed.
- If the most significant bit of the new data is received before reading received data from the received data register, the URTS pin becomes 'H'
- When the URTS pin is 'H', the UART becomes receive data storage status. Although receive operation is completed, the contents of receive shift buffer is not stored in the received data register. (*1)
- When the URTS pin is 'H', if the received data register is read, then the data of receive shift buffer in receive data storage status is stored in the received data register, and then each receive error flag and receive buffer flag for receive data stored at that time are set cumulatively, and then the URTS pin becomes 'L' (*2).
- If negative edge (level sense) is fed into the URXD input pin, receive control circuit judge that it is start bit and then sampling is executed around center of start bit. If the sampling input is 'L', receive sequence is started.

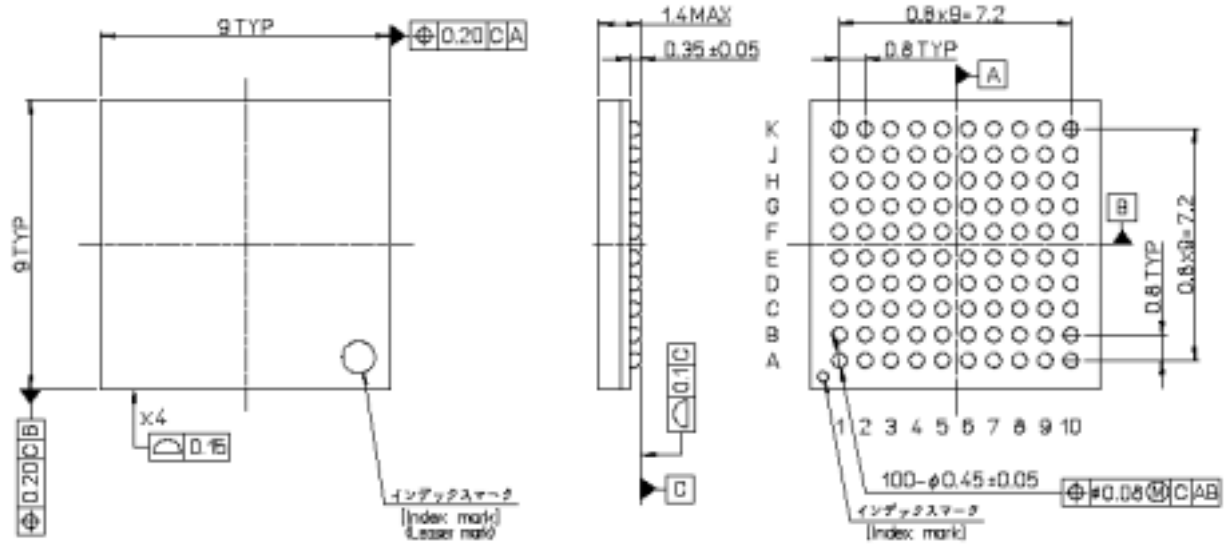
Example of **Voice Interface's behavior**



Last2 bits shall be discarded

Notes)
• VBITCLK can use the frequencies between 128Hz and 8kHz in steps of 8kHz.
• Last 2 bits of VDDATA and VUDATA will be discarded.

Package Diagram (100FHE)



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RENESAS

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REVISION HISTORY	M64110WG Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 1,2002	–	First Edition
1.10	Feb.11.2003	1,5,6	Digital supply voltage for I/O ports and analog supply voltage 2.7 to 3.3V
		1,5,6	Operating Temperature Range -40 to 85 °C