M64846FP

PRELIMINARY

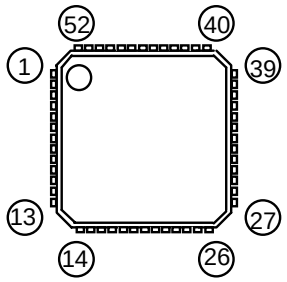
REJ03F0003-0110Z
Rev.1.10
2003.05.20

BLUETOOTH RF TRANSCEIVER LSI
(Under Development)

Description

The M64846FP is a semiconductor integrated circuit designed for 1 chip RF/IF transceiver with synthesizer for Bluetooth. It contains PLL, VCO and doubler for channel selection, PA for TX, LNA, IRM, IF-filter, limiter and discriminator for RX. It is designed using a high-frequency BiCMOS process and contributes to reduce size of system and current consumption.

PIN CONNECTIONS (TOP VIEW)



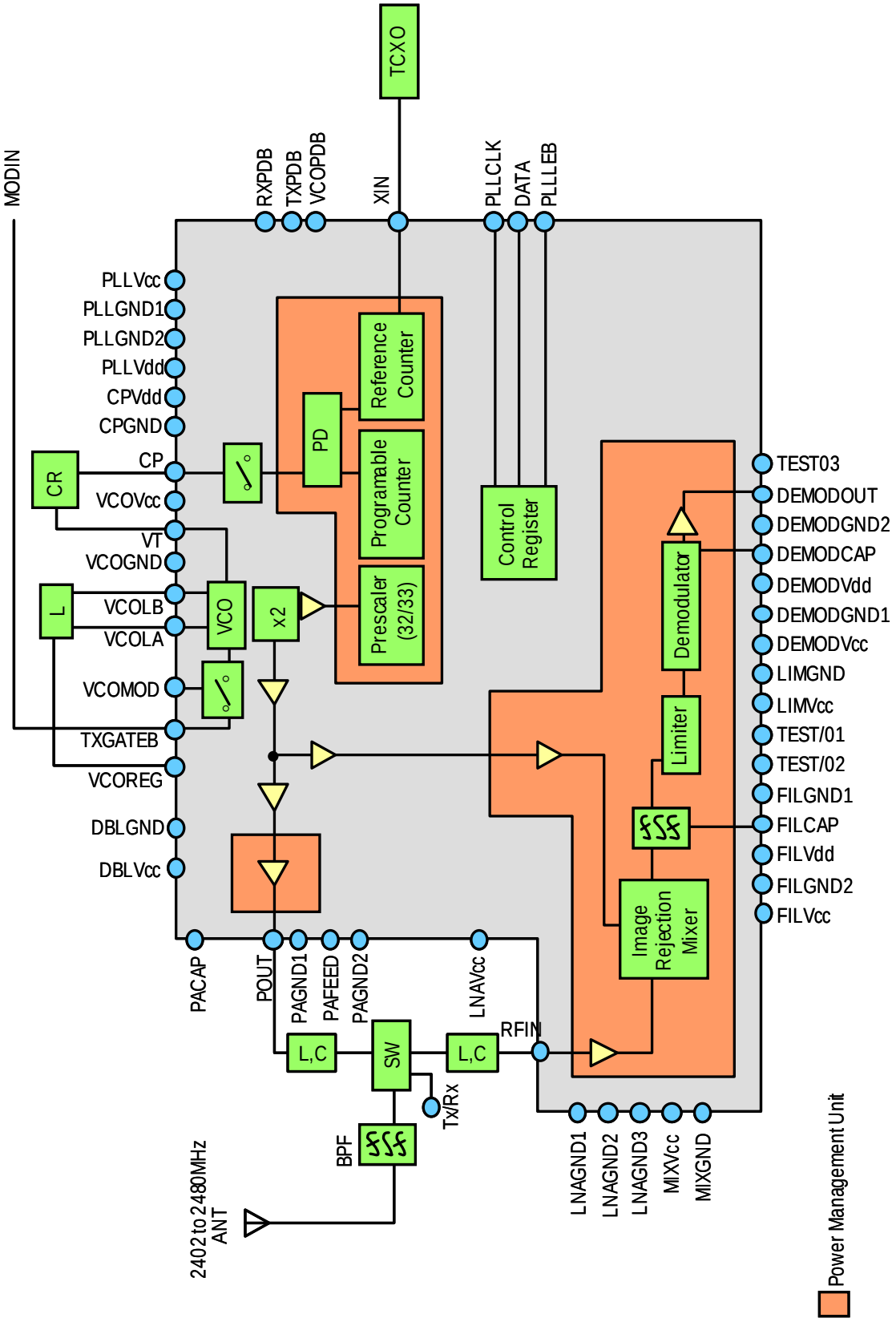
Outline 52QFN

Features

- Channel selection circuits
  - On chip 2.5GHz single PLL and 1.25GHz VCO
  - On chip Doubler (1.25GHz -> 2.5GHz)
- Transmitter circuits
  - Output power (+3dBm typ.) for Class2
- Receiver circuits
  - Minimum input sensitivity (-80dBm typ.)
  - On chip Low Noise Amplifier
  - On chip Image-Rejection-Mixer
  - Discriminator output (300mVpp at Dev.=+-150kHz <11110000...>)
- Operating Temperature Range –40 to 85 °C
- Operating Voltage 2.7 to 3.3V
- Current consumption
  - Txmode=43mA (Peak Typ.)
  - Rxmode=53mA (Peak Typ.)
  - Synthmode(Loop)=33mA (Typ.)
  - Standby=10μA or lower (Typ.)
- Small size 52pin lead less Package (Body7x7mm2, 0.4mm-pitch)

This is not a final specification. Some parameters limits are Subject to change.

Block Diagram



PIN Description (1/2)

Pin No.	Symbol	Description
1	MIXGND	Ground for RX MIX..
2	LNAGND3	Ground for RX LNA.
3	LNAGND2	Ground for RX LNA.
4	LNAGND1	Ground for RX LNA.
5	RFIN	RF signal input for RX LNA.
6	LNAVcc	Power supply for RX LNA. 2.7 to 3.3V
7	PACAP	Bias for TX PA. Pull down to GND with a resistor and a capacitor.
8	PAGND1	Ground for TX PA.
9	PAFEED	Feeder for TX PA. Pull up to Vcc with an inductor.
10	PAGND2	Ground for TX PA.
11	POUT	RF signal output for TX PA.
12	DBLVcc	Power supply for doubler. 2.7 to 3.3V
13	DBLGND	Ground for doubler.
14	VCOGND	Ground for VCO.
15	VCOLA	VCO inductor connection A.
16	VCOLB	VCO inductor connection B.
17	VCOMOD	Transmit modulation input
18	TXGATEB	Transmit modulation control input. L ;Modulation enable H ;Modulation off
19	VT	VCO tuning input.
20	VCOVcc	Power supply for VCO. 2.7 to 3.3V
21	VCOREG	VCO regulator output.
22	PLLGND1	Ground for PLL.
23	PLLVcc	Power supply for PLL (analog). 2.7 to 3.3V
24	CP	Charge-pump output.
25	CPGND	Ground for charge-pump.
26	CPVdd	Power supply for charge-pump. 2.7 to 3.3V

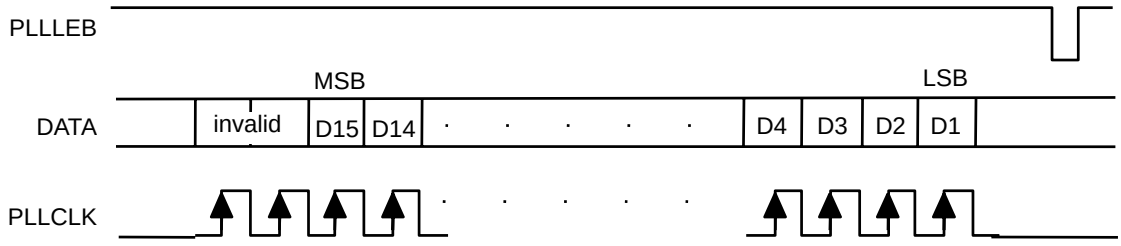
PIN Description (2/2)

Pin No.	Symbol	Description
27	XIN	Reference signal input for PLL.
28	PLLGND2	Ground for PLL.
29	PLLVdd	Power supply for PLL (digital). 2.7 to 3.3V
30	PLLLEB	Synthesizer enable signal input. H to L;DATA is loaded. H;PLL standby(except shift register) L;PLL Operating
31	PLLCLK	Clock pulse input for shift register.
32	DATA	Data input for shift register.
33	VCOPDB	Power down input for VCO (whole chip). L ;Power is off(except shift register). H ;Normal operation
34	TXPDB	Power down input for TX. L ;Power is off. H ;Normal operation
35	RXPDB	Power down input for RX. L ;Power is off. H ;Normal operation
36	DEMODGND1	Ground for discriminator.
37	DEMODOUT	Discriminator output.
38	DEMODVdd	Power supply for discriminator (Digital). 2.7 to 3.3V
39	DEMODGND2	Ground for discriminator.
40	DEMODCAP	Bias for discriminator. External LPF is connected.
41	DEMODVcc	Power supply for discriminator (analog). 2.7 to 3.3V
42	TESTO3	Test mode pin 3
43	LIMGND	Ground for LIM.
44	LIMVcc	Power supply for LIM. 2.7 to 3.3V
45	TESTI/O1	Test mode pin 1.
46	TESTI/O2	Test mode pin 2.
47	FILVdd	Power supply for RX filter (digital). 2.7 to 3.3V
48	FILCAP	Bias for RX filter. External LPF is connected.
49	FILGND1	Ground for RX filter.
50	FILVcc	Power supply for RX filter (analog). 2.7 to 3.3V
51	FILGND2	Ground for RX filter.
52	MIXVcc	Power supply for RX MIX. 2.7 to 3.3V

Functional Description

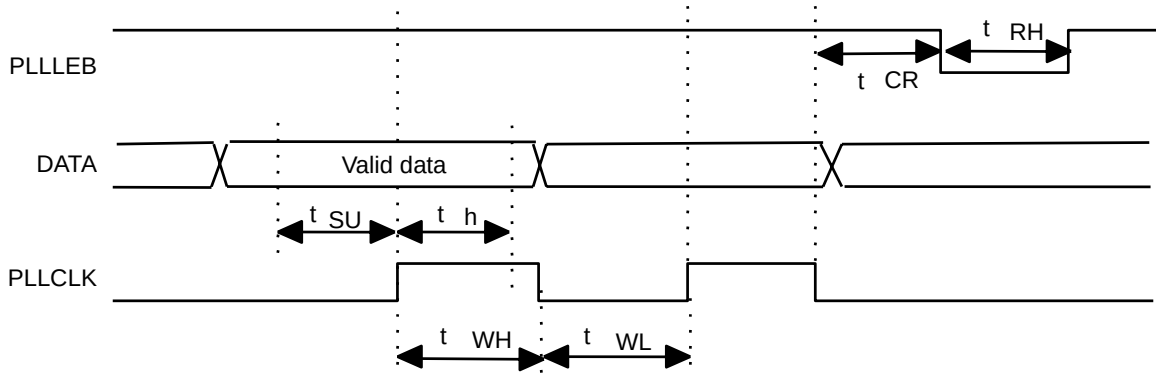
Data input for shift register of PLL

(1) Input procedure



Note 1) DATA input is taken into a shift register successively on a rising edge of PLLCLK input.
Note 2) Data input before an MSB is invalid.
Note 3) Shift register data is transferred to latches when PLLLEB change "H" to "L".

(2) Input signal timing

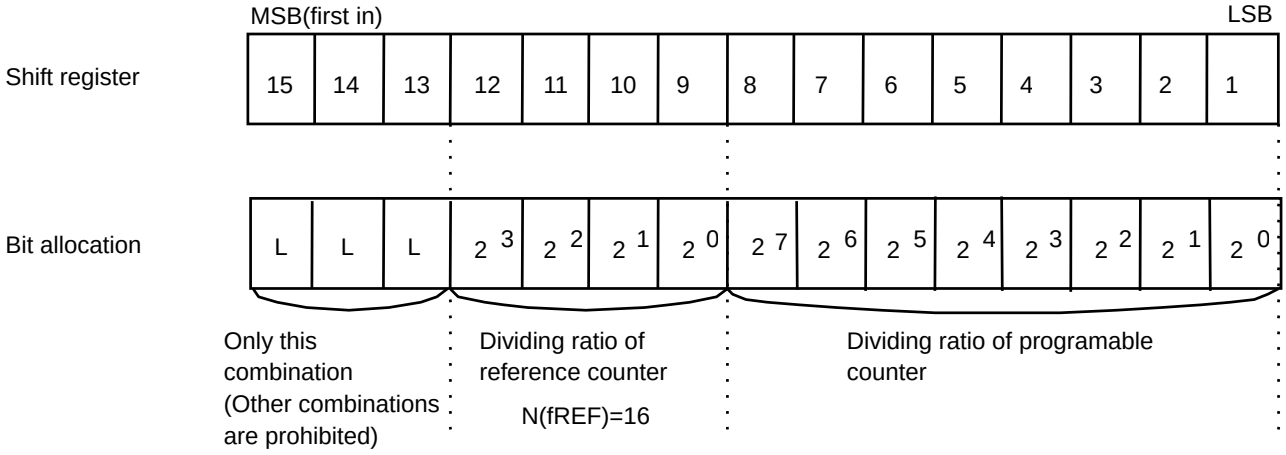


$t_{SU} = t_{WH} = t_{WL} = 40nS$ min.

$t_{CR} = 40nS$ min. $t_{RH} = 20\mu s$ min.

$t_{h} = 10nS$ min.

Bit configuration of shift register



Note 4) Dividing ratio of reference counter is fixed to 16.

N(fREF)=16

For example, if use 16MHz TCXO, fREF is set “1MHz”.

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
L	L	L	N(fREF)=16				*	*	*	*	*	*	*	*
L	L	L	*	*	*	*	Dividing ratio of programmable counter							

Note 5) Dividing ratio of a programmable counter N(VCO) is provided by 8-bit code.

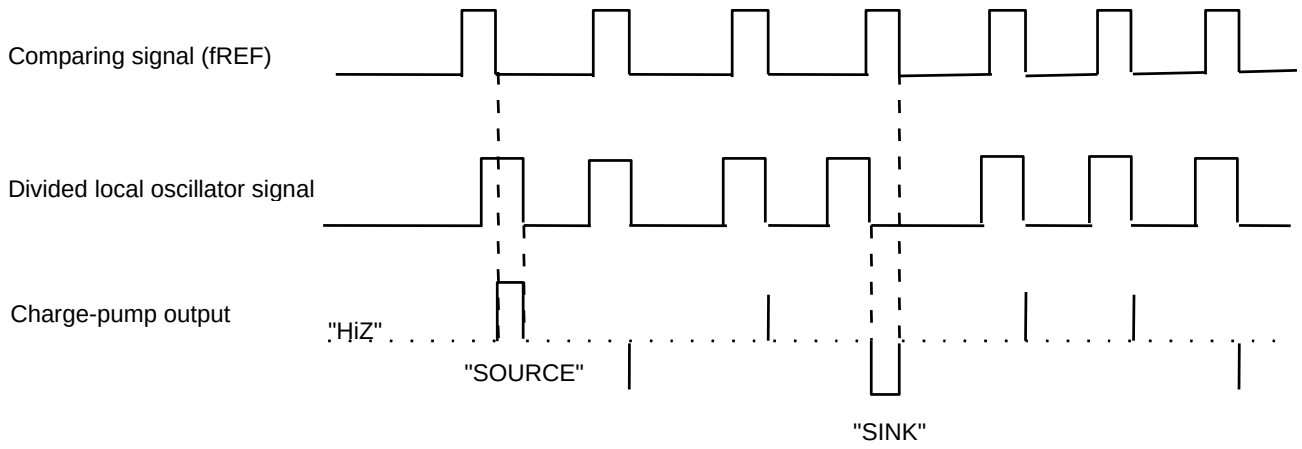
N(VCO)=2304 + M M :Set by 8-bit code(0 to 255)

For example, if use fTX=2450MHz at fREF=1MHz, N(VCO) must be set as follows.
N(VCO)=2450M/1M=2450=2304+146 i.e. M=146=27+24+21

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
L	L	L	*	*	*	*	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
L	L	L	Anything				H	L	L	H	L	L	H	L

Charge-pump



Note 6) If the phase of the divided local oscillator signal (fVCO/N) is behind the phase of comparing signal (fREF), the charge-pump output turns to "SOURCE" state. If it is ahead of that, the output turns to "SINK" state.

Power supply control input

The power supply can be turned on or off in each circuit according to states of input pins. (VCOPDB, TXPDB, RXPDB, PLLLEB)

Note 7) RX and TX power ON/OFF can be controlled by RXPDB, TXPDB and VCOPDB input.
RX part means LNA, MIX, Filter, LIM and Discriminator.
TX part means PA and TX-Buffer.
VCO part means VCO, Doubler.

PIN			BLOCK STATUS		
VCOPDB	TXPDB	RXPDB	VCO	TX	RX
L	*	*	OFF	OFF	OFF
H	H	L	ON	ON	OFF
H	L	H	ON	OFF	ON
H	L	L	ON	OFF	OFF

*; Don't care.

Note 8) PLL power ON/OFF is controlled by VCOPDB and PLLLEB input.
If Voltage source supply for all Vcc and Vdd, DATA is taken into shift register when PLL part is off.
PLL part means PD, charge-pump and divider.

PIN		BLOCK STATUS
VCOPDB	PLLLEB	PLL
H	L	ON
H	H	OFF
H	H to L	PLL DATA is loaded
L	*	OFF

*; Don't care.

VCO modulation and control input

Modulation can be controlled according to states of TXGATEB input and VCOMOD input.

PIN	STATUS	PIN	STATUS
TXGATEB	Modulation	VCOMOD	TX Frequency
H	disenable	*	fRF
L	enable	H	fRF+fd
		L	fRF-fd
		HiZ	fRF

fRF: Suitable tuned frequency for CH
fd: Frequency deviation of modulation

At useing for RX, TXGATEB input must be set to "H" or VCOMOD input must be set to "HiZ".

Absolute Maximum Ratings (Ta=-40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings		Unit
			Min.	Max.	
Vcc,Vdd	Supply voltage	GND=0V	-0.3	4.5	V
VI	Input voltage	GND=0V	-0.3	4.5	V
IO	Output current	GND=0V	-10	0	mA
Pd	Power dissipation	Ta=85 °C (allowed power dissipation of the package)		444	mW
Topr	Operating ambient temperature		-40	85	°C
Tstg	Storage ambient temperature		-40	125	°C

Recommended Operating Conditions (Ta=-40 to 85 °C, unless otherwise noted)

PLL and VCO

Symbol	Parameter	Conditions	Ratings			Unit
			Min.	Typ.	Max	
Vcc	Supply voltage		2.7	3.0	3.3	V
Vdd			2.7	3.0	3.3	V
Delta (Vcc-Vdd)					0.1	V
VXIN	XIN Input amplitude	Vcc=Vdd=2.7 to 3.3V FXIN=8 to 23MHz Sin Wave	0.5		1.5	Vpp
fXIN	XIN Input frequency	Vcc=Vdd=2.7 to 3.3V	8	16	23	MHz
fVCO	VCO frequency	Vcc=Vdd=2.7 to 3.3V	1.1		1.3	GHz

Transmitter

Symbol	Parameter	Conditions	Ratings			Unit
			Min.	Typ.	Max.	
Vcc	Supply voltage		2.7	3.0	3.3	V
fPOUT	TX Output frequency	Vcc=Vdd=2.7 to 3.3V	2.4		2.5	GHz
fVCO	VCO frequency	Vcc=Vdd=2.7 to 3.3V	1.2		1.25	GHz

Receiver

Low Noise Amplifier, Mixer

Symbol	Parameter	Conditions	Ratings			Unit
			Min.	Typ.	Max.	
Vcc	Supply voltage		2.7	3.0	3.3	V
fRFIN	LNA Input frequency	Vcc=Vdd=2.7 to 3.3V	2.4		2.5	GHz
fVCO	VCO frequency	Vcc=Vdd=2.7 to 3.3V	1.2		1.25	GHz

IF

Symbol	Parameter	Conditions	Ratings			Unit
			Min.	Typ.	Max.	
Vcc	Supply voltage		2.7	3.0	3.3	V
fIF	IF Input frequency	Vcc=Vdd=2.7 to 3.3V		3		MHz

Electrical Characteristics

Current consumption (Ta=25 °C, unless otherwise noted)

Symbol	Parameter	Objective pins	Conditions	Ratings			Unit
				Min.	Typ.	Max	
Icc1	Supply current	MIXVcc, LNAVcc, DBLVcc, VCOVcc, CPVdd, PLLVcc, PLLVdd, DEMODVcc, DEMODVdd, LIMVcc, FILVcc, FILVdd, POUT, PAFEED	Vcc=Vdd=3.0V RX and VCO are on. (TX and PLL are off.)		53		mA
Icc2			Vcc=Vdd=3.0V TX and VCO are on. (RX and PLL are off.)		43		mA
Icc3			Vcc=Vdd=3.0V PLL and VCO are on. (RX and TX are off.)		33		mA
Icc4			Vcc=Vdd=3.0V Standby (VCOPDB=L)			10	µA

PLL and Control (Ta=25 °C, unless otherwise noted)

Symbol	Parameter	Objective pins	Conditions	Ratings			Unit
				Min.	Typ.	Max	
VIH	`H` Input voltage	DATA, PLLCLK, PLLLEB, VCOPDB, RXPDB, TXPDB, TXGATEB	Vcc=Vdd=2.7 to 3.3V Ta=-40 to 85 °C	Vcc-0.4V		Vcc	V
VIL	`L` Input voltage	DATA, PLLCLK, PLLLEB, VCOPDB, RXPDB, TXPDB, TXGATEB	Vcc=Vdd=2.7 to 3.3V Ta=-40 to 85 °C	0		0.4	V
IIH	`H` Input current	DATA, PLLCLK, PLLLEB, VCOPDB, RXPDB, TXPDB, TXGATEB	Vcc=Vdd=2.7 to 3.3V VIH=3.3V Ta=-40 to 85 °C			2	µA
IIL	`L` Input current	DATA, PLLCLK, PLLLEB, VCOPDB, RXPDB, TXPDB, TXGATEB	Vcc=Vdd=2.7 to 3.3V VIL=0V Ta=-40 to 85 °C	-2			µA

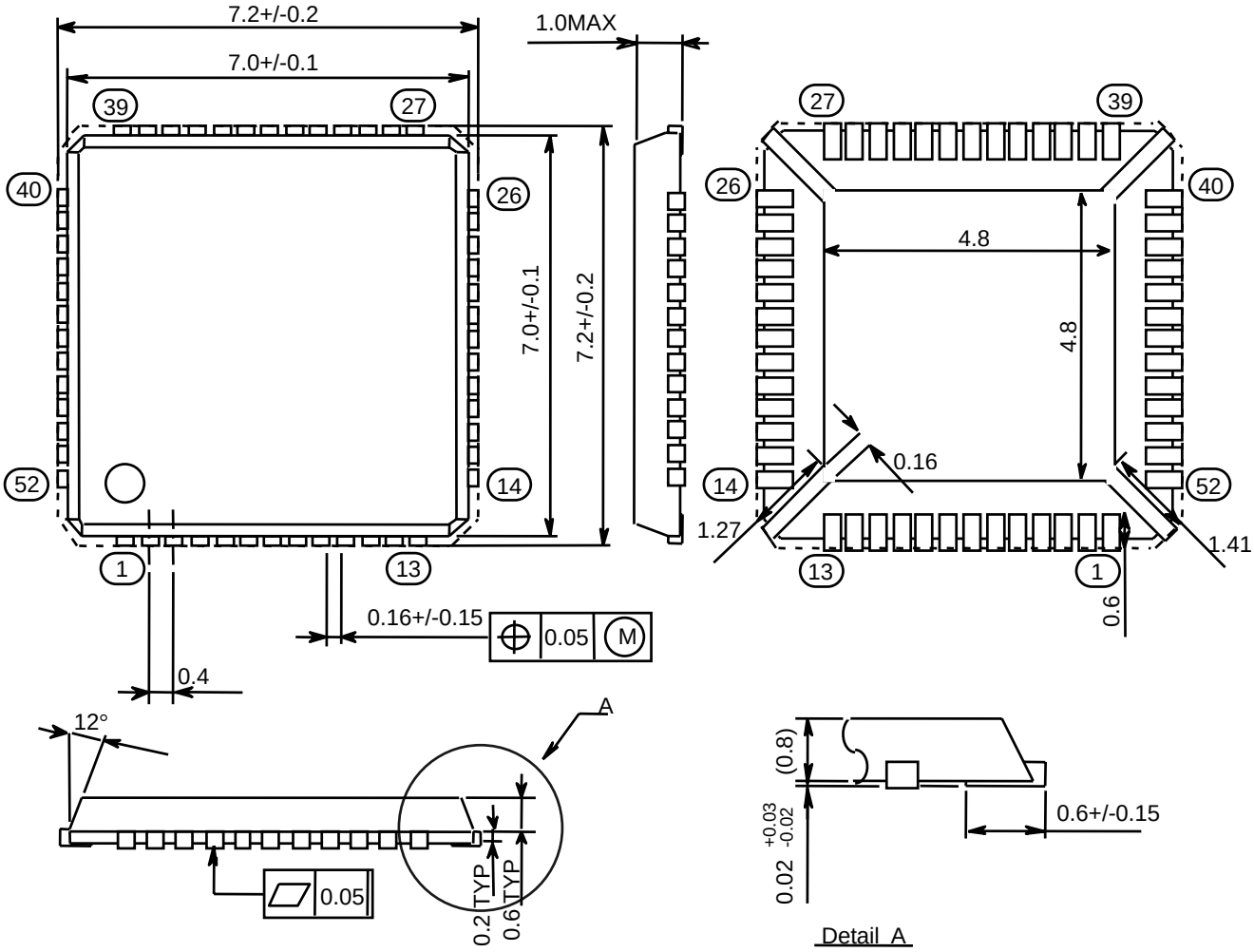
Transmitter & VCO (Ta=25 °C, unless otherwise noted)

Symbol	Parameter	Objective pins	Conditions	Ratings			Unit
				Min.	Typ.	Max	
POUT	RF Output power	POUT	Vcc=Vdd=3.0V fPOUT=2441MHz (Continuous)		+3		dBm
fmod (Delta f1avg)	VCO Modulation	POUT	Vcc=Vdd=3.0V 00001111 sequence Average		160		kHz
VmodH	Modulation `H` input voltage	VCOMOD	Vcc=Vdd=2.7 to 3.3V	Vcc-0.4		Vcc	V
VmodL	Modulation `L` input voltage	VCOMOD	Vcc=Vdd=2.7 to 3.3V	0		0.4	V
VREG	Regulated voltage	VCOREG	Vcc=Vdd= 3.0V Io=-4mA		2.7		V

Receiver (Ta=25 °C, unless otherwise noted)

Symbol	Parameter	Objective pins	Conditions	Ratings			Unit
				Min.	Typ.	Max.	
SRFIN-min	Sensitivity	RFIN, DEMODOUT	Vcc=Vdd=3.0V fRFIN=2441MHz,BER<=0.1%		-80		dBm
SRFIN-max	Maximum input level		Vcc=Vdd=3.0V fRFIN=2441MHz,BER<=0.1%		-15		dBm
IM	Intermodulation		Vcc=Vdd=3.0V fRFIN=2441MHz,-67dBm fI2-fI1=4MHz,BER<=0.1%		-28		dBc
C/I0	Co-channel interference		Vcc=Vdd=3.0V fRFIN=2441MHz,-63dBm fI=2441MHz,BER<=0.1%		+11		dBc
C/I image	Image frequency interference		Vcc=Vdd=3.0V fRFIN=2441MHz,-70dBm fI=2447MHz,BER<=0.1%		-15		dBc

Package Outline Dimensions



Precautions

1. The IC is designed utilizing fine pattern components for high performance. Therefore, proper ESD precautions in the handling are recommended to prevent the IC from high energy electrostatic discharges.
2. Though each block is powered via separated terminals for robust isolation between the circuits, an unused circuit should be powered via the corresponding supply pin and turned off by control input pins.

MEMO

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http://www.renesas.com

REVISION HISTORY	M64846FP Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 1,2002	–	First Edition
1.10	Feb.11.2003	1,9	Operating ambient temperature change
		6	Dividing ratio of reference counter change