2.4GHz Power Amplifier and Detector

The ISL3985 is a 2.4GHz monolithic SiGe Power Amplifier designed to operate in the ISM Band. It features two low voltage single supply stages. Cascaded, they deliver 20dBm (Typ) output power for the typical DSSS signal.

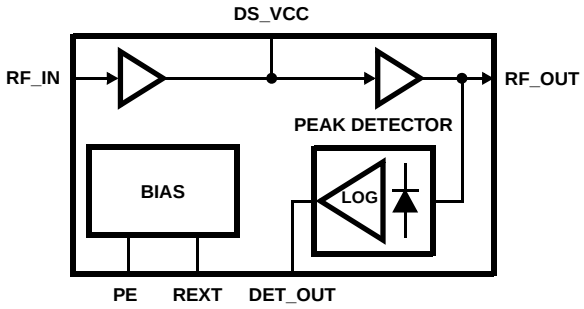
In addition, the device includes a 2.4GHz detector which is accurate over a 15dB dynamic range within (±)1dB. Therefore, an accurate ALC function can be implemented.

The ISL3985 is housed in a 16 lead QFN package.

Ordering Information

PART NUMBER	TEMP RANGE (^{o}C)	PACKAGE	PKG. DWG. #
ISL3985IR	-40 to 85	16 Ld. QFN	L16.5x5B
ISL3985IR-TK	-40 to 85	Tape and Reel (1000 units)	

Simplified Block Diagram



Features

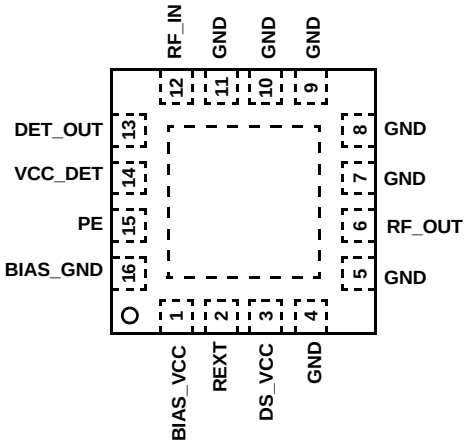
- Single Supply . . . . . 2.7V to 3.6V
- Output Power . . . . . 20dBm (Typ) at ACPR, DSSS, 1st Side Lobe < -30dBc, 2nd Side Lobe < -50dBc
- Power Gain. . . . . 25.5dB (Typ)
- Detector Linear Input Power Range 15dB
- Detector Accuracy . . . . . ±1dB
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile

Applications

- Systems Targeting IEEE802.11 WLANs @ 2.4GHz
- Wireless Local Area Networks (WLAN)
- PCMCIA Wireless Transceivers
- ISM Systems Including Automatic Level Control (ALC)
- TDMA Packet Protocol Radios

Pinouts

ISL3985 (QFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	NAME	DESCRIPTION
1	BIAS_VCC	Power Supply.
2	REXT	Bias Resistor, biasing scheme independent of absolute temperature.
3	DS_VCC	Driver Stage Power Supply.
4, 5	GND	DC and RF Ground.
6	RF_OUT	RF Output of the Power Amplifier.
7, 8, 9, 10, 11	GND	DC and RF Ground.
12	RF_IN	RF Input of the Power Amplifier.
13	DET_OUT	Detector Output.
14	VCC_DET	Detector Power Supply.
15	PE	Digital Input Control Pin to enable operation of the Power Amplifier. Enable logic level is high.
16	BIAS_GND	DC and RF Ground.
Exposed Pad	N/A	DC and RF Ground

The ISL3985 works seamlessly with the PRISM II and PRISM 2.5 and 3 WLAN chip set components to complete a highly integrated, cost effective WLAN solution in the 2.4 to 2.5GHz ISM band. The ISL3985 is fabricated in the fastest SiGe BiCMOS process available allowing superior RF performance, normally found only in GaAs ICs. Cost effective functions, normally requiring external components, are integrated into one IC. The ISL3985 integrates the following functions in one compact 16 pin QFN:

- Two Stage, 25.5dB Gain RFPA,
- Logarithmic power detect function (15dB Dynamic Range),
- CMOS level compatible Power Up/Down function,
- Single Supply, 2.7V to 3.6V Operation.

The ISL3985 contains a highly linear RFPA designed to deliver 20dBm and meet an ACPR specification of -30dBc in the 2.4 to 2.5GHz ISM band. The efficiency of this two stage RFPA can be optimized by adjusting the bias current with a dedicated resistor when lower power output is used. No external positive or negative power supplies are required to set the bias currents. The on chip bias network provides the optimum bias current temperature compensation when low TC external resistor is used. To get the best performance from the ISL3985, the output stage matching network can be tailored using external components.

The ISL3985 power detect function provides a DC output voltage that is proportional to the logarithm of the output power. For an output power of 23dBm, the detector is accurate to within 0.5dB. The slope of the detector output voltage is 100mV/dB over a 15dB dynamic range. A simple application of the detector is to provide in-line monitoring of the output power using a DC voltmeter. A more value added application would use one of Intersil PRISM Baseband Processors to dynamically monitor the ISL3985 output power and to control transmit power by adjusting the AGC of the previous state to provide the best possible error free data transfer rate for any given environment. Closed loop power control is very important feature which compensates for variability in the transmit chain (radio to radio, channel to channel, over temperature...).

The ISL3985 power up/down feature integrates the power down capability onto the IC and requires no external components thus freeing up board space and reducing external component count and cost. When the CMOS compatible Power Enable (PE) pin is driven low, the total supply current drops to under 50μA in, typically, 300ns. When the PE pin is driven high, the full ISL3985 output power is available in a few hundred nanoseconds.

In summary, the ISL3985 RFPA provides a highly cost effective solution for the PA function by integrating many features that would require significant development time, drive up the total bill of materials cost and consume precious board space. It mates seamlessly with the other PRISM ICs to provide a highly integrated, cost effective WLAN solution in the 2.4 to 2.5GHz ISM band.

Absolute Maximum Ratings

Supply Voltage 4.0V
Voltage on Any Other Pin. . . . . -0.3 to V_{CC} +0.3V
V_{CC} to V_{CC} Decouple . . . . . -0.3 to +0.3V
Any GND to GND. . . . . -0.3 to +0.3V

Operating Conditions

Temperature Range . . . . . -40 to 85^{o}C
Supply Voltage Range . . . . . 2.7V to 3.6V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
QFN Package	33	3

Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range. . . . . -65^{o}C to 150^{o}C
For Recommended soldering conditions see Tech Brief TB389.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. θ_{JC}, the "case temp" is measured at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

General DC Electrical Specifications, T_A = 25^{o}C

PARAMETER	MIN	TYP	MAX	UNITS
Supply Voltage	2.7	-	3.6	V
Total Power Amplifier Supply Current at 3.3V, 21dBm Output	-	325	360	mA
RF Detector Supply Current	-	1.4	2.0	mA
Power Down Supply Current	-	30	-	µA
Power Up/ Down Speed	-	230	-	ns
CMOS Low Level Input Voltage	-	-	0.3*V_{DD}	V
CMOS High Level Input Voltage (V_{DD} = 3.6V)	0.7*V_{DD}	-	4	V
CMOS Threshold Voltage	>0.3*V_{DD}	0.5*V_{DD}	<0.7*V_{DD}	V
CMOS High or Low Level Input Current	-10	-	+10	µA

Power Amplifier AC Electrical Specifications

V_{CC} = 3.3V, f = 2.45GHz, Unless Otherwise Specified. Typical Application Circuit (external input and output matching networks) have been used. T_A = 25^{o}C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range		2400	-	2500	MHz
Power/Voltage Gain		25.0	26.5	28.0	dB
Output P1dB		-	21	-	dBm
AM to PM @ compression		-	5.5	-	Degrees
Input 50Ω VSWR		-	-	2:1	-
Output 50Ω VSWR		-	-	3:1	-
Output Power	ACPR, DSSS, 1st Side Lobe <-30dBc, 2nd Side Lobe <-50dBc	19.5	20.7	-	dBm
Output Stability VSWR	Output Spurs Less than -60dBc	-	-	10:1	-
Output Load Mismatch	(Note 2)	-	-	10:1	-

NOTE:

2. Devices sustain no damage when subjected to a mismatch of maximum 10:1.

Peak Detector AC Electrical Specifications T_A = 25^{o}C

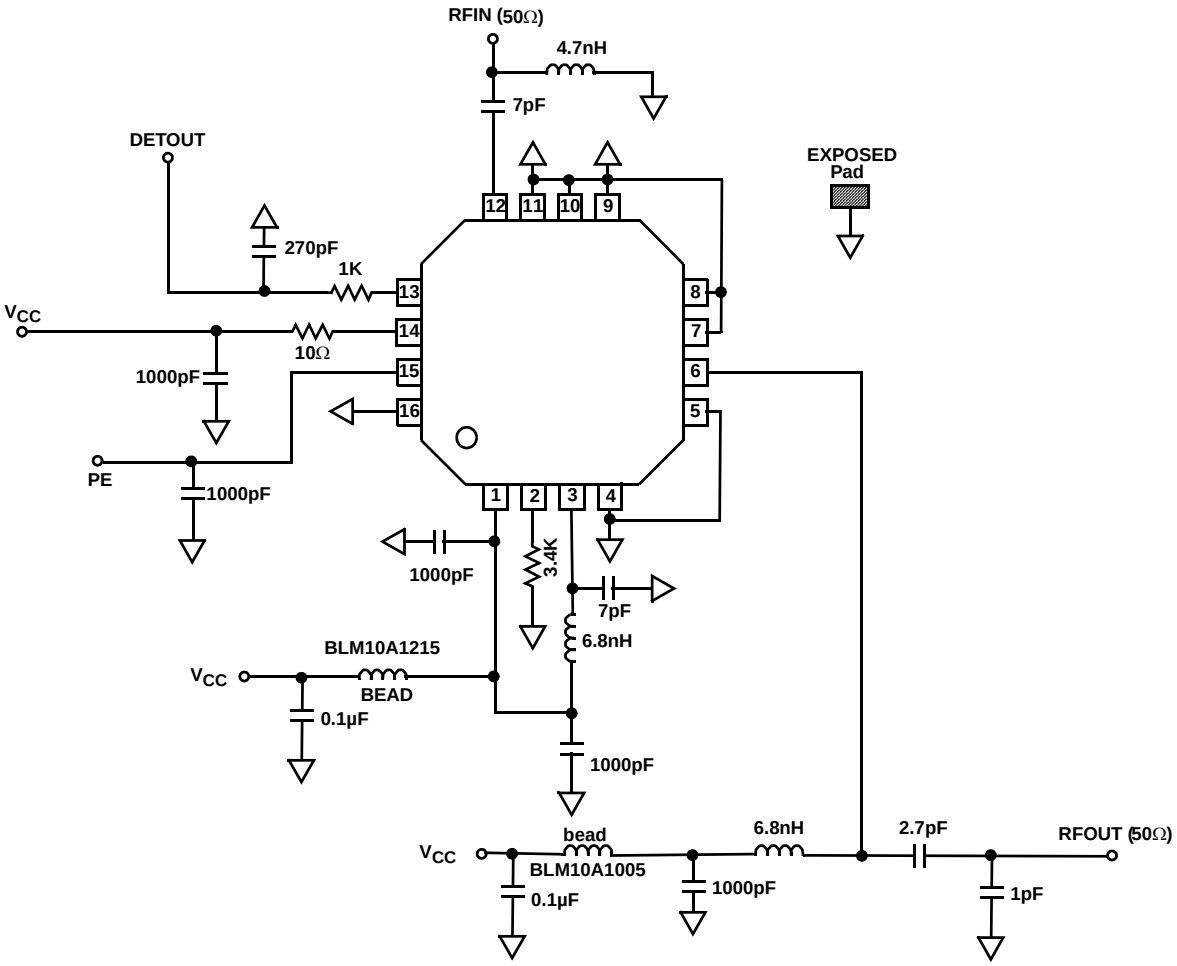
PARAMETER	TEST CONDITIONS	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
RF Output Detector Response Time	External Capacitor, C = 5pF	Full	-	0.15	-	µs
RF Output Detector Voltage Range	Load > 1M	Full	0	-	1.5	V
RF Output Detector Linearity	Over Linear Range	Full	-0.5	-	+0.5	dB/V

Peak Detector AC Electrical Specifications $T_A = 25^oC$ **(Continued)**

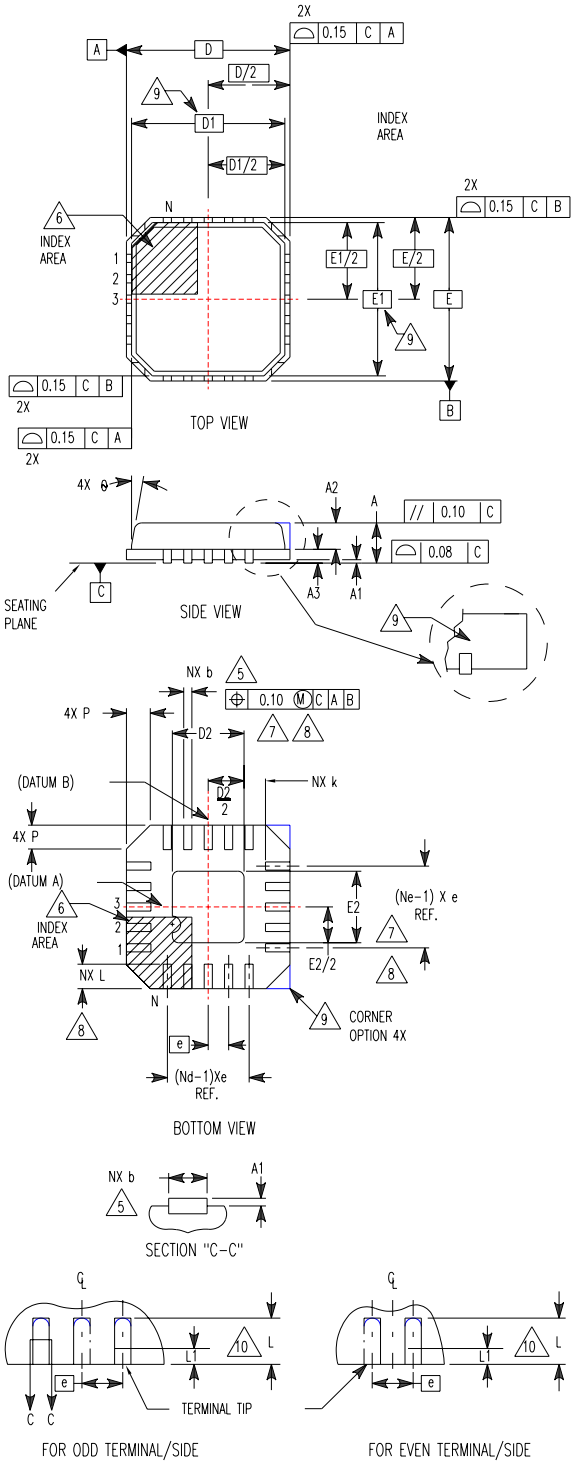
PARAMETER	TEST CONDITIONS	TEMP. (^oC)	MIN	TYP	MAX	UNITS
RF Output Detector Accuracy	600mV$_{DC}$ Output	Full	-1	-	+1	dB
RF Output Detector Slope	Over Linear Range	Full	-	10	-	dB/V

Typical Application Example

ISL3985 - 16 PIN QFN PACKAGE



Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.5x5B

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHB ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.28	0.33	0.40	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7, 8
e		0.80 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.