



# STD60NF55LA

N-CHANNEL 55V - 0.012Ω - 60A DPAK

STripFET™II MOSFET

**Table 1: General Features**

| TYPE        | V <sub>DSS</sub> | R <sub>DS(on)</sub> | I <sub>D</sub> (1) |
|-------------|------------------|---------------------|--------------------|
| STD60NF55LA | 55V              | < 0.015Ω            | 60A                |

- TYPICAL R<sub>DS(on)</sub> = 0.012Ω
- LOW THRESHOLD DRIVE

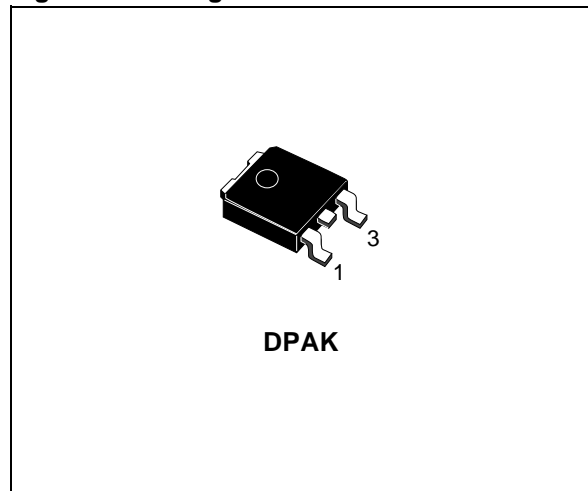
## DESCRIPTION

This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

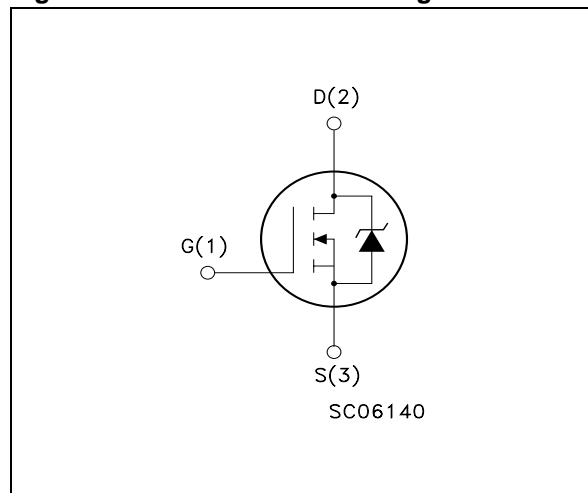
## APPLICATIONS

- HIGH CURRENT, HIGH SWITCHING SPEED

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

| Part Number   | Marking   | Package | Packaging   |
|---------------|-----------|---------|-------------|
| STD60NF55LAT4 | D60NF55LA | DPAK    | TAPE & REEL |

**Table 3: Absolute Maximum ratings**

| Symbol              | Parameter  | Value       | Unit |
|---------------------|--|-------------|------|
| V <sub>DS</sub>     | Drain-source Voltage (V <sub>GS</sub> = 0)           | 55          | V    |
| V <sub>GS</sub>     | Gate- source Voltage                                 | ± 15        | V    |
| I <sub>D</sub>      | Drain Current (continuous) at T <sub>C</sub> = 25°C  | 60          | A    |
| I <sub>D</sub>      | Drain Current (continuous) at T <sub>C</sub> = 100°C | 42          | A    |
| I <sub>DM</sub> (●) | Drain Current (pulsed)                               | 240         | A    |
| P <sub>TOT</sub>    | Total Dissipation at T <sub>C</sub> = 25°C           | 110         | W    |
|                     | Derating Factor                                      | 0.73        | W/°C |
| dv/dt (1)           | Peak Diode Recovery voltage slope                    | 16          | V/ns |
| E <sub>AS</sub> (2) | Single Pulse Avalanche Energy                        | 400         | mJ   |
| T <sub>stg</sub>    | Storage Temperature                                  | - 55 to 175 | °C   |
| T <sub>j</sub>      | Operating Junction Temperature                       |             |      |

(●) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 40A, di/dt ≤ 350A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

(2) Starting T<sub>j</sub>=25°C, I<sub>D</sub>=30A, V<sub>DD</sub>=20V

**Table 4: Thermal Data**

|                |  |      |      |
|----------------|--|------|------|
| Rthj-case      | Thermal Resistance Junction-case Max           | 1.36 | °C/W |
| Rthj-amb       | Thermal Resistance Junction-ambient Max        | 62.5 | °C/W |
| T <sub>I</sub> | Maximum Lead Temperature For Soldering Purpose | 275  | °C   |

**ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> =25°C UNLESS OTHERWISE SPECIFIED)**
**Table 5: On /Off**

| Symbol               | Parameter   | Test Conditions   | Min. | Typ.           | Max.           | Unit     |
|----------------------|---|---|------|----------------|----------------|----------|
| V <sub>(BR)DSS</sub> | Drain-source Breakdown Voltage                        | I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0  | 55   |                |                | V        |
| I <sub>DSS</sub>     | Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0) | V <sub>DS</sub> = Max Rating<br>V <sub>DS</sub> = Max Rating,<br>T <sub>C</sub> = 125°C       |      |                | 1<br>10        | μA<br>μA |
| I <sub>GSS</sub>     | Gate-body Leakage Current (V <sub>DS</sub> = 0)       | V <sub>GS</sub> = ± 15 V  |      |                | ±100           | nA       |
| V <sub>GS(th)</sub>  | Gate Threshold Voltage                                | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA                                    | 1    |                | 2              | V        |
| R <sub>DS(on)</sub>  | Static Drain-source On Resistance                     | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A<br>V <sub>GS</sub> = 5 V, I <sub>D</sub> = 30 A |      | 0.012<br>0.014 | 0.015<br>0.017 | Ω<br>Ω   |

**Table 6: Dynamic**

| Symbol              | Parameter                    | Test Conditions                                      | Min. | Typ. | Max. | Unit |
|---------------------|------------------------------|--|------|------|------|------|
| g <sub>fs</sub> (1) | Forward Transconductance     | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 30 A        |      | 35   |      | S    |
| C <sub>iss</sub>    | Input Capacitance            | V <sub>DS</sub> = 25V, f= 1 MHz, V <sub>GS</sub> = 0 |      | 1950 |      | pF   |
| C <sub>oss</sub>    | Output Capacitance           |  |      | 390  |      | pF   |
| C <sub>rss</sub>    | Reverse Transfer Capacitance |  |      | 130  |      | pF   |

## ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Switching On

| Symbol      | Parameter          | Test Conditions   | Min. | Typ. | Max. | Unit |
|-------------|--------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD} = 25\text{ V}$ , $I_D = 30\text{ A}$                                |      | 30   |      | ns   |
| $t_r$       | Rise Time          | $R_G = 4.7\Omega$ , $V_{GS} = 4.5\text{ V}$<br>(see test circuit, Figure 3) |      | 180  |      | ns   |
| $Q_g$       | Total Gate Charge  | $V_{DD} = 40\text{ V}$ , $I_D = 60\text{ A}$ ,                              |      | 40   |      | nC   |
| $Q_{gs}$    | Gate-Source Charge | $V_{GS} = 5\text{ V}$   |      | 10   |      | nC   |
| $Q_{gd}$    | Gate-Drain Charge  |   |      | 20   |      | nC   |

Table 8: Switching

| Symbol       | Parameter           | Test Conditions   | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(off)}$ | Turn-off-Delay Time | $V_{DD} = 25\text{ V}$ , $I_D = 30\text{ A}$ ,                              |      | 80   |      | ns   |
| $t_f$        | Fall Time           | $R_G = 4.7\Omega$ , $V_{GS} = 4.5\text{ V}$<br>(see test circuit, Figure 3) |      | 35   |      | ns   |

Table 9: Source Drain Diode

| Symbol        | Parameter                     | Test Conditions  | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------|--|------|------|------|------|
| $I_{SD}$      | Source-drain Current          |  |      |      | 60   | A    |
| $I_{SDM}$ (2) | Source-drain Current (pulsed) |  |      |      | 240  | A    |
| $V_{SD}$ (1)  | Forward On Voltage            | $I_{SD} = 60\text{ A}$ , $V_{GS} = 0$                                  |      |      | 1.3  | V    |
| $t_{rr}$      | Reverse Recovery Time         | $I_{SD} = 40\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}$ |      | 65   |      | ns   |
| $Q_{rr}$      | Reverse Recovery Charge       | $= 25\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$                    |      | 130  |      | nC   |
| $I_{RRM}$     | Reverse Recovery Current      | (see test circuit, Figure 5)   |      | 4    |      | A    |

(1) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

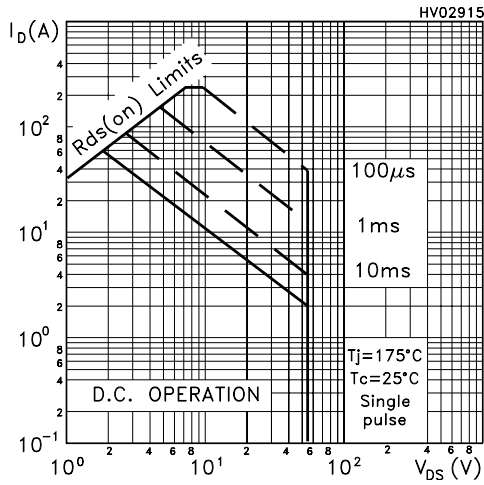


Figure 4: Output Characteristics

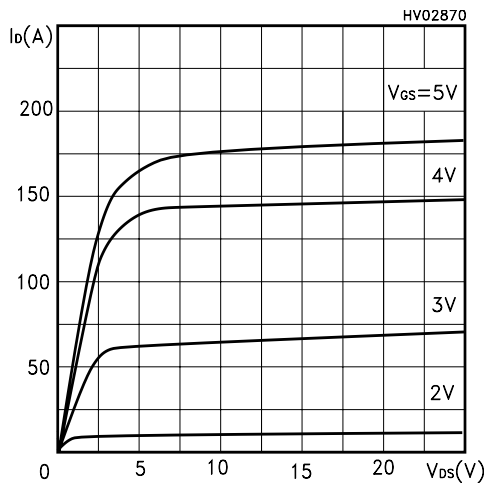


Figure 5: Transconductance

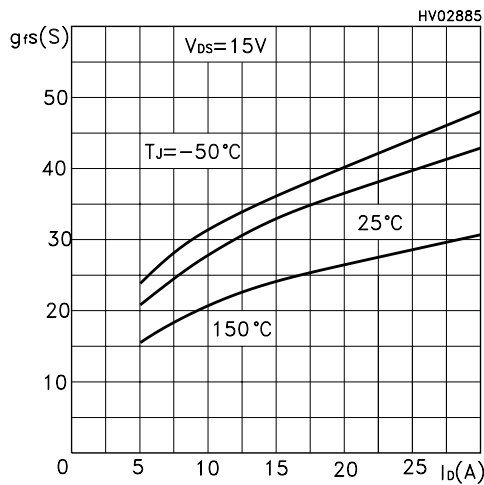


Figure 6: Thermal Impedance

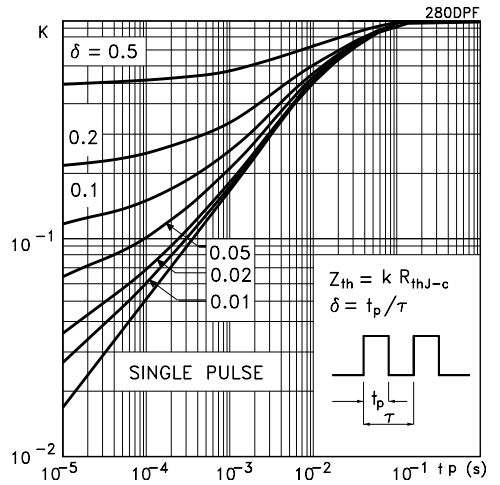


Figure 7: Transfer Characteristics

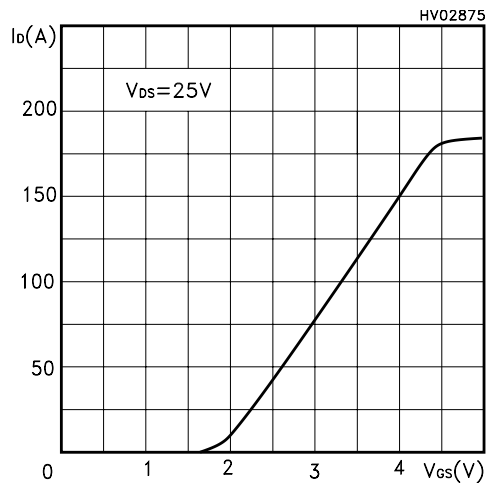


Figure 8: Static Drain-source On Resistance

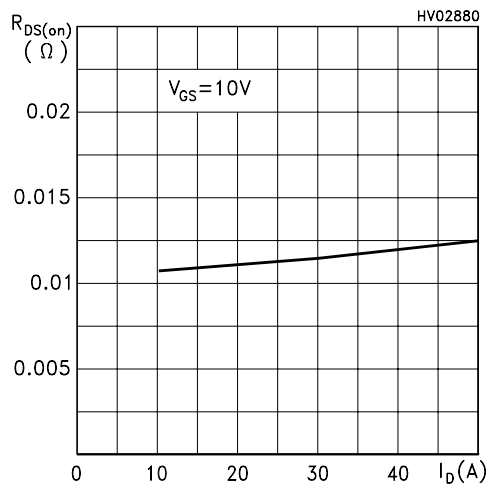


Figure 9: Gate Charge vs Gate-source Voltage

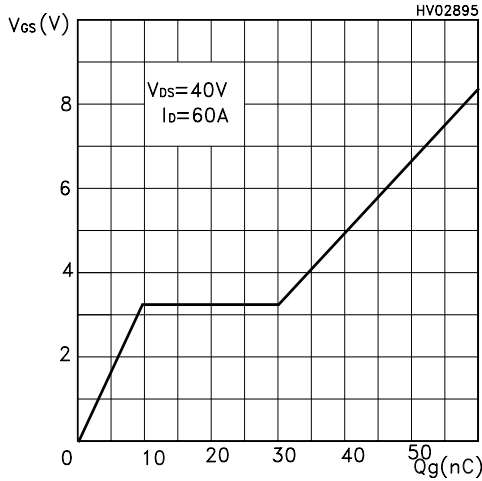


Figure 10: Normalized Gate Threshold Voltage vs Temperature

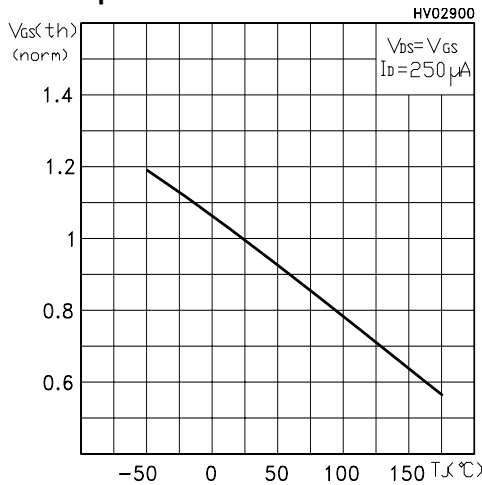


Figure 11: Normalized On Resistance vs Temperature

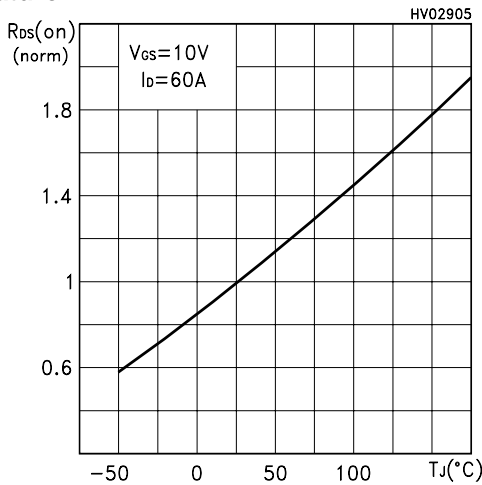


Figure 12: Capacitance Variation

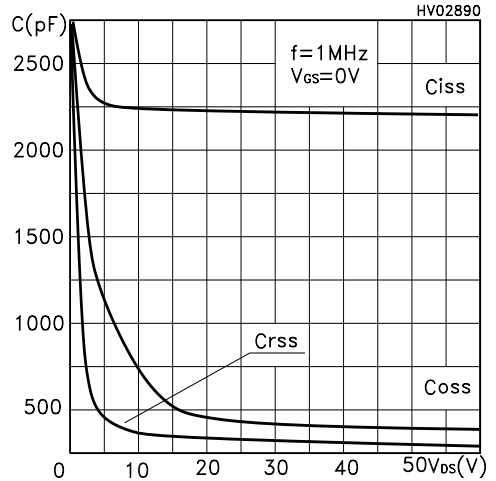


Figure 13: Source-Drain Diode Forward Characteristics

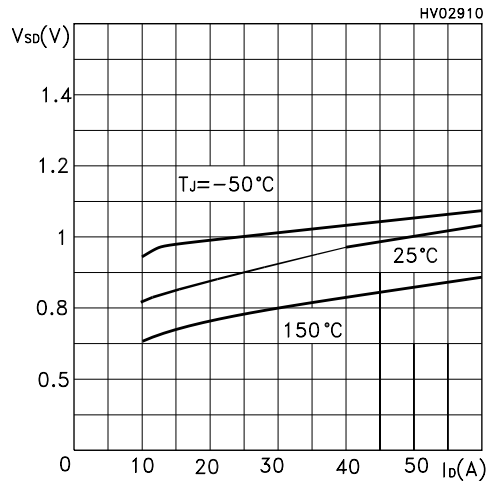
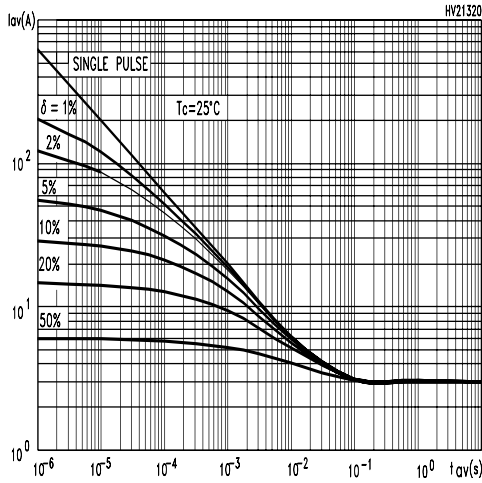


Figure 14: Allowable  $I_{AV}$  vs Time in Avalanche



The previous curve gives the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$$P_{D(AVE)} = 0.5 * (1.3 * BV_{DSS} * I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$$

Where:

$I_{AV}$  is the Allowable Current in Avalanche

$P_{D(AVE)}$  is the Average Power Dissipation in Avalanche (Single Pulse)

$t_{AV}$  is the Time in Avalanche

To derate above 25 °C, at fixed  $I_{AV}$ , the following equation must be applied:

$$I_{AV} = 2 * (T_{jmax} - T_{CASE}) / (1.3 * BV_{DSS} * Z_{th})$$

Where:

$Z_{th} = K * R_{th}$  is the value coming from Normalized Thermal Response at fixed pulse width equal to  $T_{AV}$ .

Figure 15: Switching Times Test Circuit For Resistive Load

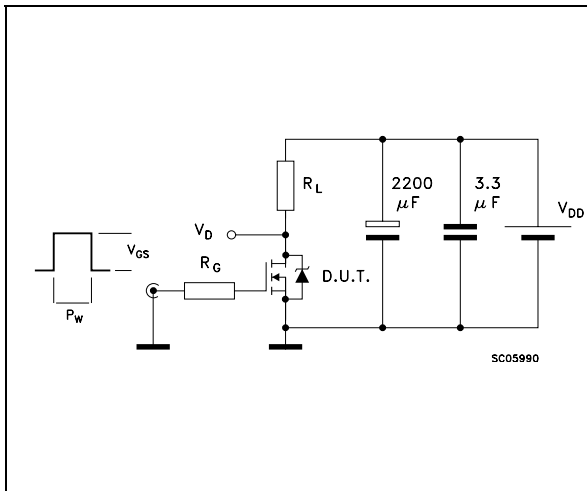


Figure 16: Test Circuit For Diode Recovery Times

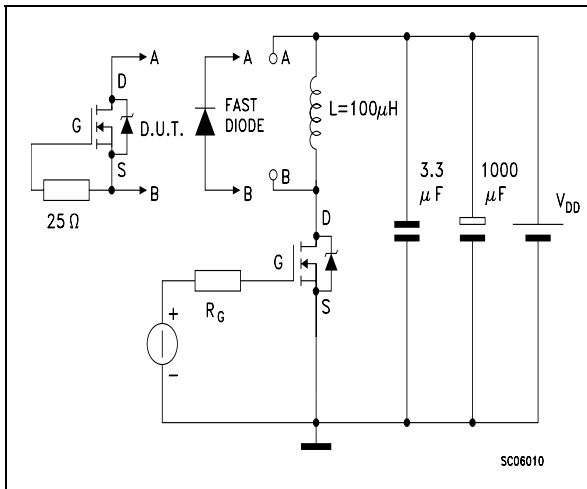
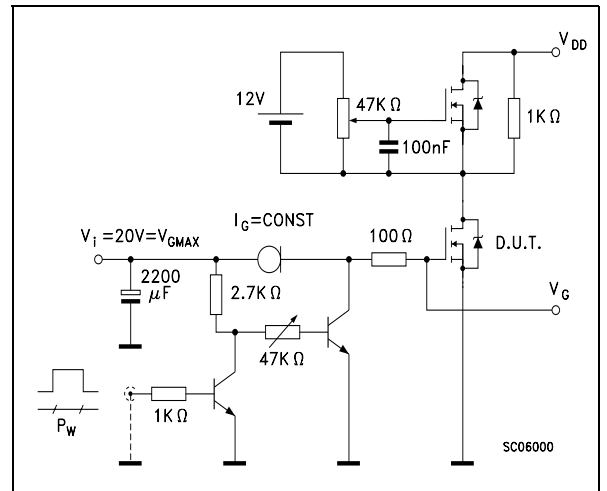
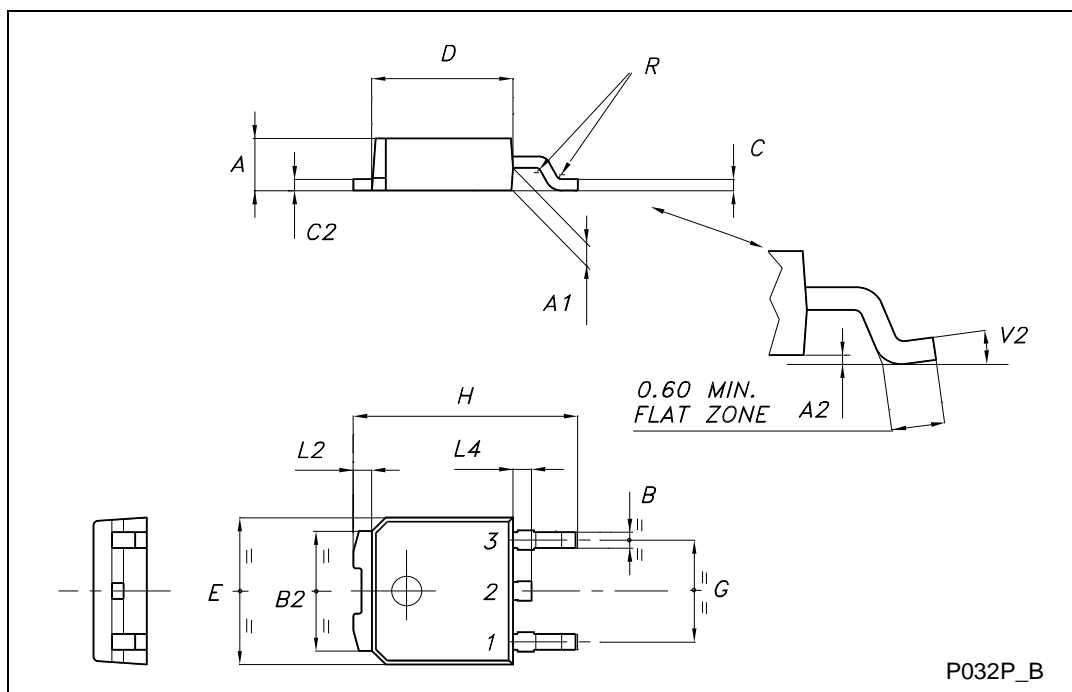


Figure 17: Gate Charge Test Circuit



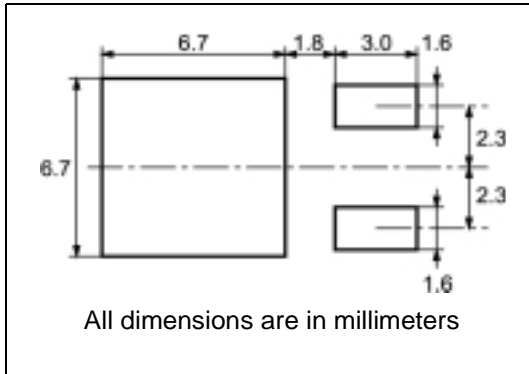
TO-252 (DPAK) MECHANICAL DATA

| DIM. | mm   |      |       | inch  |       |       |
|------|------|------|-------|-------|-------|-------|
|      | MIN. | TYP. | MAX.  | MIN.  | TYP.  | MAX.  |
| A    | 2.20 |      | 2.40  | 0.087 |       | 0.094 |
| A1   | 0.90 |      | 1.10  | 0.035 |       | 0.043 |
| A2   | 0.03 |      | 0.23  | 0.001 |       | 0.009 |
| B    | 0.64 |      | 0.90  | 0.025 |       | 0.035 |
| B2   | 5.20 |      | 5.40  | 0.204 |       | 0.213 |
| C    | 0.45 |      | 0.60  | 0.018 |       | 0.024 |
| C2   | 0.48 |      | 0.60  | 0.019 |       | 0.024 |
| D    | 6.00 |      | 6.20  | 0.236 |       | 0.244 |
| E    | 6.40 |      | 6.60  | 0.252 |       | 0.260 |
| G    | 4.40 |      | 4.60  | 0.173 |       | 0.181 |
| H    | 9.35 |      | 10.10 | 0.368 |       | 0.398 |
| L2   |      | 0.8  |       |       | 0.031 |       |
| L4   | 0.60 |      | 1.00  | 0.024 |       | 0.039 |
| V2   | 0°   |      | 8°    | 0°    |       | 0°    |

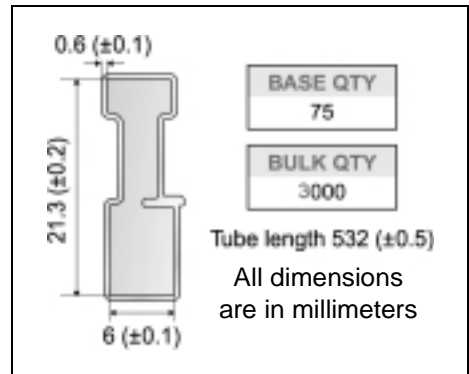




**DPAK FOOTPRINT**



**TUBE SHIPMENT (no suffix)\***



**TAPE AND REEL SHIPMENT (suffix "T4")\***

Diagram showing the tape mechanical data. It includes a top view of the tape with dimensions A, B, C, D, and a side view with dimensions T, N, and G. A 40 mm min. access hole is shown at the slot location. The tape slot in the core has a 25 mm min. width. The full radius is also indicated.

**REEL MECHANICAL DATA**

| DIM. | mm   |      | inch  |        |
|------|------|------|-------|--------|
|      | MIN. | MAX. | MIN.  | MAX.   |
| A    |      | 330  |       | 12.992 |
| B    | 1.5  |      | 0.059 |        |
| C    | 12.8 | 13.2 | 0.504 | 0.520  |
| D    | 20.2 |      | 0.795 |        |
| G    | 16.4 | 18.4 | 0.645 | 0.724  |
| N    | 50   |      | 1.968 |        |
| T    |      | 22.4 |       | 0.881  |

**TAPE MECHANICAL DATA**

| DIM. | mm   |      | inch  |       |
|------|------|------|-------|-------|
|      | MIN. | MAX. | MIN.  | MAX.  |
| A0   | 6.8  | 7    | 0.267 | 0.275 |
| B0   | 10.4 | 10.6 | 0.409 | 0.417 |
| B1   |      | 12.1 |       | 0.476 |
| D    | 1.5  | 1.6  | 0.059 | 0.063 |
| D1   | 1.5  |      | 0.059 |       |
| E    | 1.65 | 1.85 | 0.065 | 0.073 |
| F    | 7.4  | 7.6  | 0.291 | 0.299 |
| K0   | 2.55 | 2.75 | 0.100 | 0.108 |
| P0   | 3.9  | 4.1  | 0.153 | 0.161 |
| P1   | 7.9  | 8.1  | 0.311 | 0.319 |
| P2   | 1.9  | 2.1  | 0.075 | 0.082 |
| R    | 40   |      | 1.574 |       |
| W    | 15.7 | 16.3 | 0.618 | 0.641 |

**BASE QTY** 2500      **BULK QTY** 2500

Diagram showing the tape and reel shipment. It includes a top view of the tape with dimensions K0, D, P2, P0, E, F, W, B1, B0, D1, A0, P1, and a side view showing the bending radius R min. The top cover tape is also shown. The user direction of feed and feed direction are indicated. A note states: "10 pitches cumulative tolerance on tape +/- 0.2 mm".

\* on sales type

**Table 10: Revision History**

| <b>Date</b> | <b>Revision</b> | <b>Description of Changes</b> |
|-------------|-----------------|-------------------------------|
| 15-Feb-2005 | 1               | First Release.                |

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

All other names are the property of their respective owners

© 2005 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America