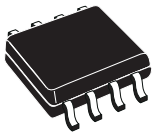
STS15N4LL

N-channel 40V - 0.0042Ω - 15A - SO-8
STripFET™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STS15N4LL	40V	<0.005Ω	15A

- Optimal $R_{DS(on)}$x Q_g trade-off @ 4.5V
- Conduction losses reduced
- Switching losses reduced

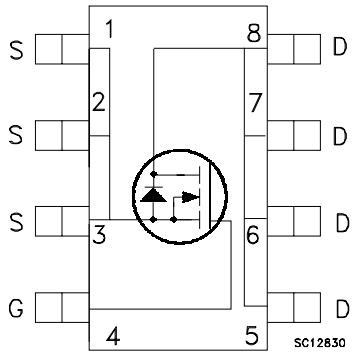


SO-8

Description

This N-channel enhancement mode Power MOSFET is the latest refinement of STMicroelectronic unique “Single Feature Size™“ strip-based process with less critical aligment steps and therefore a remarkable manufacturing reproducibility. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STS15N4LL	15N4LL-	SO-8	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximim ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	40	V
V_{GS}	Gate-source voltage	± 16	V
V_{GS} (1)	Gate- source voltage	±18	V
I_D	Drain current (continuous) at T_C = 25°C	15	A
I_D	Drain current (continuous) at T_C = 100°C	9.3	A
I_{DM} (2)	Drain current (pulsed)	60	A
P_{TOT}	Total dissipation at T_C = 25°C	2.7	W
E_{AS} (3)	Single pulse avalanche energy	2	J

1. Guaranteed for test time ≤ 15ms
2. Pulse width limited by Tjmax
3. Starting T_j =25°C, I_D =7.5A, V_{DD} =25V

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
R_{thj}-pcb(1)	Thermal resistance junction-PCB Max	47	°C/W
T_l	Maximum lead temperature for soldering	-55 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

1. When mounted of FR-4 board with 1 $inch^2$ pad, 2oz of Cu and t< 10sec

2 Electrical characteristics

(T_J = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS}= 0	40			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating, V_{DS} =max rating @125°C			10 100	µA µA
I_{GSS}	Gate body leakage Current (V_{DS} = 0)	V_{GS} = ±16V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static drain-source On resistance	V_{GS}= 10V, I_D= 7.5A V_{GS}= 4.5V, I_D= 7.5A		0.0042 0.005	0.005 0.007	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer Capacitance	V_{DS} = 25V, f=1 MHz, V_{GS}= 0		2530 574 29		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 20V, I_D = 15A V_{GS} = 4.5V *(see Figure 13)*		21.5 6.9 8.2	28	nC nC nC
R_G	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20mV open drain	1	3	5	Ω

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 20V, I_D = 7.5A, R_G = 4.7Ω, V_{GS} = 10V *(see Figure 12)*		17 25		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD} = 20V, I_D = 7.5A, R_G = 4.7Ω, V_{GS} = 10V *(see Figure 12)*		62 9		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				15 60	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 15A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 15A, V_{DD} = 30V, di/dt = 100A/µs, Tj = 150°C *(see Figure 17)*		43 64 3		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

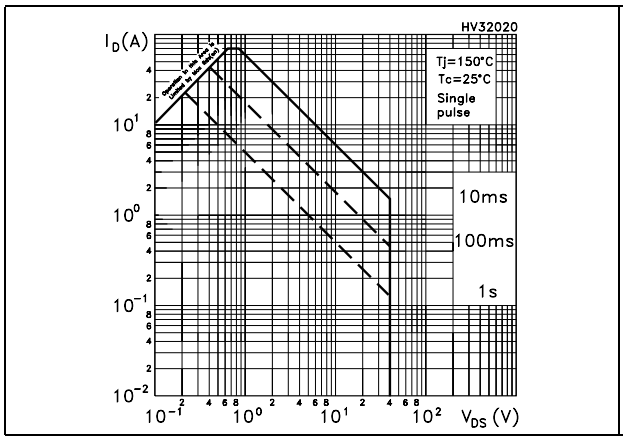


Figure 2. Thermal impedance

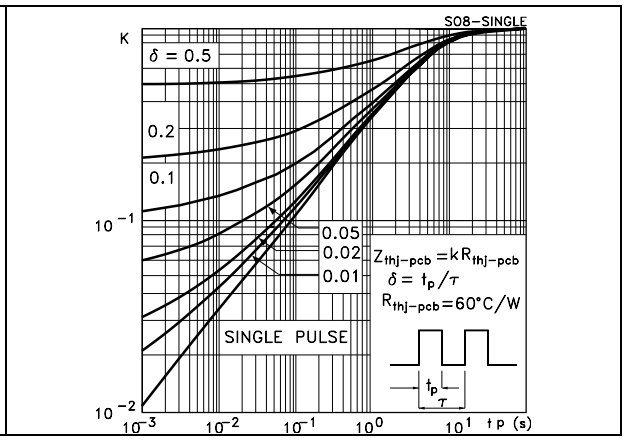


Figure 3. Output characterisics

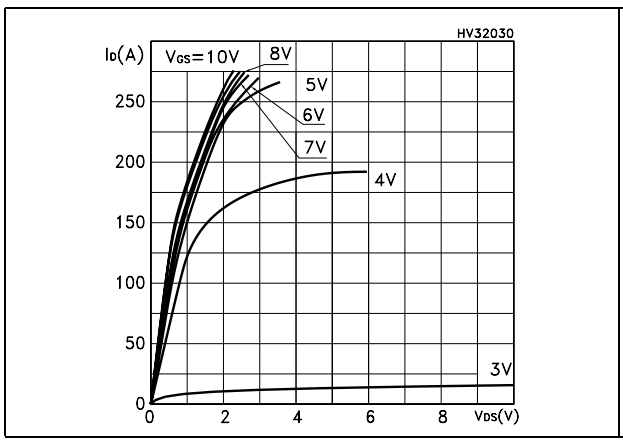


Figure 4. Transfer characteristics

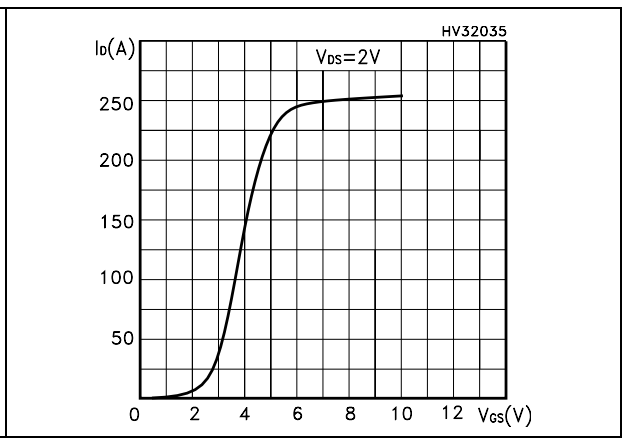


Figure 5. Normalized B_{VDSS} vs temperature

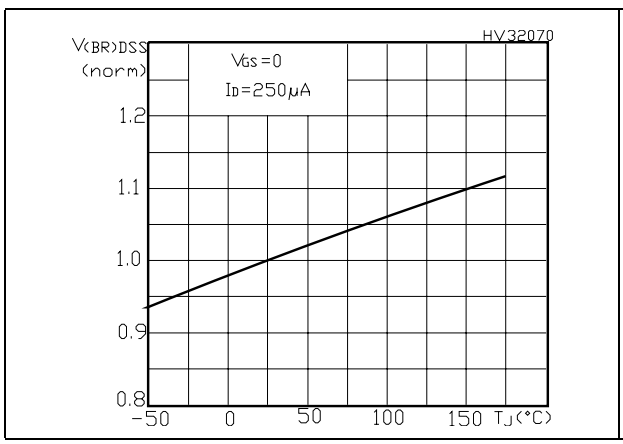


Figure 6. Static drain-source on resistance

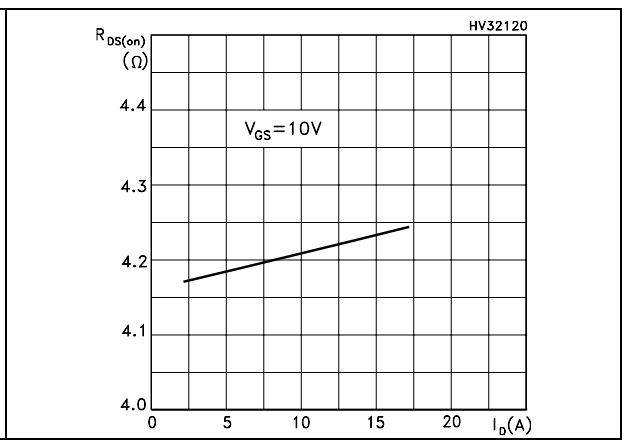


Figure 7. Gate charge vs gate-source voltage

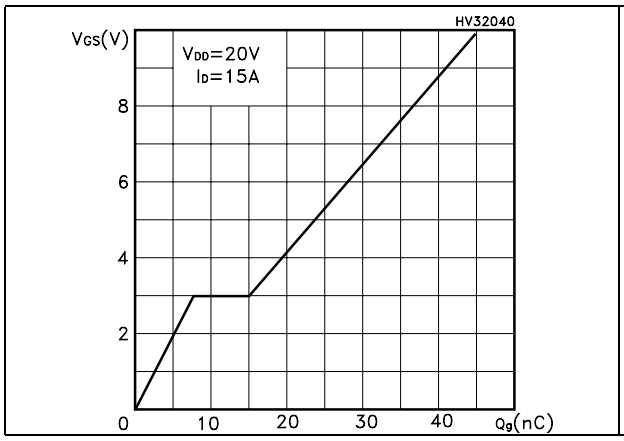


Figure 8. Capacitance variations

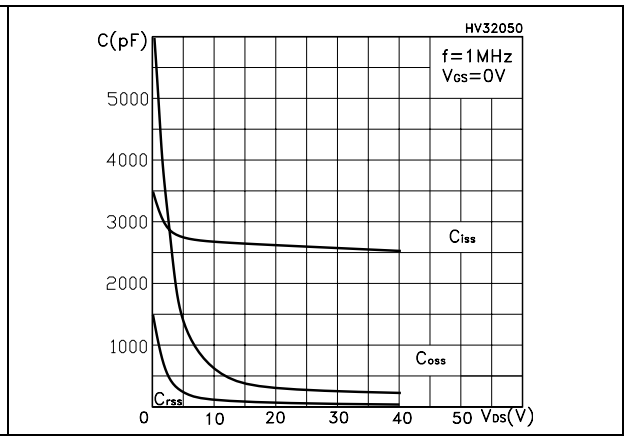


Figure 9. Normalized gate threshold voltage vs temperature

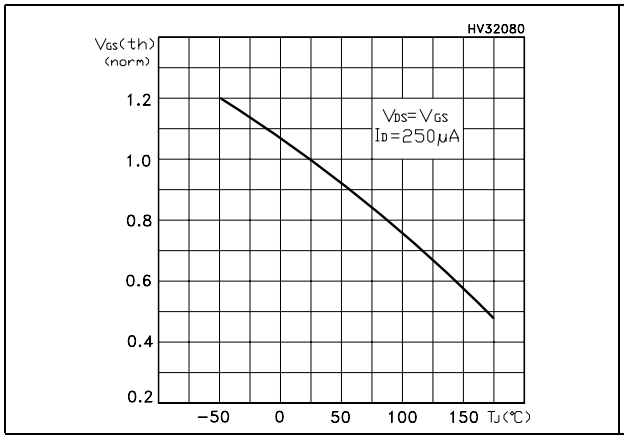


Figure 10. Normalized on resistance vs temperature

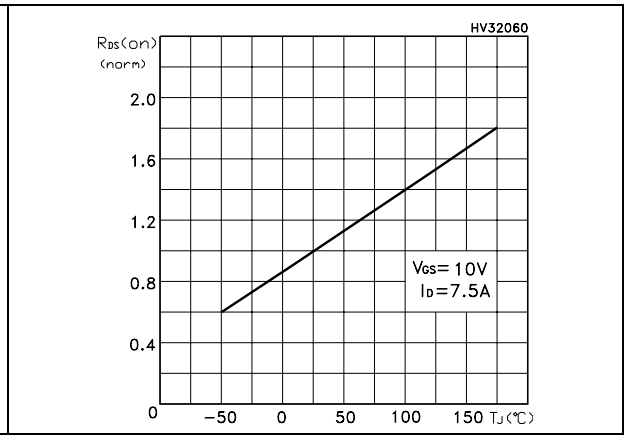
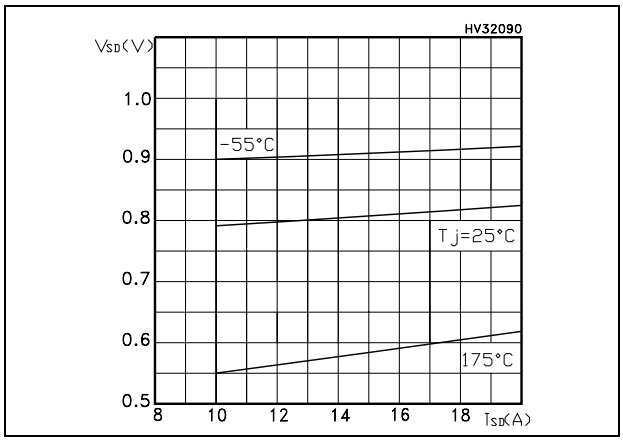


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

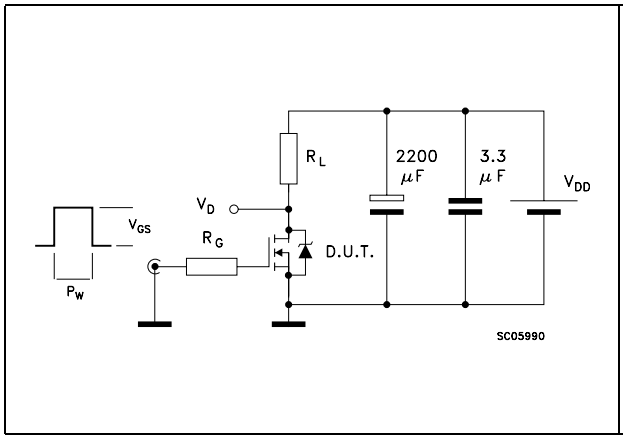


Figure 13. Gate charge test circuit

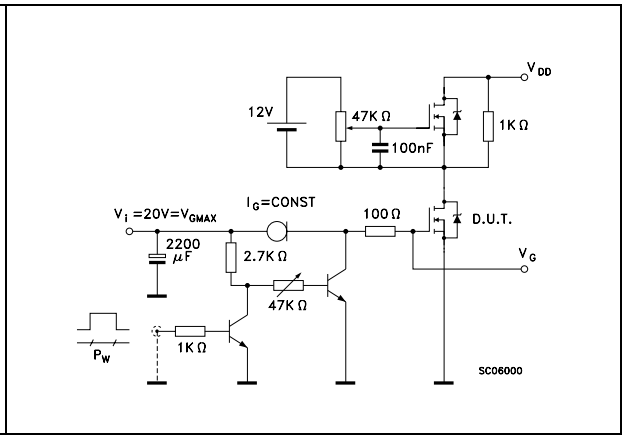


Figure 14. Test circuit for inductive load switching and diode recovery times

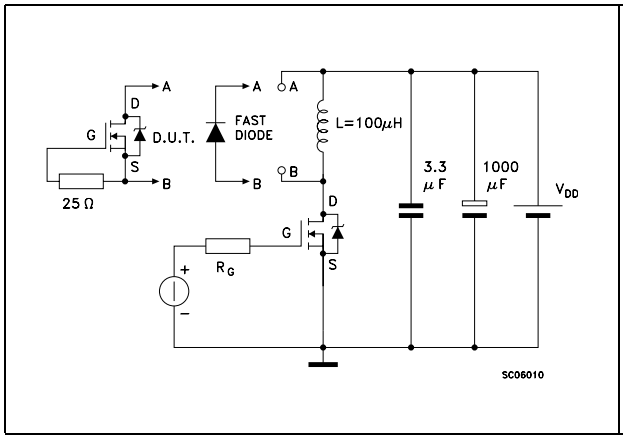


Figure 15. Unclamped Inductive load test circuit

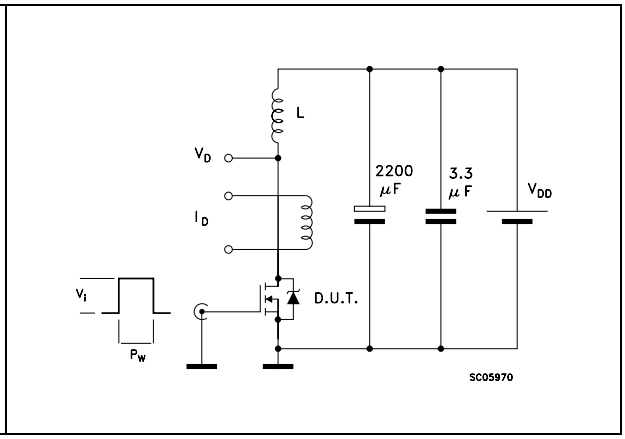


Figure 16. Unclamped inductive waveform

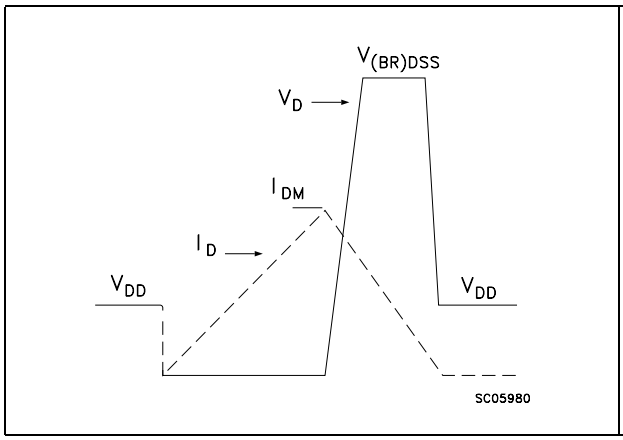
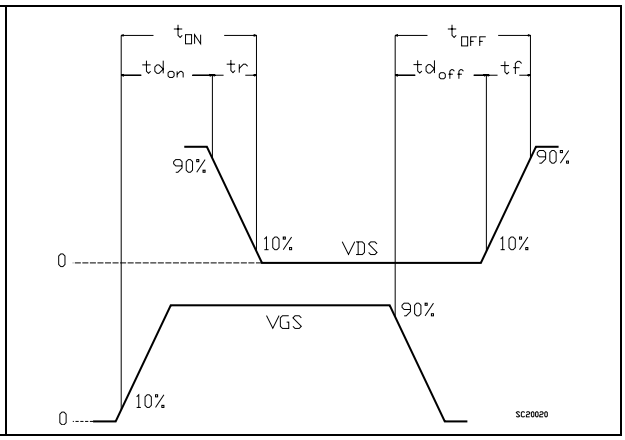


Figure 17. Switching time waveform

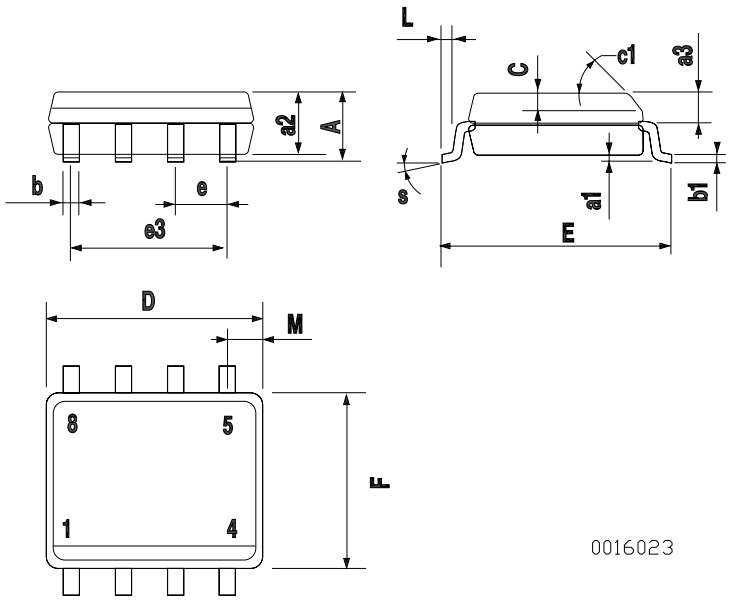


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at*www.st.com*

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 7. Revision history

Date	Revision	Changes
06-Jun-2006	1	First release

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