CMOS 4-BIT MICROCONTROLLER

TMP47C457N, TMP47C857N
TMP47C457F, TMP47C857F

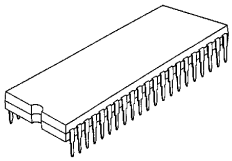
The 47C457/857 are a high-performance, 4-bit single-chip microcomputer based on the TLCS-470A CMOS series. The 47C457/857 have a build-in large-capacity RAM for repertory dial and a DTMF generator, making it ideal for application in telephones.

PART No.	ROM	RAM	PACKAGE	OTP version
TMP47C457N	4096 × 8-bit	768 × 4-bit	SDIP42-P-600-1.78	TMP47P857VN
TMP47C457F			QFP44-P-1414-0.80D	TMP47P857VF
TMP47C857N	8192 × 8-bit	1024 × 4-bit	SDIP42-P-600-1.78	TMP47P857VN
TMP47C857F			QFP44-P-1414-0.80D	TMP47P857VF

FEATURES

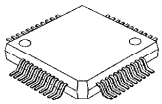
- ◆4-bit single-chip microcomputer
- ◆Instruction execution time : 2.08 μs (at 3.84MHz)
  244 μs (at 32.8kHz)
- ◆Low voltage operation: 2.7V min.
- ◆105 basic instructions
  Table look-up instructions
- ◆Sub-routine nesting: 15 levels max.
- ◆6 interruption sources (External : 2, Internal : 4)
  All sources have independent latches, and multiple interruption control is available
- ◆I/O port (35 pins)
  - Input 2 ports 5 pins
  - I/O 7 ports 27 pins
  - Output 1 ports 3 pins
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse-width measurement mode
- ◆Interval Timer
- ◆Watchdog Timer
- ◆Serial Interface with 8-bit buffer
  - Simultaneous transmission and reception
  - External/internal clock, leading/trailing edge shift mode, 4-bit/8-bit
- ◆DTMF (Dual-tone Multi frequency) output
  - DTMF output with one instruction
  - Single-tone output function

SDIP42-P-600-1.78



TMP47C457N
TMP47C857N
TMP47P857VN

QFP44-P-1414-0.80D



TMP47C457F
TMP47C857F
TMP47P857VF

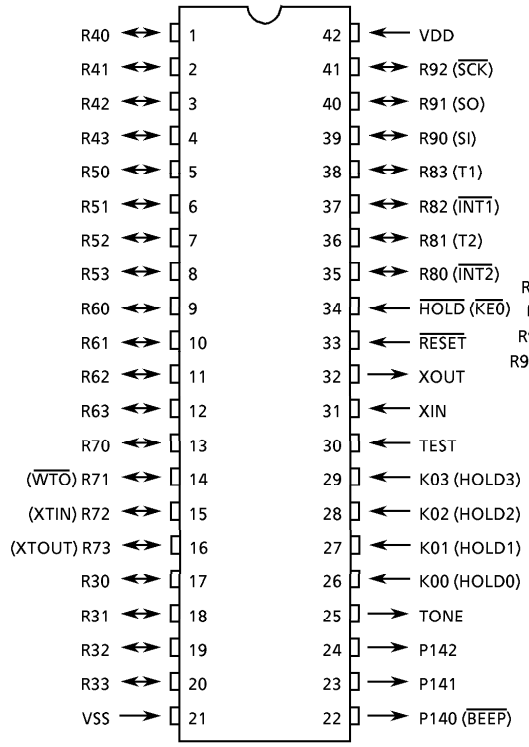
980901EBP1

◆BEEP output function
◆Warm start function
◆Dual clock operations
High-speed operation/low-electricity operation
◆Hold function
- Battery/Capacitor backup
- Hold function controlled by input port

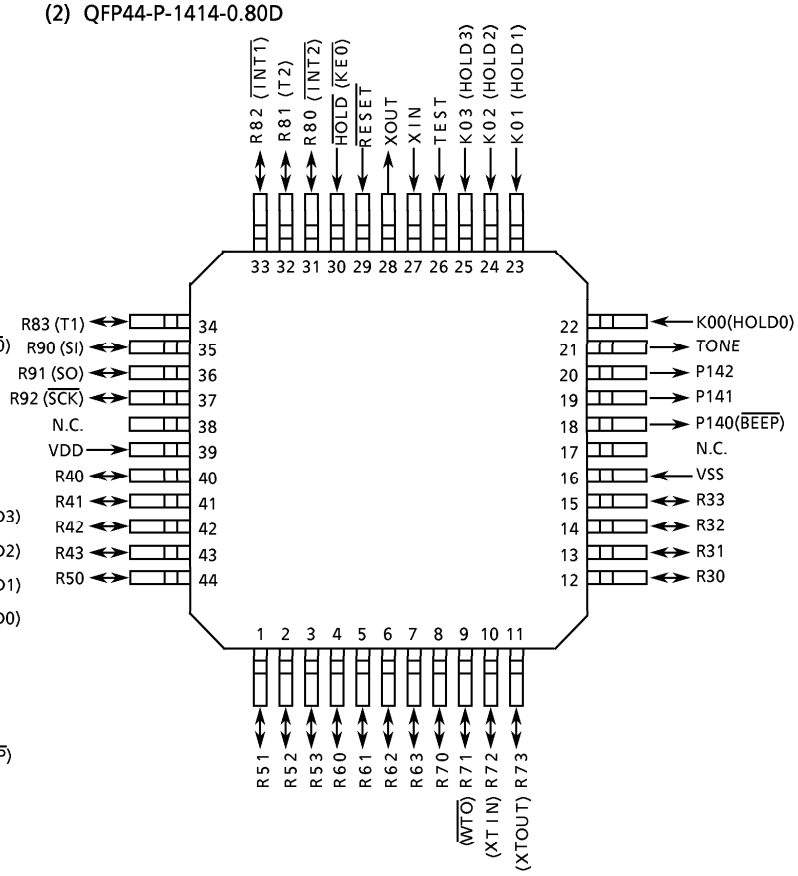
◆Real-time Emulator: BM47C857

PIN ASSIGNMENTS (TOP VIEW)

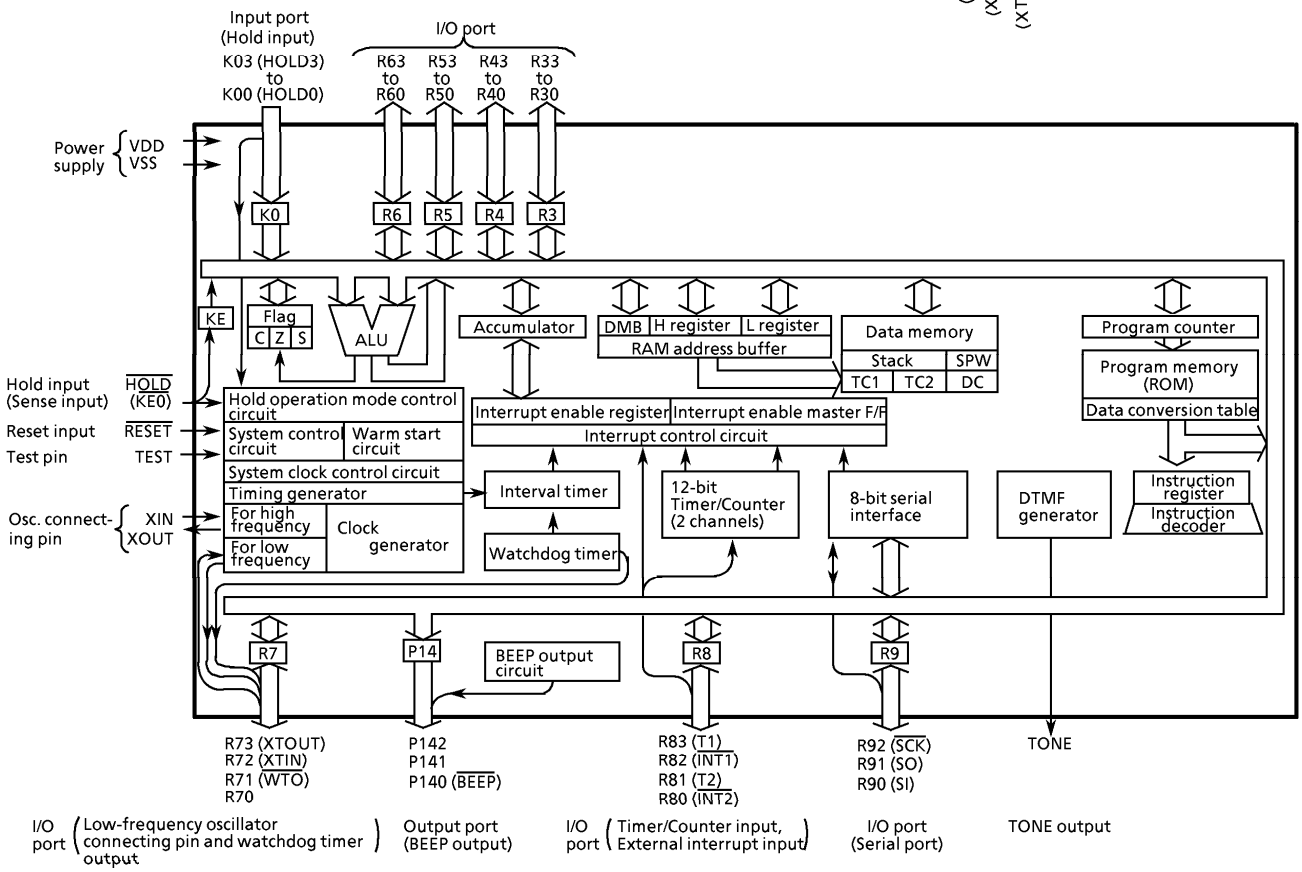
(1) SDIP42-P-600-1.78



(2) QFP44-P-1414-0.80D



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 (HOLD3) to K00 (HOLD0)	Input (input)	4-bit input port	Hold request/release signal input (Active "H")
R33 to R30	I/O	4-bit I/O port with latch. When used as the input port, the latch must be set to "1".	
R43 to R40			
R53 to R50			
R63 to R60			
R73 (XTOUT)	I/O (Output)	When R73 or R72 is used as the oscillator, it must be set to the dual clock mode. Setting, clearance and testing of 1-bit unit is possible by the bit processing instruction of the L-register indirect addressing.	Osc. connecting pin (Low-frequency). When of external clock input, input is made to XTIN and releases XTOUT.
R72 (XTIN)	I/O (Input)		
R71 ($\overline{WTO}$)	I/O (Output)		Watchdog timer output
R70	I/O		
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as the input port, external interrupt input pin or timer/countor input pin, the latch must be set to "1".	Timer/Countor 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (Input and Output)	3-bit I/O port with latch. When used as an input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
P142, P141	Output	3-bit output port with latch.	
P140 ($\overline{BEEP}$)	Output (Output)		BEEP output
TONE	Output	Tone output	
XIN	Input	Osc. connecting pin	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input	Hold request/release signal input	Sense input
TEST	Input	Test pin for outgoing test. Either opened, or fixed to low level.	
VDD	Power supply	+ 2.7V to 6.0V	
VSS		0 V (GND)	

OPERATIONAL DESCRIPTION

The configuration and function of hardware are described on the 47C457/857. Since the description emphasizes parts which differ from those on the 47C853 (TLCS-470A), make sure to also refer to the technical data for the 47C853.

1. SYSTEM CONFIGURATION

(1) Internal CPU function

With the exception of the program memory (ROM), data memory (RAM) all others are the same as those of the 47C853.

(2) Peripheral hardware function

① I/O port
② Interval timer
③ Timer/Counter
④ Watchdog timer
⑤ DTMF generator
⑥ BEEP output circuit
⑦ Warm start circuit
⑧ Serial interface

Following are descriptions of the internal CPU functions which have been added or modified to those from the 47C853, and of the peripheral hardware functions ⑤ and ⑥.

2. INTERNAL CPU FUNCTION

2.1 Program Memory (ROM)

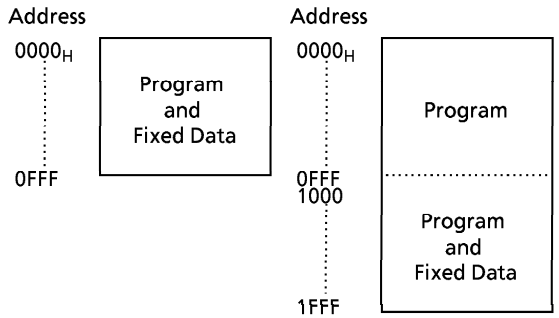
The 47C457 has a built-in program memory (mask ROM) of 4096 × 8-bit (0000 – $0FFF_H$ address), and the 47C857 has a built-in memory (mask ROM) of 8192 × 8-bit (0000 – $1FFF_H$ address).

The 5-8 bit data conversion table is placed in the last 32-byte space (0FE0 – $0FFF_H$ and 1FE0 – $1FFF_H$ addresses, respectively) of the program memory.

The fixed data which can be read out from the table look-up instructions are placed at the respective 0000 – $0FFF_H$ and 1000 – $1FFF_H$ addresses of the program memory, and address assignment is made possible by the 12-bit length data counter.

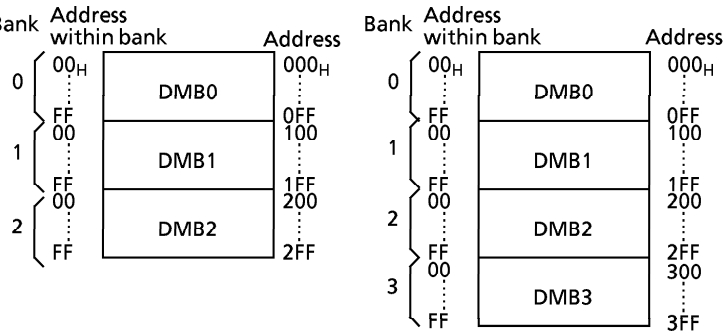
2.2 Data Memory (RAM)

The 47C457 data memory (RAM) has a total of 768 × 4-bit, which consists of three data memory banks (banks 0, 1, and 2) of 256 × 4-bit (00 – FF_H address). The 47C857 data memory (RAM) has a total of 1024 × 4-bit, which consists of four data memory banks (banks 0, 1, 2 and 3) of 256 × 4-bit (00 – FF_H address).



(a) 47C457 (b) 47C857

Figure 2-1. Program Memory



(a) 47C457 (b) 47C857

Figure 2-2. Data Memory (RAM)

3. PERIPHERAL HARDWARE FUNCTION

Table 3-1. shows the port address assignments and the I/O instructions for accessing the ports.

OPERATIONAL DESCRIPTION

The configuration and function of hardware are described on the 47C457/857. Since the description emphasizes parts which differ from those on the 47C853 (TLCS-470A), make sure to also refer to the technical data for the 47C853.

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③ Timer/Counter
④ Watchdog timer
⑤ DTMF generator
⑥ BEEP output circuit
⑦ Warm start circuit
⑧ Serial interface

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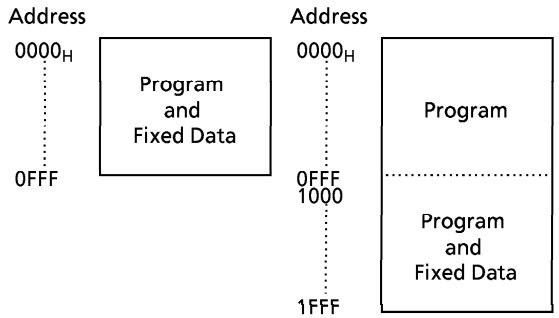
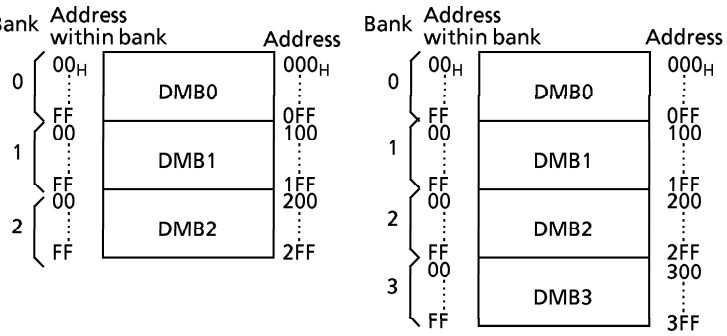


(a) 47C457 (b) 47C857

Figure 2-1. Program Memory



(a) 47C457 (b) 47C857

Figure 2-2. Data Memory (RAM)

3. PERIPHERAL HARDWARE FUNCTION

Table 3-1. shows the port address assignments and the I/O instructions for accessing the ports.

Port address (**)	Port: Input (IP**)	Port: Output (OP**)	Input/Output instruction: IN %p, A / IN %p, @HL	OUT A, %p / OUT@HL, %p	OUT #k, %p	OUTB @HL	SET %p, b / CLR %p, b	TEST %p, b / TESTP %p, b	SET @L / CLR @L / TEST @L
00_H	K0 Input port	——	○	–	–	–	–	○	–
01	ROW register	ROW register	○	○	○	○ (Note2)	○	○	–
02	COLUMN register	COLUMN register	○	○	○	○	○	○	–
03	R3 Input port	R3 Outut port	○	○	○	–	○	○	–
04	R4 〃	R4 〃	○	○	○	–	○	○	○
05	R5 〃	R5 〃	○	○	○	–	○	○	○
06	R6 〃	R6 〃	○	○	○	–	○	○	○
07	R7 〃	R7 〃	○	○	○	–	○	○	○
08	R8 〃	R8 〃	○	○	○	–	○	○	–
09	R9 〃	R9 〃	○	○	○	–	○	○	–
0A	——	——	–	–	–	–	–	–	–
0B	——	——	–	–	–	–	–	–	–
0C	——	——	–	–	–	–	–	–	–
0D	——	TONE command register	–	○	○	–	–	–	–
0E	Status input (Note3)	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial receive buffer	○	○	○	–	–	–	–
10_H	$\overline{HOLD}$ pin status	HOLD operation mode control	○	○	–	–	–	–	–
11	——	——	–	–	–	–	–	–	–
12	——	——	–	–	–	–	–	–	–
13	——	BEEP output control	–	○	–	–	–	–	–
14	——	P14 output port (BEEP output)	–	○ (Note5)	–	–	–	–	–
15	——	Watchdog timer control	–	–	–	–	–	–	–
16	——	System clock control	–	○	–	–	–	–	–
17	——	Command register (Note4)	–	○	–	–	–	–	–
18	——	——	–	–	–	–	–	–	–
19	——	Interval Timer interrupt conrol	–	○	–	–	–	–	–
1A	——	——	–	–	–	–	–	–	–
1B	——	——	–	–	–	–	–	–	–
1C	——	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	——	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	——	Serial interface 1 control	–	○	–	–	–	–	–
1F	——	Serial interface 2 control	–	○	–	–	–	–	–

Note 1. "____" means the reserved state. Unavailable for the user program.
Note 2. Automatic access to ROW and COLUMN registers by the [OUTB @HL] instruction.
Note 3. Serial interface, system clock control circuit status, and $\overline{HOLD}$ ($\overline{KE0}$) pin input.
Note 4. HOLD control input selection, warm start control and DTMF input clock selection
Note 5. To output data to P14 output port, use "MOV A, SPW13".

Table 3-1. Port Address Assignment and Available I/O Instructions

3.1 DTMF Generator

The 47C457/857 has a built-in DTMF generator which generates dialing signals for tone dialing-type telephones. There are two groups of tone dial signals, one group of 4 since wave low frequencies and another group of 4 sine wave high frequencies. All of these frequencies can be selected individually and combined with a frequency from the other group for a total of 16 different DTMF composite waves.

(DTMF : Dual-Tone Multi frequency)

3.1.1 Configuration of DTMF Generator

Figure 3-1 shows the configuration of the DTMF generator.

The 47C457/857 generates two-stepped, quasi-sine waves, and outputs tone dial signals by combining the quasi-sine waves.

The high and low groups of frequencies are selected by setting the frequency selection codes in the ROW and COLUMN registers.

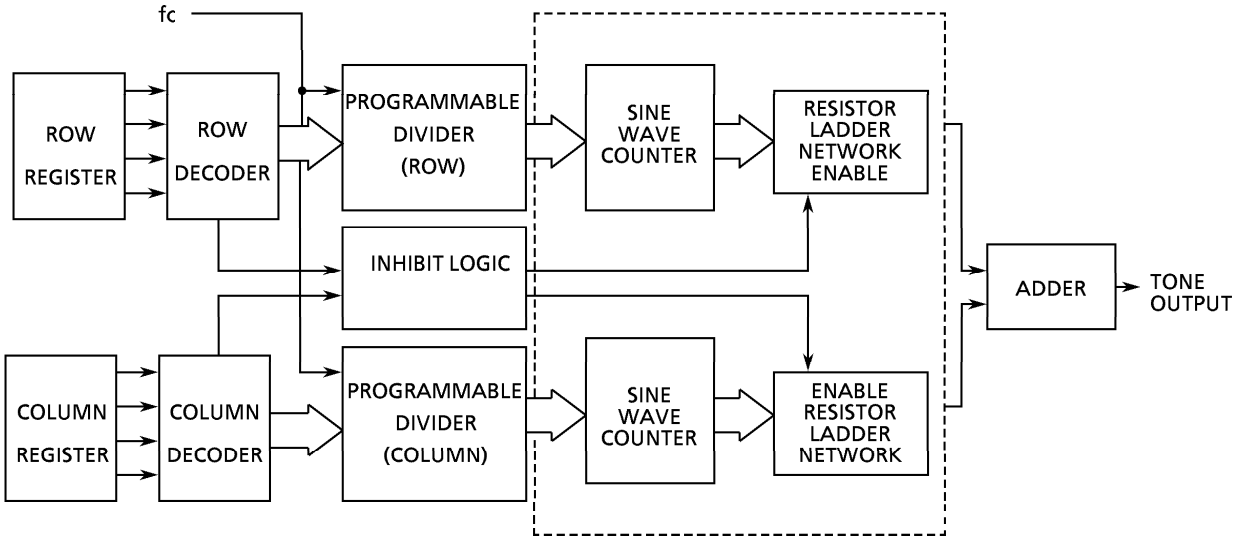


Figure 3-1. Configuration of DTMF Generator

3.1.2 Control of DTMF Generator

Selection of frequency in tone output is controlled by the ROW register (OP01/IP01) and COLUMN register (OP02/IP02). Enable/disable of single tone output is controlled by the TONE command resister (OP0D).

Note 1. **; don't care*
Note 2. *When reading STE bit, "1" is always read.*

TONE Command Register
(Port address : OP0D Initial value : 0***)

3	2	1	0
STE			

STE	Controls single tone output

0 : Disable mode of single tone output
1 : Enable mode of single tone output

Figure 3-2. TONE Command Register

ROW register
(Port address : OP01 / IP01 Initial value : 0000)

3	2	1	0

ROW tone frequency selection

0001 : Outputs 697.7Hz single tone
0010 : Outputs 769.2Hz single tone
0100 : Outputs 857.1Hz single tone
1000 : Outputs 937.5Hz single tone

COLUMN register
(Port address : OP02 / IP02 initial value : 0000)

3	2	1	0

COLUMN tone frequency selection

0001 : Outputs 1212.1Hz single tone
0010 : Outputs 1333.3Hz single tone
0100 : Outputs 1481.5Hz single tone
1000 : Outputs 1621.6Hz single tone

Figure 3-3. ROW, COLUMN Registers

Tones are outputted by entering the frequency selection codes shown in Figure 3-3. in to the ROW and COLUMN registers.
When either the ROW or COLUMN register is set with an ineffective code when the single-tone output is in the enable mode, the register's tone output enters the disable mode and only registers in which an effective code has been set will output a tone. When both registers are enabled, dual tones can be output. When the single-tone output is in the disable mode, dual tones are output only when effective codes are loaded into both the ROW and COLUMN registers. No tones are output in cases other than the preceding ones.
The [OUTB @HL] instruction can simultaneously set 8-bit data into both registers (the upper 4 bits of the ROM data in the COLUMN register, and the lower 4 bits in the ROW register).
The operation and data table for the [OUTB @HL] instructions are the same as those of the 5-8 bit conversion instructions.

Example 1 : Output of 1481.5Hz single tone (COLUMN)

```
OUT     #8, %OP0D     ; Sets the enable mode of single tone output.
OUT     #0, %OP01     ; Sets an ineffective code into ROW register.
OUT     #4, %OP02     ; Sets data "4" into COLUMN register.
```

Example 2 : 8-bit data corresponding to the 5 bits of data which link the contents of the carry flag and the data memory RAM address 90_H, are read from the ROM, and frequency selection codes are loaded into the ROW and COLUMN registers.

```
LD      HL, #90H      ; HL ← 90H (Sets the address of the data memory)
OUTB    @HL           ; Sets the ROM data into the ROW and COLUMN
                        registers.
```

Table 3.2 shows the deviation between the 47C457/857 tone output and standard frequencies. Table 3-3. shows the corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys.

ROW Tone (Low Group)						
Frequency selection code				Tone output frequency	Standard frequency	Deviation
3	2	1	0	[Hz]	[Hz]	[%]
0	0	0	1	697.7	697	+ 0.10
0	0	1	0	769.2	770	– 0.10
0	1	0	0	857.1	852	+ 0.60
1	0	0	0	937.5	941	– 0.37

COLUMN Tone (High Group)						
Frequency selection code				Tone output frequency	Standard frequency	Deviation
3	2	1	0	[Hz]	[Hz]	[%]
0	0	0	1	1212.1	1209	+ 0.26
0	0	1	0	1333.3	1336	– 0.20
0	1	0	0	1481.5	1477	+ 0.30
1	0	0	0	1621.6	1633	– 0.70

Table 3-2. Tone Output Frequencies and Deviation from Standard

		COLUMN register (OP02 / IP02)		
	Frequency selection code	0001 (1209)	0010 (1336)	0100 (1477)
ROW register (OP01 / IP01)	0001 (697)	1	2	3
	0010 (770)	4	5	6
	0100 (852)	7	8	9
	1000 (941)	*	0	#
		Standard telephone dial key		

Contents of ( ) are standard frequencies, unit: Hz

Table 3-3. Corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys

3.1.3 Test Mode for Tone Output

The 47C457/857 includes a testing mode for checking tone output waveforms. Tones are output by the relevant circuit shown in Figure 3-4. Since ROW data are input from port R6 and COLUMN data are input from R3 using the frequency selection codes shown in Figure 3-3., an optional single tone or dual tone can be output. Figure 3-5. shows a single-tone waveform and Figure 3-6. shows a dual-tone waveform.

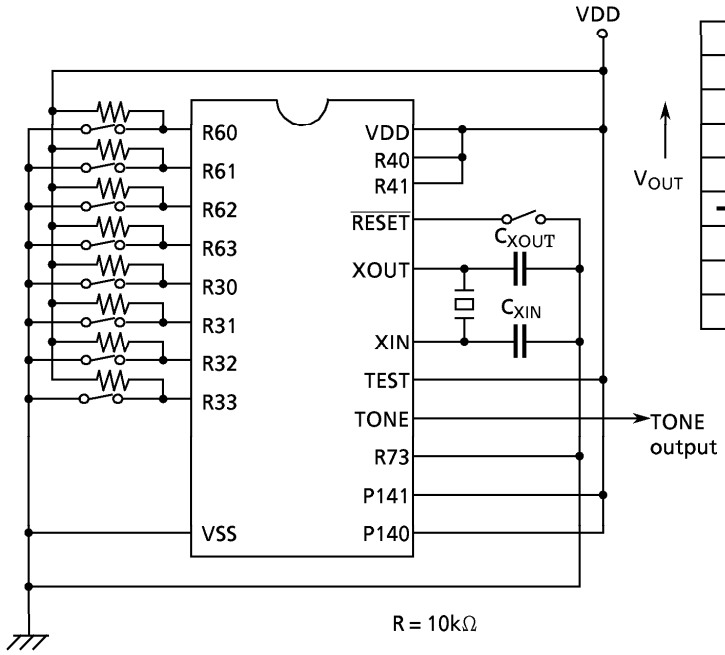


Figure 3-4. Tone Test Circuit

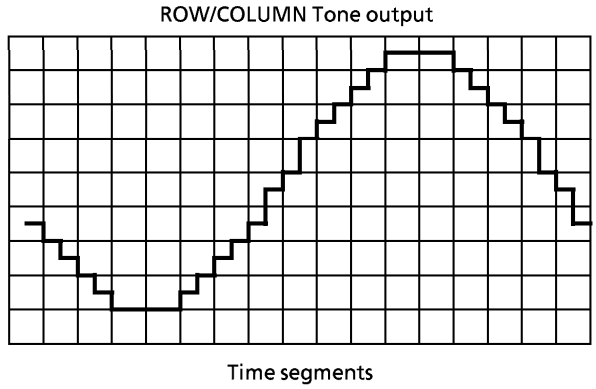


Figure 3-5. Single Tone Waveform

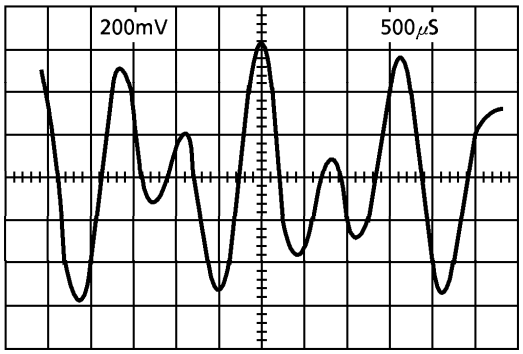


Figure 3-6. Dual Tone Waveform

3.2 BEEP Output Circuit

The BEEP Output circuit generates square waves in the audible frequency range. This circuit drives the key input confirmation tone regrator circuit for telephone applications. The BEEP output pin is shared by the P140 output. This pin controls both P140 and BEEP output.
Adjust the P140 output latch to "1" for BEEP output.

3.2.1 Configuration of BEEP Output Circuit

Figure 3-7. shows the configuration of the BEEP output circuit. The clock pulse of the BEEP output circuit is supplied from a timing generator, and the BEEP output is controlled by the frequency selection and output enable/disable setting.

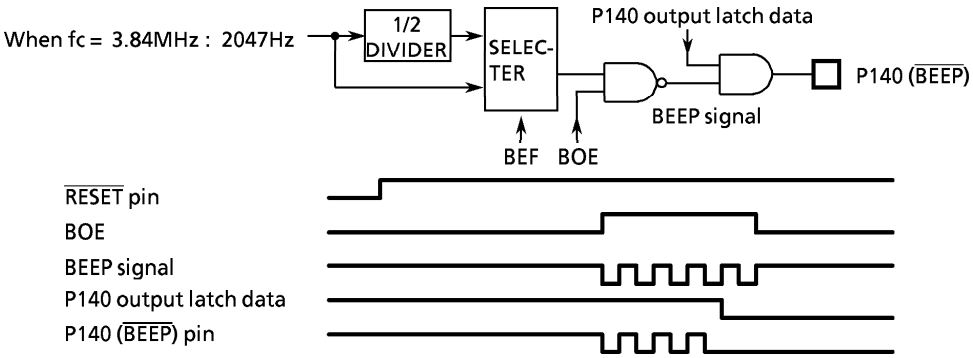


Figure 3-7. BEEP Output Circuit Configuration and Timing Chart

3.2.2 Control of BEEP Output Circuit

The BEEP output is controlled by the BEEP output control command register (OP13).

BEEP Output Control Command Register
(Port address : OP13 Initial Value : 0**0)

3	2	1	0
BOE			BEF

BOE	Control of BEEP output

0 : Disable output
1 : Enable output

BEF	Selection of BEEP output frequency

fc = 3.84MHz

	In the Normal mode	In the SLOW mode
0 :	2047 Hz	Disable output
1 :	1023 Hz	

Figure 3-8. BEEP Output Control Command Register

The BEEP output is disable in the SLOW mode.

3.3 Warm Start Function

The reset operation is executed by adjusting the warm start control command register (Bit 3 of OP17) to "0".

Warm Start Control Command Register
(Port address : OP17 Initial value : 1001)

3	2	1	0
WSC	(HCS)	0	1

WSC	Warm start control

0 : Enable warm start
1 : Disable warm start

Figure 3-9. Warm Start Control Command Register

By setting WSC to "0", "L" level signal is output to a reset terminal and reset options is executed.

Port Condition by RESET Operation

The transition of Port condition by RESET operation is shown as below.

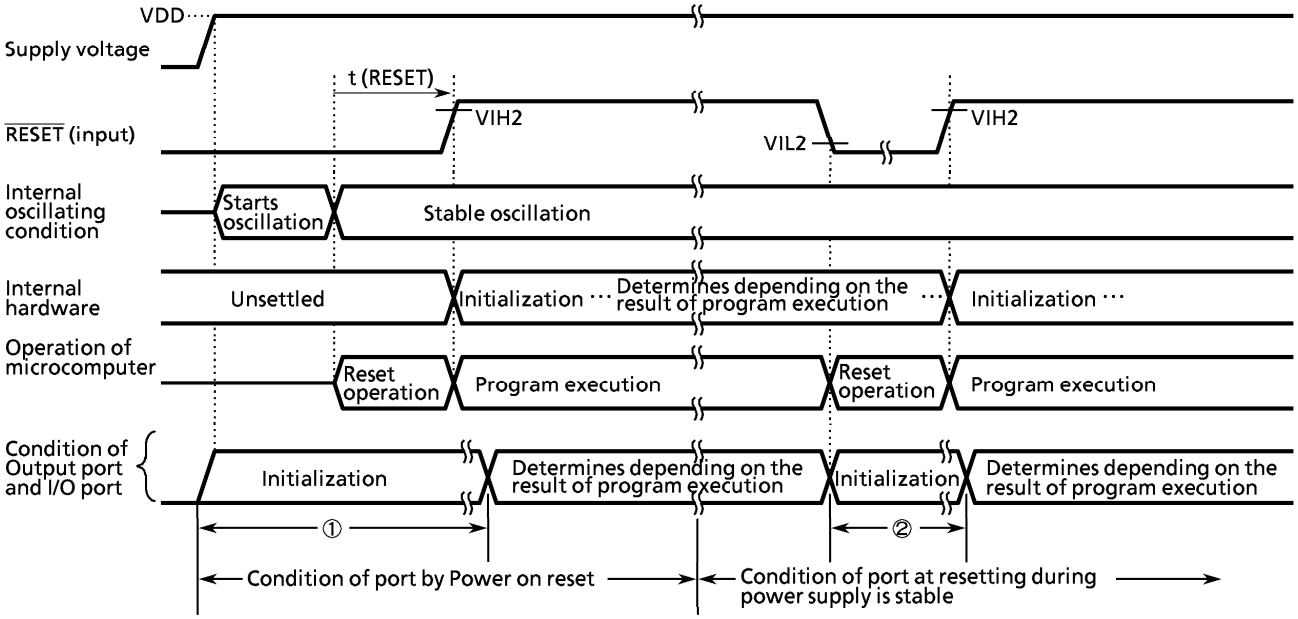


Figure 3-10. Port condition by Reset operation

Note 1: t (RESET) > 24/fc

Note 2: VIL2 : Stands for low level input voltage of $\overline{\text{RESET}}$ *pin.*
VIH2 : Stands for high level input voltage of $\overline{\text{RESET}}$ *pin.*

Note 3: The term from power on reset to the time program is executed (above ①) and also the term starting from reset operation during power supply is stable to the program is executed (above ②), the port is on the initial condition. The initial condition of Port differs from I/O circuit by each port, refer to the section of "INPUT/OUTPUT CIRCUITRY". Thus, when using Port as an output pin, in the term of the above ① and ②, the voltage level on the signal that connects with the output pin of Port to the input pin of external application circuit should be determined by the external circuitry such as pull-up resistor and / or pull-down resistor.

INPUT/OUTPUT CIRCUITRY

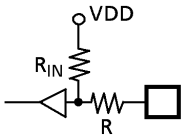
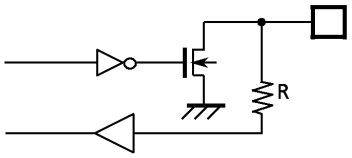
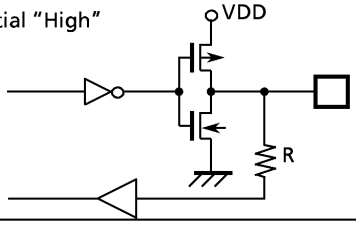
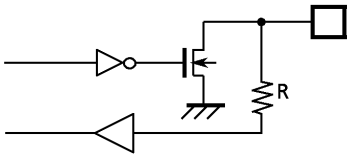
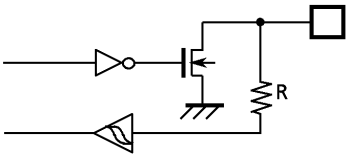
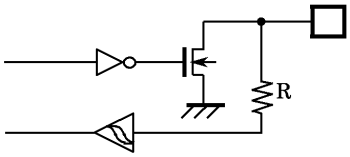
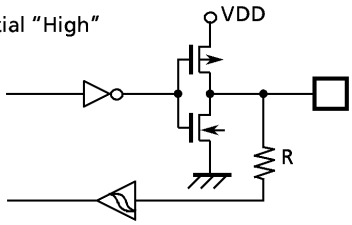
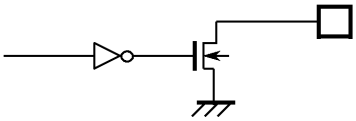
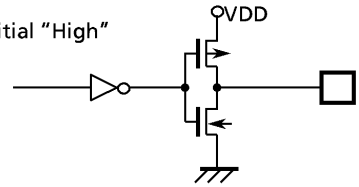
(1) Control pins

The input/output circuitries of the 47C457/857 control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output	OSC. enable R_f R R_O XIN XOUT	Resonator connecting pins R = 1kΩ (typ.) R_f = 1.5MΩ (typ.) R_O = 2kΩ (typ.)
XTIN XTOUT	Input Output	R_{fs} R R_O XTIN XTOUT	Resonator connecting pins (R = 1kΩ typ.) (R_{fs} = 6MΩ typ.) (R_O = 220kΩ typ.)
$\overline{\text{RESET}}$	Input	VDD R_{IN} R WSC (OP17 : bit2)	Hysteresis input Pull-up resistor R_{IN} = 220kΩ (typ.) R = 1kΩ (typ.)
$\overline{\text{HOLD}}$ ($\overline{\text{KE0}}$)	Input (Input)	R	Hysteresis input (Sense input) R = 1kΩ (typ.)
TEST	Input	R R_{IN}	Pull-down resistor R_{IN} = 70kΩ (typ.) R = 1kΩ (typ.)

(2) I/O Ports

The input/output circuitries of the 47C457/857 I/O ports are shown in the following chart, any of which can be chosen by a code (WB, WE, or WH) as a mask option.

Port	I/O	INPUT/OUTPUT CIRCUITRY and CODE		REMARKS
K0	Input			Pull-up resistor RIN = 70kΩ (typ.) R = 1kΩ (typ.)
R3 R4 R5 R6	I/O	WB Initial "Hi-Z" 	WE, WH Initial "High" 	Sink open drain or push-pull output R = 1kΩ (typ.)
R7	I/O	Initial "Hi-Z" 		Sink open drain output R = 1kΩ (typ.)
R8	I/O	Initial "Hi-Z" 		Sink open drein Hysteresis input R = 1kΩ (typ.)
R9	I/O	WB, WE Initial "Hi-Z" 	WH Initial "High" 	Sink open drain or push-pull output Hysteresis input R = 1kΩ (typ.)
P14	Output	WB Initial "Hi-Z" 	WE, WH Initial "High" 	Sink open drain or push-pull output

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin except R7	– 0.3 to 10	
Output Current (per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation [T_{opr} = 50℃]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	℃
Storage Temperature	T_{stg}		– 55 to 125	℃
Operating Temperature	T_{opr}		– 30 to 60	℃

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		Normal mode	2.7	6.0	V
			SLOW mode	2.7		
			HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency (High)	fc	XIN, XOUT		3.84		MHz
Clock Frequency (Low)	fs	XTIN, XTOUT		30.0	34.0	kHz

D.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V/0V	—	—	± 2	μA
	I_{IN2}	Ports R (open drain)					
Input Low Current	I_{IL}	Ports R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	—	—	– 2	mA
Input Resistance	R_{IN1}	Port K0		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LD}	Ports P, R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
Output High Voltage	V_{OH}	Ports R (push-pull)	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	—	—	V
Output Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5V, I_{OL} = 1.6mA	—	—	0.4	V
Supply Current (in the Nomal mode)	I_{DD}		Tone generating V_{DD} = 5.5V, fc = 3.84MHz	—	3	6	mA
	I_{DDT}		Tone generating V_{DD} = 5.5V, fc = 3.84MHz	—	5	10	
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0V, fs = 32.768kHz	—	30	60	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.
Note 2. Input Current I_{IN1} : The current through resistor is not included, when containing the pull-up/pull-down resistor.
Note 3. Supply Current : V_{IN} = 5.3V/0.2V
The K0 port is opened when containing the pull-up/pull-down resistor. The Voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

TONE OUTPUT CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Tone Output Voltage (ROW)	V_{TONE}	RL ≧ 10kΩ, V_{DD} = 2.2V	135	200	260	mVrms
Pre-Emphasis High Band (COL / ROW)	PEHB	PEHB = 20log (COL /ROW)	1	2	3	dB
Output Distortion	DIS		—	—	10	%
Frequency Stability	△f	Except error of osc. frequency	—	—	0.7	%

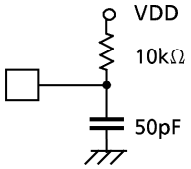
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = – 30 to 60°C)

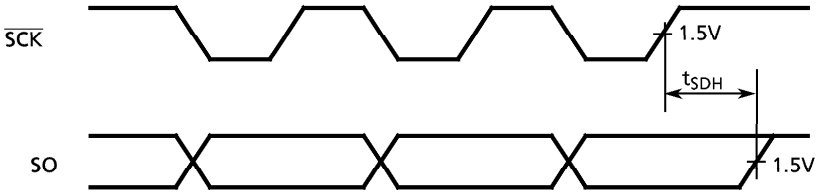
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		2.1			μs
High level clock pulse width	t_{WCH}	External clock operation	80	—	—	ns
Low level clock pulse width	t_{WCL}					
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	—	—	ns

Note. Shift Data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin.



Serial port (completion of transmission)

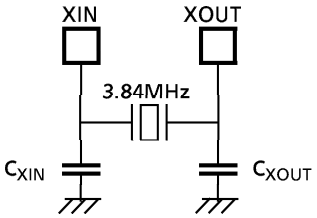


RECOMMENDED OSCILLATING CONDITIONS

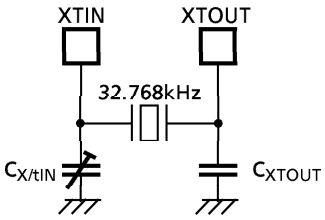
(V_{SS} = 0V, VDD = 2.7 to 6.0V, T_{OPR} = –30 to 60°C)

3.84MHz
Ceramic Resonator

CAS3.84MG901	(MURATA)	C_{XIN} = C_{XOUT} = 30pF
CAS3.84MGW901	(MURATA)	C_{XIN} = C_{XOUT} built-in



32.768kHz
Crystal Oscillator C_{XTIN}, C_{XTOUT} ; 10 to 33pF



Note : In order to get the accurate oscillation frequency, the adjustment of capacitors must be required.

TYPICAL CHARACTERISTICS