NTHS4111P

Power MOSFET

−30 V, −6.1 A, Single P−Channel, ChipFET™

Features

- Offers an Ultra Low $R_{DS(on)}$ Solution in the ChipFET Package
- ChipFET Package 40% Smaller Footprint than TSOP−6
- Low Profile (<1.1 mm) for Extremely Thin Environments
- Standard Logic Level Gate Drive

Applications

- Notebook Computer Load Switch
- Battery and Load Management Applications in Portable Equipment
- Charge Control in Battery Chargers
- Buck and Boost Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−4.4	A
		T_A = 85°C		−3.2	
	t≤10 s	T_A = 25°C		−6.1	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.3	W
	t≤10 s			2.5	
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	−3.3	A
		T_A = 85°C		−2.3	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.7	W
Pulsed Drain Current	tp = 10 μs		I_{DM}	−30	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	−2.1	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction−to−Ambient – Steady State (Note 1)	$R_{\theta JA}$	95	°C/W
Junction−to−Ambient – t≤10 s (Note 1)	$R_{\theta JA}$	50	
Junction−to−Ambient – Steady State (Note 2)	$R_{\theta JA}$	175	

1. Surface−mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface−mounted on FR4 board using the minimum recommended pad size (Cu area = 0.045 in sq).

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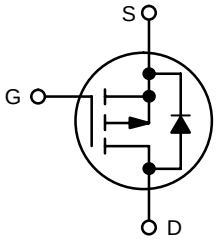
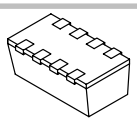
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
−30 V	33 mΩ @ −10 V	−6.1 A
	52 mΩ @ −4.5 V	

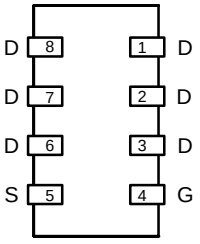


P−Channel MOSFET

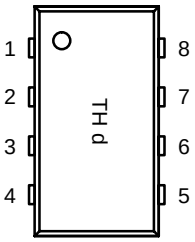


ChipFET
CASE 1206A
Style 1

PIN CONNECTIONS



MARKING DIAGRAM



TH = Specific Device Code
d = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NTHS4111PT1	ChipFET	3000 Tape / Reel
NTHS4111PT1G	ChipFET (Pb−free)	3000 Tape / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				−19		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −24 V	T_J = 25°C			−1.0	μA
			T_J = 125°C			−100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−1.0	−1.7	−3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −10 V, I_D = −4.4 A			33	45	mΩ
		V_{GS} = −4.5 V, I_D = −3.4 A			52	75	
Forward Transconductance	g_{FS}	V_{DS} = −15 V, I_D = −4.4 A			7.7		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −24 V			882	1500	pF
Output Capacitance	C_{OSS}				143		
Reverse Transfer Capacitance	C_{RSS}				105		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −10 V, V_{DD} = −15 V, I_D = −4.4 A			18.2	28	nC
Gate−to−Source Charge	Q_{GS}				2.95		
Gate−to−Drain Charge	Q_{GD}				4.25		
SWITCHING CHARACTERISTICS, V_{GS} = −10 V (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −10 V, V_{DD} = −15 V, I_D = −1.0 A, R_G = 6.0 Ω			9.0	18	ns
Rise Time	t_r				8.0	16	
Turn−Off Delay Time	$t_{d(OFF)}$				45	90	
Fall Time	t_f				26	52	
SWITCHING CHARACTERISTICS, V_{GS} = −4.5 V (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −4.5 V, V_{DD} = −15 V, I_D = −1.0 A, R_G = 6.0 Ω			11		ns
Rise Time	t_r				14		
Turn−Off Delay Time	$t_{d(OFF)}$				32		
Fall Time	t_f				23		
DRAIN − SOURCE DIODE CHARACTERISTICS							
Characteristic	**Symbol**	**Test Condition**		**Min**	**Typ**	**Max**	**Unit**
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −1.1 A	T_J = 25°C		−0.76	−1.2	V
			T_J = 125°C		−0.60		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = −1.1 A			27	54	ns
Charge Time	t_a				10		
Discharge Time	t_b				17		
Reverse Recovery Charge	Q_{RR}				12		nC

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

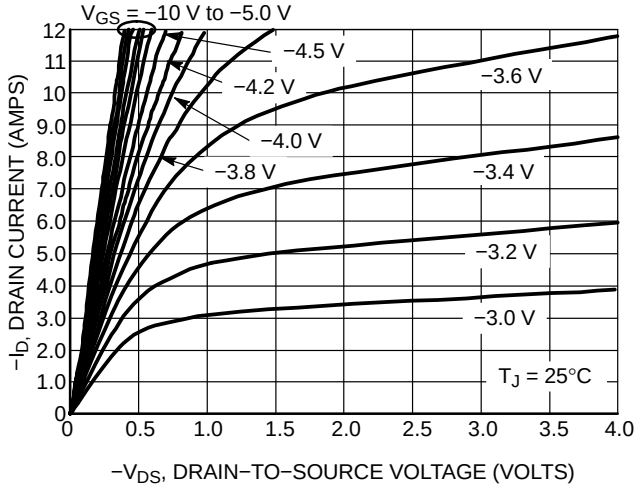


Figure 1. On−Region Characteristics

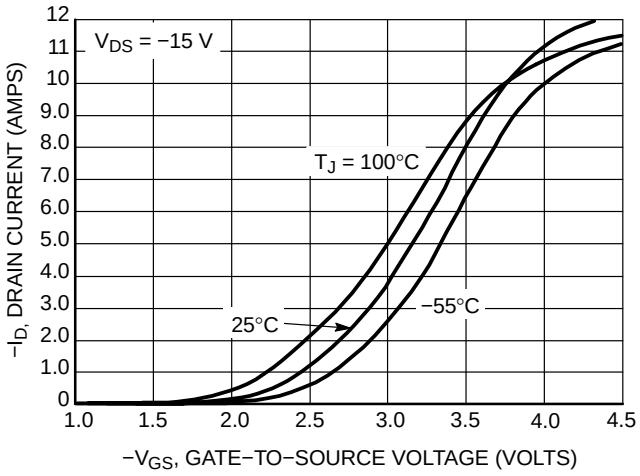


Figure 2. Transfer Characteristics

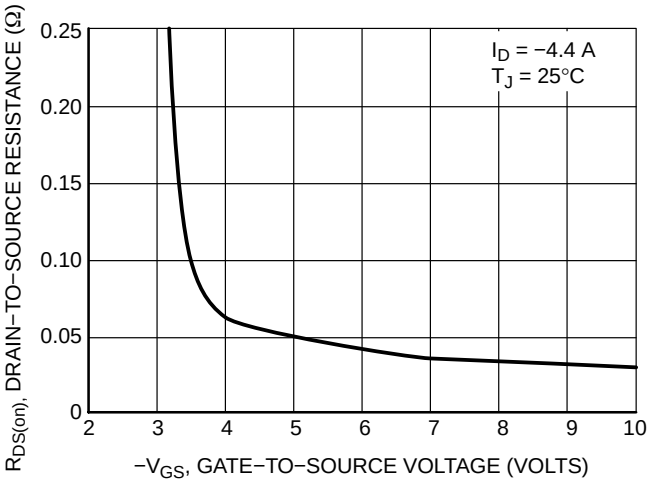


Figure 3. $R_{DS(on)}$ vs. V_{GS}

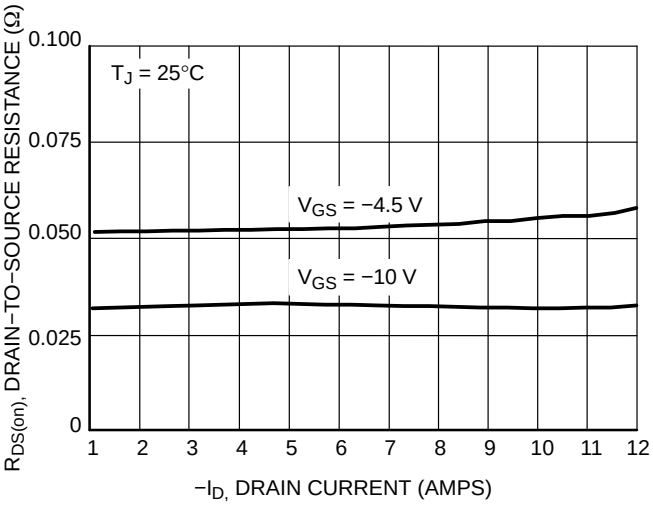


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

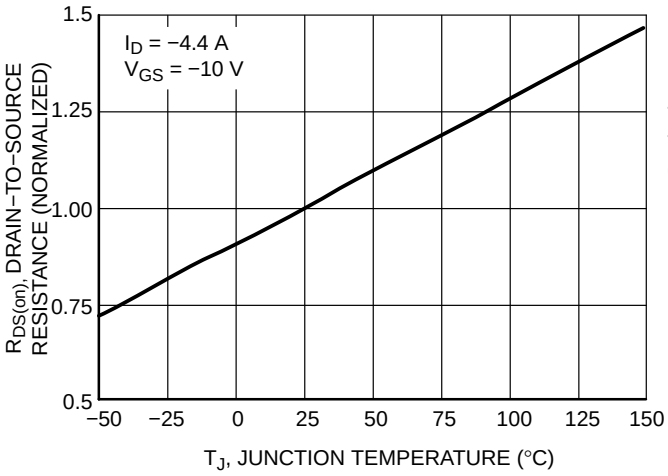


Figure 5. On−Resistance Variation with Temperature

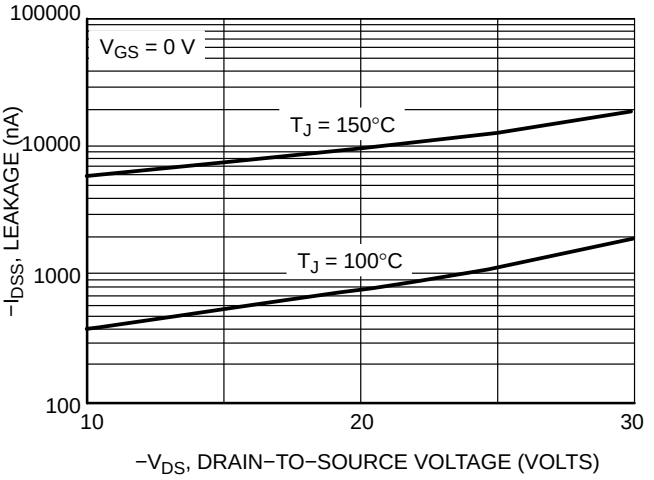


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

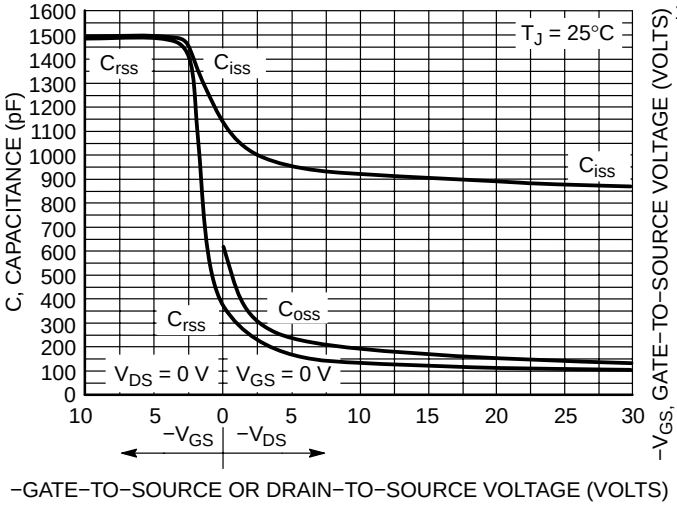


Figure 7. Capacitance Variation

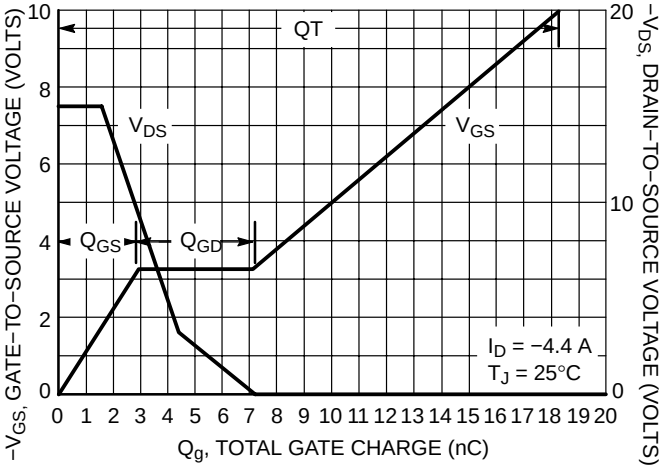


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

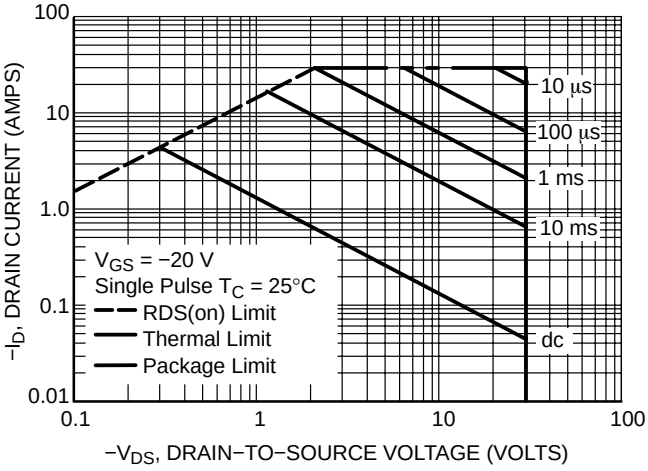


Figure 9. Maximum Rated Forward Biased Safe Operating Area

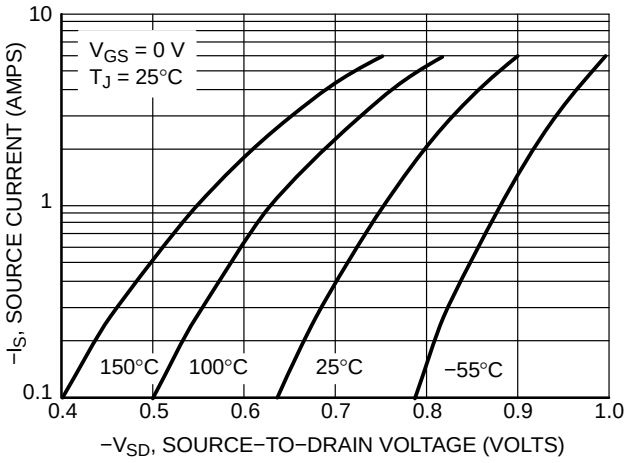


Figure 10. Diode Forward Voltage vs. Current

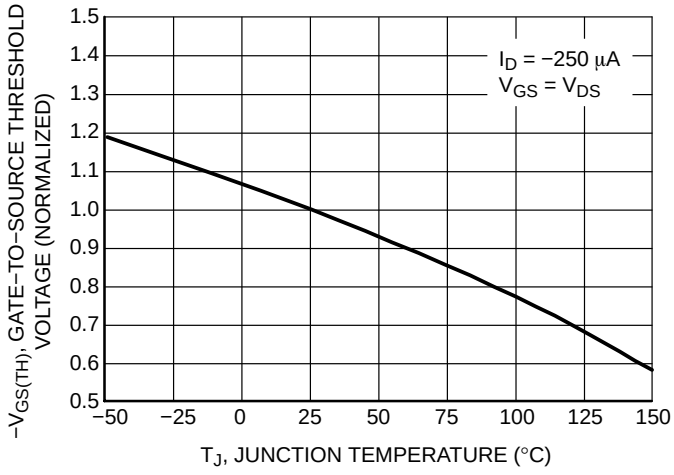


Figure 11. $V_{GS(TH)}$ Variation with Temperature

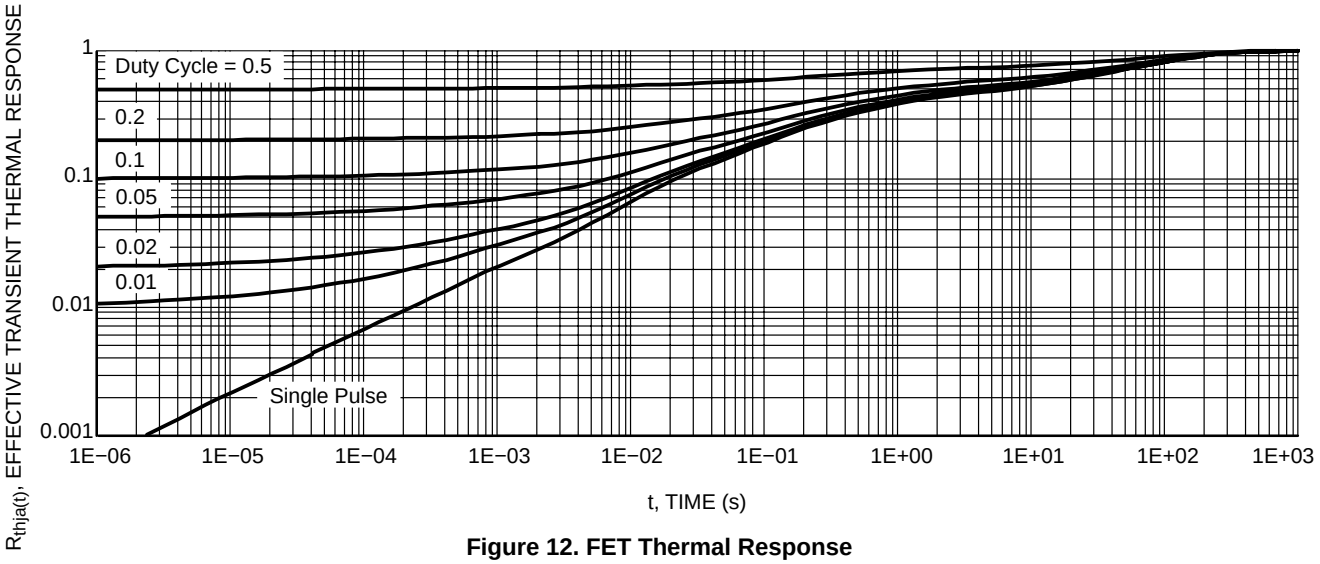
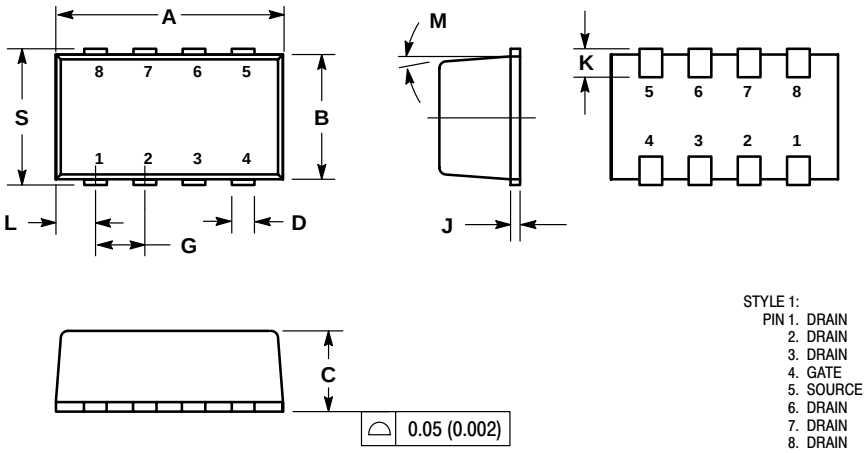


Figure 12. FET Thermal Response

PACKAGE DIMENSIONS

ChipFET
CASE 1206A−03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A−01 AND 1206A−02 OBSOLETE. NEW STANDARD IS 1206A−03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5 ° NOM		5 ° NOM	
S	1.80	2.00	0.072	0.080

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

SOLDER FOOTPRINT*

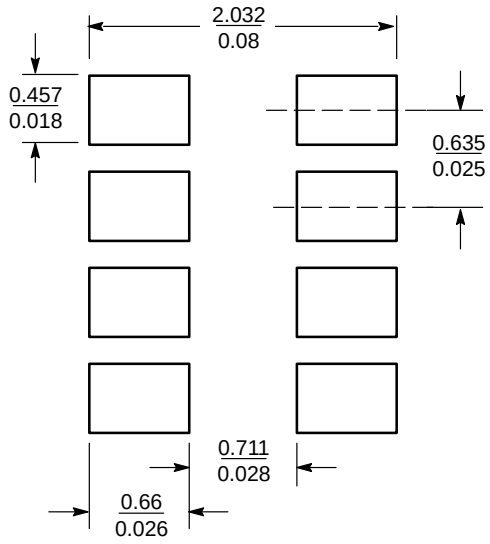


Figure 13. Basic

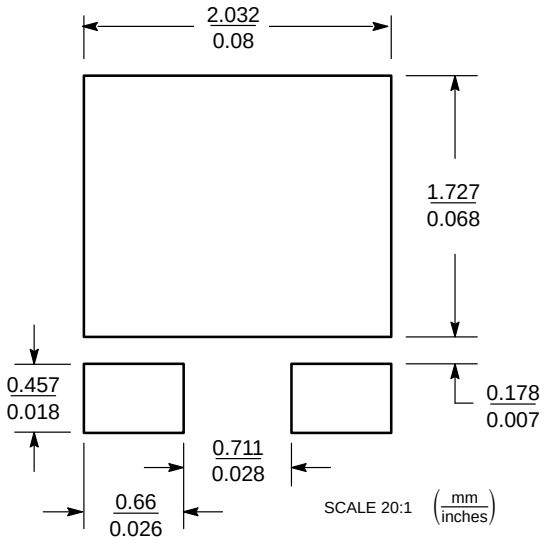


Figure 14. Style 1

*For information on soldering specifications, please refer to our Soldering Reference Manual, SOLDERRM/D.

Notes

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PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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