

# NTHS4111P

## Power MOSFET

–30 V, –6.1 A, Single P–Channel, ChipFET™

### Features

- Offers an Ultra Low  $R_{DS(on)}$  Solution in the ChipFET Package
- ChipFET Package 40% Smaller Footprint than TSOP–6
- Low Profile (<1.1 mm) for Extremely Thin Environments
- Standard Logic Level Gate Drive

### Applications

- Notebook Computer Load Switch
- Battery and Load Management Applications in Portable Equipment
- Charge Control in Battery Chargers
- Buck and Boost Converters

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Rating			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	−30	V
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain Current (Note 1)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	−4.4	A
		T <sub>A</sub> = 85°C		−3.2	
	t≤10 s	T <sub>A</sub> = 25°C		−6.1	
Power Dissipation (Note 1)	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub>	1.3	W
	t≤10 s			2.5	
Continuous Drain Current (Note 2)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	−3.3	A
		T <sub>A</sub> = 85°C		−2.3	
Power Dissipation (Note 2)		T <sub>A</sub> = 25°C	P <sub>D</sub>	0.7	W
Pulsed Drain Current	tp = 10 μs		I <sub>DM</sub>	−30	A
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>STG</sub>	−55 to 150	°C
Source Current (Body Diode)			I <sub>S</sub>	−2.1	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

### THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction–to–Ambient – Steady State (Note 1)	$R_{\theta JA}$	95	$^\circ\text{C}/\text{W}$
Junction–to–Ambient – $t \leq 10$ s (Note 1)	$R_{\theta JA}$	50	
Junction–to–Ambient – Steady State (Note 2)	$R_{\theta JA}$	175	

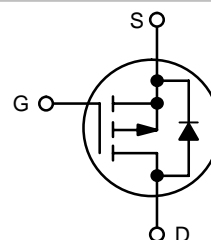
1. Surface–mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface–mounted on FR4 board using the minimum recommended pad size (Cu area = 0.045 in sq).



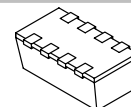
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$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
–30 V	33 m $\Omega$ @ –10 V	–6.1 A
	52 m $\Omega$ @ –4.5 V	

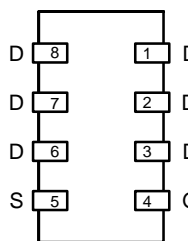


**P–Channel MOSFET**

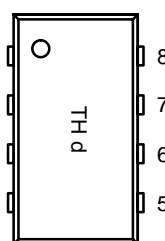


**ChipFET  
CASE 1206A  
Style 1**

### PIN CONNECTIONS



### MARKING DIAGRAM



TH = Specific Device Code  
d = Date Code

### ORDERING INFORMATION

Device	Package	Shipping†
NTHS4111PT1	ChipFET	3000 Tape / Reel
NTHS4111PT1G	ChipFET (Pb–free)	3000 Tape / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTHS4111P

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			-19		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -24 V			-1.0	μA
					-100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-1.0	-1.7	-3.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			5.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -4.4 A		33	45	mΩ
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.4 A		52	75	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -4.4 A		7.7		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = -24 V		882	1500	pF
Output Capacitance	C <sub>OSS</sub>			143		
Reverse Transfer Capacitance	C <sub>RSS</sub>			105		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = -10 V, V <sub>DD</sub> = -15 V, I <sub>D</sub> = -4.4 A		18.2	28	nC
Gate-to-Source Charge	Q <sub>GS</sub>			2.95		
Gate-to-Drain Charge	Q <sub>GD</sub>			4.25		

### SWITCHING CHARACTERISTICS, V<sub>GS</sub> = -10 V (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = -10 V, V <sub>DD</sub> = -15 V, I <sub>D</sub> = -1.0 A, R <sub>G</sub> = 6.0 Ω		9.0	18	ns
Rise Time	t <sub>r</sub>			8.0	16	
Turn-Off Delay Time	t <sub>d(OFF)</sub>			45	90	
Fall Time	t <sub>f</sub>			26	52	

### SWITCHING CHARACTERISTICS, V<sub>GS</sub> = -4.5 V (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DD</sub> = -15 V, I <sub>D</sub> = -1.0 A, R <sub>G</sub> = 6.0 Ω		11		ns
Rise Time	t <sub>r</sub>			14		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			32		
Fall Time	t <sub>f</sub>			23		

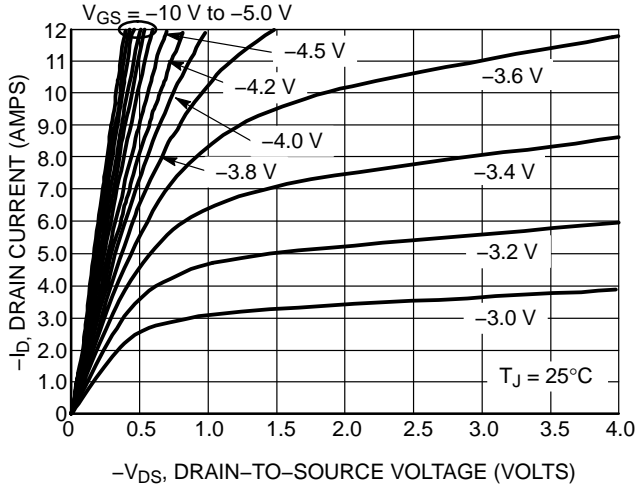
### DRAIN - SOURCE DIODE CHARACTERISTICS

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -1.1 A		-0.76	-1.2	V
				-0.60		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = -1.1 A		27	54	ns
Charge Time	t <sub>a</sub>			10		
Discharge Time	t <sub>b</sub>			17		
Reverse Recovery Charge	Q <sub>RR</sub>			12		nC

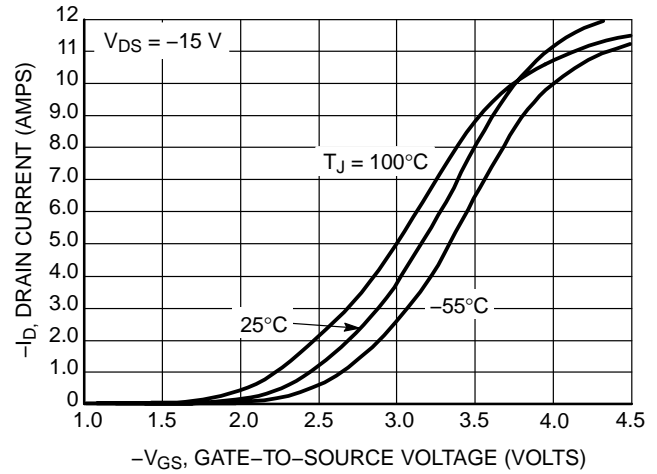
3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

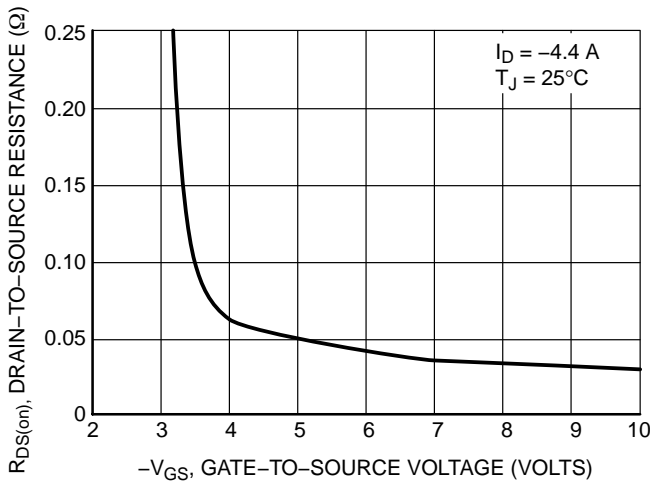
**TYPICAL PERFORMANCE CURVES** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)



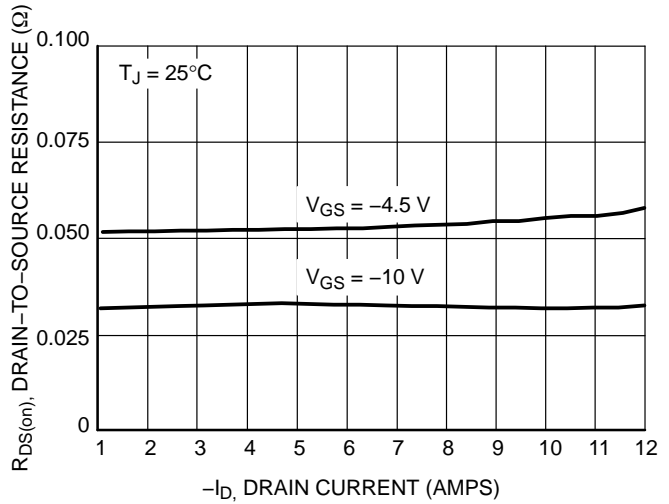
**Figure 1. On-Region Characteristics**



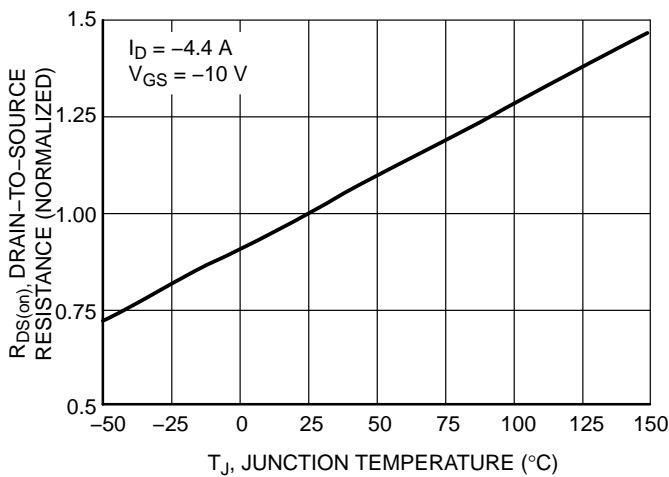
**Figure 2. Transfer Characteristics**



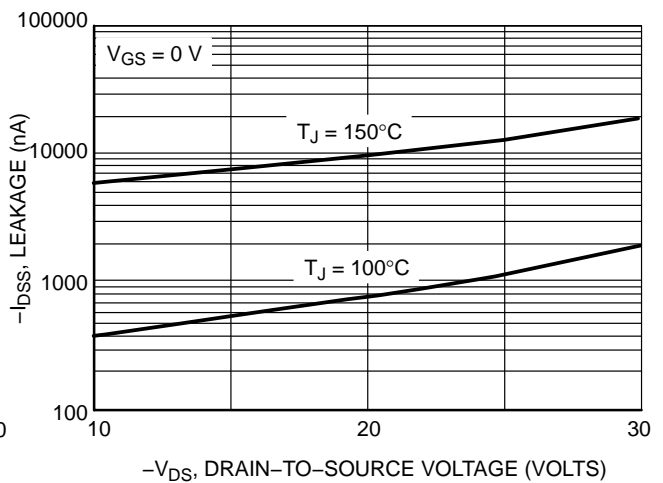
**Figure 3.  $R_{DS(on)}$  vs.  $V_{GS}$**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**

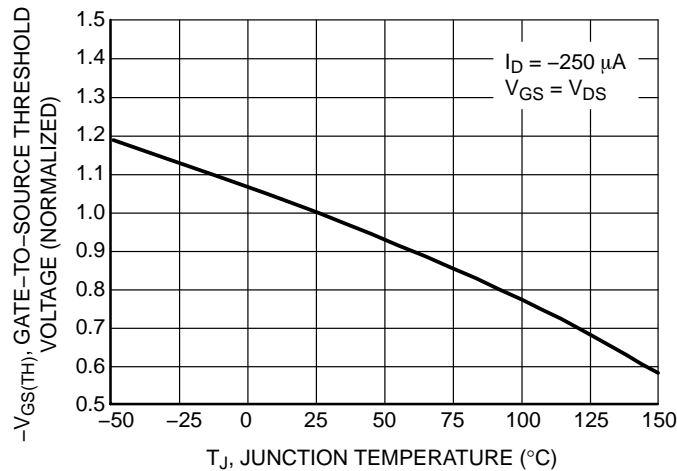
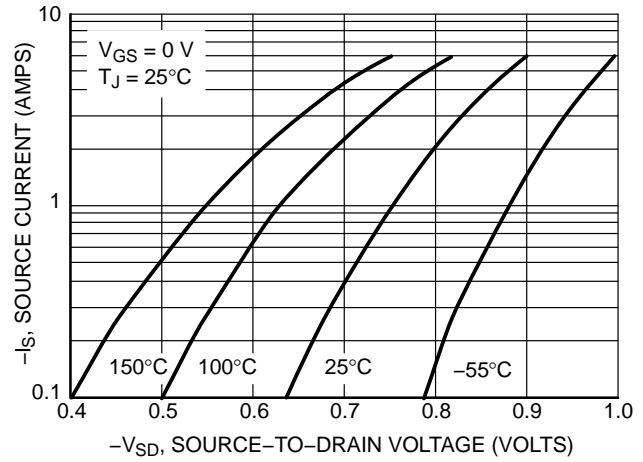
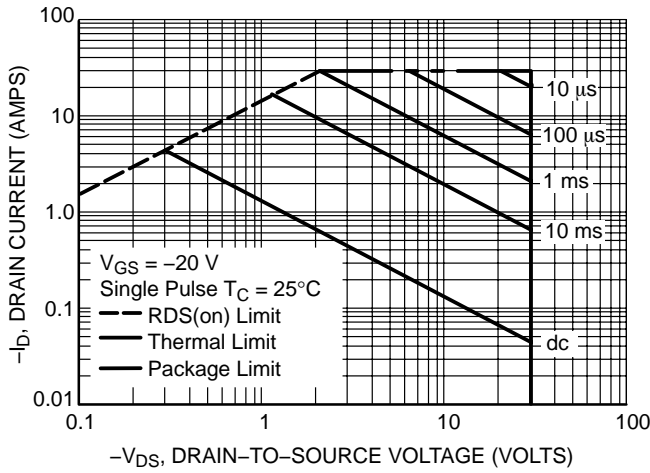
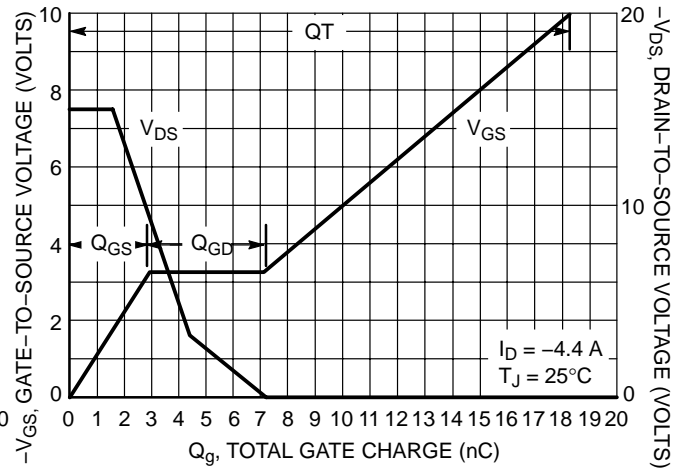
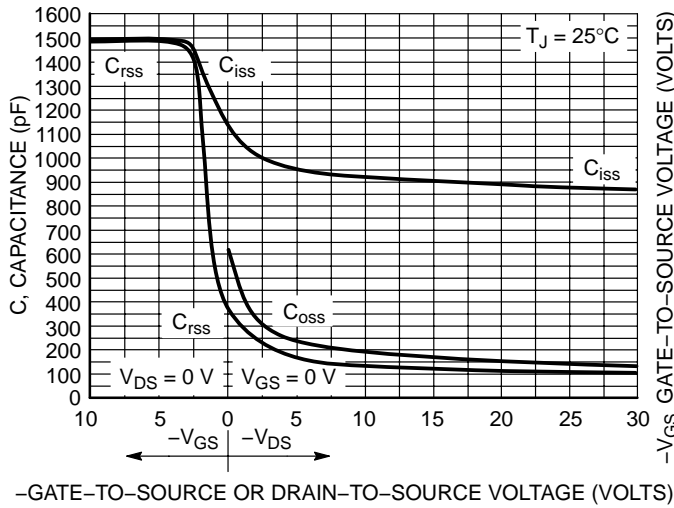


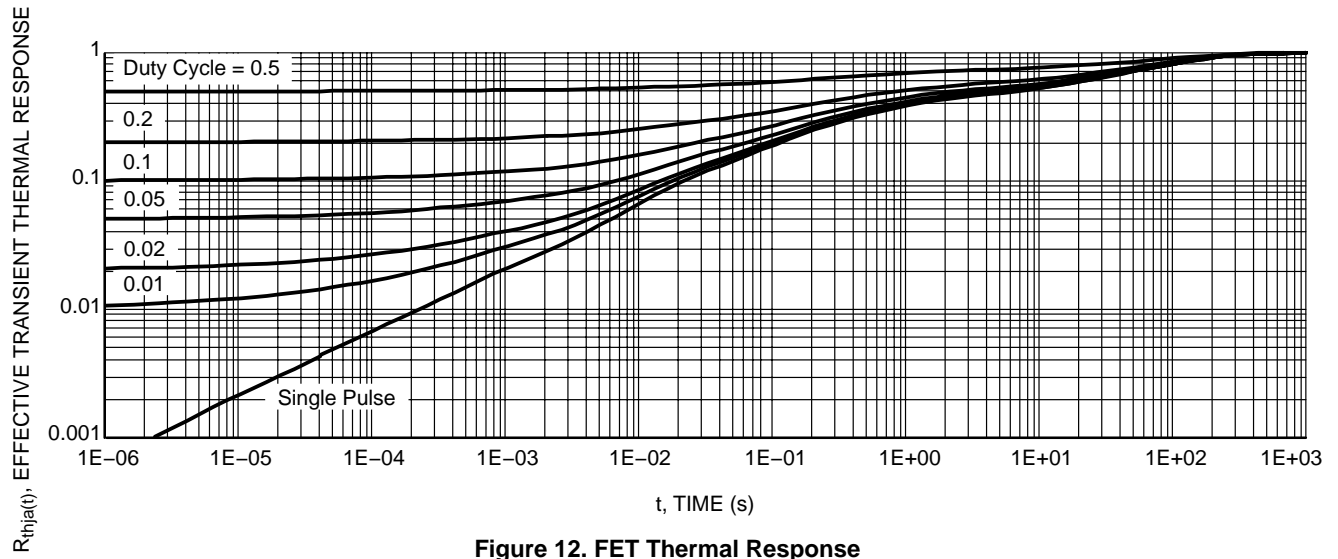
**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

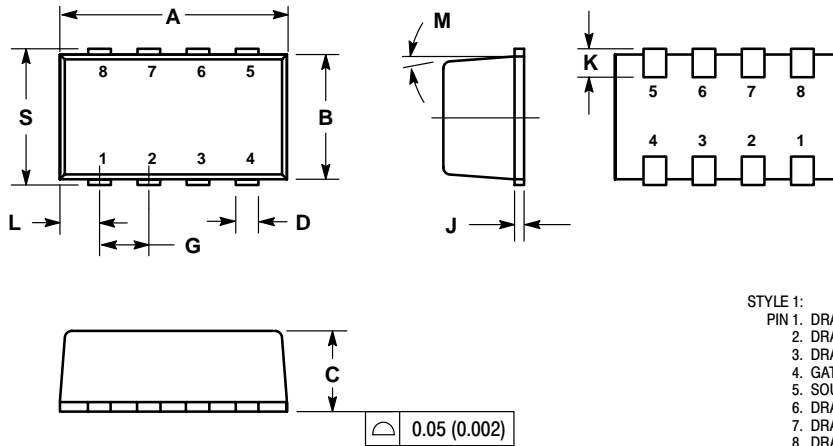




# NTHS4111P

## PACKAGE DIMENSIONS

### ChipFET CASE 1206A-03 ISSUE E



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5° NOM		5° NOM	
S	1.80	2.00	0.072	0.080

STYLE 1:  
PIN 1: DRAIN  
2: DRAIN  
3: DRAIN  
4: GATE  
5: SOURCE  
6: DRAIN  
7: DRAIN  
8: DRAIN

#### SOLDER FOOTPRINT\*

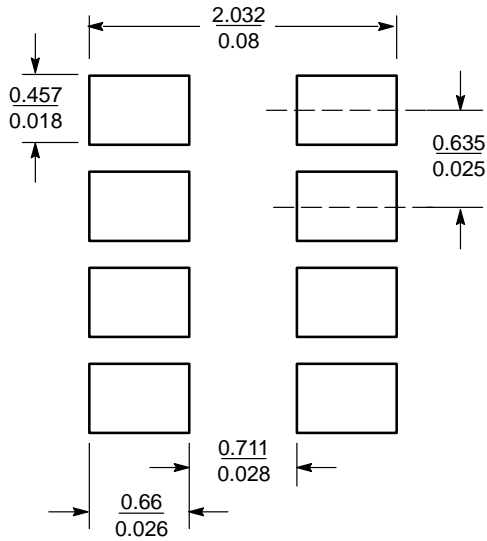


Figure 13. Basic

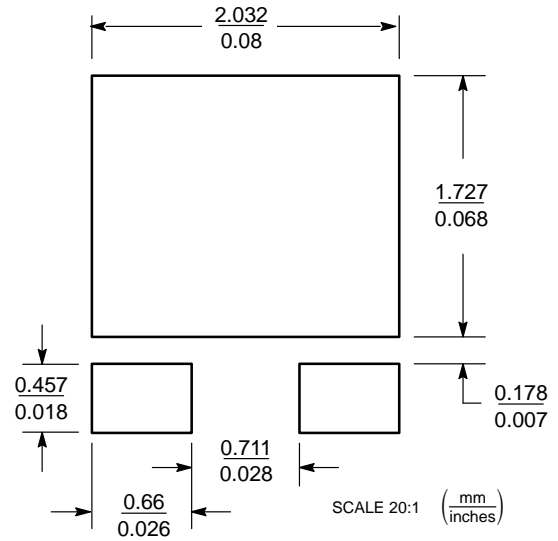



Figure 14. Style 1

\*For information on soldering specifications, please refer to our Soldering Reference Manual, SOLDERRM/D.

## **Notes**

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