

Data Sheet November 1998 File Number 4541

### Radiation Hardened Hex Inverter

The Radiation Hardened ACS04MS is a Hex Inverter. This device simply inverts the level present on each input. All inputs are buffered and the outputs are designed for balanced propagation delay and transition times.

The ACS04MS is fabricated on a CMOS Silicon on Sapphire (SOS) process, which provides an immunity to Single Event Latch-up and the capability of highly reliable performance in any radiation environment. These devices offer significant power reduction and faster performance when compared to ALSTTL types.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the ACS04MS are contained in SMD 5962-98603. A "hot-link" is provided on our homepage with instructions for downloading. www.intersil.com/data/sm/index.asp

#### **Features**

- QML Qualified Per MIL-PRF-38535 Requirements
- 1.25 Micron Radiation Hardened SOS CMOS
- Radiation Environment
  - Latch-Up Free Under Any Conditions

  - SEU LET Threshold . . . . . >100MeV/(mg/cm<sup>2</sup>)
- Input Logic Levels. . . .  $V_{IL} = (0.3)(V_{CC})$ ,  $V_{IH} = (0.7)(V_{CC})$
- Quiescent Supply Current . . . . . . . . . . . . 100μA (Max)

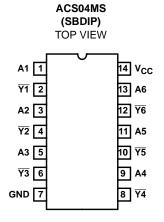
# **Applications**

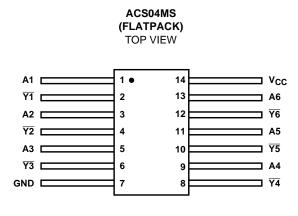
- · High Speed Control Circuits
- · Sensor Monitoring
- · Low Power Designs

# **Ordering Information**

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)	PACKAGE	DESIGNATOR
5962F9860301VCC	ACS04DMSR-03	-55 to 125	14 Ld SBDIP	CDIP2-T14
ACS04D/SAMPLE-03	ACS04D/SAMPLE-03	25	14 Ld SBDIP	CDIP2-T14
5962F9860301VXC	ACS04KMSR-03	-55 to 125	14 Ld Flatpack	CDFP4-F14
ACS04K/SAMPLE-03	ACS04K/SAMPLE-03	25	14 Ld Flatpack	CDFP4-F14
5962F9860301V9A	ACS04HMSR-03	25	Die	N/A

### **Pinouts**





## Die Characteristics

#### **DIE DIMENSIONS:**

Size:  $2390\mu m \times 2390\mu m$  (94 mils x 94 mils) Thickness:  $525\mu m \pm 25\mu m$  (20.6 mils  $\pm 1$  mil) Bond Pad:  $110\mu m \times 110\mu m$  (4.3 x 4.3 mils)

#### **METALLIZATION: AI**

Metal 1 Thickness:  $0.7\mu m \pm 0.1\mu m$ Metal 2 Thickness:  $1.0\mu m \pm 0.1\mu m$ 

#### SUBSTRATE POTENTIAL:

**Unbiased Insulator** 

#### PASSIVATION:

Type: Phosphorous Silicon Glass (PSG)

Thickness:  $1.30\mu m \pm 0.15\mu m$ 

#### **SPECIAL INSTRUCTIONS:**

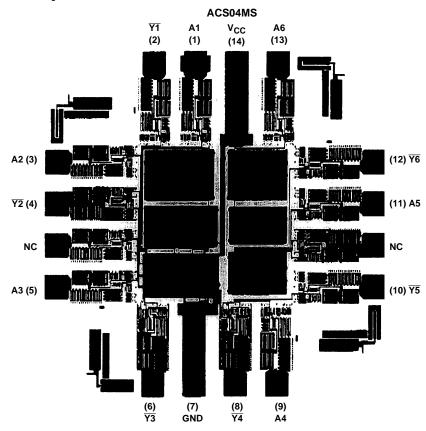
Bond V<sub>CC</sub> First

#### ADDITIONAL INFORMATION:

Worst Case Current Density: <2.0 x 10<sup>5</sup> A/cm<sup>2</sup>

Transistor Count: 82

# Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site www.intersil.com

## Sales Office Headquarters

NORTH AMERICA

Intersil Corporation P. O. Box 883, Mail Stop 53-204 Melbourne, FL 32902

TEL: (321) 724-7000 FAX: (321) 724-7240 EUROPE

Intersil SA Mercure Center 100, Rue de la Fusee 1130 Brussels, Belgium

TEL: (32) 2.724.2111 FAX: (32) 2.724.22.05

**ASIA** 

Intersil (Taiwan) Ltd. 7F-6, No. 101 Fu Hsing North Road Taipei, Taiwan Republic of China TEL: (886) 2 2716 9310

FAX: (886) 2 2715 3029