



Low Distortion, Precision, Wide Bandwidth Op Amp

AD9617

FEATURES

Usable Closed-Loop Gain Range: ± 1 to ± 40
Low Distortion: -67 dBc (2nd) at 20 MHz
Small Signal Bandwidth: 190 MHz ($A_V = +3$)
Large Signal Bandwidth: 150 MHz at 4 V p-p
Settling Time: 10 ns to 0.1%; 14 ns to 0.02%
Overdrive and Output Short Circuit Protected
Fast Overdrive Recovery
DC Nonlinearity 10 ppm

APPLICATIONS

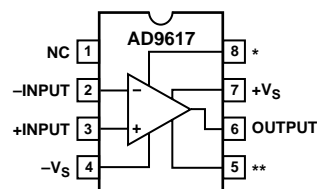
Driving Flash Converters
D/A Current-to-Voltage Converters
IF, Radar Processors
Baseband and Video Communications
Photodiode, CCD Preamps

GENERAL DESCRIPTION

The AD9617 is a current feedback amplifier which utilizes a proprietary architecture to produce superior distortion and dc precision. It achieves this along with fast settling, very fast slew rate, wide bandwidth (both small signal and large signal) and exceptional signal fidelity. The device achieves -67 dBc 2nd harmonic distortion at 20 MHz while maintaining 190 MHz small signal and 150 MHz large signal bandwidths.

These attributes position the AD9617 as an ideal choice for driving flash ADCs and buffering the latest generation of DACs. Optimized for applications requiring gain between ± 1 to ± 15 , the AD9617 is unity gain stable without external compensation.

PIN CONFIGURATION



NC = NO CONNECT

*OPTIONAL $+V_S$

**OPTIONAL $-V_S$

NOTE:
FOR BEST SETTLING TIME AND DISTORTION
PERFORMANCE, USE OPTIONAL SUPPLY
CONNECTIONS. PERFORMANCE INDICATED
IN SPECIFICATIONS IS BASED ON SUPPLY
CONNECTIONS TO THESE PINS.

The AD9617 offers outstanding performance in high fidelity, wide bandwidth applications in instrumentation ranging from network and spectrum analyzers to oscilloscopes, and in military systems such as radar, SIGINT and ESM systems. The superior slew rate, low overshoot and fast settling of the AD9617 allow the device to be used in pulse applications such as communications receivers and high speed ATE. Most monolithic op amps suffer in these precision pulse applications due to slew rate limiting.

The AD9617J operates over the range of 0°C to $+70^{\circ}\text{C}$ and is available in either an 8-lead plastic DIP or an 8-lead plastic small outline package (SOIC).

REV. B

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AD9617—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS¹

| | |
|---|-----------------|
| Supply Voltages ($\pm V_S$) | +7 V |
| Common-Mode Input Voltage | $\pm V_S$ |
| Differential Input Voltage | 3 V |
| Continuous Output Current ² | 70 mA |
| Operating Temperature Ranges | |
| AD9617JN/JR | 0°C to +70°C |
| Storage Temperature | |
| AD9617JN/JR | −65°C to +125°C |
| Junction Temperature ³ | |
| AD9617JN/JR | +150°C |
| Lead Soldering Temperature (10 Seconds) | +300°C |

NOTES

¹ Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

² Output is short circuit protected to ground, but not to supplies. Continuous short circuit to ground may affect device reliability.

³ Typical thermal impedances (part soldered onto board):
Plastic DIP: $\theta_{JA} = 140^\circ\text{C/W}$; $\theta_{JC} = 30^\circ\text{C/W}$. SOIC Package: $\theta_{JA} = 155^\circ\text{C/W}$; $\theta_{JC} = 40^\circ\text{C/W}$.

DC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $A_V = +3$; $\pm V_S = \pm 5\text{ V}$; $R_F = 400\ \Omega$; $R_{LOAD} = 100\ \Omega$)

| Parameter | Conditions | Temp | Test Level | AD9617JN/JR | | | AD9617AQ/SQ* | | | AD9617BQ/TQ* | | | Units |
|--|--------------------------------------|-------|------------|-------------|------|------|--------------|------|------|--------------|------|-------|------------------------------|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage ^{1, 2} | | +25°C | I | −1.1 | +0.5 | +2.2 | −1.1 | +0.5 | +2.2 | +0.0 | +0.5 | +1.35 | mV |
| Input Offset Voltage TC ² | | Full | IV | −4 | +3 | +25 | −4 | +3 | +25 | −4 | +3 | +25 | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current ² | | | | | | | | | | | | | |
| Inverting | | +25°C | I | −50 | 0 | +50 | −50 | 0 | +50 | −25 | 0 | +25 | μA |
| Noninverting | | +25°C | I | −25 | +5 | +35 | −25 | +5 | +35 | −15 | +5 | +20 | μA |
| Input Bias Current TC ² | | | | | | | | | | | | | |
| Noninverting | | Full | IV | −50 | +30 | +125 | −50 | +30 | +125 | −50 | +30 | +125 | $\text{nA}/^\circ\text{C}$ |
| Inverting | | Full | IV | −50 | +50 | +150 | −50 | +50 | +150 | −50 | +50 | +150 | $\text{nA}/^\circ\text{C}$ |
| Input Resistance | | | | | | | | | | | | | |
| Noninverting | | +25°C | V | | 60 | | | 60 | | | 60 | | k Ω |
| Input Capacitance | | | | | | | | | | | | | |
| Noninverting | | +25°C | V | | 1.5 | | | 1.5 | | | 1.5 | | pF |
| Common-Mode Input Range ³ | $T = T_{MAX}$ | ← | II | ±1.4 | ±1.5 | | ±1.4 | ±1.5 | | ±1.4 | ±1.5 | | V |
| | $T = T_{MIN}$ to +25°C | ← | II | ±1.7 | ±1.8 | | ±1.7 | ±1.8 | | ±1.7 | ±1.8 | | V |
| Common-Mode Rejection Ratio ⁴ | $T = T_{MIN}$ to T_{MAX} | ← | II | 44 | 48 | | 44 | 48 | | 44 | 48 | | dB |
| | $T = T_{MIN}$ to +25°C | ← | II | 48 | 51 | | 48 | 51 | | 48 | 51 | | dB |
| Power Supply Rejection Ratio | $\Delta V_S = \pm 5\%$ | Full | II | 48 | 51 | | 48 | 51 | | 48 | 51 | | dB |
| Open Loop Gain | | | | | | | | | | | | | |
| T_O | At DC | +25°C | V | | 500 | | | 500 | | | 500 | | k Ω |
| Nonlinearity | At DC | +25°C | IV | | 10 | | | 10 | | | 10 | | ppm |
| Output Voltage Range | | +25°C | II | ±3.4 | ±3.8 | | ±3.4 | ±3.8 | | ±3.4 | ±3.8 | | V |
| Output Impedance | At DC | +25°C | V | | 0.07 | | | 0.07 | | | 0.07 | | Ω |
| Output Current (50 Ω Load) | $T = +25^\circ\text{C}$ to T_{MAX} | ← | II | 60 | | | 60 | | | 60 | | | mA |
| | $T = T_{MIN}$ | ← | II | 50 | | | 50 | | | 50 | | | mA |

NOTES

*Pending obsolescence: last-time buy October 25, 1999.

¹Measured with respect to the inverting input.

²Typical is defined as the mean of the distribution.

³Measured in voltage follower configuration.

⁴Measured with $V_{IN} = +0.25\text{ V}$.

Specifications subject to change without notice.

AC ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $A_V = +3$; $\pm V_S = \pm 5\text{ V}$; $R_F = 400\ \Omega$; $R_{LOAD} = 100\ \Omega$)

| Parameter | Conditions | Temp | Test Level | AD9617JN/JR | | | AD9617AQ/SQ* | | | AD9617BQ/TQ* | | | Units |
|---|-------------------------------|-------|------------|-------------|-------|-----|--------------|-------|-----|--------------|-------|-----|---------|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| FREQUENCY DOMAIN | | | | | | | | | | | | | |
| Bandwidth (−3 dB) | | | | | | | | | | | | | |
| Small Signal | V _{OUT} ≤ 2 V p-p | Full | II | 135 | 190 | | 145 | 190 | | 145 | 190 | | MHz |
| Large Signal | V _{OUT} = 4 V p-p | Full | IV | | 150 | | 115 | 150 | | 115 | 150 | | MHz |
| Bandwidth Variation vs. A _V | A _V = −1 to ±15 | +25°C | V | | 40 | | | 40 | | | 40 | | MHz |
| Amplitude of Peaking (<50 MHz) | T = T _{MIN} to +25°C | ← | II | | 0 | | | 0 | 0.3 | | 0 | 0.3 | dB |
| | T = T _{MAX} | ← | II | | 0 | | | 0 | 0.6 | | 0 | 0.6 | dB |
| Amplitude of Peaking (>50 MHz) | T = T _{MIN} to +25°C | ← | II | | 0 | | | 0 | 0.8 | | 0 | 0.8 | dB |
| | T = T _{MAX} | ← | II | | 0 | | | 0 | 1.0 | | 0 | 1.0 | dB |
| Amplitude of Roll-Off (<60 MHz) | | Full | II | | 0.1 | | | 0.1 | 0.6 | | 0.1 | 0.6 | dB |
| Phase Nonlinearity | DC to 75 MHz | +25°C | V | | 0.5 | | | 0.5 | | | 0.5 | | Degree |
| 2nd Harmonic Distortion | 2 V p-p; 4.3 MHz | Full | IV | | −86 | −78 | | −86 | −78 | | −86 | −78 | dBc |
| | 2 V p-p; 20 MHz | Full | IV | | −67 | −59 | | −67 | −59 | | −67 | −59 | dBc |
| | 2 V p-p; 60 MHz | Full | II | | −51 | −43 | | −51 | −43 | | −51 | −43 | dBc |
| 3rd Harmonic Distortion | 2 V p-p; 4.3 MHz | Full | IV | | −83 | −75 | | −83 | −75 | | −83 | −75 | dBc |
| | 2 V p-p; 20 MHz | Full | IV | | −69 | −61 | | −69 | −61 | | −69 | −61 | dBc |
| | 2 V p-p; 60 MHz | Full | II | | −54 | −46 | | −54 | −46 | | −54 | −46 | dBc |
| Input Noise Voltage | 10 MHz | +25°C | V | | 1.2 | | | 1.2 | | | 1.2 | | nV/√Hz |
| Inverting Input Noise Current | 10 MHz | +25°C | V | | 29 | | | 29 | | | 29 | | pA/√Hz |
| Average Equivalent Integrated Input Noise Voltage | 0.1 MHz to 200 MHz | +25°C | V | | 55 | | | 55 | | | 55 | | μV, rms |
| TIME DOMAIN | | | | | | | | | | | | | |
| Slew Rate | V _{OUT} = 4 V Step | Full | IV | | 1400 | | 1100 | 1400 | | 1100 | 1400 | | V/μs |
| Rise/Fall Time | | | | | | | | | | | | | |
| V _{OUT} = 2 V Step | | Full | IV | | 2.0 | | | 2.0 | 2.5 | | 2.0 | 2.5 | ns |
| V _{OUT} = 4 V Step | T = +25°C to T _{MAX} | ← | IV | | 2.4 | | | 2.4 | 3.3 | | 2.4 | 3.3 | ns |
| V _{OUT} = 4 V Step | T = T _{MIN} | ← | IV | | 2.4 | | | 2.4 | 3.5 | | 2.4 | 3.5 | ns |
| Overshoot | V _{OUT} = 2 V Step | Full | IV | | 3 | | | 3 | 14 | | 3 | 14 | % |
| Settling Time | | | | | | | | | | | | | |
| To 0.1% | V _{OUT} = 2 V Step | Full | IV | | 10 | | | 10 | 15 | | 10 | 15 | ns |
| To 0.02% | V _{OUT} = 2 V Step | Full | IV | | 14 | | | 14 | 23 | | 14 | 23 | ns |
| To 0.1% | V _{OUT} = 4 V Step | Full | IV | | 11 | | | 11 | 16 | | 11 | 16 | ns |
| To 0.02% | V _{OUT} = 4 V Step | Full | IV | | 16 | | | 16 | 24 | | 16 | 24 | ns |
| 2× Overdrive Recovery to ±2 mV of Final Value | V _{IN} = 1.7 V Step | +25°C | V | | 50 | | | 50 | | | 50 | | ns |
| Propagation Delay | | +25°C | V | | 2 | | | 2 | | | 2 | | ns |
| Differential Gain ¹ | | Full | V | | <0.01 | | | <0.01 | | | <0.01 | | % |
| Differential Phase ¹ | | Full | V | | 0.01 | | | 0.01 | | | 0.01 | | Degree |
| POWER SUPPLY REQUIREMENTS | | | | | | | | | | | | | |
| Quiescent Current | | | | | | | | | | | | | |
| +I _S | | Full | II | | 34 | 48 | | 34 | 48 | | 34 | 48 | mA |
| −I _S | | Full | II | | 34 | 48 | | 34 | 48 | | 34 | 48 | mA |

NOTES

*Pending obsolescence: last-time buy October 25, 1999.

¹Frequency = 4.3 MHz; $R_L = 150\ \Omega$; $A_V = +3$.

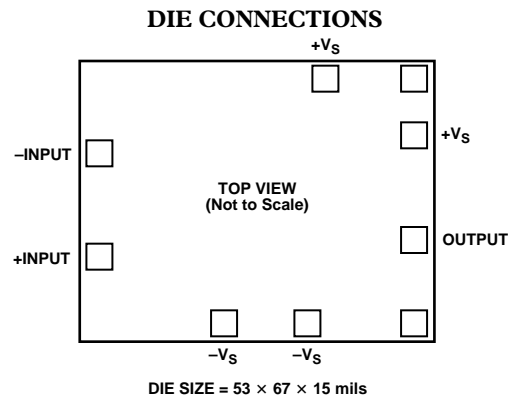
Specifications subject to change without notice.

AD9617

EXPLANATION OF TEST LEVELS

Test Level

- I - 100% production tested.
- II - 100% production tested at +25°C and sample tested at specified temperatures. AC testing of J grade devices done on sample basis.
- III - Sample tested only.
- IV - Parameter is guaranteed by design and characterization testing.
- V - Parameter is a typical value only.
- VI - All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---------------|-------------------|---------------------|----------------|
| AD9617JN | 0°C to +70°C | Plastic DIP | N-8 |
| AD9617JR | 0°C to +70°C | SOIC | SO-8 |
| AD9617JR-REEL | 0°C to +70°C | 13" Tape and Reel | SO-8 |

Typical Performance Characteristics ($A_V = +3$; $\pm V_S = \pm 5$ V; $R_F = 400$ Ω , unless otherwise noted)

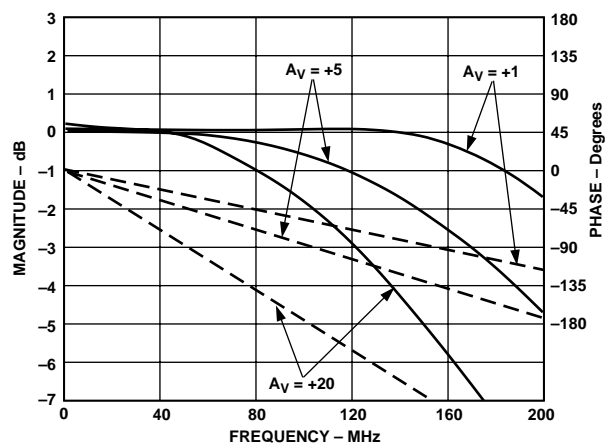


Figure 1. Noninverting Frequency Response

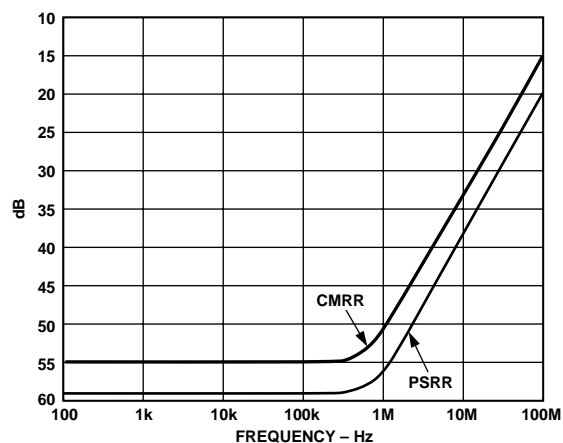


Figure 4. CMRR and PSRR

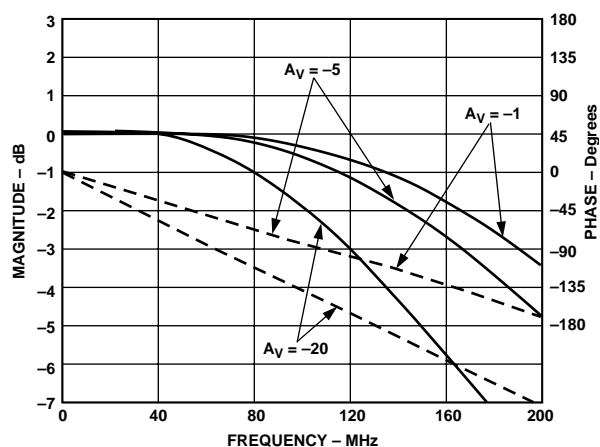


Figure 2. Inverting Frequency Response

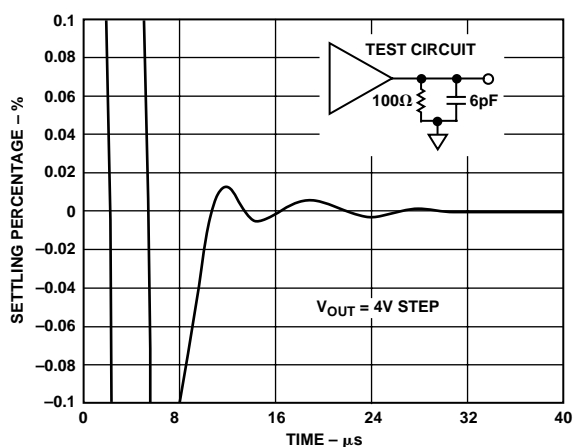


Figure 5. Settling Time

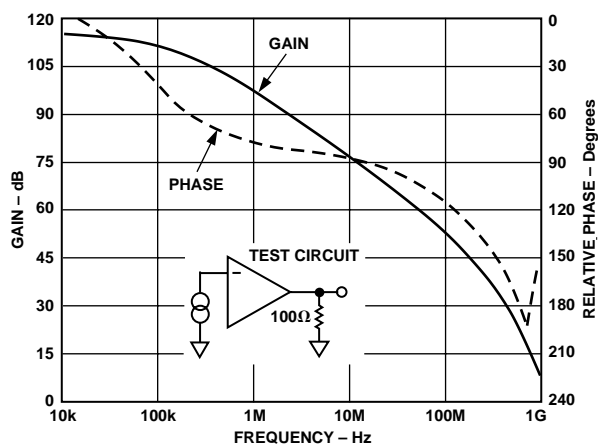
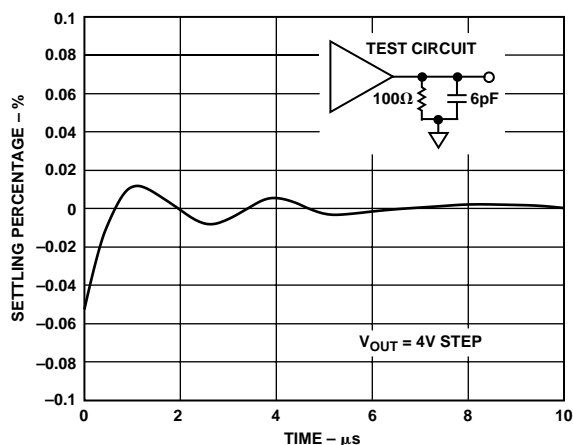
Figure 3. Open Loop Transimpedance Gain [$T(s)$ Relative to 1 Ω]

Figure 6. Long Term Settling Time

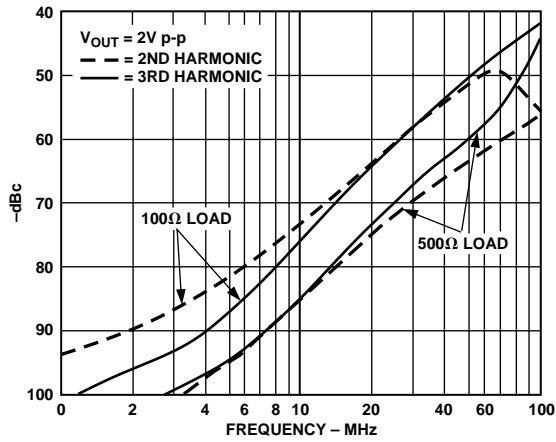


Figure 7. Harmonic Distortion

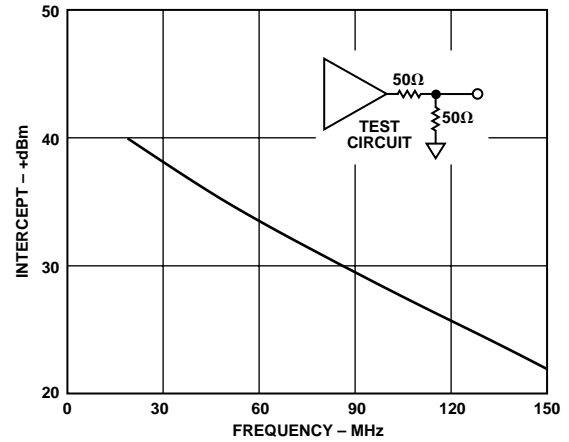


Figure 10. Intermodulation Distortion (IMD)

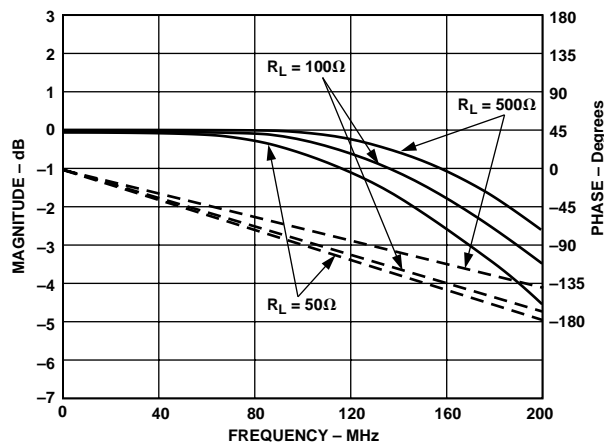


Figure 8. Frequency Response vs. R_{LOAD}

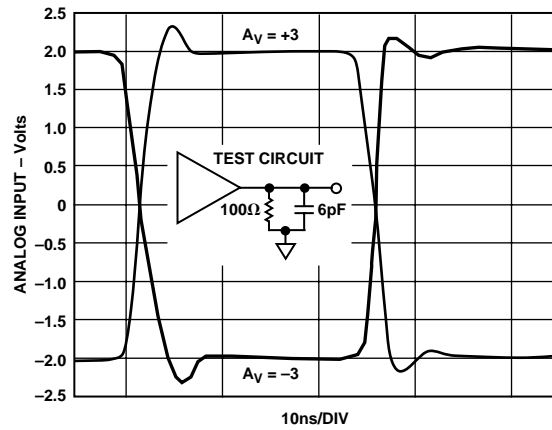


Figure 11. Large Signal Pulse Response

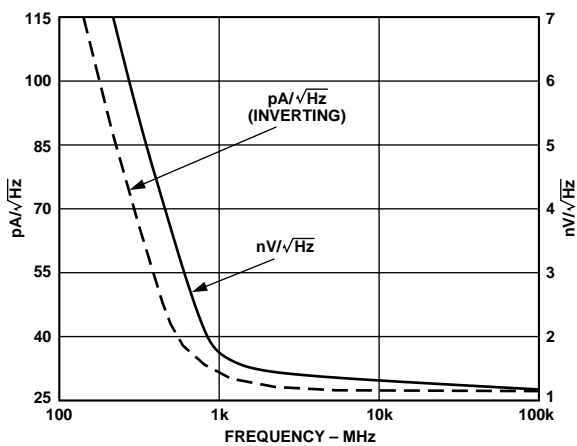


Figure 9. Equivalent Input Noise

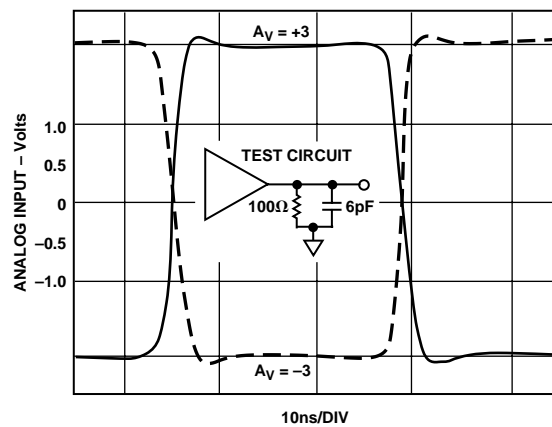


Figure 12. Small Signal Pulse Response

AD9617

AC GAIN CHARACTERISTICS

Closed-loop bandwidth at high frequencies is determined primarily by the roll-off of $T(s)$. But circuit layout is critical to minimize external parasitics which can degrade performance by causing premature peaking and/or reduced bandwidth.

The inverting and noninverting dynamic characteristics are similar. When driving the noninverting input, the inverting input capacitance (C_I) will cause the noninverting closed-loop bandwidth to be higher than the inverting bandwidth for gains less than two (2). In the remaining cases, inverting and noninverting responses are nearly identical.

For best overall dynamic performance, the value of the feedback resistor (R_F) should be 400 ohms. Although bandwidth reduces as closed-loop gain increases, the change is relatively small due to low equivalent series input impedance, Z_S . (See typical performance charts.) The simplified equations governing the device's dynamic performance are shown below.

Closed-Loop Gain vs. Frequency:
(noninverting operation)

$$\frac{V_O}{V_I} \approx \frac{1 + \frac{R_F}{R_I}}{\pi \tau \left(1 + \frac{R_S}{R_I}\right)} + 1 \quad (6)$$

where: $\tau = R_F \times C_C = 0.9 \text{ ns}$ ($R_F = 400 \Omega$)

$$\text{Slew Rate} \approx \frac{\Delta V_O}{R_F K C_C} \times e^{-\tau / R_F K C_C} \quad (7)$$

where: $K = 1 + \frac{R_S}{R_I}$

Increasing Bandwidth at Low Gains

By reducing R_F , wider bandwidth and faster pulse response can be attained beyond the specified values, although increased overshoot, settling time and possible ac peaking may result. As a rule of thumb, overshoot and bandwidth will increase by 1% and 8%, respectively, for a 5% reduction in R_F at gains of ± 10 . Lower gains will increase these sensitivities.

Equations 6 and 7 are simplified and do not accurately model the second order (open loop) frequency response term which is the primary contributor to overshoot, peaking and nonlinear bandwidth expansion. (See Open Loop Bode Plots.) The user should exercise caution when selecting R_F values much lower than 400 Ω . Note that a feedback resistor must be used in all situations, including those in which the amplifier is used in a noninverting unity gain configuration.

Increasing Bandwidth at High Gains

Closed loop bandwidth can be extended at high closed loop gain by reducing R_F . Bandwidth reduction is a result of the feedback current being split between R_S and R_I . As the gain increases (for a given R_F), more feedback current is shunted through R_I , which reduces closed loop bandwidth (see Equation 6). To maintain

specified BW, the following equations can be used to approximate R_F and R_I for any gain from ± 1 to ± 15 .

$$R_F = 424 \pm 8 G \quad (8)$$

(+ for inverting and – for noninverting)

$$R_I \approx \frac{424 - 8 G}{G - 1} \quad (\text{noninverting}) \quad (9)$$

$$R_I \approx \frac{424 + 8 G}{G - 1} \quad (\text{inverting}) \quad (10)$$

$G = \text{Closed Loop Gain.}$

Bandwidth Reduction

The closed loop bandwidth can be reduced by increasing R_F . Equations 6 and 7 can be used to determine the closed loop bandwidth for any value R_F . Do not connect a feedback capacitor across R_F , as this will degrade dynamic performance and possibly induce oscillation.

DC Precision and Noise

Output offset voltage results from both input bias currents and input offset voltage. These input errors are multiplied by the noise gain term $(1 + R_F/R_I)$ and algebraically summed at the output as shown below.

$$V_O = V_{IO} \times \left(1 + \frac{R_F}{R_I}\right) \pm I_{Bn} \times R_N \times \left(1 + \frac{R_F}{R_I}\right) \pm I_{Bi} \times R_F \quad (11)$$

Since the inputs are asymmetrical, I_{Bi} and I_{Bn} do not correlate. Canceling their output effects by making $R_N = R_F \parallel R_I$ will not reduce output offset errors, as it would for voltage feedback amplifiers. Typically, I_{Bn} is 5 μA and V_{IO} is +0.5 mV (1 sigma = 0.3 mV), which means that the dc output error can be reduced by making $R_N \approx 100 \Omega$. Note that the offset drift will not change significantly because the I_{Bn} TC is relatively small. (See specification table.)

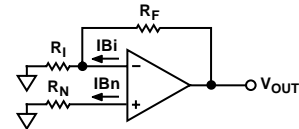


Figure 15. Output Offset Voltage

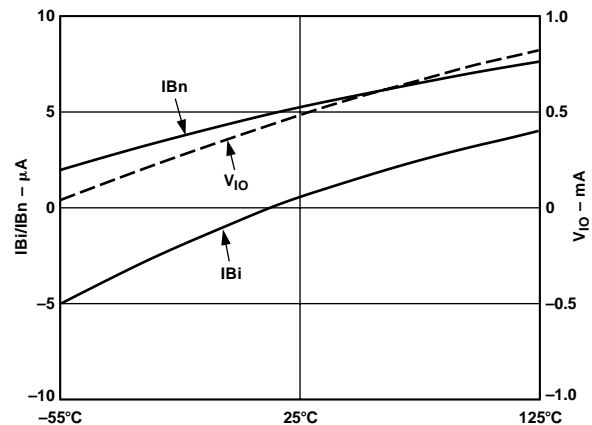


Figure 16. DC Accuracy

The effective noise at the output of the amplifier can be determined by taking the root sum of the squares of Equation 11 and applying the spectral noise values found in the typical graph section. This applies to noise from the op amp only. Note that both the noise figure and equivalent input offset voltages improve as the closed loop gain is increased (by keeping R_F fixed and reducing R_I with $R_N = 0 \Omega$).

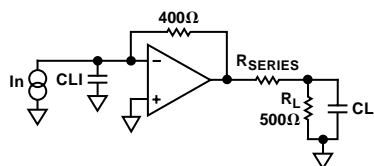


Figure 17. Capacitive Load Figure

Capacitive Load Considerations

Due to the low inverting input resistance (R_S) and output buffer design, the AD9617 can directly handle input and/or output load capacitances of up to 20 pF. See the chart below.

A small series resistor can be used at the output of the amplifier and outside of the feedback loop to facilitate driving larger capacitive loads or for obtaining faster settling time. For capacitive loads above 20 pF, R_{SERIES} should be considered.

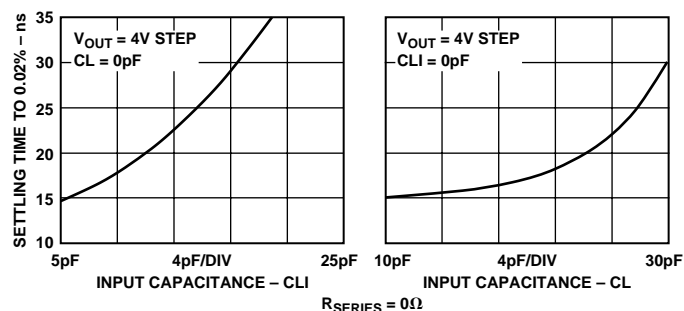


Figure 18. Input/Output Capacitance Comparisons

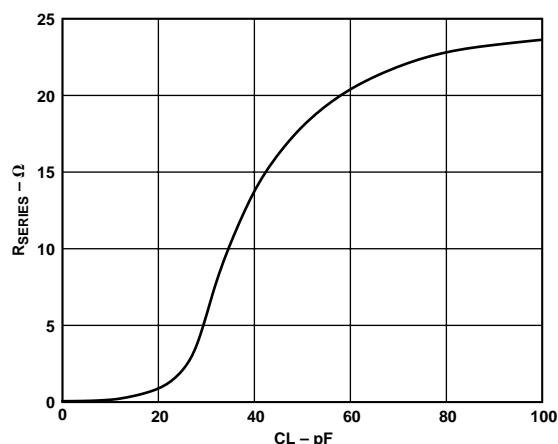


Figure 19. Recommended R_{SERIES} vs. CL

APPLYING THE AD9617

The superior frequency and time domain specifications of the AD9617 make it an obvious choice for driving flash converters and buffering the outputs of high speed DACs. Its outstanding distortion and noise performance make it well suited as a driver for analog to digital converters (ADCs) with resolutions as high as 16 bits.

Typical circuits for inverting and noninverting applications are shown in Figures 20 and 21.

Closed-loop gain for noninverting configurations is determined by the value of R_I according to the equation:

$$G = 1 + \frac{R_F}{R_I} \quad (12)$$

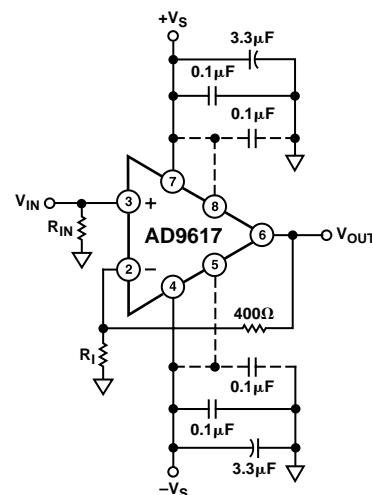


Figure 20. Noninverting Operation

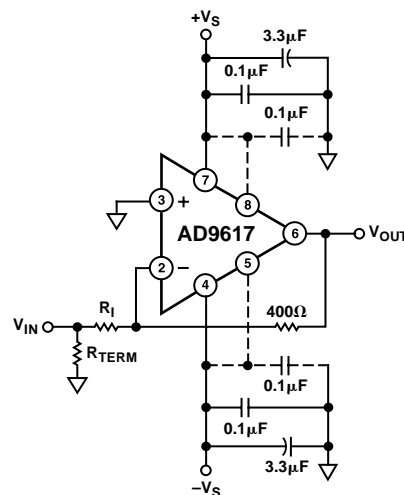


Figure 21. Inverting Operation

AD9617

LAYOUT CONSIDERATIONS

As with all high performance amplifiers, printed circuit layout is critical in obtaining optimum results with the AD9617. The ground plane in the area of the amplifier should cover as much of the component side of the board as possible. Each power supply trace should be decoupled close to the package with at least a 3.3 μ F tantalum and a low inductance, 0.1 μ F ceramic capacitor.

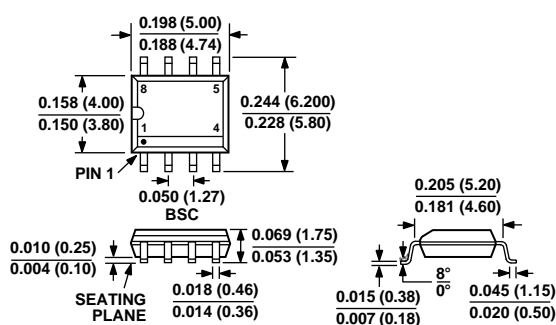
All lead lengths for input, output and the feedback resistor should be kept as short as possible. All gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave resistors and/or carbon resistors.

Stripline techniques should be used for lead lengths in excess of one inch. Sockets should be avoided if possible because of their stray inductance and capacitance.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Small Outline Package (SO-8)



Plastic DIP (N-8)

