8-BIT PROGRAMMABLE PULSE GENERATOR (SERIES PPG38F)



PACKAGES

FEATURES

- Digitally programmable in 256 steps
- Monotonic pulse-width-vs-address variation
- · Rising edge triggered
- Two separate outputs: inverting & non-inverting
- Precise and stable pulse width
- Input & outputs fully TTL interfaced & buffered
- 10 T²L fan-out capability
- Fits standard 40-pin DIP socket
- Auto-insertable

TRIG 1 N/C 🗆 2 39 OUT/ оит 🗆 з 38 N/C GND □4 37 N/C N/C 🗆 5 36□ VCC N/C □6 35 A0 RES □7 34 A1 GND 🗆 8 33 A2 N/C 🗆 9 32 VCC N/C 🗖 10 31 A3 N/C 🗆 11 30 A4 GND 🗆 12 29 A5 N/C 🗆 13 28 VCC N/C | 14 27 N/C N/C | 15 26 N/C GND 🗆 16 25 VCC A7 🗖 17 24 N/C N/C | 18 23 A6 N/C | 19 22 N/C GND 20 21 N/C

PPG38F-xx DIP PPG38F-xxC5 Gull-Wing PPG38F-xxM Military DIP PPG38F-xxMC5 Military Gull-Wing

FUNCTIONAL DESCRIPTION

The PPG38F-series device is a 8-bit digitally programmable pulse generator. The width, PW_A, depends on the address code (A7-A0) according to the following formula:

$$PW_A = PW_0 + T_{INC} * A$$

where A is the address code, T_{INC} is the incremental pulse width of the device, and PW_0 is the inherent pulse width of the device. The

PIN DESCRIPTIONS

TRIG Trigger Input
OUT Non-inverted Output
OUT/ Inverted Output
A0-A7 Address Bits
RES Reset

VCC +5 Volts GND Ground

incremental width is specified by the dash number of the device and can range from 0.5ns through 400ns, inclusively. RESET is held LOW during normal operation. When it is brought HIGH, OUT and OUT/ are forced into LOW and HIGH states, respectively, and the unit is ready for the next trigger input. The address is not latched and must remain asserted while the output pulse is active.

SERIES SPECIFICATIONS

 Programmed pulse width tolerance: 5% or 2ns, whichever is greater

Inherent width (PW₀): 20ns typical
 Inherent delay (T_{TO}): 10ns ± 2ns
 Operating temperature: 0° to 70° C
 Supply voltage V_{CC}: 5VDC ± 5%
 Supply current: I_{CC} = 80ma typical

DASH NUMBER SPECIFICATIONS

| Part Number | Incremental Width Per Step (ns) | Total Width Change (ns) | | |
|----------------|------------------------------------|----------------------------|--|--|
| PPG38F5 | .5 ± .3 | 127.5 ± 6.4 | | |
| PPG38F-1 | 1 ± .5 | 255 ± 12.8 | | |
| PPG38F-2 | 2 ± .5 | 510 ± 25.5 | | |
| PPG38F-5 | 5 ± 1.5 | $1,275 \pm 63.8$ | | |
| PPG38F-10 | 10 ± 2.0 | $2,550 \pm 127.5$ | | |
| PPG38F-20 | 20 ± 2.0 | $5,100 \pm 255.0$ | | |
| PPG38F-50 | 50 ± 2.5 | $12,750 \pm 637.5$ | | |
| PPG38F-100 | 100 ± 5.0 | $25,500 \pm 1275$ | | |
| PPG38F-200 | 200 ± 10.0 | $51,000 \pm 2550$ | | |
| PPG38F-400 | 400 ± 20.0 | 102,000 ± 5100 | | |

NOTE: Any dash number between .5 and 400 not shown is also available.

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APPLICATION NOTES

DEVICE TIMING

The timing definitions and restrictions for the PPG38F are shown in Figure 1. The unit is activated by a rising edge on the TRIG input. After a time, T_{TO} (called the inherent delay), the rising edge of the pulse appears at OUT. The duration of the pulse is given by the above equation. For the duration of the pulse, the device ignores subsequent triggers. Once the falling edge of the pulse has appeared at OUT, an additional time, T_{OTR} , is required before the device can respond to the next trigger.

At power-up, the state of the PPG38F is unknown. Consequently, after power is applied, the unit may not respond to input triggers for a time equal to the maximum pulse width, PW_T . After this time, the unit will function properly. If your application requires that the device function immediately, issue a quick reset at power-up.

POWER SUPPLY BYPASSING

The PPG38F relies on a stable power supply to produce repeatable pulses within the stated tolerances. A 0.1uf capacitor from VCC to GND, located as close as possible to each VCC pin, is recommended. A wide VCC trace should connect all VCC pins externally, and a clean ground plane should be used.

INCREMENT TOLERANCES

Please note that the increment tolerances listed represent a design goal. Although most increments will fall within tolerance, they are not guaranteed throughout the address range of the unit. Monotonicity is, however, guaranteed over all addresses.

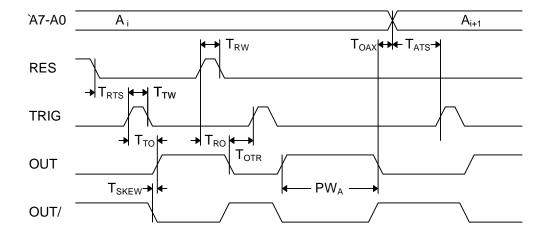


Figure 1: Timing Diagram

DEVICE SPECIFICATIONS

TABLE 1: AC CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---------------------------------|-------------------|------|------|------|------------------|
| Total Programmable Pulse Width | PW_T | | 255 | | T _{INC} |
| Inherent Pulse Width | PW_0 | 15.0 | 20.0 | 27.0 | ns |
| Trigger to Output Delay | T _{TO} | 8.0 | 10.0 | 12.0 | ns |
| Reset to Output Delay | T_{RO} | | | 17.0 | ns |
| Output Skew | T _{SKEW} | | 1.5 | | ns |
| Trigger Pulse Width | T_TW | 5.0 | | | ns |
| Reset Pulse Width | T_RW | 10.0 | | | ns |
| Reset to Trigger Setup Time | T _{RTS} | 9.0 | | | ns |
| Address to Trigger Setup Time | T _{ATS} | 6.0 | | | ns |
| Output Low to Address Change | T _{OAX} | 0.0 | | | ns |
| Output to Trigger Recovery Time | T _{OTR} | 10.0 | | | ns |

TABLE 2: ABSOLUTE MAXIMUM RATINGS

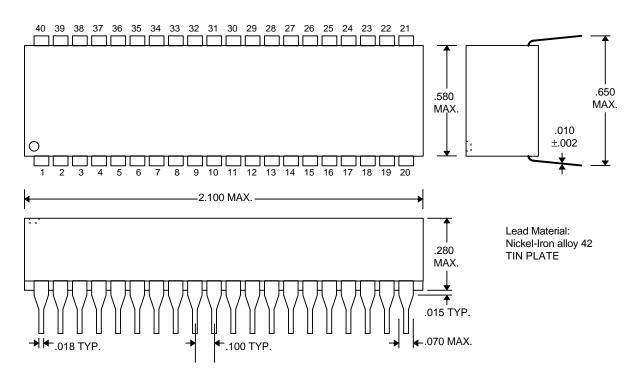
| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---------------------|------------|------|----------------------|-------|--------|
| DC Supply Voltage | V_{CC} | -0.3 | 7.0 | V | |
| Input Pin Voltage | V_{IN} | -0.3 | V _{DD} +0.3 | V | |
| Storage Temperature | T_{STRG} | -55 | 150 | С | |
| Lead Temperature | T_{LEAD} | | 300 | С | 10 sec |

TABLE 3: DC ELECTRICAL CHARACTERISTICS

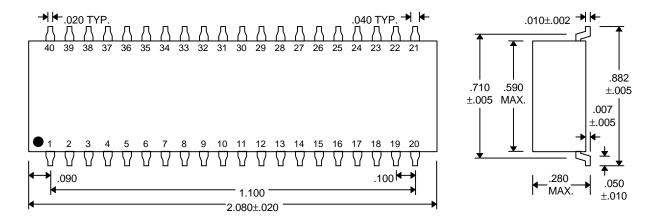
(0C to 70C, 4.75V to 5.25V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|------------------------------|------------------|-----|------|------|-------|------------------------------|
| High Level Output Voltage | V_{OH} | 2.5 | 3.4 | | V | $V_{CC} = MIN, I_{OH} = MAX$ |
| | | | | | | $V_{IH} = MIN, V_{IL} = MAX$ |
| Low Level Output Voltage | V_{OL} | | 0.35 | 0.5 | V | $V_{CC} = MIN, I_{OL} = MAX$ |
| | | | | | | $V_{IH} = MIN, V_{IL} = MAX$ |
| High Level Output Current | I _{OH} | | | -1.0 | mΑ | |
| Low Level Output Current | I_{OL} | | | 20.0 | mΑ | |
| High Level Input Voltage | V_{IH} | 2.0 | | | V | |
| Low Level Input Voltage | V_{IL} | | | 8.0 | V | |
| Input Clamp Voltage | V_{IK} | | | -1.2 | V | $V_{CC} = MIN, I_I = I_{IK}$ |
| Input Current at Maximum | I _{IHH} | | | 0.1 | mΑ | $V_{CC} = MAX, V_I = 7.0V$ |
| Input Voltage | | | | | | |
| High Level Input Current | I _{IH} | | | 20 | μΑ | $V_{CC} = MAX, V_I = 2.7V$ |
| Low Level Input Current | IιL | | | -0.6 | mΑ | $V_{CC} = MAX, V_I = 0.5V$ |
| Short-circuit Output Current | Ios | -60 | | -150 | mΑ | $V_{CC} = MAX$ |
| Output High Fan-out | | | | 25 | Unit | |
| Output Low Fan-out | | | | 12.5 | Load | |

PACKAGE DIMENSIONS



DIP (PPG38F-xx, PPG38F-xxM)



Gull-Wing (PPG38F-xxC5, PPG38F-xxMC5)

DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT: OUTPUT:

Ambient Temperature: $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$ **Load:** 1 FAST-TTL Gate

Supply Voltage (Vcc): $5.0V \pm 0.1V$ C_{load}: $5pf \pm 10\%$

Input Pulse: High = $3.0V \pm 0.1V$ Threshold: 1.5V (Rising & Falling)

 $\label{eq:Low} \begin{array}{ll} \text{Low} = 0.0 \text{V} \pm 0.1 \text{V} \\ \text{Source Impedance:} & 50\Omega \text{ Max.} \end{array}$

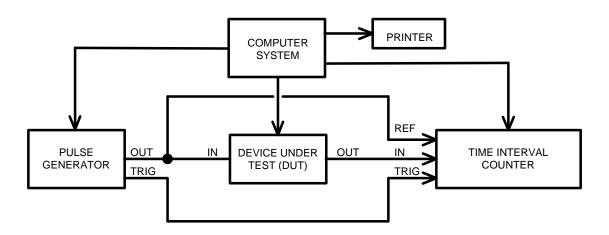
Rise/Fall Time: 3.0 ns Max. (measured

between 0.6V and 2.4V)

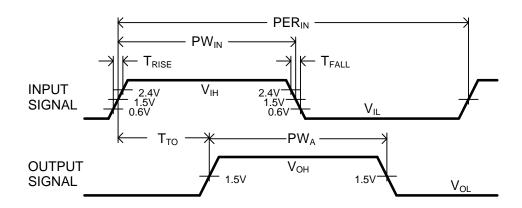
Pulse Width: $PW_{IN} = 10$ ns

Period: $PER_{IN} = 2 \times Max$. Pulse Width

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Test Setup



Timing Diagram For Testing