NTD80N02

Power MOSFET

24 V, 80 A, N−Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Pb−Free Packages are Available

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	24	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	±20	Vdc
Drain Current − Continuous @ T_C = 25°C − Single Pulse (t_p = 10 μs)	I_D I_{DM}	80* 200	Adc
Total Power Dissipation @ T_C = 25°C	P_D	75	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 24 Vdc, V_{GS} = 10 Vdc, I_L = 17 Apk, L = 5.0 mH, R_G = 25 Ω)	E_{AS}	733	mJ
Thermal Resistance − Junction−to−Case − Junction−to−Ambient (Note 1) − Junction−to−Ambient (Note 2)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 1.65 67 120	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 in^2).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in^2).

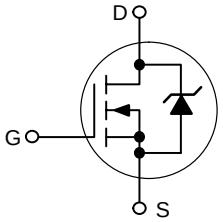
*Chip current capability limited by package.

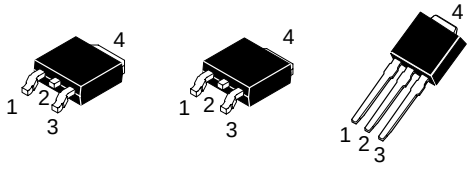
ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
24 V	5.0 mΩ	80 A

N−Channel



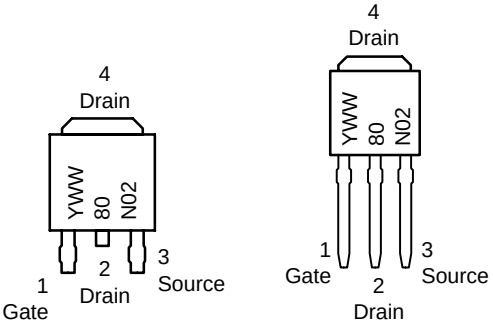


CASE 369AA DPAK (Surface Mount) STYLE 2

CASE 369C DPAK (Surface Mount) STYLE 2

CASE 369D DPAK (Straight Lead) STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENTS



Y = Year
WW = Work Week
80N02 = Device Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

© Semiconductor Components Industries, LLC, 2004

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			24	27	−	
Positive Temperature Coefficient			−	25	−	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{GS} = 0 Vdc, V_{DS} = 24 Vdc)			−	−	1.0	
(V_{GS} = 0 Vdc, V_{DS} = 24 Vdc, T_J = 125°C)			−	−	10	
Gate−Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	−	−	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			1.0	1.9	3.0	
Negative Threshold Temperature Coefficient			−	−3.8	−	mV/°C
Static Drain−to−Source On−Resistance (Note 3)		$R_{DS(on)}$				mΩ
(V_{GS} = 10 Vdc, I_D = 80 Adc)			−	5.0	5.8	
(V_{GS} = 4.5 Vdc, I_D = 40 Adc)			−	7.5	9.0	
(V_{GS} = 10 Vdc, I_D = 20 Adc)			−	5.0	5.8	
(V_{GS} = 4.5 Vdc, I_D = 20 Adc)				7.5	9.0	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 10 Adc) (Note 3)		g_{FS}	−	20	−	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 20 Vdc, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	−	2250	2600	pF
Output Capacitance		C_{oss}	−	900	1100	
Transfer Capacitance		C_{rss}	−	400	525	
SWITCHING CHARACTERISTICS (Note 4)						
Turn−On Delay Time	(V_{GS} = 4.5 Vdc, V_{DD} = 20 Vdc, I_D = 20 Adc, R_G = 2.5 Ω)	$t_{d(on)}$	−	17	30	ns
Rise Time		t_r	−	67	125	
Turn−Off Delay Time		$t_{d(off)}$	−	28	45	
Fall Time		t_f	−	40	75	
Gate Charge	(V_{GS} = 4.5 Vdc, I_D = 20 Adc, V_{DS} = 20 Vdc) (Note 3)	Q_T	−	30	42	nC
		Q1	−	7.0	12	
		Q2	−	18	28	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage		V_{SD}				Vdc
(I_S = 20 Adc, V_{GS} = 0 Vdc) (Note 3)			−	0.92	1.2	
(I_S = 40 Adc, V_{GS} = 0 Vdc)			−	1.05	−	
(I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 150°C)			−	0.70	−	
Reverse Recovery Time	(I_S = 20 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	−	38	52	ns
		t_a	−	20	−	
		t_b	−	18	−	
Reverse Recovery Stored Charge		Q_{rr}	−	0.038	−	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

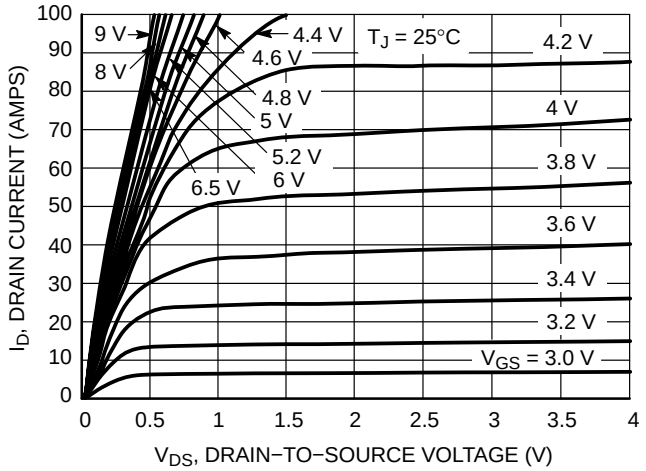


Figure 1. On−Region Characteristics

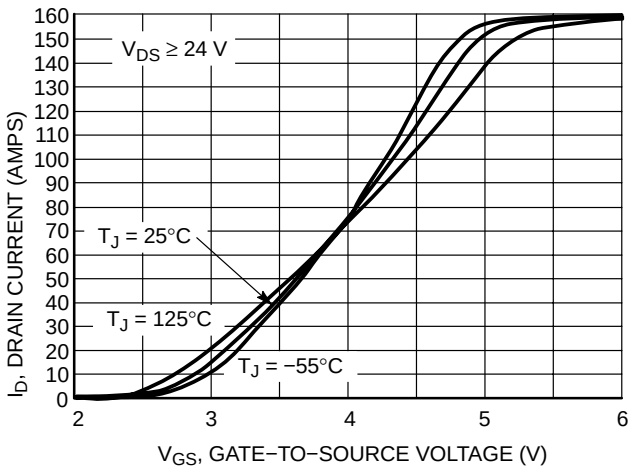


Figure 2. Transfer Characteristics

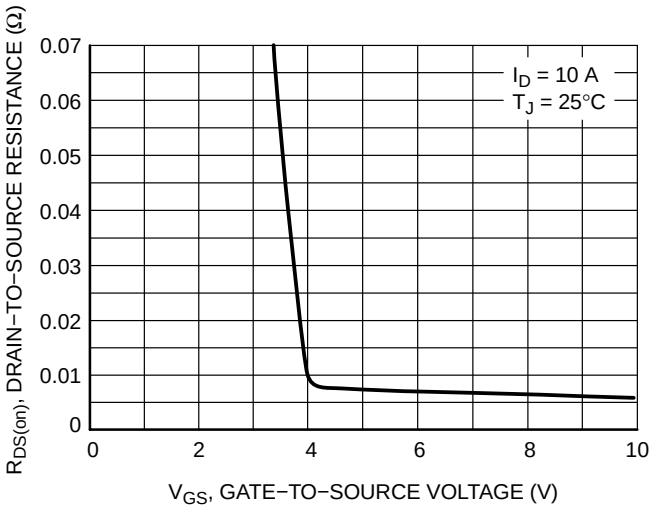


Figure 3. On−Resistance versus Gate−To−Source Voltage

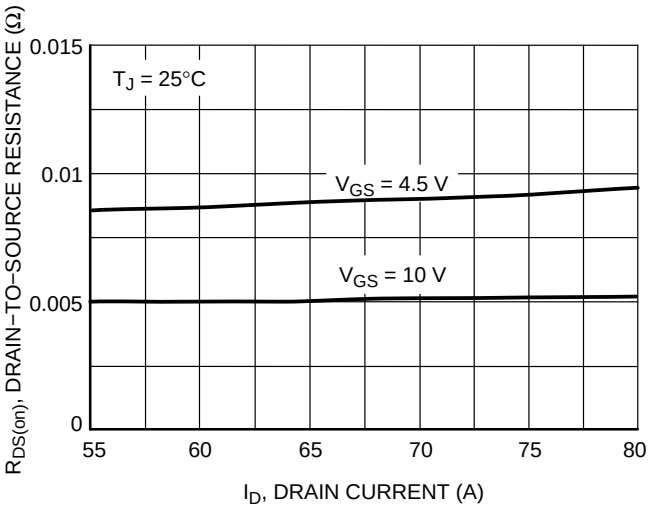


Figure 4. On−Resistance versus Drain Current and Gate Voltage

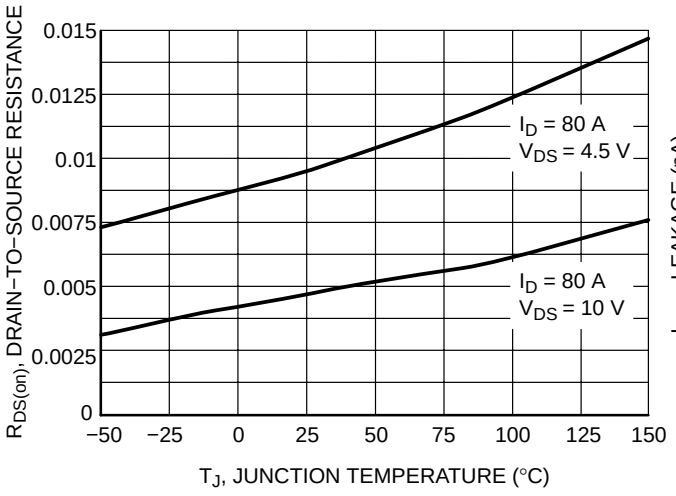


Figure 5. On−Resistance Variation with Temperature

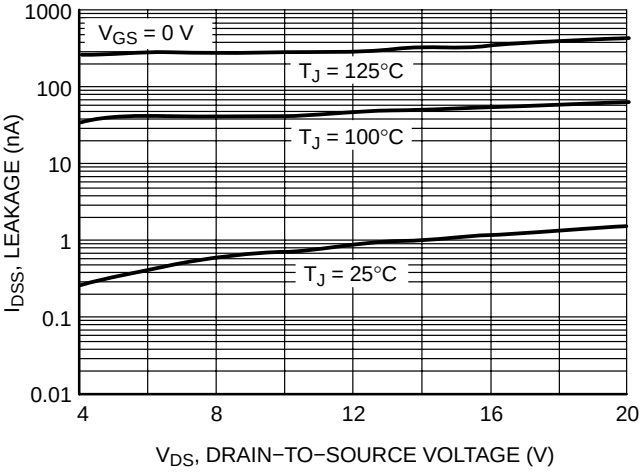


Figure 6. Drain−To−Source Leakage Current versus Voltage

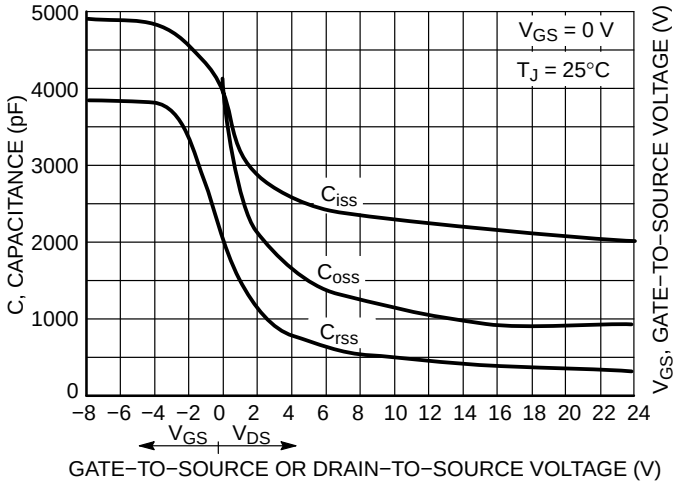


Figure 7. Capacitance Variation

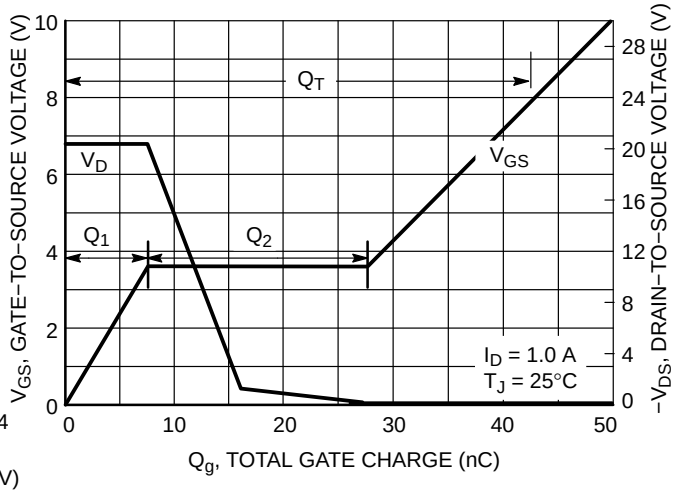


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

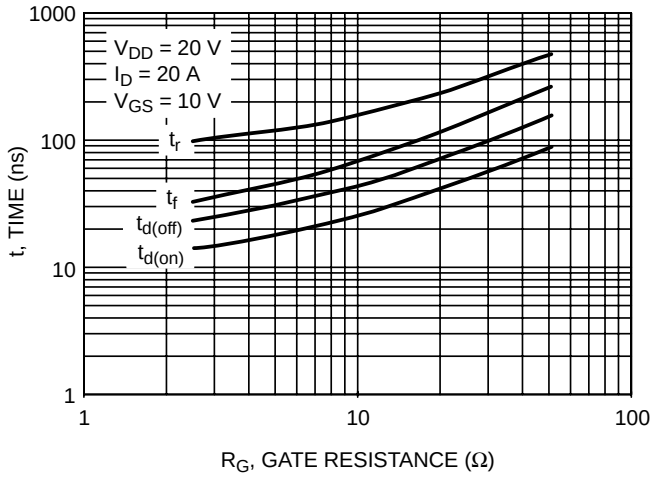


Figure 9. Resistive Switching Time Variation versus Gate Resistance

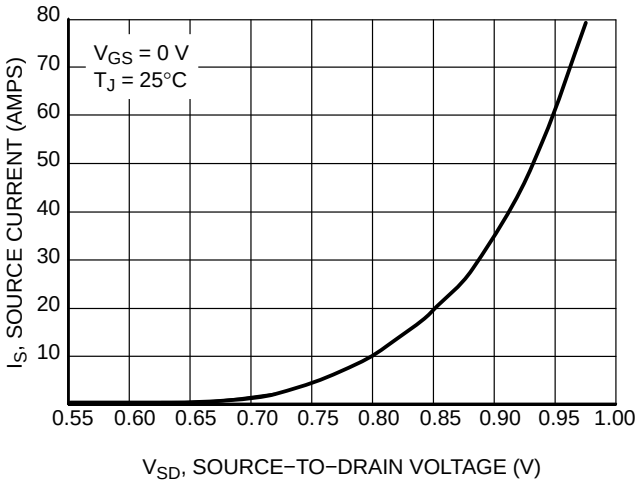


Figure 10. Diode Forward Voltage versus Current

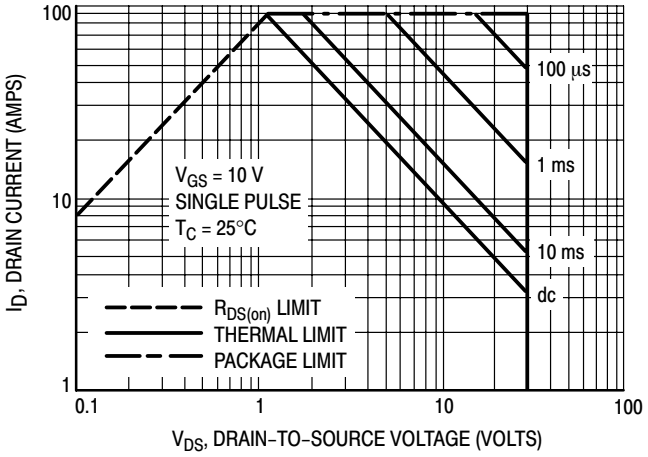


Figure 11. Maximum Rated Forward Biased Safe Operating Area

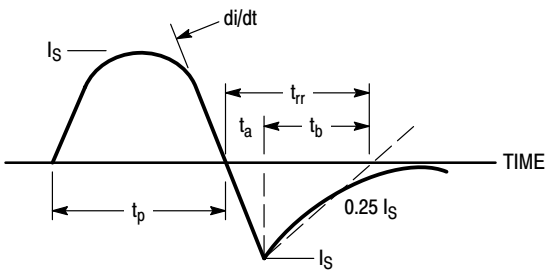


Figure 12. Diode Reverse Recovery Waveform

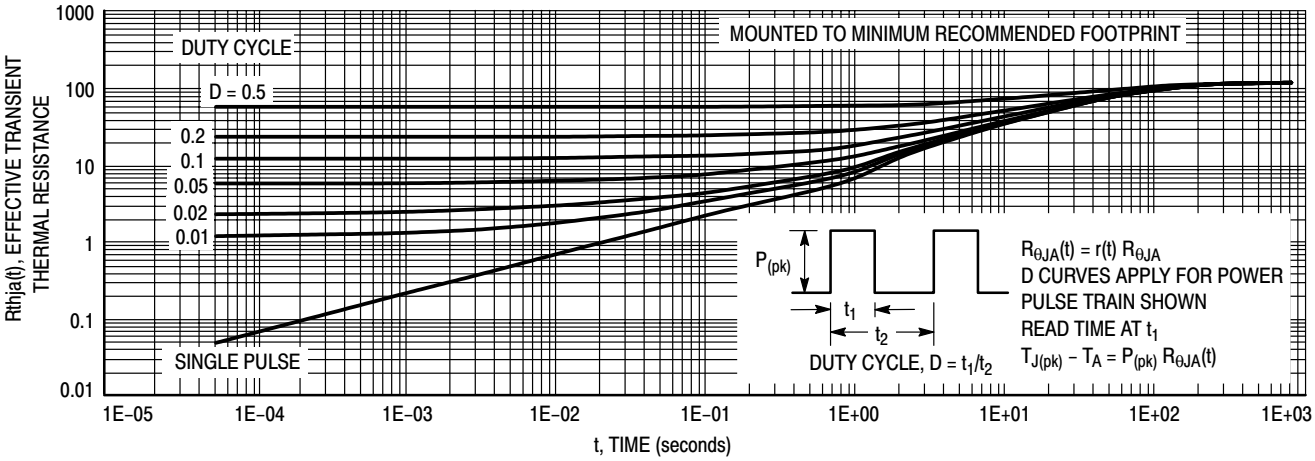


Figure 13. Thermal Response − Various Duty Cycles

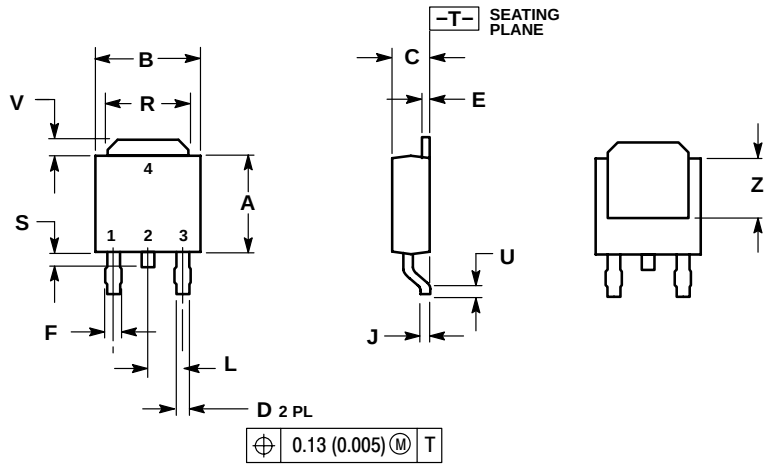
ORDERING INFORMATION

Order Number	Package	Shipping†
NTD80N02	DPAK−3	75 Units / Rail
NTD80N02G	DPAK−3 (Pb−Free)	75 Units / Rail
NTD80N02T4	DPAK−3	2500 / Tape & Reel
NTD80N02T4G	DPAK−3 (Pb−Free)	2500 / Tape & Reel
NTD80N02−001	DPAK−3 Straight Lead	75 Units / Rail
NTD80N02−1G	DPAK−3 Straight Lead (Pb−Free)	75 Units / Rail
NTD80N02−032	DPAK−3 Straight Lead (3.2 ± 0.5 mm)	75 Units / Rail
NTD80N02−032G	DPAK−3 Straight Lead (3.2 ± 0.5 mm) (Pb−Free)	75 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DPAK
CASE 369AA−01
ISSUE O

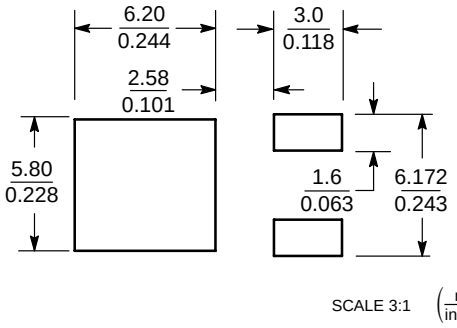


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.88
E	0.018	0.024	0.46	0.61
F	0.033	0.045	0.83	1.14
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*

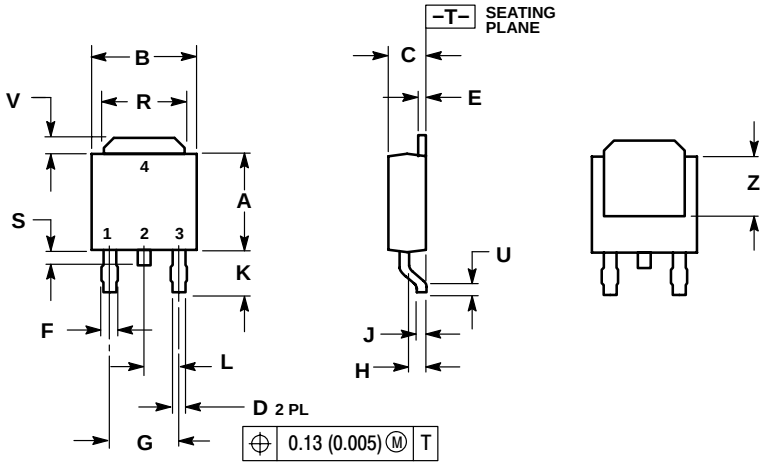


SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

DPAK
CASE 369C−01
ISSUE O

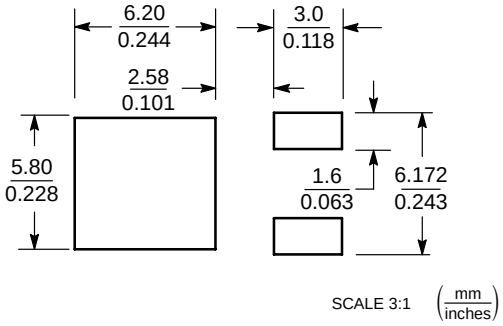


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

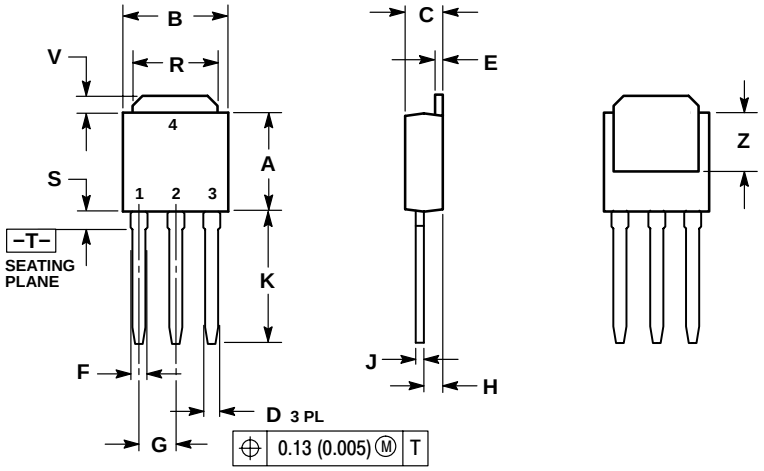
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

DPAK
CASE 369D−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.

NTD80N02/D