ANALOG DEVICES

4-Channel, 1.5 MSPS, 12-Bit and 10-Bit Parallel ADCs with a Sequencer

AD7933/AD7934

FEATURES

Fast throughput rate: 1.5 MSPS
Specified for V_{DD} of 2.7 V to 5.25 V
Low power
    8 mW max at 1.5 MSPS with 3 V supplies
    16 mW max at 1.5 MSPS with 5 V supplies
4 analog input channels with a sequencer
Software configurable analog inputs
    4-channel single-ended inputs
    2-channel fully differential inputs
    2-channel pseudo-differential inputs
Accurate on-chip 2.5 V reference
Wide input bandwidth
    70 dB SNR at 50 kHz input frequency
No pipeline delays
High speed parallel interface—word/byte modes
Full shutdown mode: 1 μA max
28 lead TSSOP package
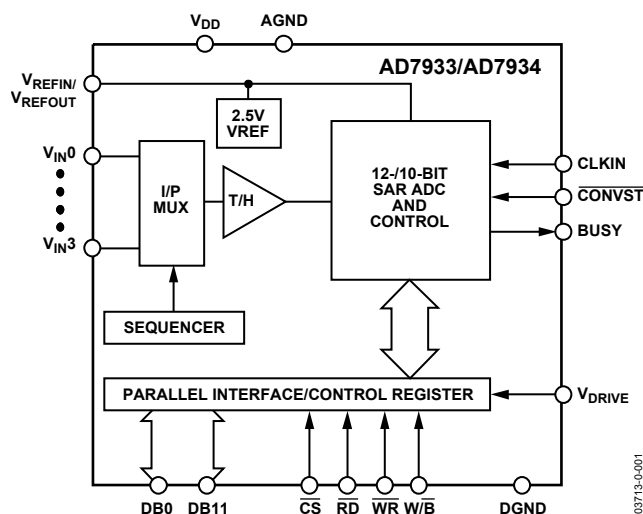
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

GENERAL DESCRIPTION

The AD7933/AD7934 are 12-bit and 10-bit, high speed, low power, successive approximation (SAR) ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates to 1.5 MSPS. The parts contain a low noise, wide bandwidth, differential track-and-hold amplifier that can handle input frequencies up to 20 MHz.

The AD7933/AD7934 feature 4 analog input channels with a channel sequencer to allow a consecutive sequence of channels to be converted on. These parts can accept either single-ended, fully differential, or pseudo-differential analog inputs.

The conversion process and data acquisition are controlled using standard control inputs, which allows for easy interfacing to microprocessors and DSPs. The input signal is sampled on the falling edge of $\overline{CONVST}$ and the conversion is also initiated at this point.

The AD7933/AD7934 has an accurate on-chip 2.5 V reference that can be used as the reference source for the analog-to-digital conversion. Alternatively, this pin can be overdriven to provide an external reference.

These parts use advanced design techniques to achieve very low power dissipation at high throughput rates. They also feature flexible power management options. An on-chip control register allows the user to set up different operating conditions, including analog input range and configuration, output coding, power management, and channel sequencing.

PRODUCT HIGHLIGHTS

1. High throughput with low power consumption.
2. Four analog inputs with a channel sequencer.
3. Accurate on-chip 2.5 V reference.
4. Software configurable analog inputs. Single-ended, pseudo-differential, or fully differential analog inputs that are software selectable.
5. Single-supply operation with V_{DRIVE} function. The V_{DRIVE} function allows the parallel interface to connect directly to 3 V, or 5 V processor systems independent of V_{DD}.
6. No pipeline delay.
7. Accurate control of the sampling instant via a $\overline{CONVST}$ input and once off conversion control.

TABLE OF CONTENTS

REVISION HISTORY

8/04—Revision PrG: Preliminary Version

AD7933—SPECIFICATIONS

$V_{DD} = V_{DRIVE} = 2.7$ V to 5.25 V, Internal/External $V_{REF} = 2.5$ V, unless otherwise noted, $F_{CLKIN} = 24$ MHz, $F_{SAMPLE} = 1.5$ MSPS; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			$F_{IN} = 50$ kHz sine wave
Signal-to-Noise + Distortion (SINAD)[2]	60	dB min	
Signal-to-Noise Ratio (SNR)[2]	60	dB min	
Total Harmonic Distortion (THD)[2]	−73	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	−73	dB max	
Intermodulation Distortion (IMD)[2]			fa = 40.1 kHz, fb = 51.5 kHz
Second-Order Terms	−75	dB typ	
Third-Order Terms	−75	dB typ	
Channel-to-Channel Isolation	−75	dB typ	
Aperture Delay[2]	5	ns typ	
Aperture Jitter[2]	50	ps typ	
Full Power Bandwidth[2, 3]	20	MHz typ	@ 3 dB
	2.5	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity[2]	±0.5	LSB max	
Differential Nonlinearity[2]	±0.5	LSB max	Guaranteed no missed codes to 10 bits
Total Unadjusted Error	TBD	LSB max	
Single-Ended and Pseudo Differential Input			Straight binary output coding
Offset Error[2]	±4.5	LSB max	
Offset Error Match[2]	±0.5	LSB max	
Gain Error[2]	±2	LSB max	
Gain Error Match[2]	±0.6	LSB max	
Fully Differential Input			Twos complement output coding offset
Positive Gain Error[2]	±2	LSB max	
Positive Gain Error Match[2]	±0.6	LSB max	
Zero-Code Error[2]	±3	LSB max	
Zero-Code Error Match[2]	±1	LSB max	
Negative Gain Error[2]	±2	LSB max	
Negative Gain Error Match[2]	±0.6	LSB max	
ANALOG INPUT			
Single-Ended Input Range	0 to V_{REF} or 0 to $2 \times V_{REF}$	V	Depending on RANGE bit setting
Pseudo-Differential Input Range: V_{IN+}	0 to V_{REF} or $2 \times V_{REF}$	V	Depending on RANGE bit setting
V_{IN-}	−0.1 to +0.4	V	
Fully Differential Input Range: V_{IN+} and V_{IN-}	$V_{CM} \pm V_{REF}/2$	V	V_{CM} = common-mode voltage[4] = $V_{REF}/2$
V_{IN+} and V_{IN-}	$V_{CM} \pm V_{REF}$	V	$V_{CM} = V_{REF}$, V_{IN+} or V_{IN-} must remain within GND/V_{DD}
DC Leakage Current[5]	±1	µA max	
Input Capacitance	45	pF typ	When in track
	10	pF typ	When in hold
REFERENCE INPUT/OUTPUT			
V_{REF} Input Voltage[6]	2.5	V	±1% specified performance
DC Leakage Current[5]	±1	µA max	
V_{REF} Input Impedance	10	kΩ	
V_{REFOUT} Output Voltage	2.5	V	±0.1% @ 25°C
V_{REFOUT} Temperature Coefficient	15	ppm/°C typ	
V_{REF} Noise	10	µV typ	0.1 Hz to 10 Hz bandwidth
	130	µV typ	0.1 Hz to 1 MHz bandwidth

Parameter	B Version[1]	Unit	Test Conditions/Comments
V$_{REF}$ Output Impedance	10	Ω typ	
V$_{REF}$ Input Capacitance	15	pF typ	When in track
	25	pF typ	When in hold
LOGIC INPUTS			
Input High Voltage, V$_{INH}$	2.4	V min	
Input Low Voltage, V$_{INL}$	0.8	V max	
Input Current, I$_{IN}$	±1	µA max	Typically 10 nA, V$_{IN}$ = 0 V or V$_{DRIVE}$
Input Capacitance, C$_{IN}$[5]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V$_{OH}$	2.4	V min	I$_{SOURCE}$ = 200 µA;
Output Low Voltage, V$_{OL}$	0.4	V max	I$_{SINK}$ = 200 µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[5]	10	pF max	
Output Coding	Straight (Natural) Binary		CODING bit = 0
	Twos Complement		CODING bit = 1
CONVERSION RATE			
Conversion Time	t$_2$ + 13 $_{tclk}$ + t$_{20}$	ns	
Track-and-Hold Acquisition Time	135	ns max	Full scale step input
Throughput Rate	1.5	MSPS max	
POWER REQUIREMENTS			
V$_{DD}$	2.7/5.25	V min/max	
V$_{DRIVE}$	2.7 /5.25	V min/max	
I$_{DD}$[7]			Digital I/Ps = 0 V or V$_{DRIVE}$
Normal Mode(Static)	0.5	mA typ	V$_{DD}$ = 2.7 V to 5.25 V, SCLK on or off
Normal Mode (Operational)	3.2	mA max	V$_{DD}$ = 4.75 V to 5.25 V
	2.6	mA max	V$_{DD}$ = 2.7 V to 3.6 V
Auto StandBy Mode	1.55	mA typ	F$_{SAMPLE}$ = 250 kSPS
	90	µA max	(Static)
Auto Shutdown Mode	1	mA typ	F$_{SAMPLE}$ = 250 kSPS
	1	µA max	(Static)
Full Shutdown Mode	1	µA max	SCLK on or off
Power Dissipation			
Normal Mode (Operational)	16	mW max	V$_{DD}$ = 5 V
	8	mW max	V$_{DD}$ = 3 V
Auto Standby Mode (Static)	450	µW max	V$_{DD}$ = 5 V
	270	µW max	V$_{DD}$ = 3 V
Auto Shutdown Mode (Static)	5	µW max	V$_{DD}$ = 5 V
	3	µW max	V$_{DD}$ = 3 V
Full Shutdown Mode	5	µW max	V$_{DD}$ = 5 V
	3	µW max	V$_{DD}$ = 3 V

---

[1] Temperature range is as follows: B Versions: −40°C to +85°C.

[2] See Terminology section.

[3] Analog inputs with slew rates exceeding 27 V/µs (full-scale input sine wave >3.5 MHz) within the acquisition time may cause an incorrect conversion result to be returned by the converter.

[4] For full common-mode range see

[5] Sample tested during initial release to ensure compliance.

[6] This device is operational with an external reference in the range 0.1 V to 3.5 V differential mode and 0.1 V to V$_{DD}$ in pseudo-differential and single-ended modes.

[7] Measured with a midscale dc input.

AD7934—SPECIFICATIONS

$V_{DD} = V_{DRIVE} = 2.7$ V to 5.25 V, Internal/External $V_{REF} = 2.5$ V, unless otherwise noted, $F_{CLKIN} = 24$ MHz, $F_{SAMPLE} = 1.5$ MSPS; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			$F_{IN} = 50$ kHz sine wave
Signal-to-Noise + Distortion (SINAD)[2]	70	dB min	
Signal-to-Noise Ratio (SNR)[2]	70	dB min	
Total Harmonic Distortion (THD)[2]	−75	dB max	−80 dB typ
Peak Harmonic or Spurious Noise (SFDR)[2]	−75	dB max	−82 dB typ
Intermodulation Distortion (IMD)[2]			fa = 40.1 kHz, fb = 51.5 kHz
Second-Order Terms	−85	dB typ	
Third-Order Terms	−85	dB typ	
Channel-to-Channel Isolation	−85	dB typ	
Aperture Delay[2]	5	ns typ	
Aperture Jitter[2]	50	ps typ	
Full Power Bandwidth[2, 3]	20	MHz typ	@ 3 dB
	2.5	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity[2]	±1	LSB max	
Differential Nonlinearity[2]	±0.95	LSB max	Guaranteed no missed codes to 12 bits
Total Unadjusted Error	TBD	LSB max	
Single-Ended and Pseudo-Differential Input			Straight binary output coding
Offset Error[2]	±4.5	LSB max	
Offset Error Match[2]	±0.5	LSB max	
Gain Error[2]	±2	LSB max	
Gain Error Match[2]	±0.6	LSB max	
Fully Differential Input			Twos complement output coding
Positive Gain Error[2]	±2	LSB max	
Positive Gain Error Match[2]	±0.6	LSB max	
Zero-Code Error[2]	±3	LSB max	
Zero-Code Error Match[2]	±1	LSB max	
Negative Gain Error[2]	±2	LSB max	
Negative Gain Error Match[2]	±0.6	LSB max	
ANALOG INPUT			
Single-Ended Input Range	0 to V_{REF} or 0 to $2 \times V_{REF}$	V	Depending on RANGE bit setting
Pseudo-Differential Input Range: V_{IN+}	0 to V_{REF} or $2 \times V_{REF}$	V	Depending on RANGE bit setting
$V_{IN−}$	−0.1 to +0.4	V	
Fully Differential Input Range: V_{IN+} and $V_{IN−}$	$V_{CM} \pm V_{REF}/2$	V	V_{CM} = common-mode voltage[4] = $V_{REF}/2$
V_{IN+} and $V_{IN−}$	$V_{CM} \pm V_{REF}$	V	$V_{CM} = V_{REF}$, V_{IN+} or $V_{IN−}$ must remain within GND/V_{DD}
DC Leakage Current[5]	±1	µA max	
Input Capacitance	45	pF typ	When in track
	10	pF typ	When in hold
REFERENCE INPUT/OUTPUT			
V_{REF} Input Voltage[6]	2.5	V	±1% specified performance
DC Leakage Current	±1	µA max	
V_{REF} Input Impedance	10	kΩ typ	
V_{REFOUT} Output Voltage	2.5	V	±0.1% @ 25℃
V_{REFOUT} Temperature Coefficient	15	ppm/℃ typ	
V_{REF} Noise	10	µV typ	0.1 Hz to 10 Hz bandwidth
	130	µV typ	0.1 Hz to 1 MHz bandwidth

Parameter	B Version[1]	Unit	Test Conditions/Comments
V_{REF} Output Impedance	10	Ω typ	
V_{REF} Input Capacitance	15	pF typ	When in track-and-hold
	25	pF typ	When in track-and-hold
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[5]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 200 µA;
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[5]	10	pF max	
Output Coding	Straight (Natural) Binary		CODING bit = 0
	Twos Complement		CODING bit = 1
CONVERSION RATE			
Conversion Time	$t_2 + 13_{tclk} + t_{20}$	ns	
Track-and-Hold Acquisition Time	135	ns max	Full scale step input
Throughput Rate	1.5	MSPS max	
POWER REQUIREMENTS			
V_{DD}	2.7/5.25	V min/max	
V_{DRIVE}	2.7 /5.25	V min/max	
I_{DD}[7]			Digital I/Ps = 0 V or V_{DRIVE}
Normal Mode(Static)	0.5	mA typ	V_{DD} = 2.7 V to 5.25 V, SCLK on or off
Normal Mode (Operational)	3.2	mA max	V_{DD} = 4.75 V to 5.25 V
	2.6	mA max	V_{DD} = 2.7 V to 3.6 V
Auto StandBy Mode	1.55	mA typ	F_{SAMPLE} = 250 kSPS
	90	µA max	(Static)
Auto Shutdown Mode	1	mA typ	F_{SAMPLE} = 250 kSPS
	1	µA max	(Static)
Full Shutdown Mode	1	µA max	SCLK on or off
Power Dissipation			
Normal Mode (Operational)	16	mW max	V_{DD} = 5 V
	8	mW max	V_{DD} = 3 V
Auto Standby Mode (Static)	450	µW max	V_{DD} = 5 V
	270	µW max	V_{DD} = 3 V
Auto Shutdown Mode (Static)	5	µW max	V_{DD} = 5 V
	3	µW max	V_{DD} = 3 V
Full Shutdown Mode	5	µW max	V_{DD} = 5 V
	3	µW max	V_{DD} = 3 V

[1] Temperature ranges is as follows: B Versions: −40°C to +85°C.

[2] See Terminology section.

[3] Analog inputs with slew rates exceeding 27 V/µs (full-scale input sine wave > 3.5 MHz) within the acquisition time may cause an incorrect result to be returned by the converter.

[4] For full common mode range see

[5] Sample tested during initial release to ensure compliance.

[6] This device is operational with an external reference in the range 0.1 V to 3.5 V in differential mode and 0.1 V to V_{DD} in pseudo-differential and single-ended modes. See the Reference Section for more information.

[7] Measured with a midscale dc input.

TIMING SPECIFICATIONS[1]

V_{DD} = V_{DRIVE} =2.7 V to 5.25 V, Internal/External V_{REF} = 2.5 V, unless otherwise noted, F_{CLKIN} = 24 MHz, F_{SAMPLE} = 1.5 MSPS; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

| Parameter | Limit at T_{MIN}, T_{MAX} | | Unit | Description |
	AD7933	AD7934		
f_{CLKIN}[2]	10	10	kHz min	
	24	24	MHz max	
t_{QUIET}	10	10	ns min	Minimum time between end of read and start of next conversion, i.e., time from when the data bus goes into three-state until the next falling edge of CONVST.
t_1	10	10	ns min	CONVST Pulse Width.
t_2	20	20	ns min	CONVST Falling Edge to CLKIN Falling Edge Setup Time.
t_3	TBD	TBD	ns min	CLKIN Falling Edge to BUSY Rising Edge.
t_4	0	0	ns min	CS to WR Setup Time.
t_5	0	0	ns min	CS to WR Hold Time.
t_6	25	25	ns min	WR Pulse Width.
t_7	10	10	ns min	Data Setup Time before WR.
t_8	5	5	ns min	Data Hold after WR.
t_9	0.5 t_{CLKIN}	0.5 t_{CLKIN}	ns min	New Data Valid before Falling Edge of BUSY.
t_{10}	0	0	ns min	CS to RD Setup Time.
t_{11}	0	0	ns min	CS to RD Hold Time.
t_{12}	55	55	ns min	RD Pulse Width.
t_{13}[3]	50	50	ns max	Data Access Time after RD.
t_{14}[4]	5	5	ns min	Bus Relinquish Time after RD.
	40	40	ns max	Bus Relinquish Time after RD.
t_{15}	15	15	ns min	HBEN to RD Setup Time.
t_{16}	5	5	ns min	HBEN to RD Hold Time.
t_{17}	10	10	ns min	Minimum Time between Reads/Writes.
t_{18}	0	0	ns min	HBEN to WR Setup Time.
t_{19}	5	5	ns min	HBEN to WR Hold Time.
t_{20}	TBD	TBD	ns min	CLKIN Falling Edge to BUSY Rising Edge.

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. All timing specifications given above are with a 25 pF load capacitance. See Figure 37. AD7933/AD7934 Parallel Interface—Conversion and Read Cycle in Word Mode (W/ = 1), Figure 38, Figure 39, and Figure 40.

[2] Mark/space ratio for CLKIN is 40/60 to 60/40.

[3] The time required for the output to cross TBD.

[4] t_{14} is derived from the measured time taken by the data outputs to change 0.5 V. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, t_{14}, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to AGND/DGND	−0.3 V to +7 V
V_{DRIVE} to AGND/DGND	−0.3 V to V_{DD} +0.3 V
Analog Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to +7 V
V_{DRIVE} to V_{DD}	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
V_{REFIN} to AGND	−0.3 V to V_{DD} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	97.9°C/W (TSSOP)
θ_{JC} Thermal Impedance	14°C/W (TSSOP)
Lead Temperature, Soldering	
Reflow Temperature (10 sec to 30 sec)	255°C
ESD	2 kV

[1] Transient currents of up to 100 mA will not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
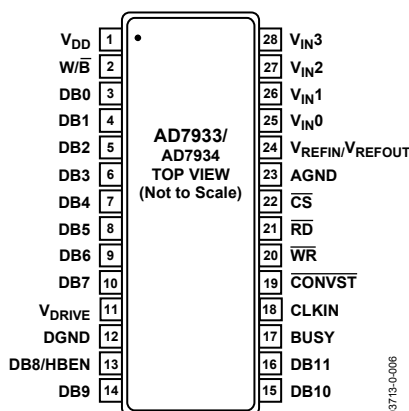
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 2. Pin Configuration

Table 5. Pin Function Description

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. The V_{DD} range for the AD7933/AD7934 is from 2.7 V to 5.25 V. The supply should be decoupled to AGND with a 0.1 µF capacitor and a 10 µF tantalum capacitor.
2	W/$\overline{B}$	Word/Byte Input. When this input is logic high, word transfer mode is enabled and data is transferred to and from the AD7933/AD7934 in 12-/10-bit words on Pins DB0/DB2 to DB11. When this pin is logic low, byte transfer mode is enabled. Data and the channel ID is transferred on Pins DB0 to DB7 and Pin DB8/HBEN assumes its HBEN functionality.
3 to 10	DB0 to DB7	Data Bits 0 to 7. Three-state parallel digital I/O pins that provide the conversion result and also allow the control register to be programmed. These pins are controlled by $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$. The logic high/low voltage levels for these pins are determined by the V_{DRIVE} input. When reading from the AD7933, the two LSBs (DB0 and DB1) are always 0 and the LSB of the conversion result is available on DB2.
11	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the parallel interface of the AD7933/AD7934 will operate. This pin should be decoupled to DGND. The voltage at this pin may be different to that at V_{DD} but should never exceed V_{DD} by more than 0.3 V.
12	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7933/AD7934. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
13	DB8/HBEN	Data Bit 8/High Byte Enable. When W/$\overline{B}$ is high, this pin acts as Data Bit 8, a three-state I/O pin that is controlled by $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$. When W/$\overline{B}$ is low, this pin acts as the high byte enable pin. When HBEN is low, the low byte of data written to or read from the AD7933/AD7934 is on DB0 to DB7. When HBEN is high, the top four bits of the data being written to or read from the AD7933/AD7934 are on DB0 to DB3 When reading from the device, DB4 of the high byte is always 0 and DB5 and DB6 will contain the ID of the channel for which the conversion result corresponds (see Channel Address Bits in Table 9). When writing to the device, DB4 to DB7 of the high byte must be all 0s. Note that when reading from the AD7933, the two LSBs in the low byte are 0s and the remaining 6 bits, conversion data.
14 to 16	DB9 to DB11	Data Bits 9 to 11. Three-state parallel digital I/O pins that provide the conversion result and also allow the control register to be programmed in word mode. These pins are controlled by $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$. The logic high/low voltage levels for these pins are determined by the V_{DRIVE} input.
17	BUSY	Busy Output. Logic output indicating the status of the conversion. The BUSY output goes high following the falling edge of $\overline{CONVST}$ and stays high for the duration of the conversion. Once the conversion is complete and the result is available in the output register, the BUSY output will go low. The track-and-hold returns to track mode just prior to the falling edge of BUSY, and the acquisition time for the part begins when BUSY goes low.
18	CLKIN	Master Clock Input. The clock source for the conversion process is applied to this pin. Conversion time for the AD7933/AD7934 takes 13.5 clock cycles. The frequency of the master clock input therefore determines the conversion time and achievable throughput rate.
19	$\overline{CONVST}$	Conversion Start Input. A falling edge on $\overline{CONVST}$ is used to initiate a conversion. The track-and-hold goes from track to hold mode on the falling edge of $\overline{CONVST}$ and the conversion process is initiated at this point. Following power-down, when operating in the auto shutdown or auto standby mode, a rising edge on $\overline{CONVST}$ is used to power up the device.

Pin No.	Mnemonic	Description
20	$\overline{WR}$	Write Input. Active low logic input used in conjunction with $\overline{CS}$ to write data to the control register.
21	$\overline{RD}$	Read Input. Active low logic input used in conjunction with $\overline{CS}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of $\overline{RD}$ read while $\overline{CS}$ is low.
22	$\overline{CS}$	Chip Select. Active low logic input used in conjunction with $\overline{RD}$ and $\overline{WR}$ to read conversion data or write data to the control register.
23	AGND	Analog Ground. This is the ground reference point for all analog circuitry on the AD7933/AD7934. All analog input signals and any external reference signal should be referred to this AGND voltage. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
24	V_{REFIN}/V_{REFOUT}	Reference Input/Output. This pin is connected to the internal reference and is the reference source for the ADC. The nominal internal reference voltage is 2.5 V and this appears at this pin. This pin can be overdriven by an external reference. The input voltage range for the external reference is 0.1 V to 3.5 V for differential mode and is 0.1 V to V_{DD} in single-ended and pseudo-differential mode, depending on V_{DD}.
25 to 28	$V_{IN}0$ to $V_{IN}3$	Analog Input 0 to Analog Input 3. Four analog input channels that are multiplexed into the on-chip track-and-hold. The analog inputs can be programmed to be four single ended inputs, two fully differential pairs or two pseudo-differential pairs by setting the MODE bits in the control register appropriately (see Table 9). The analog input channel to be converted can either be selected by writing to the address bits (ADD1 and ADD0) in the control register prior to the conversion, or the on-chip sequencer can be used. The input range for all input channels can either be 0 V to V_{REF} or 0 V to $2 \times V_{REF}$ and the coding can be binary or twos complement, depending on the states of the RANGE and CODING bits in the control register. Any unsed input channels should be connected to AGND to avoid noise pickup.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . .000) to (00 . . . 001) from the ideal, i.e., AGND + 1 LSB

Offset Error Match
This is the difference in offset error between any two channels.

Gain Error
This is the deviation of the last code transition (111 . . .110) to (111 . . . 111) from the ideal (i.e., V_{REF} − 1 LSB) after the offset error has been adjusted out.

Gain Error Match
This is the difference in gain error between any two channels.

Zero-Code Error
This applies when using the twos complement output coding option, in particular to the $2 \times V_{REF}$ input range with $−V_{REF}$ to $+V_{REF}$ biased about the V_{REFIN} point. It is the deviation of the midscale transition (all 0s to all 1s) from the ideal V_{IN} voltage, i.e., V_{REF}.

Zero-Code Error Match
This is the difference in zero-code error between any two channels.

Positive Gain Error
This applies when using the twos complement output coding option, in particular to the $2 \times V_{REF}$ input range with $−V_{REF}$ to $+V_{REF}$ biased about the V_{REFIN} point. It is the deviation of the last code transition (011. . .110) to (011 .. . 111) from the ideal (i.e., $+V_{REF}$ − 1 LSB) after the zero-code error has been adjusted out.

Positive Gain Error Match
This is the difference in positive gain error between any two channels.

Negative Gain Error
This applies when using the twos complement output coding option, in particular to the $2 \times V_{REF}$ input range with $−V_{REF}$ to $+V_{REF}$ biased about the V_{REF} point. It is the deviation of the first code transition (100 . . . 000) to (100 . . . 001) from the ideal (i.e., $−V_{REFIN}$ + 1 LSB) after the zero-code error has been adjusted out.

Negative Gain Error Match
This is the difference in negative gain error between any two channels.

Channel-to-Channel Isolation
It is a measure of the level of crosstalk between channels. It is measured by applying a full-scale sine wave signal to the three nonselected input channels and applying a 50 kHz signal to the selected channel. The channel-to-channel isolation is defined as the ratio of the power of the 50 kHz signal on the selected channel to the power of the noise signal that appears in the FFT of this channel.

Power Supply Rejection Ratio (PSRR)
It is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the ADC V_{DD} supply of frequency f_S. The frequency of the input varies from 1 kHz to 1 MHz.

$$PSRR \text{ (dB)} = 10\log(Pf/Pf_S)$$

Pf is the power at frequency f in the ADC output; Pf_S is the power at frequency f_S in the ADC output.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns into track mode and the end of conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal-to-(Noise + Distortion) Ratio (SINAD)
This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\,N + 1.76) \text{ dB}$$

Thus, for a 12-bit converter, this is 74 dB, and for a 10-bit converter, this is 62 dB.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7933/AD7934, it is defined as

$$THD(\text{dB}) = -20\log\frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + V_5{}^2 + V_6{}^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa – fb), while the third-order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7933/AD7934 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

TBD

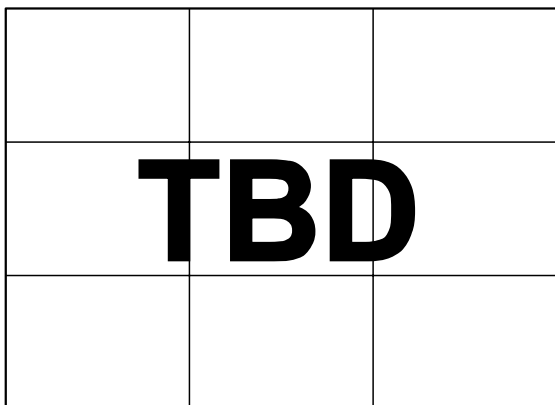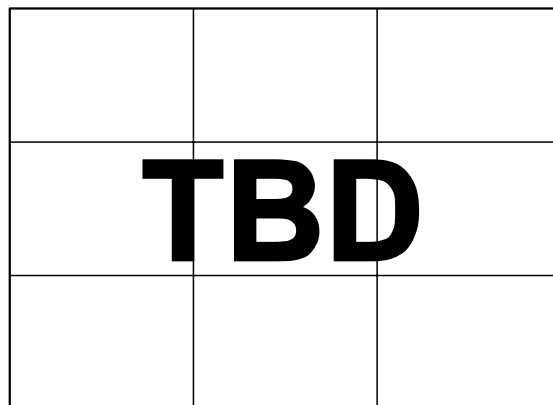Figure 3. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

TBD

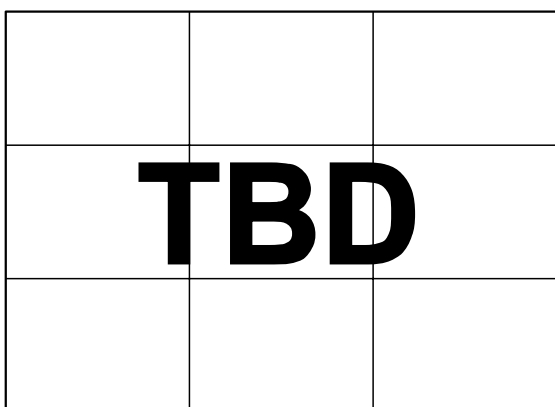Figure 6. AD7934 FFT @ V_{DD} = 5 V

TBD

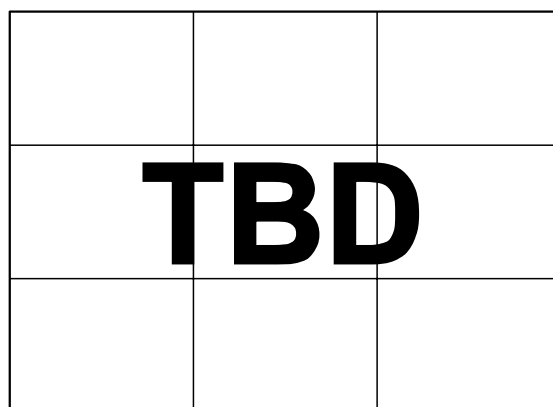Figure 4. Channel-to-Channel Isolation

TBD

Figure 7. AD7934 Typical DNL @ V_{DD} = 5 V
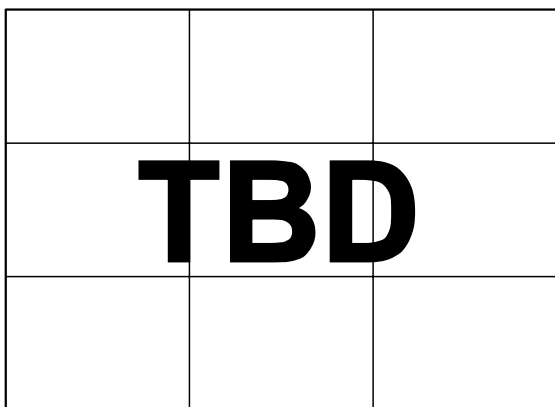
TBD

Figure 5. AD7934 SINAD vs. Analog Input Frequency for Various Supply Voltages

TBD
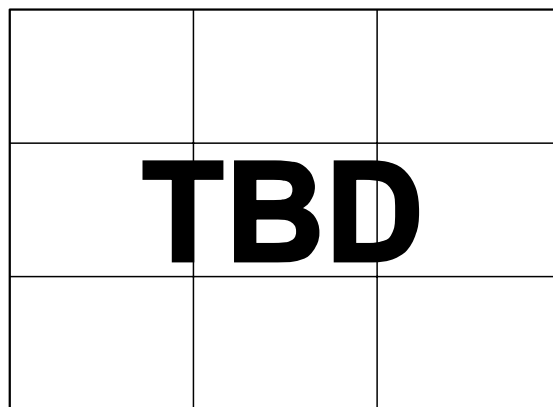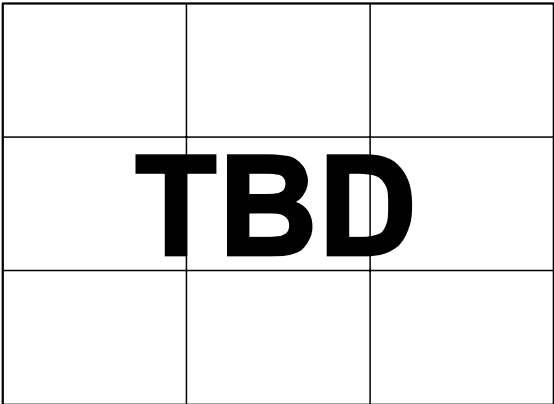
Figure 8. AD7934 Typical INL @ V_{DD} = 5 V

Figure 9. AD7934 Change in INL vs. V_{REF} for V_{DD} = 5 V
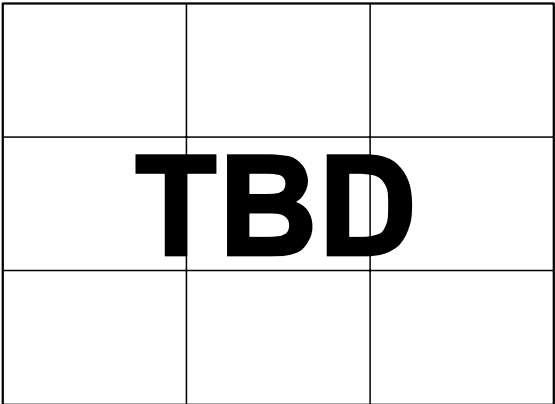
Figure 12. AD7934 Offset vs. V_{REF}

Figure 10.AD7934 Change in DNL vs. V_{REF} for V_{DD} = 5 V

Figure 13. AD7934 Histogram of Codes @ V_{DD} = 5 V with the Internal Reference

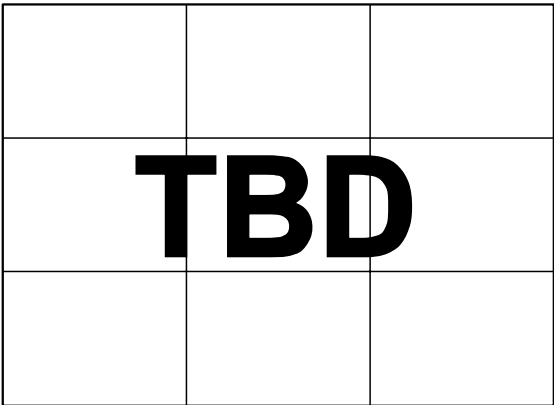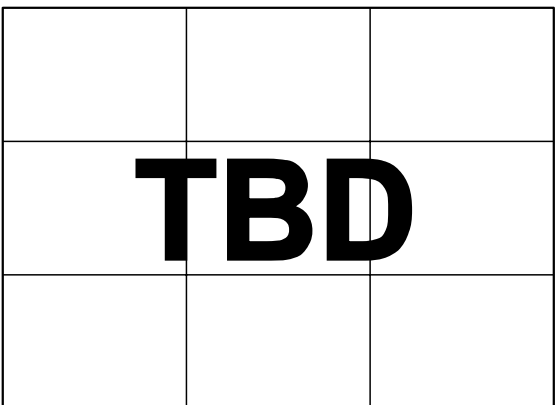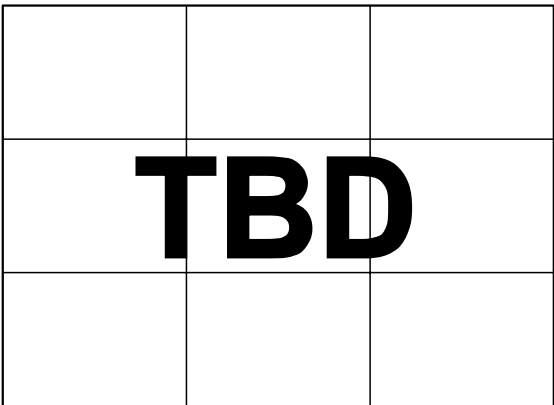*Figure 11. AD7934 Change in ENOB vs. V_{REF} for V_{DD} = 5 V*

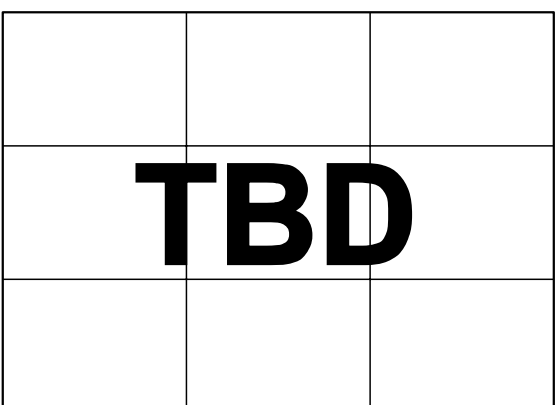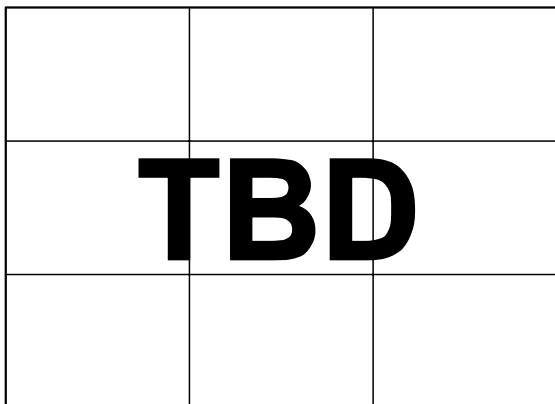*Figure 14. AD7934 Histogram of Codes @ V_{DD} = 5 V with an External Reference*

TBD

Figure 15. AD7933 FFT @ V_{DD} = 5 V

TBD

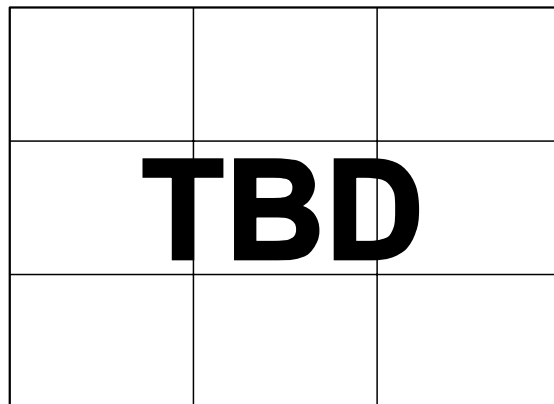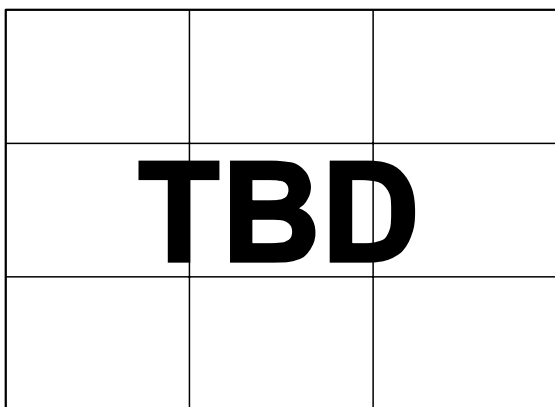*Figure 17. AD7933 Typical INL @ V_{DD} = 5 V*

TBD

Figure 16. AD7933 Typical DNL @ V_{DD} = 5 V

CONTROL REGISTER

The control register on the AD7933/AD7934 is a 12-bit, write-only register. Data is written to this register using the $\overline{CS}$ and $\overline{WR}$ pins. The control register is shown below and the functions of the bits are described in Table 7. At power-up, the default bit settings in the control register are all 0s.

Table 6. Control Register Bits

MSB											LSB
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PM1	PM0	CODING	REF	ZERO	ADD1	ADD0	MODE1	MODE0	SEQ1	SEQ0	RANGE

Table 7. Control Register Bit Function Description

Bit No.	Mnemonic	Description
11, 10	PM1, PM0	Power Management Bits. These two bits are used to select the power mode of operation. The user can choose between either normal mode or various power-down modes of operation as shown in Table 8.
9	CODING	This bit selects the output coding of the conversion result. If this bit is set to 0, the output coding is straight (natural) binary. If this bit is set to 1, the output coding is twos complement.
8	REF	This bit selects whether the internal or an external reference is used to perform the conversion. If this bit is Logic 0, an external reference should be applied to the V_{REF} pin, and if it is Logic 1, the internal reference is selected (see the Reference Section).
7	ZERO	This bit is not used so it should always be set to Logic 0.
6, 5	ADD1, ADD0	These two address bits are used to either select which analog input channel is to be converted in the next conversion, if the sequencer is not being used, or to select the final channel in a consecutive sequence when the sequencer is being used as described in Table 10. The selected input channel is decoded as shown in Table 9.
4, 3	MODE1, MODE0	The two mode pins select the type of analog input on the four V_{IN} pins. The AD7933/AD7934 have either four single-ended inputs, two fully differential inputs, or two pseudo-differential inputs (see Table 9).
2	SEQ1	The SEQ1 bit in the control register is used in conjunction with the SEQ0 bit to control the sequencer function (see Table 10).
1	SEQ0	The SEQ0 bit in the control register is used in conjunction with the SEQ1 bit to control the sequencer function (see Table 10).
0	RANGE	This bit selects the analog input range of the AD7933/AD7934. If it is set to 0, the analog input range extends from 0 V to V_{REF}. If it is set to 1, the analog input range extends from 0 V to $2 \times V_{REF}$. When this range is selected, AV_{DD} must be 4.75 V to 5.25 V.

Table 8. Power Mode Selection using the Power Management Bits in the Control Register

PM1	PM0	Mode	Description
0	0	Normal Mode	When operating in normal mode, all circuitry is fully powered up at all times.
0	1	Auto Shutdown	When operating in auto shutdown mode, the AD7933/AD7934 will enter full shutdown mode at the end of each conversion. In this mode, all circuitry is powered down.
1	0	Auto Standby	When the AD7933/AD7934 enter this mode, all circuitry is partially powered down. This mode is similar to the auto shutdown mode but it allows the part to power up in 1 μs.
1	1	Full Shutdown	When the AD7933/AD7934 enters this mode, all circuitry is powered down. The information in the control register is retained.

Table 9. Analog Input Type Selection

Channel Address		MODE0 = 0, MODE1 = 0		MODE0 = 0, MODE1 = 1		MODE0 = 1, MODE1 = 0		MODE0 = 1, MODE1 = 1	
		Four Single-Ended I/P Channels		Two Fully Differential I/P Channels		Two Pseudo-Differential I/P Channels		Not Used	
ADD1	ADD0	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}		
0	0	VIN0	AGND	VIN0	VIN1	VIN0	VIN1		
0	1	VIN1	AGND	VIN1	VIN0	VIN1	VIN0		
1	0	VIN2	AGND	VIN2	VIN3	VIN2	VIN3		
1	1	VIN3	AGND	VIN3	VIN2	VIN3	VIN2		

SEQUENCER OPERATION

The configuration of the SEQ0 and SEQ1 bits in the control register allow the user to use the sequencer function. Table 10 outlines the two sequencer modes of operation.

Table 10. Sequence Selection Modes

SEQ0	SEQ1	Sequence Type
0	0	This configuration is selected when the sequence function is not used. The analog input channel selected on each individual conversion is determined by the contents of the channel address bits, ADD1 and ADD0, in each prior write operation. This mode of operation reflects the normal operation of a multichannel ADC, without the sequencer function being used, where each write to the AD7933/AD7934 selects the next channel for conversion.
0	1	Not Used.
1	0	Not Used.
1	1	This configuration is used in conjunction with the channel address bits, ADD1 and ADD0, to program continuous conversions on a consecutive sequence of channels from Channel 0 through to a selected final channel as determined by the channel address bits in the control register. When in differential or pseudo-differential mode, inverse channels (e.g., VIN1, VIN0) are not converted in this mode.

CIRCUIT INFORMATION

The AD7933/AD7934 are fast, 4-channel, 12-bit and 10-bit, single-supply, successive approximation analog-to-digital converters. The parts operate from either a 2.7 V to 3.6 V or 4.75 V to 5.25 V power supply and feature throughput rates up to 1.5 MSPS.

The AD7933/AD7934 provide the user with an on-chip track-and-hold, an internal accurate reference, an analog-to-digital converter, and a parallel interface housed in a 28-lead TSSOP package.

The AD7933/AD7934 have four analog input channels that can be configured to be four single-ended inputs, two fully differential pairs, or two pseudo-differential pairs. There is an on-chip channel sequencer that allows the user to select a consecutive sequence of channels through which the ADC can cycle with each falling edge of $\overline{CONVST}$.

The analog input range for the AD7933/AD7934 is 0 to V_{REF} or 0 to $2 \times V_{REF}$, depending on the status of the RANGE bit in the control register. The output coding of the ADC can be either binary or twos complement, depending on the status of the CODING bit in the control register.

The AD7933/AD7934 provide flexible power management options to allow users to achieve the best power performance for a given throughput rate. These options are selected by programming the power management bits, PM1 and PM0, in the control register.

CONVERTER OPERATION

The AD7933/AD7934 are a successive approximation ADC based on two capacitive DACs. Figure 18 and Figure 19 show simplified schematics of the ADC in acquisition and conversion phase, respectively. The ADC comprises of control logic, a SAR, and two capacitive DACs. Both figures show the operation of the ADC in differential/pseudo-differential mode. Single-ended mode operation is similar but V_{IN-} is internally tied to AGND. In the acquisition phase, SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.
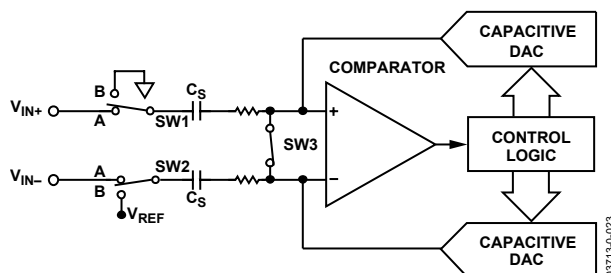

Figure 18. ADC Acquisition Phase

When the ADC starts a conversion (Figure 19), SW3 will open and SW1 and SW2 will move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC's output code. The output impedances of the sources driving the V_{IN+} and the V_{IN-} pins must be matched; otherwise, the two inputs will have different settling times, resulting in errors.
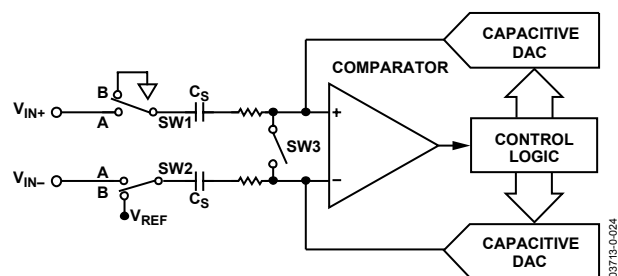
Figure 19. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding for the AD7933/AD7934 is either straight binary or twos complement, depending on the status of the CODING bit in the control register. The designed code transitions occur at successive LSB values (i.e., 1 LSB, 2 LSBs, and so on) and the LSB size is $V_{REF}/1024$ for the AD7933 and $V_{REF}/4096$ for the AD7934. The ideal transfer characteristics of the AD7933/AD7934 for both straight binary and twos complement output coding are shown in Figure 20 and Figure 21, respectively.

NOTE: V_{REF} IS EITHER V_{REF} OR $2 \times V_{REF}$

Figure 20. AD7933/AD7934 Ideal Transfer Characteristic with Straight Binary Output Coding

$$1 \text{ LSB} = 2 \times V_{REF}/4096 \text{ (AD7934)}$$
$$1 \text{ LSB} = 2 \times V_{REF}/1024 \text{ (AD7933)}$$

Figure 21. AD7933/AD7934 Ideal Transfer Characteristic with Twos Complement Output Coding
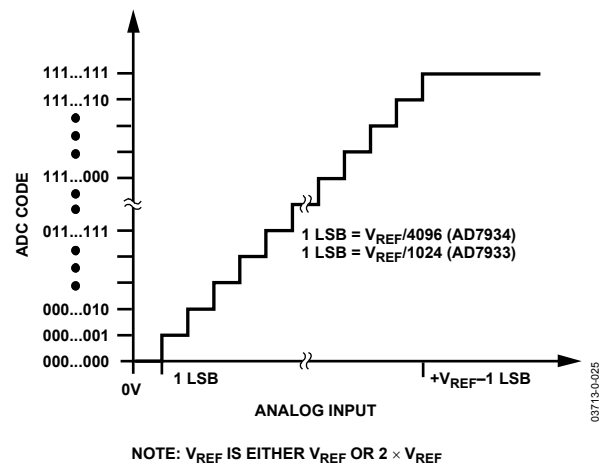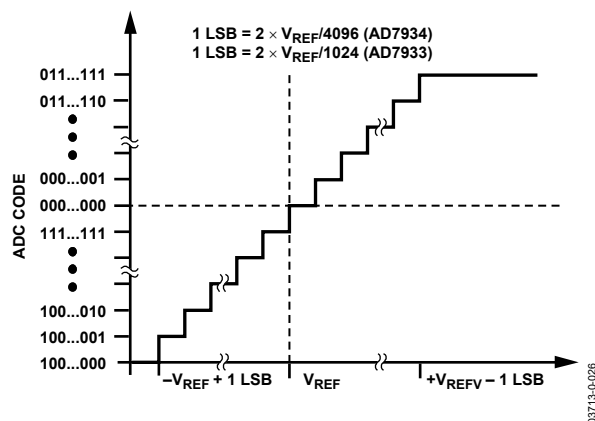
TYPICAL CONNECTION DIAGRAM

Figure 22 shows a typical connection diagram for the AD7933/AD7934. The AGND and DGND pins are connected together at the device for good noise suppression. The V_{REFIN}/V_{REFOUT} pin is decoupled to AGND with a 0.47 μF capacitor to avoid noise pickup, if the internal reference is used. Alternatively, V_{REFIN}/V_{REFOUT} can be connected to a external reference source, and in this case, the reference pin should be decoupled with a 0.1 μF capacitor. In both cases, the analog input range can either be 0 V to V_{REF} (RANGE bit = 0) or 0 V to $2 \times V_{REF}$ (RANGE bit = 1). The analog input configuration is either four single-ended inputs, two differential pairs or two pseudo-differential pairs (see Table 9). The V_{DD} pin connects to either a 3 V or 5 V supply. The voltage applied to the V_{DRIVE} input controls the voltage of the digital interface, and here, it is connected to the same 3 V supply of the microprocessor to allow a 3 V logic interface (see the Digital Inputs section).
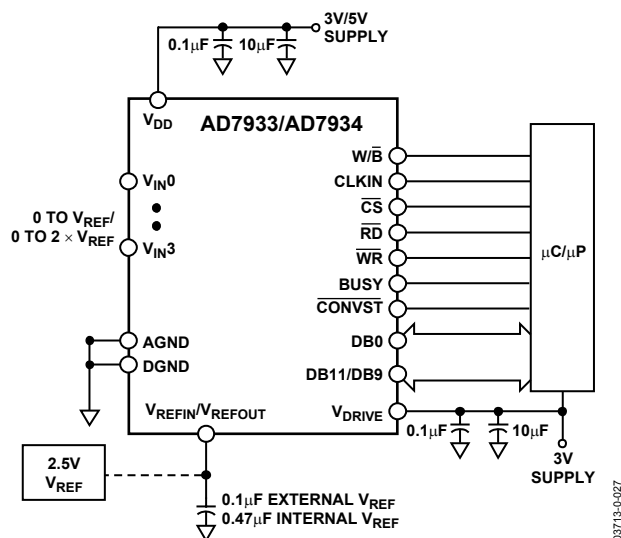

Figure 22. Typical Connection Diagram

ANALOG INPUT STRUCTURE

Figure 23 shows the equivalent circuit of the analog input structure of the AD7933/AD7934 in differential/pseudo-differential mode. In single-ended mode, V_{IN-} is internally tied to AGND. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This causes these diodes to become forward-biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

The C1 capacitors, in Figure 23, are typically 4 pF and can primarily be attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The C2 capacitors, in Figure 23, are the ADC's sampling capacitors and have a typical capacitance of 16 pF.

For ac applications, removing high frequency components from the analog input signal is recommended by using an RC low-pass filter on the relevant analog input pins. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.
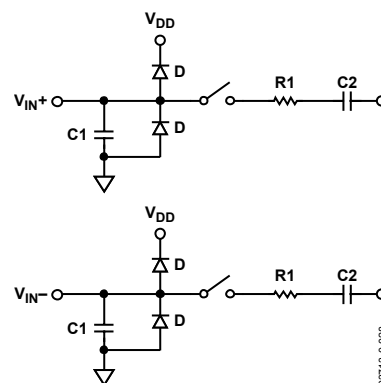
Figure 23. Equivalent Analog Input Circuit, Conversion Phase—Switches, Open Track Phase—Switches Closed

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance will depend on the amount of THD that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 24 shows a graph of the THD versus the analog input signal frequency for different source impedances for both $V_{DD} = 5$ V and 3 V.
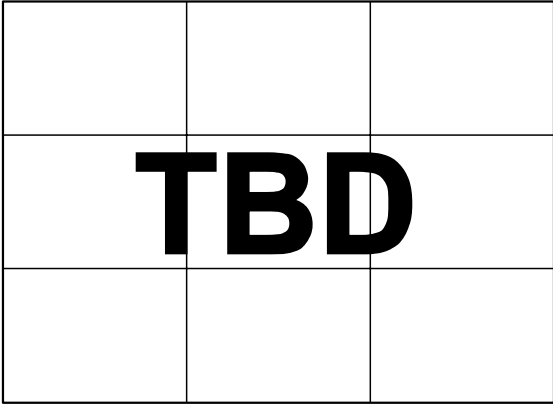
Figure 24. THD vs. Analog Input Frequency for Various Source Impedances

Figure 25 shows a graph of the THD versus the analog input frequency for various supplies, while sampling at 1.5 MHz with an SCLK of 20 MHz. In this case, the source impedance is 10 Ω.

Figure 25. THD vs. Analog Input Frequency for Various Supply Voltages

ANALOG INPUTS

The AD7933/AD7934 have software selectable analog input configurations. Users can choose either four single-ended inputs, two fully differential pairs, or two pseudo-differential pairs. The analog input configuration is chosen with Bits MODE0/MODE1 in the internal control register (see Table 9).

Single-Ended Mode

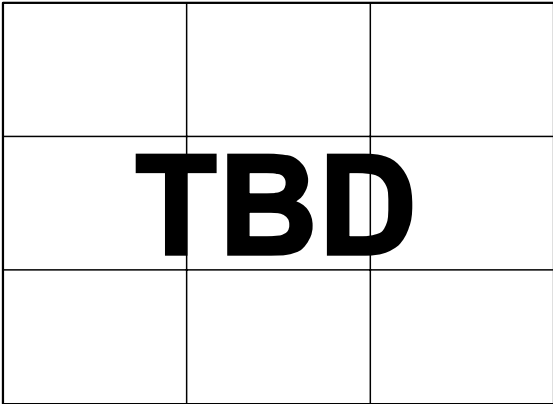The AD7933/AD7934 can have four single-ended analog input channels by setting the MODE0 and MODE1 bits in the control register both to 0. In applications where the signal source has a high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range is either 0 to V_{REF} or 0 to $2 \times V_{REF}$.

If the analog input signal to be sampled is bipolar, the internal reference of the ADC can be used to externally bias up this signal to make it of the correct format for the ADC.

Figure 26 shows a typical connection diagram when operating the ADC in single-ended mode.
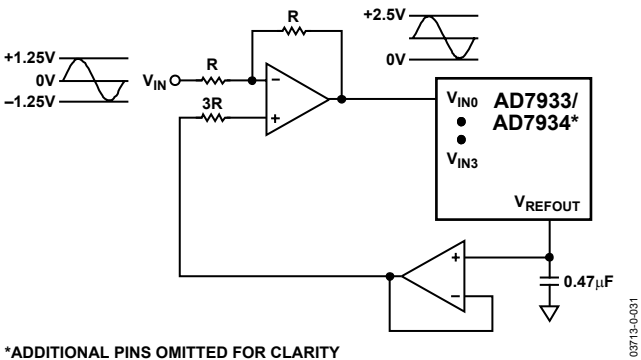

*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 26. Single-Ended Mode Connection Diagram

Differential Mode

The AD7933/AD7934 can have two differential analog input pairs by setting Bits MODE0 and MODE1 in the control register to 0 and 1, respectively.

Differential signals have some benefits over single-ended signals, including noise immunity based on the device's common-mode rejection and improvements in distortion performance. Figure 27 defines the fully differential analog input of the AD7933/AD7934.

*ADDITIONAL PINS OMITTED FOR CLARITY
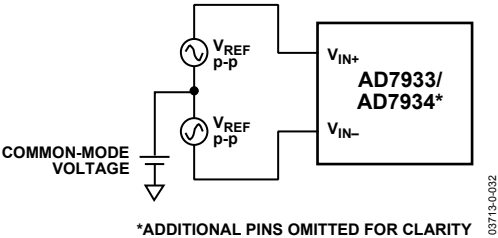
Figure 27. Differential Input Definition

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins in each differential pair (i.e., $V_{IN+} - V_{IN-}$). V_{IN+} and V_{IN-} should be simultaneously driven by two signals, each of amplitude V_{REF} that are 180° out of phase. The amplitude of the differential signal is therefore $-V_{REF}$ to $+V_{REF}$ peak-to-peak (i.e., $2 \times V_{REF}$). This is regardless of the common mode (CM). The common mode is the average of the two signals, i.e. $(V_{IN+} + V_{IN-})/2$, and is therefore the voltage that the two inputs are centered on. This results in the span of each input being CM $\pm V_{REF}/2$. This voltage has to be set up externally and its range varies with V_{REF}. As the value of V_{REF} increases, the common-mode range decreases. When driving the inputs with an amplifier, the actual common-mode range is determined by the amplifier's output voltage swing.

Figure 28 and Figure 29 show how the common-mode range typically varies with V_{REF} for both a 5 V and a 3 V power supply. The common mode must be in this range to guarantee the functionality of the AD7933/AD7934.

When a conversion takes place, the common mode is rejected resulting in a virtually noise free signal of amplitude $-V_{REF}$ to $+V_{REF}$ corresponding to the digital codes of 0 to 1024 for the AD7933 and 0 to 4096 for the AD7934.

Figure 28. Input Common-Mode Range vs.
V_{REF} (0 to V_{REF} Range, V_{DD} = 5 V)

Figure 29. Input Common-Mode Range vs.
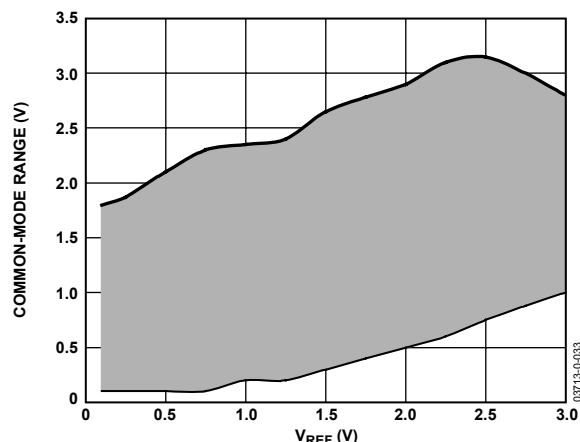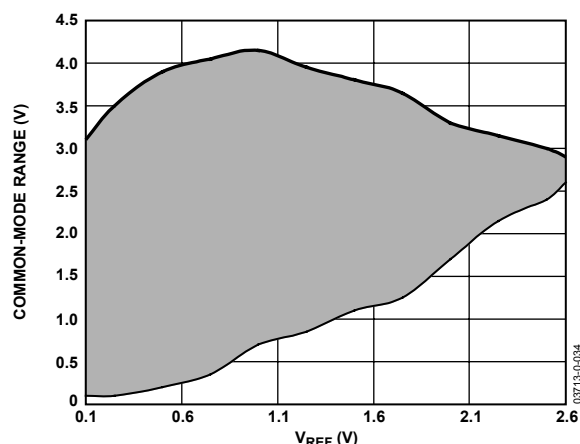*V_{REF} (2 × V_{REF} Range, V_{DD} = 5 V)*

Driving Differential Inputs

Differential operation requires that V_{IN+} and V_{IN-} be simultaneously driven with two equal signals that are 180° out of phase. The common mode must be set up externally and have a range that is determined by V_{REF}, the power supply, and the particular amplifier used to drive the analog inputs. Differential modes of operation with either an ac or dc input provide the best THD performance over a wide frequency range. Since not all applications have a signal preconditioned for differential operation, there is often a need to perform single-ended-to-differential conversion.

Using an Op Amp Pair

An op amp pair can be used to directly couple a differential signal to one of the analog input pairs of the AD7933/AD7934. The circuit configurations shown in Figure 30 and Figure 31 show how a dual op amp can be used to convert a single-ended signal into a differential signal for both a bipolar and unipolar input signal, respectively.

The voltage applied to Point A sets up the common-mode voltage. In both diagrams, it is connected in some way to the reference, but any value in the common-mode range can be input here to set up the common mode. A suitable dual op amp that could be used in this configuration to provide differential drive to the AD7933/AD7934 is the AD8022.

Take care when choosing the op amp; the selection depends on the required power supply and system performance objectives. The driver circuits in Figure 30 and Figure 31 are optimized for dc coupling applications requiring best distortion performance.

The circuit configuration shown in Figure 30 converts a unipolar, single-ended signal into a differential signal.

The circuit configuration in Figure 31 is configured to convert and level shift a single-ended, ground-referenced (bipolar) signal to a differential signal centered at the V_{REF} level of the ADC.
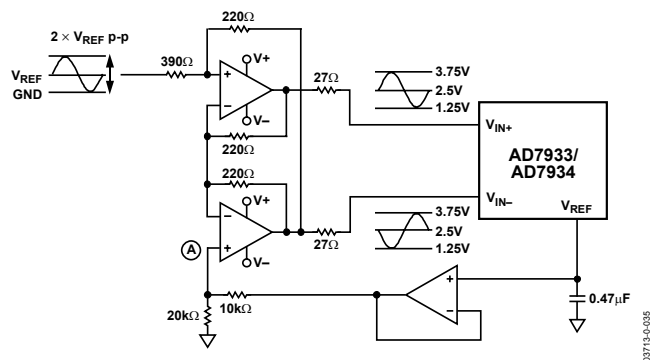

Figure 30. Dual Op Amp Circuit to Convert a
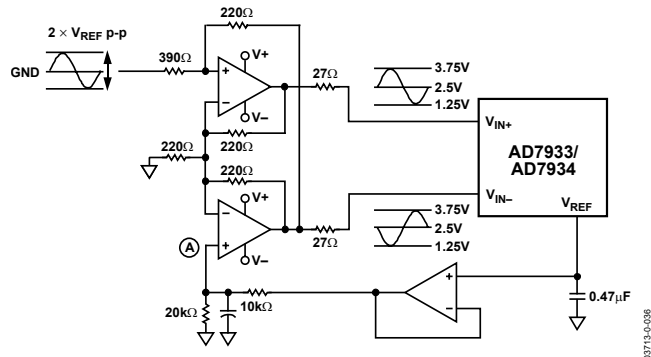*Single-Ended Unipolar Signal into a Differential Signal*

Figure 31. Dual Op Amp Circuit to Convert a
Single-Ended Bipolar Signal into a Differential Signal

Pseudo-Differential Mode

The AD7933/AD7934 can have two pseudo-differential pairs by setting Bits MODE0 and MODE1 in the control register to 1, 0, respectively. $V_{IN}+$ is connected to the signal source that must have an amplitude of V_{REF} to make use of the full dynamic range of the part. ADC input is applied to the V_{IN-} pin. The voltage applied to this input provides an offset from ground or a pseudo ground for the $V_{IN}+$ input. The benefit of pseudo-differential inputs is that they separate the analog input signal ground from the ADC's ground allowing dc common-mode voltages to be cancelled. Figure 32 shows a connection diagram for the pseudo-differential mode.
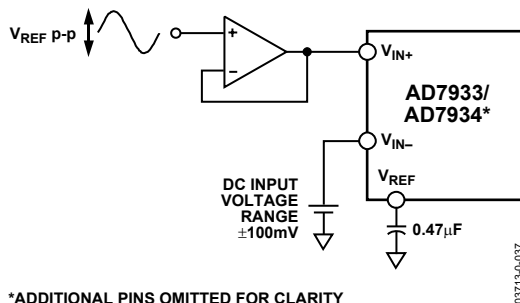
Figure 32. Pseudo-Differential Mode Connection Diagram

ANALOG INPUT SELECTION

As shown in Table 9, users can set up their analog input configuration by setting the values in Bits MODE0 and MODE1 in the control register. Assuming the configuration is chosen, there are two different ways of selecting the analog input to be converted depending on the state of the SEQ0 and SEQ1 bits in the control register.

Normal Multichannel Operation (SEQ0 = SEQ1 = 0)

Any one of four analog input channels or two pairs of channels may be selected for conversion in any order by setting the SEQ0 and SEQ1 bits in the control register both to 0. The channel to be converted is selected by writing to Bits ADD1 and ADD0 in the control register to program the multiplexer prior to the conversion. This mode of operation is of a normal multichannel ADC where each data write selects the next channel for conversion. Figure 33 shows a flow chart of this mode of operation. The channel configurations are shown in Table 9.
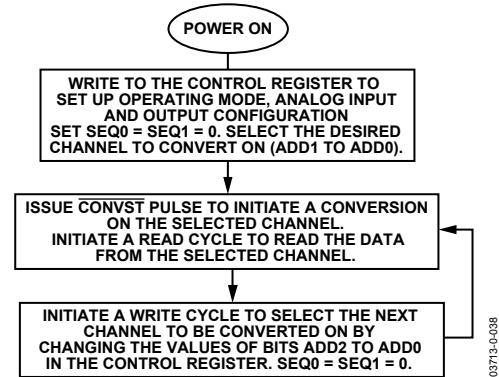
Figure 33. Normal Multichannel Operation Flow Chart

Using the Sequencer: Consecutive Sequence (SEQ0 = 1, SEQ1 = 1)

A sequence of consecutive channels can be converted beginning with Channel 0 and ending with a final channel selected by writing to Bits ADD1 and ADD0 in the control register. This is done by setting the SEQ0 and SEQ1 bits in the control register both to 1. Once the control register is written to set this mode up, the next conversion is on Channel 0, then Channel 1, and so on until the channel selected by the address bits, ADD1 and ADD0, is reached. The ADC then returns to Channel 0 and starts the sequence again. The $\overline{WR}$ input must be kept high to ensure that the control register is not accidentally overwritten and the sequence interrupted. This pattern continues until such time as the AD7933/AD7934 is written to. Figure 34 shows the flow chart of the consecutive sequence mode.
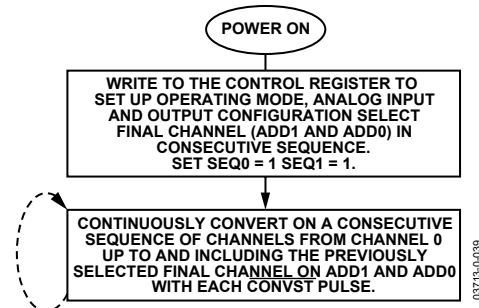
Figure 34. Consecutive Sequence Mode Flow Chart

REFERENCE SECTION

The AD7933/AD7934 can operate with either the on-chip reference or an external reference. The internal reference is selected by setting the REF bit in the internal control register to 1. A block diagram of the internal reference circuitry is shown in Figure 35. The internal reference circuitry includes an on-chip 2.5 V band gap reference and a reference buffer. When using the internal reference, the V_{REFIN}/V_{REFOUT} pin should be decoupled to AGND with a 0.47 μF capacitor. This internal reference not only provides the reference for the analog-to-digital conversion, but it also is used externally in the system. It is recommended that the reference output is buffered using an external precision op amp before applying it anywhere in the system.

Figure 35. Internal Reference Circuit Block Diagram

Alternatively, an external reference can be applied to the V_{REFIN}/V_{REFOUT} pin of the AD7933/AD7934. An external reference input is selected by setting the REF bit in the internal control register to 0. When using an external reference, the V_{REFIN}/V_{REFOUT} pin should be decoupled to AGND with a 0.1 μF capacitor. When operating in differential mode, the external reference input range is 0.1 V to 3.5V, and in single-ended and pseudo-differential mode, the external reference input range is 0.1 V to V_{DD}. In all cases, the specified reference is 2.5 V.

It is important to ensure that, when choosing the reference value, the maximum analog input range ($V_{IN\ MAX}$) is never greater than V_{DD} + 0.3 V to comply with the maximum ratings of the device. In pseudo differential mode, the user must ensure that $V_{REFIN} − V_{IN-} \le V_{DD}$.

The following two examples calculate the maximum V_{REF} input that can be used when operating the AD7933/AD7934 in differential mode with a V_{DD} of 5 V and 3 V, respectively.

Example 1

$$V_{IN\ MAX} = V_{DD} + 0.3$$

$$V_{IN\ MAX} = V_{REF} + V_{REF}/2$$

If V_{DD} = 5 V, then $V_{IN\ MAX}$ = 5.3 V.

Therefore, $3 \times V_{REF}/2$ = 5.3 V.

$$V_{REF\ MAX} = 3.5\ V$$

Therefore, when operating at V_{DD} = 5 V, the value of V_{REF} can range from 100 mV to a maximum value of 3.5 V. When V_{DD} = 4.75 V, $V_{REF\ MAX}$ = 3.17 V.

Example 2

$$V_{IN\ MAX} = V_{DD} + 0.3$$

$$V_{IN\ MAX} = V_{REF} + V_{REF}/2$$

If V_{DD} = 3.6 V, then $V_{IN\ MAX}$ = 3.9 V.

Therefore, $3 \times V_{REF}/2$ = 3.6 V.

$$V_{REF\ MAX} = 2.6\ V$$

Therefore, when operating with at V_{DD} = 3 V, the value of V_{REF} can range from 100 mV to a maximum value of 2.4 V. When V_{DD} = 2.7 V, $V_{REF\ MAX}$ = 2 V.

These examples show that the maximum reference applied to the AD7933/AD7934 is directly dependant on the value applied to V_{DD}.

The performance of the part at different reference values is shown in Figures TBD to TBD. The value of the reference sets the analog input span and the common-mode voltage range. Errors in the reference source result in gain errors in the AD7933/AD7934 transfer function and add to the specified full-scale errors on the part. Table 11 lists suitable voltage references available from ADI that could be used, and Figure 36 shows a typical connection diagram for an external reference.

Table 11. Examples of Suitable Voltage References

Reference	Output Voltage	Initial Accuracy (% max)	Operating Current (μA)
AD780	2.5/3	0.04	1000
ADR421	2.5	0.04	500
ADR420	2.048	0.05	500

Figure 36. Typical V_{REF} Connection Program

Digital Inputs

The digital inputs applied to the AD7933/AD7934 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs applied can go to 7 V and are not restricted by the AV_{DD} + 0.3 V limit that is on the analog inputs.

Another advantage of the digital inputs not being restricted by the AV_{DD} + 0.3 V limit is the fact that power supply sequencing issues are avoided. If any of these inputs are applied before AV_{DD}, then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V was applied prior to AV_{DD}.

V_{DRIVE} Input

The AD7933/AD7934 has a V_{DRIVE} feature. V_{DRIVE} controls the voltage at which the parallel interface operates. V_{DRIVE} allows the ADC to easily interface to 1.8 V, 3 V, and 5 V processors. V_{DRIVE} of 1.8 V can only be used if V_{DD} = 2.7 V to 3.6 V.

For example, if the AD7933/AD7934 operated with an AV_{DD} of 5 V and the V_{DRIVE} pin could be powered from a 3 V supply, the AD7933/AD7934 has better dynamic performance with an AV_{DD} of 5 V while still being able to interface to 3 V processors. Care should be taken to ensure V_{DRIVE} does not exceed AV_{DD} by more than 0.3 V (see Table 4).

PARALLEL INTERFACE

The AD7933/AD7934 have a flexible, high speed, parallel interface. This interface is 12-bits (AD7934) or 10-bits (AD7933) wide and is capable of operating in either word (W/$\overline{B}$ tied high) or byte (W/$\overline{B}$ tied low) mode. The $\overline{CONVST}$ signal is used to initiate conversions, and when operating in auto shutdown or auto standby mode, it is used to power up the ADC.

A falling edge on the $\overline{CONVST}$ signal is used to initiate conversions, and it also puts the ADC track-and-hold into track. Once the $\overline{CONVST}$ signal goes low, the BUSY signal goes high for the duration of the conversion. In between conversions, $\overline{CONVST}$ must be brought high for a minimum time of t_1. This must happen after the 14th rising edge of CLKIN; otherwise, the conversion will be aborted and the track-and-hold will go back into track. At the end of the conversion, BUSY goes low and can be used to activate an interrupt service routine. The $\overline{CS}$ and $\overline{RD}$ lines are then activated in parallel to read the 12 bits or 10 bits of conversion data. When power supplies are first applied to the device, a rising edge on $\overline{CONVST}$ puts the track-and-hold into track. The acquisition time of 135 ns minimum must be allowed before $\overline{CONVST}$ is brought low to initiate a conversion. The ADC will then go into hold on the falling edge of $\overline{CONVST}$ and back into track on the 13th rising edge of CLKIN after this (see Figure 37). When operating the device in auto shutdown or auto standby mode, where the ADC powers down at the end of each conversion, a rising edge on the $\overline{CONVST}$ signal is used to power up the device.
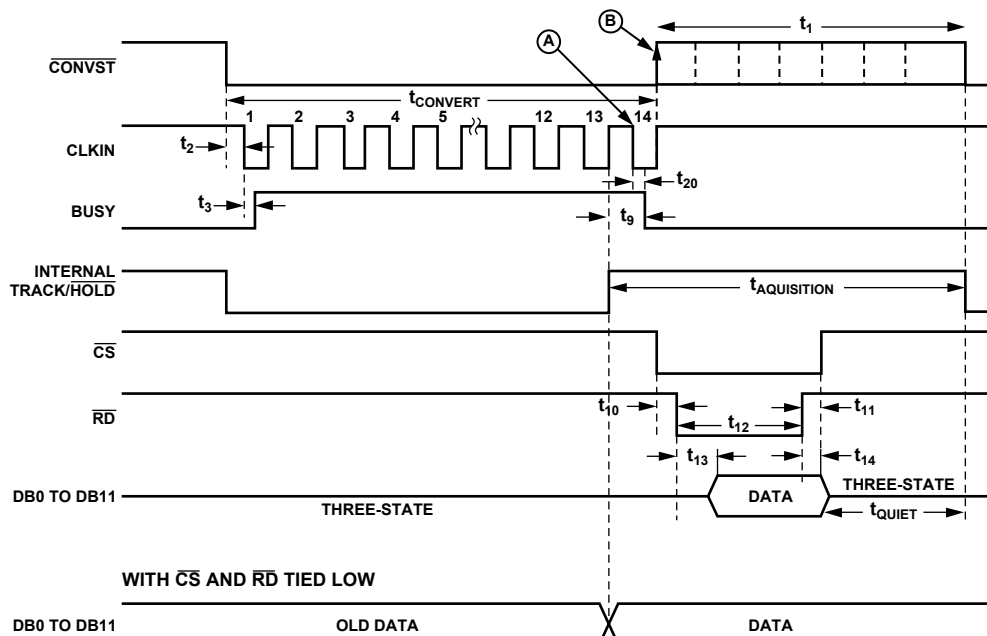

Figure 37. AD7933/AD7934 Parallel Interface—Conversion and Read Cycle in Word Mode (W/$\overline{B}$ = 1)

Reading Data from the AD7933/AD7934

With the W/$\overline{B}$ pin tied logic high, the AD7933/AD7934 interface operates in word mode. In this case, a single read operation from the device accesses the conversion data-word on Pins DB0/DB2 to DB11. The DB8/HBEN pin assumes its DB8 function. With the W/$\overline{B}$ pin tied to logic low, the AD7933/AD7934 interface operates in byte mode. In this case, the DB8/HBEN pin assumes its HBEN function. Conversion data from the AD7933/ AD7934 must be accessed in two read operations with 8 bits of data provided on DB0 to DB7 for each of the read operations. The HBEN pin determines whether the read operation accesses the high byte or the low byte of the12- or 10-bit word. For a low byte read, DB0 to DB7 provide the eight LSBs of the 12-bit word. For 10-bit operation, the two LSBs of the low byte are 0s and are followed by 6 bits of conversion data. For a high byte read, DB0 to DB3 provide the 4 MSBs of the 12-/10-bit word. DB4 of the high byte is always 0 and DB5 and DB6 of the high byte provide the Channel ID. Figure 37 shows the read cycle timing diagram for a 12-/10-bit

transfer. When operated in word mode, the HBEN input does not exist and only the first read operation is required to access data from the device. When operated in byte mode, the two read cycles shown in Figure 38 are required to access the full data-word from the device.

The $\overline{CS}$ and $\overline{RD}$ signals are gated internally and level triggered active low. In either word mode or byte mode, $\overline{CS}$ and $\overline{RD}$ may be tied together as the timing specification t_{10} and t_{11} is 0 ns minimum. The data is placed onto the data bus a time t_{13} after both $\overline{CS}$ and $\overline{RD}$ go low. The $\overline{RD}$ rising edge can be used to latch data out of the device. After a time, t_{14}, the data lines will become three-stated.

Alternatively, $\overline{CS}$ and $\overline{RD}$ can be tied permanently low and the conversion data will be valid and placed onto the data bus a time, t_9, before the falling edge of BUSY.
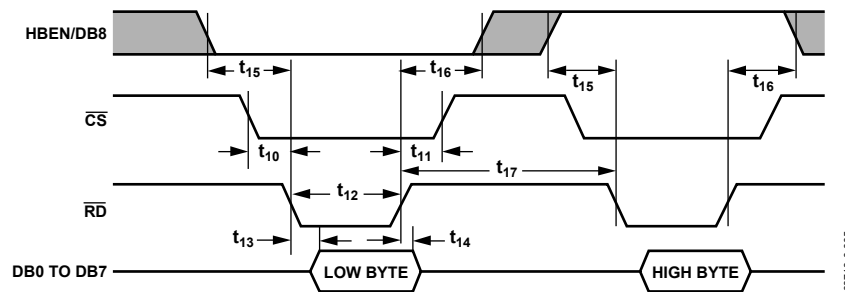

Figure 38. AD7933/AD7934 Parallel Interface—Read Cycle Timing for Byte Mode Operation (W/$\overline{B}$ = 0)

Writing Data to the AD7933/AD7934

With W/$\overline{B}$ tied logic high, a single write operation transfers the full data-word on DB0 to DB11 to the control register on the AD7933/AD7934. The DB8/HBEN pin assumes its DB8 function. Data written to the AD7933/AD7934 should be provided on the DB0 to DB11 inputs with DB0 being the LSB of the data-word. With W/$\overline{B}$ tied logic low, the AD7933/AD7934 requires two write operations to transfer a full 12-bit word. DB8/HBEN assumes its HBEN function. Data written to the AD7933/AD7934 should be provided on the DB0 to DB7 inputs. HBEN determines whether the byte written is high byte or low byte data. The low byte of the data-word has DB0 being the LSB of the full data-word. For the high byte write, HBEN should be high and the data on the DB0 input should be data bit 8 of the 12 bit word.

Figure 39 shows the write cycle timing diagram of the AD7933/AD7934. When operated in word mode, the HBEN input does not exist and only the one write operation is required to write the word of data to the device. Data should be provided on DB0 to DB11. When operated in byte mode, the two write cycles shown in Figure 40 are required to write the full data-word to the AD7933/AD7934. In Figure 40, the first write transfers the lower 8 bits of the data-word from DB0 to DB7 and the second write transfers the upper 4 bits of the data-word.

When writing to the AD7933/AD7934, the top 4 bits in the high byte must be 0s.

The data is latched into the device on the rising edge of $\overline{WR}$. The data needs to be setup a time, t_7, before the $\overline{WR}$ rising edge and held for a time, t_8, after the $\overline{WR}$ rising edge. The $\overline{CS}$ and $\overline{WR}$ signals are gated internally. $\overline{CS}$ and $\overline{WR}$ may be tied together as the timing specification for t_4 and t_5 is 0 ns minimum (assuming $\overline{CS}$ and $\overline{RD}$ have not already been tied together).
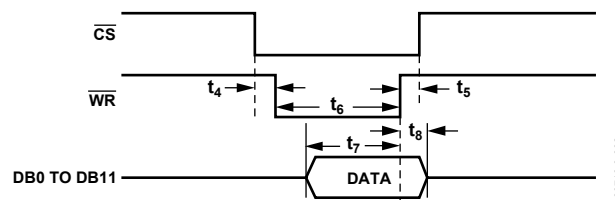

Figure 39. AD7933/AD7934 Parallel Interface—Write Cycle Timing for Word Mode Operation (W/$\overline{B}$ = 1)
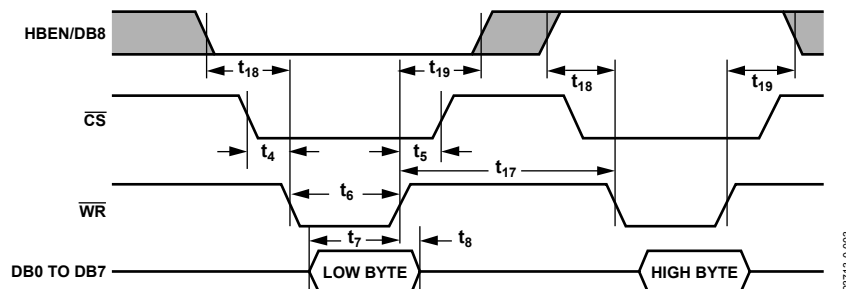

Figure 40. AD7933/AD7934 Parallel Interface—Write Cycle Timing for Byte Mode Operation (W/$\overline{B}$ = 0)

POWER MODES OF OPERATION

The AD7933/AD7934 have four different power modes of operation. These modes are designed to provide flexible power management options. Different options can be chosen to optimize the power dissipation/throughput rate ratio for differing applications. The mode of operation is selected by the power management bits, PM1 and PM0, in the control register, as detailed in Table 8. When power is first applied to the AD7933/AD7934 an on-chip, power-on reset circuit ensures the default power-up condition is normal mode.

Note that, after power-on, track-and-hold is in hold mode and the first rising edge of $\overline{CONVST}$ places the track-and-hold into track mode.

Normal Mode (PM1 = PM0 = 0)

This mode is intended for the fastest throughput rate performance because the user does not have to worry about any power-up times because the AD7933/AD7934 remain fully powered up at all times. At power-on reset, this mode is the default setting in the control register.

Auto Shutdown (PM1 = 0; PM0 = 1)

In this mode of operation, the AD7933/AD7934 automatically enter full shutdown at the end of each conversion, which is shown at Point A in Figure 37. In shutdown mode, all internal circuitry on the device is powered. The part retains information in the control register during shutdown. It remains in shutdown mode until the next rising edge of $\overline{CONVST}$ (see Point B in Figure 37). In order to keep the device in shutdown for as long as possible, $\overline{CONVST}$ should idle low between conversions as shown in Figure 41. On this rising edge, the part begins to power-up and track-and-hold returns to track mode. The power-up time required depends on whether the user is operating with the internal or external reference. With the

internal reference, the power-up time is typically TBD, and with an external reference, the power-up time is typically TBD. The user should ensure that the power-up time has elapsed before initiating a conversion.

Auto Standby (PM1 = 1; PM0 = 0)

In this mode of operation, the AD7933/AD7934 automatically enter standby mode at the end of each conversion. When this mode is entered, all circuitry on the AD7933/AD7934 is powered down except for the reference and reference buffer. Also, track-and-hold goes into hold at this point and remains in hold as long as the device is in standby The part remains in standby until the next rising edge of $\overline{CONVST}$ powers up the device, which takes at least TBD. The user should ensure this power-up time has elapsed before initiating another conversion, as shown in Figure 41. This rising edge of CONVST also places track-and-hold back into track mode.

Full Shutdown Mode (PM1 = 1; PM0 = 1)

When this mode is entered, all circuitry on the AD7933/AD7934 is powered down upon completion of the write operation, i.e., on rising edge of $\overline{WR}$. The part retains the information in the control register while the part is in shutdown. The AD7933/AD7934 remain in full shutdown mode, and track-and-hold in hold mode, until the power management bits (PM1 and PM0) in the control register are changed. If a write to the control register occurs while the part is in full shutdown mode, and the power management bits are changed to PM0 = PM1 = 0, i.e., normal mode, the part begins to power up on the $\overline{WR}$ rising edge and the track and hold returns to track.. To ensure the part is fully powered up before a conversion is initiated, the power-up time, TBD, should be allowed before the $\overline{CONVST}$ falling edge; otherwise, invalid data is read.
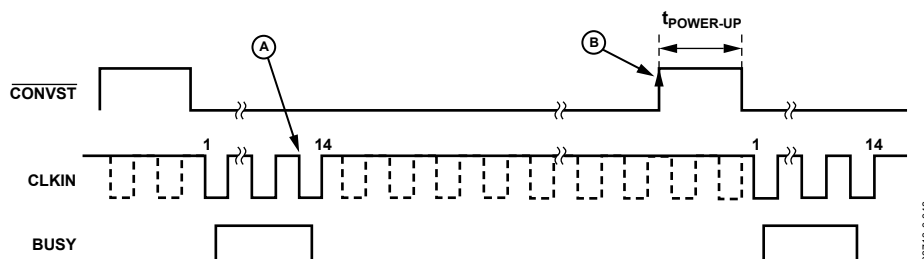

Figure 41. Auto-Shutdown/Auto-Standby Mode

POWER VS. THROUGHPUT RATE

A big advantage of powering the ADC down after a conversion is that the power consumption of the part is significantly reduced at lower throughput rates. When using the different power modes, the AD7933/AD7934 is only powered up for the duration of the conversion. Therefore, the average power consumption per cycle is significantly reduced. Figure 42 and Figure 43 show plots of the power versus the throughput when operating in auto shutdown and auto standby modes.
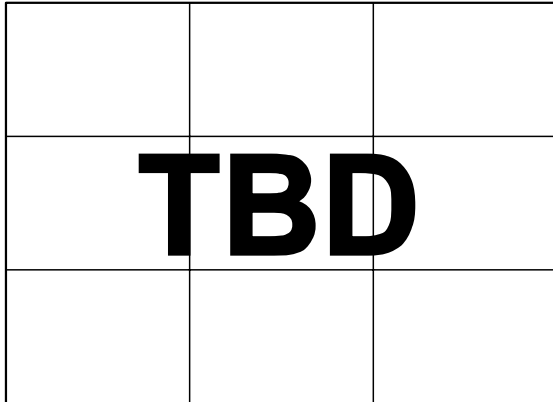

Figure 42. Power vs. Throughput in Auto Shutdown Mode
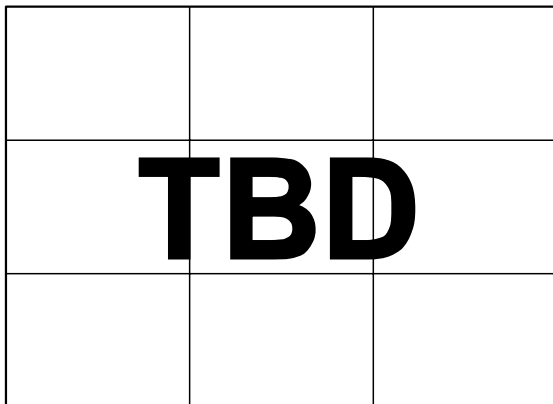

Figure 43. Power vs. Throughput in Auto Standby Mode

MICROPROCESSOR INTERFACING
AD7933/AD7934 to ADSP-21xx Interface

Figure 44 shows the AD7933/AD7934 interfaced to the ADSP-21xx series of DSPs as a memory mapped device. A single wait state may be necessary to interface the AD7933/AD7934 to the ADSP-21xx, depending on the clock speed of the DSP. The wait state can be programmed via the data memory wait state control register of the ADSP-21xx (see the ADSP-21xx family User's Manual for details). The following instruction reads from the AD7933/AD7934:

$$MR = DM (ADC)$$

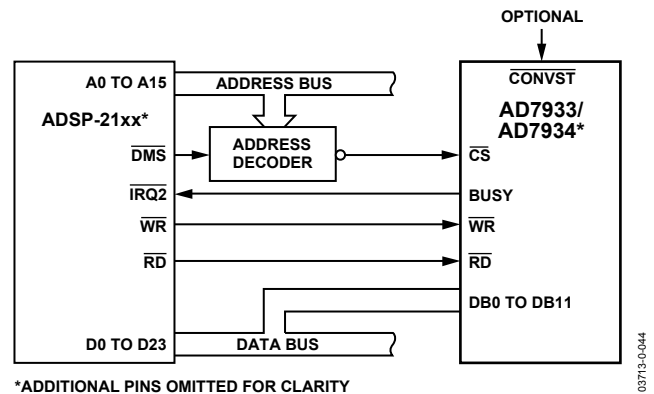where ADC is the address of the AD7933/AD7934.

Figure 44. Interfacing to the ADSP-21xx

AD7933/AD7934 to ADSP-21065L Interface

Figure 45 shows a typical interface between the AD7933/AD7934 and the ADSP-21065L SHARC processor. This interface is an example of one of three DMA handshake modes. The $\overline{MS_x}$ control line is actually three memory select lines. Internal $ADDR_{25-24}$ are decoded into $\overline{MS_{3-0}}$, these lines are then asserted as chip selects. The $\overline{DMAR_1}$ (DMA request 1) is used in this setup as the interrupt to signal the end of the conversion. The rest of the interface is standard handshaking operation.
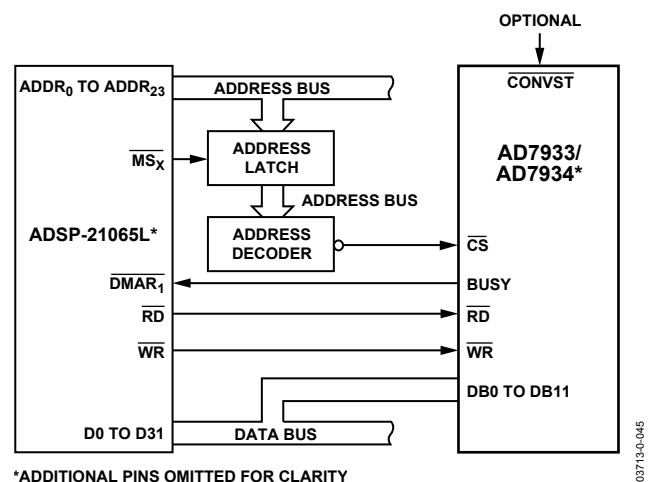

Figure 45. Interfacing to the ADSP-21065L

AD7933/AD7934 to TMS32020, TMS320C25, and TMS320C5x Interface

Parallel interfaces between the AD7933/AD7934 and the TMS32020, TMS320C25 and TMS320C5x family of DSPs are shown in Figure 46. The memory mapped address chosen for the AD7933/AD7934 should be chosen to fall in the I/O memory space of the DSPs. The parallel interface on the AD7933/AD7934 is fast enough to interface to the TMS32020 with no extra wait states. If high speed glue logic, such as 74AS devices, are used to drive the $\overline{RD}$ and the $\overline{WR}$ lines when interfacing to the TMS320C25, then again, no wait states are necessary. However, if slower logic is used, data accesses may be slowed sufficiently when reading from and writing to the part to require the insertion of one wait state. Extra wait states will be necessary when using the TMS320C5x at their fastest clock speeds (see the TMS320C5x User's Guide for details).

Data is read from the ADC using the following instruction:

IN D, ADC

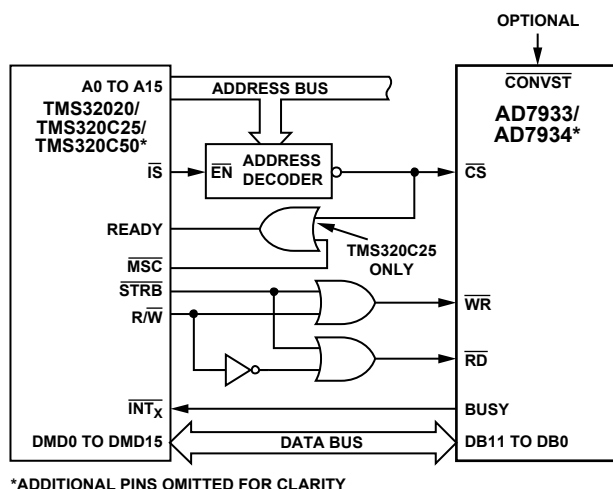where D is the data memory address, and ADC is the AD7933/AD7934 address.

Figure 46. Interfacing to the TMS32020/C25/C5x

AD7933/AD7934 to 80C186 Interface

Figure 47 shows the AD7933/AD7934 interfaced to the 80C186 microprocessor. The 80C186 DMA controller provides two independent high speed DMA channels where data transfer can occur between memory and I/O spaces. Each data transfer consumes two bus cycles, one cycle to fetch data and the other to store data. After the AD7933/AD7934 has finished a conversion, the BUSY line generates a DMA request to Channel 1 (DRQ1). As a result of the interrupt, the processor performs a DMA READ operation which also resets the interrupt latch. Sufficient priority must be assigned to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion.
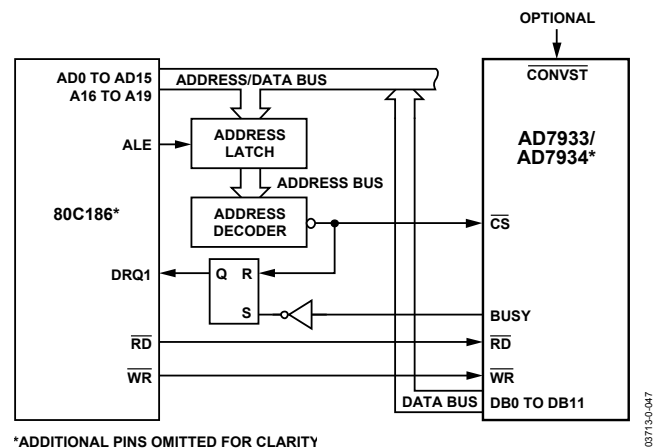

Figure 47. Interfacing to the 80C186

APPLICATION HINTS

GROUNDING AND LAYOUT

The printed circuit board that houses the AD7933/AD7934 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined in only one place, and the connection should be a star ground point established as close to the ground pins on the AD7933/AD7934 as possible. Avoid running digital lines under the device as this couples noise onto the die. The analog ground plane should be allowed to run under the AD7933/AD7934 to avoid noise coupling. The power supply lines to the AD7933/AD7934 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board.

In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 μF tantalum capacitors in parallel with 0.1 μF capacitors to GND. To achieve the best from these decoupling components, they must be placed as close as possible to the device.

EVALUATING THE AD7933/AD7934 PERFORMANCE

The recommended layout for the AD7933/AD7934 is outlined in the evaluation board documentation. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the evaluation board controller. The evaluation board controller can be used in conjunction with the AD7933/AD7934 evaluation board, as well as many other ADI evaluation boards ending in the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7933/AD7934.

The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7933/AD7934. The software and documentation are on the CD that ships with the evaluation board.
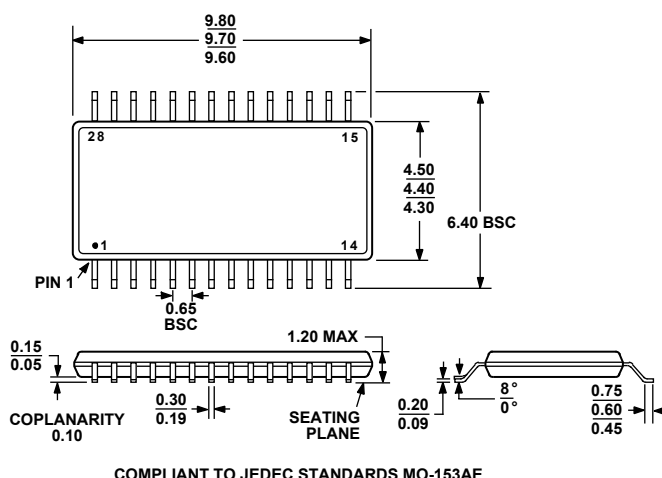
OUTLINE DIMENSIONS

Figure 48. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Option	Package Descriptions
AD7934BRU	−40°C to +85°C	±1	RU-28	Thin Shrink Small Outline Package (TSSOP)
AD7933BRU	−40°C to +85°C	±1	RU-28	Thin Shrink Small Outline Package (TSSOP)
EVAL-AD7934CB[2]				Evaluation Board
EVAL-AD7933CB[3]				Evaluation Board
EVAL-CONTROL BRD2[4]				Controller Board

[1] Linearity error here refers to integral linearity error.
[2] This can be used as a standalone evaluation board or in conjunction with the Evaluation Board Controller for evaluation/demonstration purposes.
[3] This can be used as a standalone evaluation board or in conjunction with the Evaluation Board Controller for evaluation/demonstration purposes.
[4] Evaluation Board Controller. This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. The following needs to be ordered to obtain a complete evaluation kit: the ADC Evaluation Board (EVAL-AD7934CB), the EVAL-CONTROL BRD2, and a 12 V ac transformer. See the EVAL-AD7933/34CB evaluation board technical note for more details.

NOTES

**ANALOG
DEVICES**

w w w . a n a l o g . c o m