# Schottky Barrier Diodes

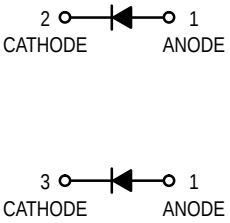
Designed primarily for UHF mixer applications but suitable also for use in detector and ultra–fast switching circuits. Supplied in an inexpensive plastic package for low–cost, high–volume consumer requirements. Also available in Surface Mount package.

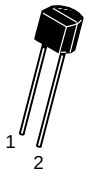
- Low Noise Figure — 6.0 dB Typ @ 1.0 GHz
- Very Low Capacitance — Less Than 1.0 pF @ Zero Volts
- High Forward Conductance — 0.5 Volts (Typ) @ $I_F$ = 10 mA

**MBD101**
**MMBD101LT1**

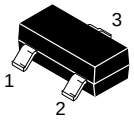
**Motorola Preferred Devices**

**SILICON SCHOTTKY BARRIER DIODES**




**CASE 182–02, STYLE 1**
**(TO–226AC)**




**CASE 318–08, STYLE 8**
**SOT–23 (TO–236AB)**

**MAXIMUM RATINGS**

| | | MBD101 | MMBD101LT1 | |
|---|---|---|---|---|
| **Rating** | **Symbol** | **Value** | | **Unit** |
| Reverse Voltage | $V_R$ | 7.0 | | Volts |
| Forward Power Dissipation<br>@ $T_A$ = 25°C<br>Derate above 25°C | $P_F$ | <br>280<br>2.2 | <br>225<br>1.8 | <br>mW<br>mW/°C |
| Junction Temperature | $T_J$ | +150 | | °C |
| Storage Temperature Range | $T_{stg}$ | –55 to +150 | | °C |

**DEVICE MARKING**

MMBD101LT1 = 4M

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Reverse Breakdown Voltage<br>($I_R$ = 10 μAdc) | $V_{(BR)R}$ | 7.0 | 10 | — | Volts |
| Diode Capacitance<br>($V_R$ = 0, f = 1.0 MHz, Note 1) | $C_T$ | — | 0.88 | 1.0 | pF |
| Forward Voltage(1)<br>($I_F$ = 10 mAdc) | $V_F$ | — | 0.5 | 0.6 | Volts |
| Reverse Leakage<br>($V_R$ = 3.0 Vdc) | $I_R$ | — | 0.02 | 0.25 | μAdc |

NOTE: MMBD101LT1 is also available in bulk packaging. Use MMBD101L as the device title to order this device in bulk.

**Preferred** devices are Motorola recommended choices for future use and best overall value.

Thermal Clad is a registered trademark of the Berquist Company.

## TYPICAL CHARACTERISTICS

($T_A$ = 25°C unless noted)

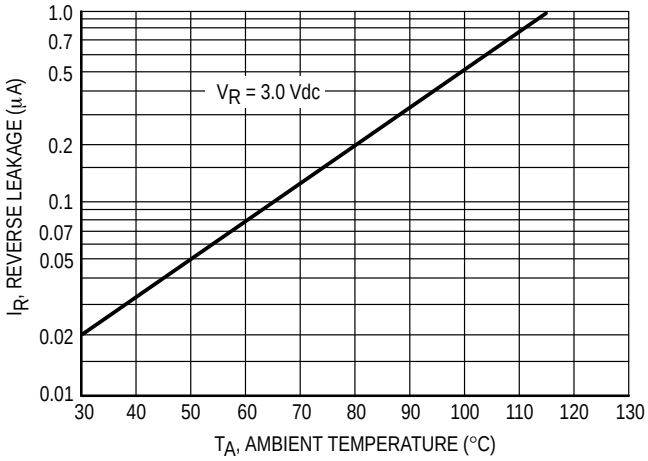



**Figure 1. Reverse Leakage**

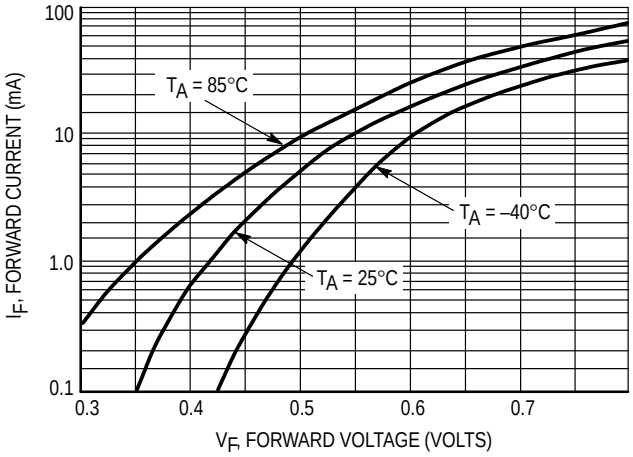



**Figure 2. Forward Voltage**

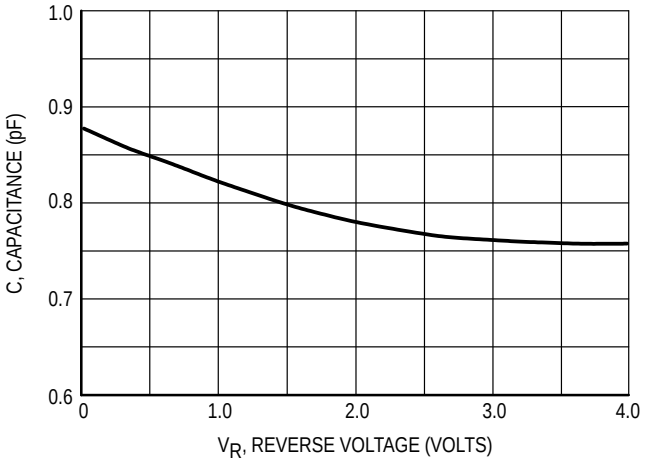



**Figure 3. Capacitance**

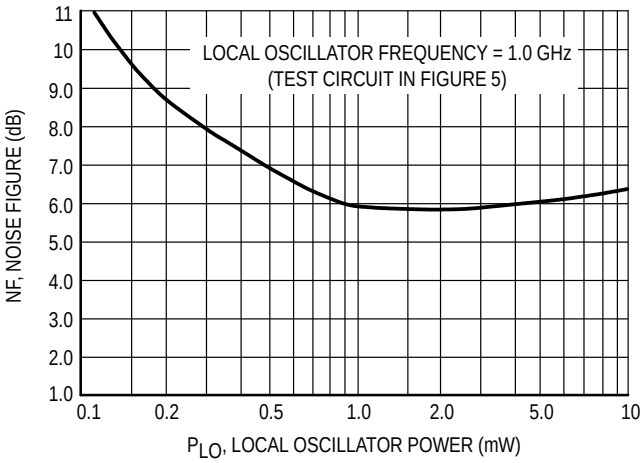



**Figure 4. Noise Figure**

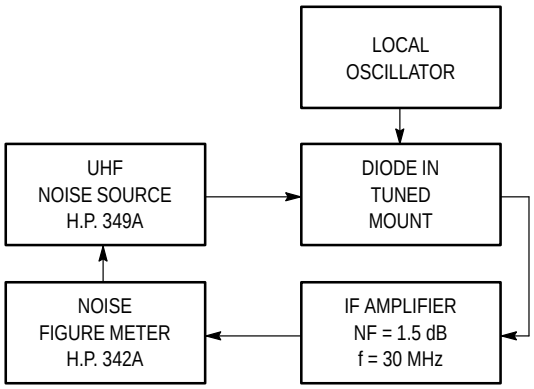



**Figure 5. Noise Figure Test Circuit**

**NOTES ON TESTING AND SPECIFICATIONS**

Note 1 — $C_C$ and $C_T$ are measured using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

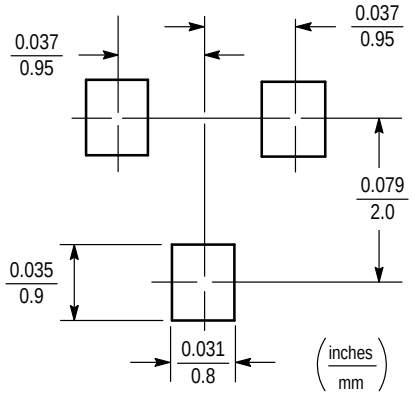
Note 2 — Noise figure measured with diode under test in tuned diode mount using UHF noise source and local oscillator (LO) frequency of 1.0 GHz. The LO power is adjusted for 1.0 mW. IF amplifier NF = 1.5 dB, f = 30 MHz, see Figure 5.

Note 3 — $L_S$ is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).

# INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




**SOT–23**

## SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–23 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

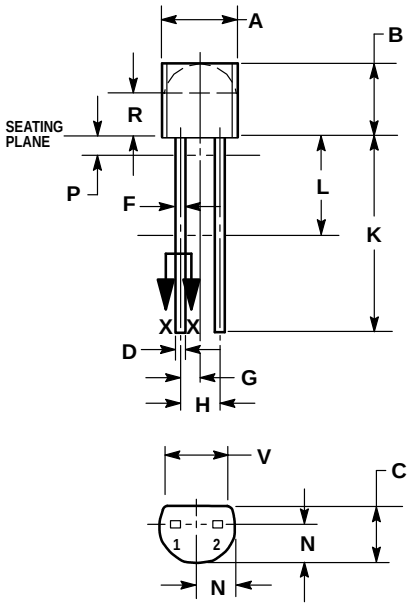
## SOLDERING PRECAUTIONS

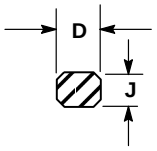
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## PACKAGE DIMENSIONS



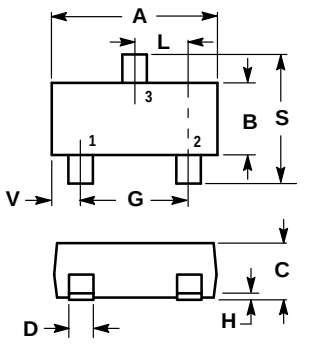

SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND ZONE R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSIONS D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIM K MINIMUM.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.175 | 0.205 | 4.45 | 5.21 |
| B | 0.170 | 0.210 | 4.32 | 5.33 |
| C | 0.125 | 0.165 | 3.18 | 4.49 |
| D | 0.016 | 0.022 | 0.41 | 0.56 |
| F | 0.016 | 0.019 | 0.407 | 0.482 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.100 BSC | | 3.54 BSC | |
| J | 0.014 | 0.016 | 0.36 | 0.41 |
| K | 0.500 | — | 12.70 | — |
| L | 0.250 | — | 6.35 | — |
| N | 0.080 | 0.105 | 2.03 | 2.66 |
| P | — | 0.050 | — | 1.27 |
| R | 0.115 | — | 2.93 | — |
| V | 0.135 | — | 3.43 | — |

STYLE 1:
PIN 1. ANODE
2. CATHODE

**CASE 182–02**
**(TO–226AC)**
**ISSUE H**




STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.1102 | 0.1197 | 2.80 | 3.04 |
| B | 0.0472 | 0.0551 | 1.20 | 1.40 |
| C | 0.0350 | 0.0440 | 0.89 | 1.11 |
| D | 0.0150 | 0.0200 | 0.37 | 0.50 |
| G | 0.0701 | 0.0807 | 1.78 | 2.04 |
| H | 0.0005 | 0.0040 | 0.013 | 0.100 |
| J | 0.0034 | 0.0070 | 0.085 | 0.177 |
| K | 0.0140 | 0.0285 | 0.35 | 0.69 |
| L | 0.0350 | 0.0401 | 0.89 | 1.02 |
| S | 0.0830 | 0.1039 | 2.10 | 2.64 |
| V | 0.0177 | 0.0236 | 0.45 | 0.60 |

**CASE 318–08**
**ISSUE AF**
**SOT–23 (TO–236AB)**



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