TDA8295

Digital global standard low IF demodulator for analog TV and FM radio

Rev. 01 — 4 February 2008 | Product data sheet

1. General description

The TDA8295 is an alignment-free digital multistandard vision and sound low IF signal PLL demodulator for positive and negative video modulation including AM and FM mono sound processing. It can be used in all countries worldwide for M/N, B/G/H, I, D/K, L and L-accent standard. CVBS and SSIF/mono audio is provided via two DACs. FM radio preprocessing is included for simple interfacing with demodulator/stereo decoder backends.

The IC is especially suited for the application with the NXP Silicon Tuner TDA8275A or TDA1827x.

All the processing is done in the digital domain.

The chip has an ‘easy programming’ mode to make the I²C-bus protocol very simple. In principle, only one bit sets the proper standard with recommended content. However, if this is not suitable, free programming is always possible.

2. Features

- Digital IF demodulation for all analog TV standards worldwide (M/N, B/G/H, D/K, I, L and L-accent standard)
- Multistandard true synchronous demodulation with active carrier regeneration
- Alignment-free
- 16 MHz typical reference frequency input (from low IF tuner) or operating as crystal oscillator
- Internal PLL synthesizer which allows the use of a low-cost crystal (typically 16 MHz)
- Especially suited for the NXP Silicon Tuner TDA8275A or TDA1827x
- No SAW filter needed
- Low application effort and external component count in combination with the TDA8275A or TDA1827x
- Pin compatible with predecessor TDA8290
- Simple upgrade of TDA8290 possible
- 12-bit IF ADC on chip running with 54 MHz or 27 MHz
- Two 10-bit DACs on chip for CVBS and SSIF or audio
- Easy programming for I²C-bus
- High flexibility due to various I²C-bus programming registers
- I²C-bus interface and I²C-bus feed-through for tuner programming
- Four I²C-bus addresses selectable via two external pins

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- Gated IF AGC acting on black level by using H/V PLL or peak IF AGC (I^2C-bus selectable)
- Internal digital logarithmic IF AGC amplifier with up to 48 dB gain and 68 dB control range
- Peak search tuner IF AGC for optimal adaptive drive of the IF ADC
- Switchable IF PLL and IF AGC loop bandwidths
- Precise AFC and lock detector
- Accurate group delay equalization for all standards
- Very robust IF demodulator coping with adverse field conditions
- Wide PLL pull-in range up to ±1660 kHz (I^2C-bus selectable)
- CVBS and SSIF or audio output with simple postfilter (capacitor only)
- CVBS gain levelling stage to provide nearly constant signal amplitude during overmodulation
- Video equalizer with eight settings
- Nyquist filter in video baseband
- Excellent video S/N (typically 62 dB weighted)
- High selectivity video low-pass filter for all standards
- Low video into sound crosstalk
- Sound performance comparable to QSS single reference concepts
- AM/FM mono sound demodulator
- Switchable de-emphasis
- Excellent FM sound
- Good AM sound
- High FM Deviation mode for China
- Preprocessing of FM radio (mono and stereo) with highly selective digital band-pass filter
- No ceramic filter or external components needed for FM radio
- FM radio available in mono
- Automatic or forced mute for mono sound
- Automatic or forced blank for video
- Mostly digital FIR filter implementation (NSC notches and video low-pass filters)
- Three GPIO pins
- Low total power dissipation (typically 324 mW)
- Standby mode (typically 7 mW)
- 40-pin HVQFN package
- CMOS technology (0.12 µm 1.2 V and 3.3 V)

3. Applications

- PC TV applications
- DVD recorders

4. Quick reference data

Table 1. Quick reference data

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power supply							
$V_{DD(1V2)}$	supply voltage (1.2 V)	digital and analog		1.08	1.2	1.32	V
$V_{DD(3V3)}$	supply voltage (3.3 V)	digital and analog		2.97	3.3	3.63	V
$I_{DD(tot)(1V2)}$	total supply current (1.2 V)			-	28	33	mA
$I_{DD(tot)(3V3)}$	total supply current (3.3 V)		[1]	-	125	136	mA
P_{tot}	total power dissipation	default settings; 75 Ω drive; f_s = 54 MHz at ADC; including DAC loads; R_{RSET} = 1 kΩ	[1]	-	434	490	mW
		Power-save mode; f_s = 54 MHz at ADC; including DAC loads; R_{RSET} = 2 kΩ; see Section 13.6	[2]	-	324	369	mW
		Standby mode		-	7	10	mW
IF input							
$V_{i(p-p)}$	peak-to-peak input voltage	for full-scale ADC input (0 dBFS)		1.8	2.0	2.2	V
V_i	input voltage	operational input related to ADC full scale; all standards; sum of all signals		–3	–3	–3	dBFS
f_i	input frequency	PC / SC1					
		M/N standard		-	5.75 / 1.25	-	MHz
		B standard		-	6.75 / 1.25	-	MHz
		G/H standard		-	7.75 / 2.25	-	MHz
		I standard		-	7.75 / 1.75	-	MHz
		DK and L standard		-	7.75 / 1.25	-	MHz
		L-accent standard		-	1.25 / 7.75	-	MHz
		FM radio		-	1.25	-	MHz
Carrier recovery FPLL							
$B_{-3dB(cl)}$	closed-loop –3 dB bandwidth	wide		60	60	60	kHz
Δf_{pullin}	pull-in frequency range		[3]	±830	±830	±830	kHz
$m_{over(PC)}$	picture carrier overmodulation index	black for L/L-accent standard; flat field white else		115	117	-	%
IF demodulation (video equalizer in Flat mode)							
$\alpha_{sup(stpb)}$	stop-band suppression	video low-pass filter (M/N, B/G/H, I, D/K, L/L-accent standard)		-	–60	-	dB
$t_{ripple(GDE)}$	group delay equalizer ripple time	peak value for B/G/H half, D/K half, I flat, M (FCC) full, L/L-accent full standard		-	20	40	ns

Table 1. Quick reference data *…continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CVBS output						
$V_{o(p-p)}$	peak-to-peak output voltage	negative PC modulation (all standards except L/L-accent); 75 Ω DC load; sync-white modulation				
		90 % (nominal)	0.8	1.0	1.2	V
		positive PC modulation (L/L-accent standard); 75 Ω DC load; sync-white modulation				
		97 % (nominal)	0.8	1.0	1.2	V
$B_{video(-3dB)}$	–3 dB video bandwidth	overall video response; CVBS equalizer flat				
		all standards except M/N	4.8	4.85	-	MHz
		M/N standard	3.9	4.05	-	MHz
$\alpha_{resp(f)}$	frequency response	video equalizer; 8 equally spaced settings; value at 3.9 MHz	–5	-	+4.5	dB
G_{dif}	differential gain	*"ITU-T J.63 line 330"*	-	1.5	3	%
φ_{dif}	differential phase	*"ITU-T J.63 line 330"*	-	1.5	3	deg
$(S/N)_w$	weighted signal-to-noise ratio	all standards; unified weighting filter (*"ITU-T J.61"*); PC at –6 dBFS	58	62	-	dB
SSIF/mono sound output						
$V_{o(SSIF)(RMS)}$	RMS SSIF output voltage	1 kΩ DC or AC load; no modulation; PC / SC1 = 13 dB; scaled linearly for all other ratios				
		all standards except B/G/H	30	35	40	mV
		B/G/H standard	27	32	37	mV
		FM radio (single carrier)	460	530	610	mV
$V_{o(AF)(RMS)}$	RMS AF output voltage	1 kΩ DC or AC load				
		M standard; 54 % modulation degree (±13.5 kHz FM deviation before pre-emphasis)	125	143	165	mV
		B, G/H, I, D, K standard; 54 % modulation degree (±27 kHz FM deviation before pre-emphasis)	125	143	165	mV
$\alpha_{hr(AF)}$	AF headroom	before clipping; 1 kΩ DC or AC load				
		M standard; related to ±25 kHz peak deviation before pre-emphasis	7	7	7	dB
		B, G/H, I, D, K standard; related to ±50 kHz peak deviation before pre-emphasis	7	7	7	dB
THD	total harmonic distortion	FM; for 50 kHz deviation before pre-emphasis (25 kHz for M standard)	-	0.1	0.2	%
		AM; m = 80 %	-	0.6	1	%

Table 1. Quick reference data *…continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$B_{AF(-3dB)}$	−3 dB AF bandwidth	AM	20	27	-	kHz
		FM	40	50	-	kHz
$(S/N)_{w(AF)}$	AF weighted signal-to-noise ratio	via internal mono sound demodulator; *"ITU-R BS.468-4"*; FM mode related to 27 kHz deviation before pre-emphasis; 10 % residual PC; SC1				
		color bar picture	54	58	-	dB
		via internal mono sound demodulator; *"ITU-R BS.468-4"*; AM; m = 54 %; 3 % residual PC; SC1				
		color bar picture	43	46	-	dB

[1] 50 % ADC current; 100 % video DAC current; 50 % sound DAC current.

[2] 50 % ADC current; 50 % video DAC current; 25 % sound DAC current.

[3] The pull-in range can be doubled to ±1660 kHz by I^2C-bus register like described in Table 16. Then the AFC read-out has 256 steps.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8295HN	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1

6. Functional diagram

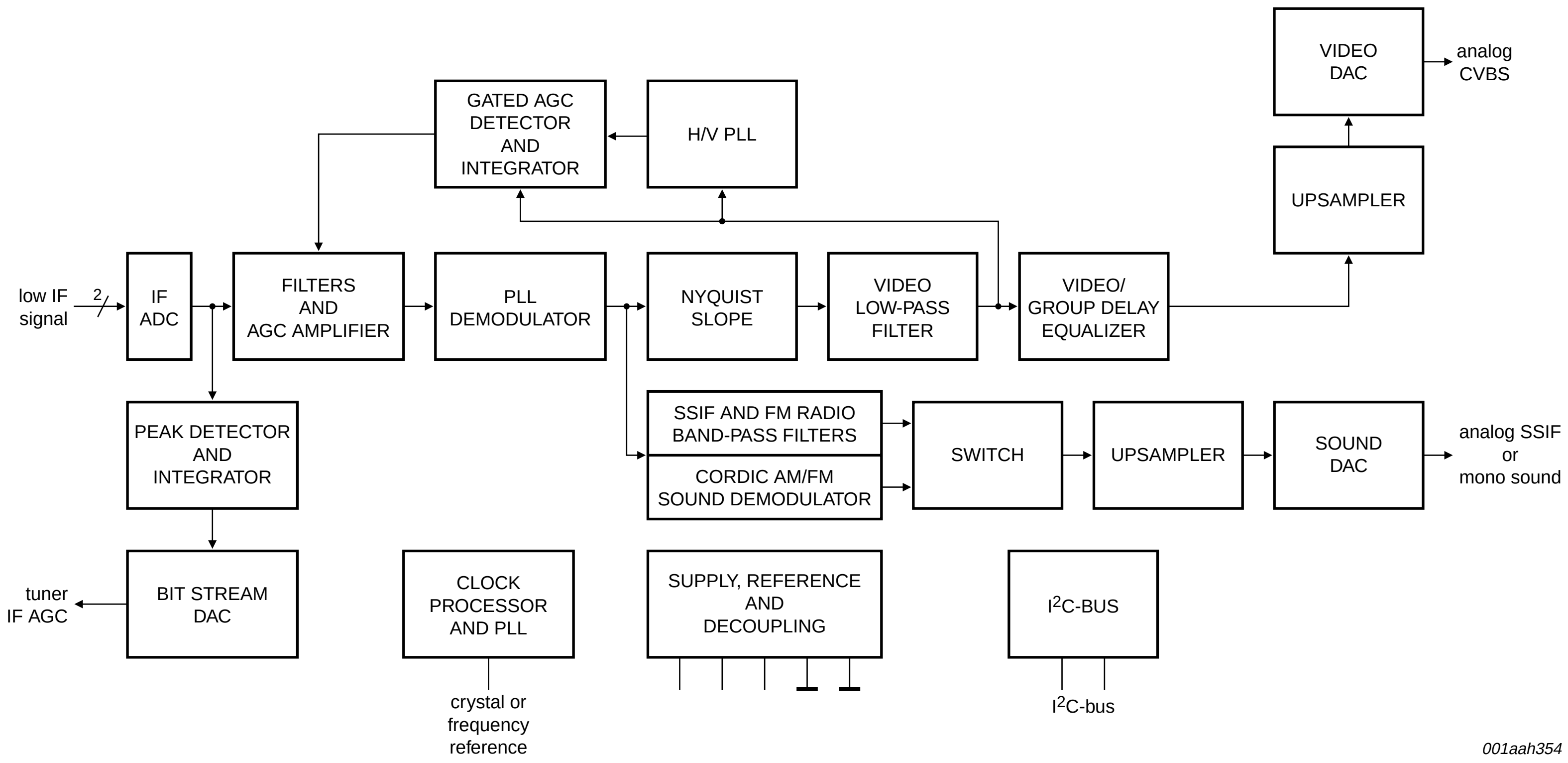


Fig 1. Functional diagram of TDA8295

7. Pinning information

7.1 Pinning

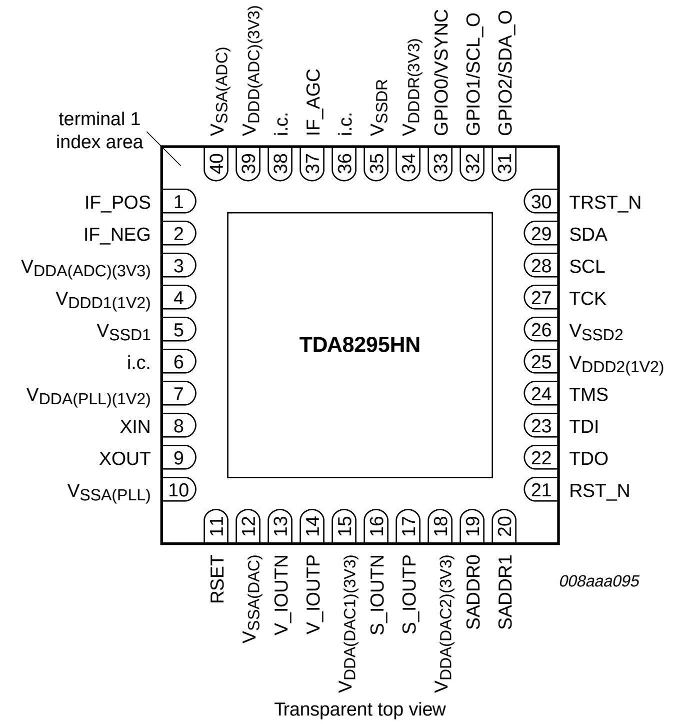


Fig 2. Pin configuration for HVQFN40

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol
1	IF_POS	2	IF_NEG
3	$V_{DDA(ADC)(3V3)}$	4	$V_{DDD1(1V2)}$
5	V_{SSD1}	6	i.c.
7	$V_{DDA(PLL)(1V2)}$	8	XIN
9	XOUT	10	$V_{SSA(PLL)}$
11	RSET	12	$V_{SSA(DAC)}$
13	V_IOUTN	14	V_IOUTP
15	$V_{DDA(DAC1)(3V3)}$	16	S_IOUTN
17	S_IOUTP	18	$V_{DDA(DAC2)(3V3)}$
19	SADDR0	20	SADDR1
21	RST_N	22	TDO
23	TDI	24	TMS
25	$V_{DDD2(1V2)}$	26	V_{SSD2}
27	TCK	28	SCL
29	SDA	30	TRST_N

Table 3. Pin allocation table *...continued*

Pin	Symbol	Pin	Symbol
31	GPIO2/SDA_O	32	GPIO1/SCL_O
33	GPIO0/VSYNC	34	$V_{DDDR(3V3)}$
35	V_{SSDR}	36	i.c.
37	IF_AGC	38	i.c.
39	$V_{DDD(ADC)(3V3)}$	40	$V_{SSA(ADC)}$

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type[1][2]	Description
Reset			
RST_N	21	I	The RST_N input is asynchronous and active LOW, and clears the TDA8295. When RST_N goes LOW, the circuit immediately enters its Reset mode and normal operation will resume four XIN signal falling edges later after RST_N returns HIGH. Internal register contents are all initialized to their default values. The minimum width of RST_N at LOW level is four XIN clock periods.
Reference			
XIN	8	I	Crystal oscillator input pin. In Slave mode (typically), the XIN input simply receives a 16 MHz clock signal from an external device (typically from the TDA8275A or TDA1827x). In Oscillator mode, a fundamental 16 MHz (typically) crystal is connected between pin XIN and pin XOUT.
XOUT	9	O	Crystal oscillator output pin. In Slave mode, the XOUT output is not connected. In Oscillator mode a fundamental 16 MHz (typically) crystal is connected between pin XIN and pin XOUT.
I²C-bus			
SDA	29	I/O, OD	I²C-bus bidirectional serial data. SDA is an open-drain output and therefore requires an external pull-up resistor (typically 4.7 kΩ).
SCL	28	I	I²C-bus clock input. SCL is nominally a square wave with a maximum frequency of 400 kHz. It is generated by the system I²C-bus master.
SADDR0	19	I	These two bits allow to select four possible I²C-bus addresses, and therefore permits to use several TDA8295 in the same application and/or to avoid conflict with other ICs. The complete I²C-bus address is: 1, 0, 0, SADDR1, 0, 1, SADDR0 (see also Section 9.1).
SADDR1	20	I	
I²C-bus feed-through switch or GPIO			
GPIO2/SDA_O	31	I/O, OD	SDA_O is equivalent to SDA but can be 3-stated by I²C-bus programming. It is the output of a switch controlled by I2CSW_EN parameter. SDA_O is an open-drain output and therefore requires an external pull-up resistor (see Section 9.3.20).
GPIO1/SCL_O	32	I/O, OD	SCL_O is equivalent to SCL input but can be 3-stated by I²C-bus programming. SCL_O is an open-drain output and therefore requires an external pull-up resistor (see Section 9.3.20). For proper functioning of the I²C-bus feed-through, a capacitor C = 33 pF to GND must be added (see Section 13.6).
V-sync or GPIO			
GPIO0/VSYNC	33	I/O, OD	vertical synchronization pulse needed for the NXP Silicon Tuner (see Section 9.3.20)
Tuner IF AGC			
IF_AGC	37	I/O, OD, T	tuner IF AGC output

Table 4. Pin description *…continued*

Symbol	Pin	Type[1][2]	Description
Boundary scan			
TMS	24	I	Test mode select provides the logic levels needed to change the TAP controller from state to state during the boundary scan test.
TRST_N	30	I	Test reset is used to reset the TAP controller (active LOW). Grounding is mandatory in Functional mode.
TCK	27	I	Test clock is used to drive the TAP controller.
TDI	23	I	Test data input is the serial data input for the test data instruction.
TDO	22	O	Test data output is the serial test data output pin. The data is provided on the falling edge of TCK.
ADC			
IF_POS	1	AI	IF positive analog input for internal ADC
IF_NEG	2	AI	IF negative analog input for internal ADC
DAC			
V_IOUTP	14	AO	positive analog current output of the video output
V_IOUTN	13	AO	negative analog current output of the video output
S_IOUTP	17	AO	positive analog current output of the SSIF/mono sound output
S_IOUTN	16	AO	negative analog current output of the SSIF/mono sound output
RSET	11	I	External bias setting of the DACs. An external resistor (1 kΩ typical) has to be connected between RSET and the analog ground of the board. This resistor generates the current into the DACs and also defines the full scale output current. The total parasitic capacitance seen externally from the RSET pin has to be lower than 20 pF.
Supplies and grounds			
$V_{DDA(DAC1)(3V3)}$	15	PS	DAC1 (video DAC) and DAC reference module analog supply voltage (3.3 V typical)
$V_{DDA(DAC2)(3V3)}$	18	PS	DAC2 (sound DAC) analog supply voltage (3.3 V typical)
$V_{SSA(DAC)}$	12	GND	DAC reference module analog ground supply voltage (0 V typical)
$V_{DDA(ADC)(3V3)}$	3	PS	IF ADC analog supply voltage (3.3 V typical)
$V_{DDD(ADC)(3V3)}$	39	PS	IF ADC digital supply voltage (3.3 V typical)
$V_{SSA(ADC)}$	40	GND	ADC analog ground supply voltage (0 V typical)
$V_{DDD1(1V2)}$	4	PS	ADC, PLL and DACs digital supply voltage (1.2 V typical)
V_{SSD1}	5	GND	ADC, PLL and DACs digital ground supply voltage (0 V typical)
$V_{DDA(PLL)(1V2)}$	7	PS	crystal oscillator and clock PLL analog supply voltage (1.2 V typical)
$V_{SSA(PLL)}$	10	GND	crystal oscillator and clock PLL analog ground supply voltage (0 V typical)
$V_{DDD2(1V2)}$	25	PS	core digital supply voltage (1.2 V typical)
V_{SSD2}	26	GND	core digital ground supply voltage (0 V typical)
$V_{DDDR(3V3)}$	34	PS	ring digital supply voltage (3.3 V typical)
V_{SSDR}	35	GND	ring digital ground supply voltage (0 V typical)
Other pins			
i.c.	36	I	internally connected; connect to ground
i.c.	38	I	internally connected; connect to ground
i.c.	6	I	internally connected; connect to ground

[1] All digital inputs are 5 V tolerant (except pin XIN).

[2] The pin types are defined in Table 5.

Table 5. Pin type description

Type	Description
AI	analog input
AO	analog output
GND	ground
I	digital input
I/O	digital input and output
O	digital output
OD	open-drain output
PS	power supply
T	3-state

8. Functional description

8.1 IF ADC

The low IF spectrum (1 MHz to 10 MHz) from the Silicon Tuner TDA8725A or TDA1827x is fed symmetrically to the 12-bit IF ADC of the TDA8295, where it is sampled with 54 MHz or 27 MHz. All the anti-aliasing filtering is already done in the Silicon Tuner.

8.2 Filters

The internal filters permit to reduce the sampling rate to 13.5 MHz, and to form a complex signal to ease the effort of further signal processing. Before this, the DC offset (coming from the ADC) is removed.

In addition, standard dependent notch filters for the adjacent sound carriers protect the picture carrier PLL from malfunctioning and avoid disturbances (i.e. moire) becoming visible in the video output.

8.3 PLL demodulator

The second-order PLL is the core block of the whole IC. It is very robust against adverse field conditions, like excessive overmodulation, no residual carrier presence or unwanted phase or frequency modulation of the picture carrier. The PLL output is the synchronously demodulated channel.

The AFC data is available via the I^2C-bus.

8.4 Nyquist filter, video low-pass filter, video and group delay equalizer, video leveling

The afore-mentioned down-mixed complex signal at the mixer CORDIC output, already consisting of the demodulated content of the picture carrier together with the sound carriers (the so-called intercarriers), is running through a Nyquist filter to get a flat video response and is made real.

Afterwards, a video low-pass filter suppresses the sound carriers and other disturbers.

Next comes the equalizer circuit to remove the transmitter group delay predistortion.

A video leveling stage follows, which brings the output within the SCART specification (3dB overall), despite heavy overmodulation. The response time is made very slow.

Finally, a video equalizer allows to compensate the perhaps non-flat frequency response from the tuner or to change the overall video response according to customer wish (i.e. peaking or early roll-off).

8.5 Upsampler and video DAC

The filtered and compensated CVBS signal is connected to the oversampled 10-bit video DAC (f_s = 108 MHz) via an interpolation stage. The strong oversampling replaces a former complicated LCR postfiltering by a simple first-order RC low-pass filter to remove the DAC image frequencies sufficiently. This holds also for the sound DAC, described in Section 8.6.

8.6 SSIF/mono sound processing

The complex signal is routed via a band-pass and interpolation filter to the 10-bit sound DAC for the recovery of the second sound carriers (SSIF). A very sharp band-pass filter at 5.5 MHz is added in the FM Radio mode to remove neighbor channels. This also eases the dynamic burden on the following ADC in the demodulator/decoder chip. The afore-mentioned high-selectivity band-pass, which replaces the former ceramic filter, is located behind a frequency shifter. In there, the incoming wanted FM radio channel from the Silicon Tuner is changed from 1.25 MHz to 5.5 MHz.

Moreover, the complex signal is demodulated in a linear CORDIC detector and low-pass filtered to attenuate the video spectrum and the second sound carrier, respectively other disturbers above the intercarrier. The output of the linear CORDIC (phase information) is differentiated for getting the demodulated FM audio. The AM demodulation is executed in a synchronous fashion by using a narrow-band PLL demodulator.

A de-emphasis filter is implemented for FM standards, before the audio is interpolated to 108 MHz as in the CVBS case.

The mono audio is made available in the sound DAC via an I^2C-bus controlled selector in case the intercarrier path is not used for driving an external stereo demodulator.

However, if the mono audio output has to meet the SCART specification, an external cheap operational amplifier with 12 dB gain becomes necessary, because the low supply voltage for the TDA8295 doesn’t allow such high levels like 2 V (RMS) maximum.

8.7 Tuner IF AGC

This AGC controls the tuner IF AGC amplifier in the TDA8275A or TDA1827x in such a way, that the IF ADC is always running with a permanent headroom of 3 dB for the sum of all signals present at the ADC input. This ensures an always optimal exploitation of the dynamic range in the IF ADC.

The detection is done in peak Search mode during a field period. The attack time is made much faster than the decay time in order to avoid transient clipping effects in the IF ADC. This can happen during channel change or airplane flutter conditions.

The above wideband, slowly acting AGC loop (uncorrelated) is of first-order integral action. It is closed via the continuous tuner IF AGC amplifier in the Silicon Tuner via a bit stream DAC (PWM signal at 13.5 MHz, 27 MHz or 54 MHz) and an external and uncritical first-order RC low-pass.

8.8 Digital IF AGC

Common to both IF AGC concepts is the peak search algorithm as long as the H/V PLL is not locked. This is of advantage for the acquisition by avoiding hang-ups due to excessive overloading, so being able to leave the saturated condition by reducing the gain.

Two Detection modes are made available in the IC via I^{2}C-bus.

- Black level gated AGC:

  The first mode uses an IF AGC detector which is gated with a very robust and well-proven H/V sync PLL block on board. Gating occurs on the black level (most of the time on the back porch) of the video signal and the control is delivered after an error integration and exponential weighting to the internal IF AGC amplifier. This IF AGC amplifier, in fact a multiplier, has a control range of −20 dB to +48 dB.

- Peak AGC:

  A fast attack and slow decay action cares for a good and nearly clip-free transient behavior. This proved to be more robust for non-standard signals, like sync clipping along the transmitter/receiver chain.

  With respect to the IF AGC speed generally, only the gated black level or peak sync IF AGC can be made fast. However the peak search one, used for positive modulation standards (L and L-accent standard), is rather slow because the VITS is present only once in a field.

  The correlated or narrow-band AGC loop, closed via the continuous IF AGC amplifier in the TDA8295, is of first-order integral action and settles at a constant IF input level with a permanent headroom of 12 dB (picture carrier). This headroom is needed for the own sound carriers and the leaking neighbor (N – 1) spectrum.

8.9 Clock generation

Finally, either an external reference frequency (i.e. from the Silicon Tuner) or an own on-chip crystal oscillator in the TDA8295 feeds the internal PLL synthesizer to generate the necessary clock signals.

9. I^{2}C-bus control

9.1 Protocol of the I^{2}C-bus serial interface

The TDA8295 internal registers are accessible by means of the I^{2}C-bus serial interface. The SDA bidirectional pin is used as the data input/output pin and SCL as the clock input pin. The highest SCL speed is 400 kHz.

9.1.1 Write mode

S	BYTE 1	A	BYTE 2	A	BYTE 3	A		BYTE n	A	P
start	address 0	ack	start index	ack	data 1	ack	....	data n	ack	stop

001aad381

Fig 3. I²C-bus Write mode

Table 6. Address format

7	6	5	4	3	2	1	0
1	0	0	SADDR1	0	1	SADDR0	R/W

Table 7. I²C-bus transfer description

Field	Bit	Description
S	-	START condition
Byte 1	7 to 5	device address
	4	SADDR1
	3 and 2	device address
	1	SADDR0
	0	R/W = 0 for write action
A	-	acknowledge
Byte 2	7 to 0	start index
A	-	acknowledge
Byte 3	7 to 0	data 1
A	-	acknowledge
:		
Byte n	7 to 0	data n
A	-	acknowledge
P	-	STOP condition

S	BYTE 1	A	BYTE 2	A	BYTE 3	A	P
start	1000 0100	ack	0000 0001	ack	0000 0010	ack	stop

001aah355

a. Address 84h, write 02h in register 01h

S	BYTE 1	A	BYTE 2	A	BYTE 3	A	BYTE 4	A	P
start	1000 0100	ack	0000 0010	ack	0000 0101	ack	0000 0100	ack	stop

001aah356

b. Address 84h, write 05h in register 02h and 04h in register 03h

Fig 4. Examples I²C-bus Write mode

9.1.2 Read mode

S	BYTE 1	A	BYTE 2	A	S	BYTE 3	A	BYTE 4	A		BYTE n	A	P
start	address 0	ack	start index	ack	start	address 1	ack	value 1	ack	....	value n	ack	stop

001aad423

Fig 5. I^2C-bus Read mode

Table 8. I^2C-bus transfer description

Field	Bit	Description
S	-	START condition
Byte 1	7 to 5	device address
	4	SADDR1
	3 and 2	device address
	1	SADDR0
	0	R/W = 0 for write action
A	-	acknowledge
Byte 2	7 to 0	start index
A	-	acknowledge
S	-	START condition (without stop before)
Byte 3	7 to 5	device address
	4	SADDR1
	3 and 2	device address
	1	SADDR0
	0	R/W = 1 for read action
A	-	acknowledge
Byte 4	7 to 0	value 1
A	-	acknowledge
:		
Byte n	7 to 0	value n
A	-	acknowledge
P	-	STOP condition

S	BYTE 1	A	BYTE 2	A	S	BYTE 3	A	BYTE 4	A	BYTE 5	A	P
start	1000 0100	ack	0000 0010	ack	start	1000 0101	ack	0000 0101	ack	0000 0100	ack	stop

001aah357

Address 84h, read register 02h with value 05h and read register 03h with value 04h

Fig 6. Example I^2C-bus Read mode

9.2 Register overview

The TDA8295 internal registers are accessible by means of the I^2C-bus serial interface as described in Section 9.1. In Table 9 and Table 10 an overview of all the registers is given, the register description can be found in Section 9.3.

Table 9. I^{2}C-bus registers

Index	Name	7 (MSB)	6	5	4	3	2	1	0 (LSB)
00h	STANDARD	STANDARD[7:0]							
01h	EASY_PROG	-	-	-	-	-	-	-	ACTIVE
02h	DIV_FUNC	AGC_SEL	AGC_TRI	-	-	0	POL_DET	VID_MOD	IF_SWAP
03h	ADC_HEADR	-	-	-	-	ADC_HEADR[3:0]			
04h	PC_PLL_FUNC	PC_PLL_BW[4:0]					PLL_ON	PULL_IN	CAR_DET
05h	PC_PLL_THRES	-	-	-	-	PH_ERR_THRES[3:0]			
06h	PC_PLL_WGT	PHASE_PER	PHASE_GAIN[6:0]						
07h	PC_FLL_FUNC	FLL_ON	LIM_ON	FLL_LIM[5:0]					
08h	CARDET_LEVEL	-	-	-	CAR_DET_LVL[4:0]				
09h	DTO_PC_LOW	DTO_PC[7:0]							
0Ah	DTO_PC_MID	DTO_PC[15:8]							
0Bh	DTO_PC_HIGH	DTO_PC[23:16]							
0Ch	DTO_SC_LOW	DTO_SC[7:0]							
0Dh	DTO_SC_MID	DTO_SC[15:8]							
0Eh	DTO_SC_HIGH	DTO_SC[23:16]							
0Fh	FILTERS_1	VID_FILT[2:0]			NOTCH_FILT[4:0]				
10h	FILTERS_2	-	-	-	DC_NOTCH	SBP[3:0]			
11h	GRP_DELAY	-	-	-	GRP_DEL[4:0]				
12h	D_IF_AGC_SET_1	D_IF_AGC_ CORR	D_IF_AGC_ MODE	D_IF_AGC_AVG[4:0]					RST_INT
13h	D_IF_AGC_SET_2	D_AGC_ERR_ LIM	D_IF_AGC_BW[6:0]						
14h	D_IF_AGC_FORCE	D_FORCE	D_FORCE_VAL[6:0]						
15h	T_IF_AGC_SET	POL_TIF	T_IF_AGC_SPEED[6:0]						
16h	T_IF_AGC_LIM	UP_LIM[3:0]				LOW_LIM[3:0]			
17h	T_IF_AGC_FORCE	T_FORCE	T_FORCE_VAL[6:0]						
18h	T_IF_AGC_FS	-	-	-	-	-	T_IF_AGC_FS[2:0]		
19h to 1Bh	reserved	reserved							
1Ch	V_SYNC_DEL	VS_WIDTH[1:0]		VS_POL	VS_DEL[4:0]				
1Dh	CVBS_SET	-	-	-	-	-	FOR_BLK	AUTO_BLK	VID_LVL

Table 9. **I²C-bus registers** *…continued*

Index	Name	7 (MSB)	6	5	4	3	2	1	0 (LSB)
1Eh	CVBS_LEVEL	CVBS_LVL[7:0]							
1Fh	CVBS_EQ	CVBS_EQ[7:0]							
20h	SOUNDSET_1	-	AM_FM_SND[1:0]		DEEMPH[4:0]				
21h	SOUNDSET_2	-	-	-	HD_DK	FOR_MUTE	AUTO_MUTE	SSIF_SND[1:0]	
22h	SOUND_LEVEL	-	-	-	SND_LVL[4:0]				
23h	SSIF_LEVEL	-	-	-	SSIF_LVL[4:0]				
24h	ADC_SAT	ADC_SAT[7:0]							
25h	AFC	AFC[7:0]							
26h	HVPLL_STAT	-	-	NOISE_DET	MAC_DET	FIDT	V_LOCK	F_H_LOCK	N_H_LOCK
27h	D_IF_AGC_STAT	D_IF_AGC_STAT[7:0]							
28h	T_IF_AGC_STAT	T_IF_AGC_STAT[7:0]							
29h	reserved	reserved							
2Ah	ANALOG_DEBUG	-	-	-	-	-	-	ADC_TEST	DAC_TEST
2Bh to 2Eh	not used	-	-	-	-	-	-	-	-
2Fh	IDENTITY	IDENTITY[7:0]							
30h	CLB_STDBY	-	-	-	-	-	-	STDBY	CLB
31h	reserved	-	-	-	-	reserved			
32h	ANALOG_STAT	-	LOAD_DACV	LOAD_DACS	PLL_LOCK	reserved			
33h	ADC_CTL	GAINSET	CS[2:0]			DCIN	TWOS	SLEEP	PD_ADC
34h	ADC_CTL_2	-	-	-	-	-	-	AD_PLL_BYP	AD_SR54M
35h	VIDEODAC_CTL	0	B_DA_V[5:0]						PD_DA_V
36h	AUDIODAC_CTL	0	B_DA_S[5:0]						PD_DA_S
37h	DAC_REF_CLK_CTL	-	DA_CLK_INV	DA_PLL_BYP	B_REF[3:0]				PD_DA_REF
38h	PLL_REG00	0	0	PLL_AUTO	0	0	0	0	0
39h to 3Bh	not used	-	-	-	-	-	-	-	-
3Ch	PLL_REG04	-	-	-	-	-	0	0	0
3Dh	not used	-	-	-	-	-	-	-	-
3Eh	PLL_REG06	0	CLK_EN	BYP_PLL	DIRECTO	DIRECTI	0	0	PD_PLL

Table 9. I²C-bus registers *…continued*

Index	Name	7 (MSB)	6	5	4	3	2	1	0 (LSB)
3Fh	PLL_REG07	-	0	0	0	0	0	0	0
40h	PLL_REG08	MSEL[7:0]							
41h	PLL_REG09	NSEL[6:0]							0
42h	PLL_REG10	0	0	0	PSEL[4:0]				
43h	XTALOSC_CTL	-	-	-	-	-	HF	0	0
44h	GPIOREG_0	GP1_CF[3:0]				GP0_CF[3:0]			
45h	GPIOREG_1	I2CSW_EN	I2CSW_ON	-	-	GP2_CF[3:0]			
46h	GPIOREG_2	CLK_INV_GP2	CLK_INV_GP1	CLK_INV_GP0	-	-	GP2_VAL	GP1_VAL	GP0_VAL

Table 10. I²C-bus register reference

Index	Name	I²C-bus access	Default value	Reference
00h	STANDARD	R/W	01h	Table 11
01h	EASY_PROG	R/W	00h	Table 12
02h	DIV_FUNC	R/W	04h	Table 14
03h	ADC_HEADR	R/W	01h	Table 15
04h	PC_PLL_FUNC	R/W	27h	Table 16
05h	PC_PLL_THRES	R/W	04h	Table 17
06h	PC_PLL_WGT	R/W	10h	Table 18
07h	PC_FLL_FUNC	R/W	84h	Table 19
08h	CARDET_LEVEL	R/W	08h	Table 20
09h	DTO_PC_LOW	R/W	85h	Table 21
0Ah	DTO_PC_MID	R/W	F6h	Table 21
0Bh	DTO_PC_HIGH	R/W	92h	Table 21
0Ch	DTO_SC_LOW	R/W	55h	Table 22
0Dh	DTO_SC_MID	R/W	55h	Table 22
0Eh	DTO_SC_HIGH	R/W	55h	Table 22
0Fh	FILTERS_1	R/W	21h	Table 23
10h	FILTERS_2	R/W	11h	Table 24
11h	GRP_DELAY	R/W	01h	Table 25
12h	D_IF_AGC_SET_1	R/W	A0h	Table 26
13h	D_IF_AGC_SET_2	R/W	90h	Table 27
14h	D_IF_AGC_FORCE	R/W	67h	Table 28
15h	T_IF_AGC_SET	R/W	88h	Table 29
16h	T_IF_AGC_LIM	R/W	F0h	Table 30
17h	T_IF_AGC_FORCE	R/W	3Fh	Table 31
18h	T_IF_AGC_FS	R/W	02h	Table 32
19h	reserved	R/W	88h	-
1Ah	reserved	R/W	80h	-
1Bh	reserved	R/W	00h	-
1Ch	V_SYNC_DEL	R/W	6Fh	Table 33
1Dh	CVBS_SET	R/W	01h	Table 34
1Eh	CVBS_LEVEL	R/W	73h	Table 35
1Fh	CVBS_EQ	R/W	08h	Table 36
20h	SOUNDSET_1	R/W	21h	Table 37
21h	SOUNDSET_2	R/W	02h	Table 38
22h	SOUND_LEVEL	R/W	08h	Table 39
23h	SSIF_LEVEL	R/W	04h	Table 40
24h	ADC_SAT	R	-	Table 41
25h	AFC	R	-	Table 42
26h	HVPLL_STAT	R	-	Table 44
27h	D_IF_AGC_STAT	R	-	Table 45
28h	T_IF_AGC_STAT	R	-	Table 46

Table 10. I²C-bus register reference *...continued*

Index	Name	I²C-bus access	Default value	Reference
29h	reserved	R	-	-
2Ah	ANALOG_DEBUG	R/W	00h	Table 47
2Bh to 2Eh	not used	-	-	-
2Fh	IDENTITY	R	-	Table 48
30h	CLB_STDBY	R/W	01h	Table 49
31h	reserved	R/W	00h	-
32h	ANALOG_STAT	R	-	Table 50
33h	ADC_CTL	R/W	24h	Table 51
34h	ADC_CTL_2	R/W	01h	Table 52
35h	VIDEODAC_CTL	R/W	7Eh	Table 53
36h	AUDIODAC_CTL	R/W	00h	Table 54
37h	DAC_REF_CLK_CTL	R/W	00h	Table 55
38h	PLL_REG00	R/W	20h	Table 56
39h to 3Bh	not used	-	-	-
3Ch	PLL_REG04	R/W	00h	Table 57
3Dh	not used	R/W	-	-
3Eh	PLL_REG06	R/W	61h	Table 58
3Fh	PLL_REG07	R/W	00h	Table 60
40h	PLL_REG08	R/W	1Ah	Table 60
41h	PLL_REG09	R/W	02h	Table 60
42h	PLL_REG10	R/W	01h	Table 60
43h	XTALOSC_CTL	R/W	00h	Table 61
44h	GPIOREG_0	R/W	11h	Table 62
45h	GPIOREG_1	R/W	01h	Table 63
46h	GPIOREG_2	R/W	07h	Table 65

9.3 Register description

If registers (or bit groups contained in registers) are programmed with invalid values, i.e. values different from those described in the tables below, the default behavior is chosen for the related block.

9.3.1 Standard setting with easy programming

With the implemented ‘easy programming’, only one bit sets the TV or FM radio standard with recommended register content. If not suitable however, any of these registers can be written with other settings. With the rising edge of the bit ACTIVE, the registers 02h to 23h are programmed internally with the standard dependent settings according to Table 13. The content of registers with address 24h and higher is untouched.

Table 11. STANDARD register (address 00h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 0	STANDARD[7:0]	R/W		TV or FM radio standard selection (easy programming)
			0000 0001*	M/N standard
			0000 0010	B standard
			0000 0100	G/H standard
			0000 1000	I standard
			0001 0000	D/K standard
			0010 0000	L standard
			0100 0000	L-accent standard
			1000 0000	FM radio

Table 12. EASY_PROG register (address 01h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 1	-	R/W	-	not used
0	ACTIVE	R/W		With the rising edge of this bit, the registers 02h to 23h are programmed with the standard dependent settings (see Table 13).
			0*	no action
			1	no action
			0 to 1	activate easy programming

Example: To set the device to B standard e.g., please do the following steps.

1. Write 02h to register STANDARD, address 00h (set B standard)
2. Write 00h to register EASY_PROG, address 01h (make sure that ACTIVE = 0)
3. Write 01h to register EASY_PROG, address 01h (due to 0 to 1 transition of ACTIVE the device is set to B standard, i.e. registers 02h to 23h are programmed automatically according to Table 13)
4. Write 01h to register EASY_PROG, address 01h (reset ACTIVE to logic 0)

Table 13. Easy programming values

Register		Standard							
Index	Name	M/N[1]	B	G/H	I	D/K	L	L-accent	FM radio
02h	DIV_FUNC	04h	04h	04h	04h	04h	06h	07h	00h
03h	ADC_HEADR	01h	01h	01h	01h	01h	01h	01h	01h
04h	PC_PLL_FUNC	27h	27h	27h	27h	27h	27h	27h	22h
05h	PC_PLL_THRES	04h	04h	04h	04h	04h	04h	04h	04h
06h	PC_PLL_WGT	10h	10h	10h	10h	10h	10h	10h	10h
07h	PC_FLL_FUNC	84h	84h	84h	84h	84h	84h	84h	04h
08h	CARDET_LEVEL	08h	08h	08h	08h	08h	08h	08h	08h
09h	DTO_PC_LOW	85h	00h	7Bh	7Bh	7Bh	7Bh	26h	00h
0Ah	DTO_PC_MID	F6h	00h	09h	09h	09h	09h	B4h	00h
0Bh	DTO_PC_HIGH	92h	80h	6Dh	6Dh	6Dh	6Dh	17h	80h
0Ch	DTO_SC_LOW	55h	DAh	DAh	1Dh	5Fh	5Fh	5Fh	DAh
0Dh	DTO_SC_MID	55h	4Bh	4Bh	C7h	42h	42h	42h	4Bh
0Eh	DTO_SC_HIGH	55h	68h	68h	71h	7Bh	7Bh	7Bh	68h
0Fh	FILTERS_1	21h	42h	44h	44h	44h	44h	44h	90h
10h	FILTERS_2	11h	12h	12h	12h	12h	12h	12h	14h
11h	GRP_DELAY	01h	02h	02h	10h	04h	08h	08h	10h
12h	D_IF_AGC_SET_1	A0h	A0h	A0h	A0h	A0h	A0h	A0h	A0h
13h	D_IF_AGC_SET_2	90h	90h	90h	90h	90h	90h	90h	08h
14h	D_IF_AGC_FORCE	67h	67h	67h	67h	67h	67h	67h	E7h
15h	T_IF_AGC_SET	88h	88h	88h	88h	88h	88h	88h	88h
16h	T_IF_AGC_LIM	F0h	F0h	F0h	F0h	F0h	F0h	F0h	F0h
17h	T_IF_AGC_FORCE	3Fh	3Fh	3Fh	3Fh	3Fh	3Fh	3Fh	3Fh
18h	T_IF_AGC_FS	02h	02h	02h	02h	02h	02h	02h	02h
19h	reserved	88h	88h	88h	88h	88h	88h	88h	88h
1Ah	reserved	80h	80h	80h	80h	80h	80h	80h	80h
1Bh	reserved	00h	00h	00h	00h	00h	00h	00h	00h
1Ch	V_SYNC_DEL	6Fh	6Fh	6Fh	6Fh	6Fh	6Fh	6Fh	6Fh
1Dh	CVBS_SET	01h	01h	01h	01h	01h	01h	01h	04h
1Eh	CVBS_LEVEL	73h	73h	73h	73h	73h	6Ch	6Ch	73h
1Fh	CVBS_EQ	08h	08h	08h	08h	08h	08h	08h	10h
20h	SOUNDSET_1	21h	22h	22h	22h	22h	44h	44h	22h
21h	SOUNDSET_2	02h	02h	02h	02h	02h	02h	02h	02h
22h	SOUND_LEVEL	08h	04h	04h	04h	04h	04h	04h	02h
23h	SSIF_LEVEL	04h	04h	04h	04h	04h	04h	04h	04h

[1] M/N standard settings are equal to the power-on reset (default) values.

9.3.2 Diverse functions (includes tuner IF AGC Pin mode)

Table 14. DIV_FUNC register (address 02h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	AGC_SEL	R/W		It determines the tuner IF AGC output Pin mode. The open-drain output can be used in special applications in need of a higher control voltage.
			0*	Normal mode
			1	Open-drain mode
6	AGC_TRI	R/W		When AGC_TRI is set to logic 1 the tuner IF AGC output pin is in 3-state mode. This mode is useful for paralleling a channel decoder for instance.
			0*	Normal mode
			1	3-state mode
5 and 4	-	R/W	-	not used
3	-	R/W	0	reserved, must be set to logic 0
2	POL_DET	R/W		The polarity detector ensures the proper polarity of the video signal. So, the sync impulses of the video output are near ground level.
			0	polarity detector off
			1*	polarity detector on
1	VID_MOD	R/W		Selects video modulation. The only standards with positive video modulation are L and L-accent.
			0*	negative video modulation
			1	positive video modulation
0	IF_SWAP	R/W		When HIGH, the demodulator expects a swapped IF spectrum. This is the case in L-accent standard. This option is also built in for flexibility reasons.
			0*	normal IF spectrum expected
			1	swapped IF spectrum expected

9.3.3 ADC headroom

Table 15. ADC_HEADR register (address 03h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 4	-	R/W	-	not used
3 to 0	ADC_HEADR[3:0]	R/W		ADC_HEADR adjusts the needed headroom for the wanted channel's own sound carriers and the N – 1 adjacent sound carriers (PC in L-accent standard). The ADC headroom is related to the sum of all signals. This function is built in for debugging purposes.
			0001*	ADC headroom 3 dB
			0010	ADC headroom 6 dB
			0100	ADC headroom 9 dB
			1000	ADC headroom 12 dB

9.3.4 Picture carrier PLL functions

Table 16. PC_PLL_FUNC register (address 04h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 3	PC_PLL_BW[4:0]	R/W		picture carrier PLL loop bandwidth selection
			0 0001	loop bandwidth 15 kHz
			0 0010	loop bandwidth 30 kHz
			0 0100*	loop bandwidth 60 kHz
			0 1000	loop bandwidth 130 kHz
			1 0000	loop bandwidth 280 kHz (for very bad transmitter quality)
2	PLL_ON	R/W		the picture carrier PLL can be disengaged (e.g. in FM radio standard)
			0	PLL off (FM radio)
			1*	PLL on
1	PULL_IN	R/W		PULL_IN selects the pull-in range of the picture carrier PLL/FPLL
			0	pull-in range ±1.66 MHz
			1*	pull-in range ±830 kHz
0	CAR_DET	R/W		The carrier detector freezes the PLL in case of a picture carrier overmodulation (especially when the picture carrier is very low or disappears). In addition, the picture carrier DTO value is forced to an optimal one to avoid picture carrier phase drift. To adjust the threshold see CAR_DET_LVL.
			0*	carrier detector off
			1	carrier detector on

Table 17. PC_PLL_THRES register (address 05h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 4	-	R/W	-	not used
3 to 0	PH_ERR_THRES[3:0]	R/W		When the settable threshold for the linear phase detector as part of the picture carrier PLL is passed, the phase detector slope is weighted according to the settings in PHASE_GAIN. This feature is of advantage during adverse field conditions. In case multipath happens like ghosts, the PC PLL should not follow the sudden phase jumps. So, the PC PLL is made slow (lower loop bandwidth) with PC_PLL_THRES after surpassing the threshold. This threshold is related to a fraction of FS. There, FS is 90° if PHASE_PER is logic 0 (default) or 180° when logic 1. If the ICPM or ICFM is large because of bad transmitters with oscillator pulling or modulator imbalance, the PC PLL should follow as true as possible. This can be done by increasing the loop bandwidth with overweighting (see PHASE_GAIN, Table 18).
			0001	$\frac{1}{32}$ FS
			0010	$\frac{1}{16}$ FS
			0100*	$\frac{1}{8}$ FS
			1000	$\frac{1}{4}$ FS

Table 18. PC_PLL_WGT register (address 06h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	PHASE_PER	R/W		By default, the linear phase detector transfer function is repetitive in π. This allows a good picture carrier overmodulation performance, because the PC PLL doesn't need to reacquire the 180° phase modulation, caused by the excessive AM index above m = 100 % (negative residual picture carrier).
			0*	π (needed for overmodulation)
			1	2π
6 to 0	PHASE_GAIN[6:0]	R/W		phase error weighting (adaptive loop speed), see also PH_ERR_THRES in Table 17 for explanation
			000 0001	$\times \frac{1}{16}$
			000 0010	$\times \frac{1}{8}$
			000 0100	$\times \frac{1}{4}$
			000 1000	$\times \frac{1}{2}$
			001 0000*	flat (no weighting)
			010 0000	$\times 2$
			100 0000	$\times 4$

Table 19. PC_FLL_FUNC register (address 07h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	FLL_ON	R/W		The FLL can be switched off for debugging purposes. In Functional mode, FLL_ON must be logic 1 for all cases.
			0	FLL off (only for debugging)
			1*	FLL on
6	LIM_ON	R/W		The default value is logic 0 to have a normal action FLL. However, some flexibility has been included for field investigations and debugging purposes.
			0*	limitation off
			1	limitation on
5 to 0	FLL_LIM[5:0]	R/W		With these settings, the FLL action can be reduced. For better acquisition behavior, a large value should be chosen. The settings are 'don't care' if LIM_ON is logic 0.
			00 0001	$1/4096$ FS
			00 0010	$1/2048$ FS
			00 0100*	$1/1024$ FS
			00 1000	$1/512$ FS
			01 0000	$1/256$ FS
			10 0000	$1/128$ FS

Table 20. CARDET_LEVEL register (address 08h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 5	-	R/W	-	not used
4 to 0	CAR_DET_LVL[4:0]	R/W		determines the action threshold of the above carrier detector; if carrier detector is off, CAR_DET_LVL settings are irrelevant
			0 0001	carrier detector action below 0.5 % residual PC
			0 0010	carrier detector action below 1 % residual PC
			0 0100	carrier detector action below 2 % residual PC
			0 1000*	carrier detector action below 4 % residual PC
			1 0000	carrier detector action below 8 % residual PC
			X XXXX	don't care if CAR_DET = 0

9.3.5 Picture and sound carrier DTO

Table 21. DTO_PC_LOW, DTO_PC_MID and DTO_PC_HIGH register (address 09h to 0Bh) bit description

*Legend: * = default value.*

Address	Register	Bit	Symbol	Access	Value	Description
09h	DTO_PC_LOW	7 to 0	DTO_PC[7:0]	R/W	85h*	With the digitally tuned picture carrier oscillator (DTO_PC), the IF frequency for the picture carrier demodulation can be set. This function is implemented for general purpose applications which are different from nominal TV standards. It can also be used for debugging purposes. The DTO_PC is part of the picture carrier PLL. To set the DTO_PC value to a certain PC input frequency (f_{IF}), please use the following formula: $DTO\_PC = \frac{13.5\ MHz - f_{IF}}{13.5\ MHz} \times 2^{24}$. If e.g. the IF picture carrier input frequency is 5.75 MHz (M/N standard), one gets 92 F685h as result for DTO_PC.
0Ah	DTO_PC_MID	7 to 0	DTO_PC[15:8]	R/W	F6h*	
0Bh	DTO_PC_HIGH	7 to 0	DTO_PC[23:16]	R/W	92h*	

Table 22. DTO_SC_LOW, DTO_SC_MID and DTO_SC_HIGH register (address 0Ch to 0Eh) bit description

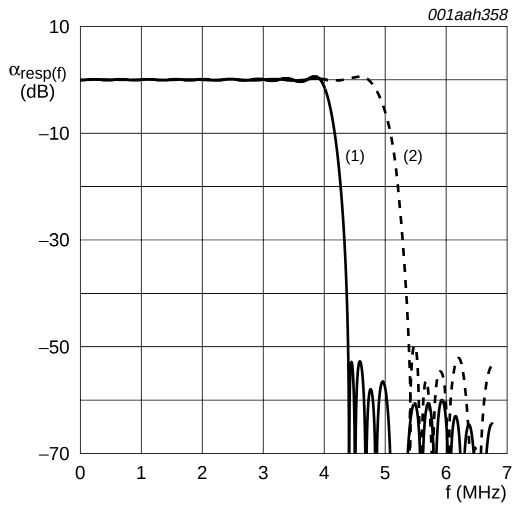
*Legend: * = default value.*

Address	Register	Bit	Symbol	Access	Value	Description
0Ch	DTO_SC_LOW	7 to 0	DTO_SC[7:0]	R/W	55h*	The DTO_SC is part of the FM/AM mono sound demodulator. DTO_SC is calculated in the same way as DTO_PC (described above). In case of M/N standard (sound carrier at 4.5 MHz), one gets 55 5555h for DTO_SC.
0Dh	DTO_SC_MID	7 to 0	DTO_SC[15:8]	R/W	55h*	
0Eh	DTO_SC_HIGH	7 to 0	DTO_SC[23:16]	R/W	55h*	

9.3.6 Filter settings

Table 23. FILTERS_1 register (address 0Fh) bit description
*Legend: * = default value.*

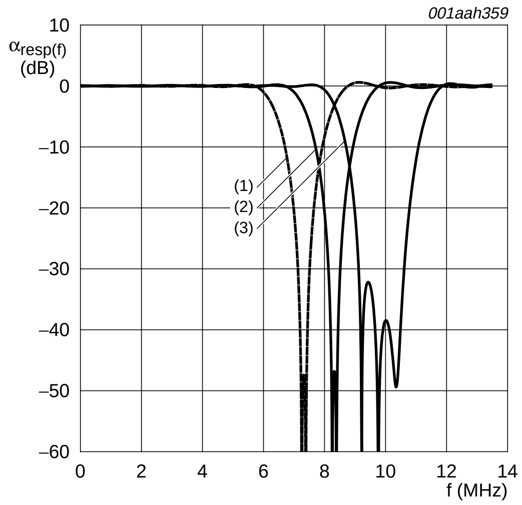
Bit	Symbol	Access	Value	Description
7 to 5	VID_FILT[2:0]	R/W		video low-pass filter to remove all unwanted frequencies (own sound carriers) above video content (see Figure 7)
			001*	video low-pass filter 4 MHz
			010	video low-pass filter 5 MHz
			100	video low-pass filter off
4 to 0	NOTCH_FILT[4:0]	R/W		The notch filter attenuates the adjacent sound carrier N – 1, which is located differently dependent on channel spacing 6 MHz, 7 MHz or 8 MHz (see Figure 8).
			0 0001*	notch filter for 6 MHz channel spacing (M/N standard)
			0 0010	notch filter for 7 MHz channel spacing (B standard)
			0 0100	notch filter for 8 MHz channel spacing (G/H, D/K, I, L and L-accent standard)
			1 0000	notch/low-pass filter off



(1) M/N standard.

(2) All other standards.

Fig 7. Video low-pass filters for sound carrier suppression



Notch filter for NSC (NPC for L-accent standard)

(1) M/N standard.

(2) B standard.

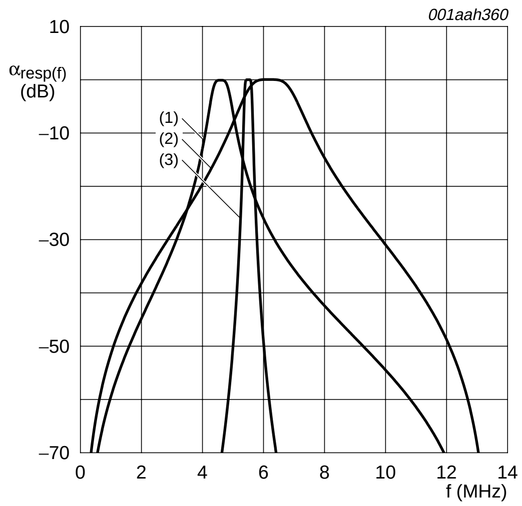
(3) G/H, D/K, I, L and L-accent standard.

Fig 8. Notch filter for adjacent sound carrier suppression

Table 24. FILTERS_2 register (address 10h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 5	-	R/W	-	not used
4	DC_NOTCH	R/W		notch filter to remove ADC DC offset
			0	off
			1*	on
3 to 0	SBP[3:0]	R/W		The SSIF band-pass attenuates unwanted video frequencies, e.g. color carrier. For FM radio standard it provides almost channel selectivity (see Figure 9).
			0001*	SSIF band-pass 4.5 MHz (M/N standard)
			0010	SSIF band-pass 6.2 MHz (all other TV standards)
			0100	SSIF band-pass 5.5 MHz high selectivity (FM radio)
			1000	SSIF band-pass off



(1) M/N standard.

(2) All other standards.

(3) FM radio.

Fig 9. SSIF and FM radio band-pass filters

9.3.7 Group delay equalization

Table 25. GRP_DELAY register (address 11h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 5	-	R/W	-	not used
4 to 0	GRP_DEL[4:0]	R/W		group delay equalization to correct the transmitter predistortion
			0 0001*	group delay M/N standard
			0 0010	group delay B/G/H standard
			0 0100	group delay D/K standard
			0 1000	group delay L/L-accent standard
			1 0000	group delay I (flat) standard

9.3.8 Digital IF AGC functions

Table 26. D_IF_AGC_SET_1 register (address 12h) bit description
*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	D_IF_AGC_CORR	R/W		This determines the condition under which the digital IF AGC switches to Correlated mode. If D_IF_AGC_CORR is HIGH, the digital IF AGC works in a Correlated mode only if N_H_LOCK, F_H_LOCK and V_LOCK are active (see H/V PLL read-out in Table 44). If LOW, the Correlated mode is activated when N_H_LOCK and V_LOCK are active.
			0	H-lock + V-lock
			1*	H-lock + fast H-lock + V-lock
6	D_IF_AGC_MODE	R/W		If HIGH, the digital IF AGC detection and gating is done during the back porch of the video signal. This Detection mode can be used for all standards (also L/L-accent standard) without impact on the IF AGC loop speed.
			0*	peak sync AGC (slow peak white L/L-accent standard)
			1	black level AGC detection
5 to 1	D_IF_AGC_AVG[4:0]	R/W		With D_IF_AGC_AVG the number of lines for averaging during the digital IF AGC gating window is set. This is only valid if the AGC mode is correlated (H/V PLL locked). With the averaging, the line noise at low RF levels is reduced.
			0 0001	2 samples
			0 0010	4 samples
			0 0100	8 samples
			0 1000	16 samples
			1 0000*	32 samples
0	RST_INT	R/W		The digital IF AGC integrator can be set to zero (i.e. lowest digital IF AGC gain). This option can be used for debugging purposes.
			0*	normal operation
			1	reset IF AGC integrator

Table 27. D_IF_AGC_SET_2 register (address 13h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	D_AGC_ERR_LIM	R/W		With D_AGC_ERR_LIM the digital IF AGC error slope is limited. This can improve performance under the presence of e.g. impulsive noise that can confuse the AGC detector.
			0	limitation off
			1*	limitation on
6 to 0	D_IF_AGC_BW[6:0]	R/W		digital IF AGC 3 dB-loop bandwidth setting
			000 0001	25 Hz
			000 0010	50 Hz
			000 0100	100 Hz
			000 1000	200 Hz
			001 0000*	400 Hz
			010 0000	800 Hz
			100 0000	1.6 kHz

Table 28. D_IF_AGC_FORCE register (address 14h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	D_FORCE	R/W		the IF AGC output voltage can be forced externally to a fixed voltage, determined by IF_AGC_EXT
			0*	IF AGC normal operation
			1	IF AGC output voltage determined by D_FORCE_VAL
6 to 0	D_FORCE_VAL[6:0]	R/W		This determines the digital IF AGC forced value and is a 'don't care' if D_FORCE is LOW. The format is twos complement. The default is 67h, which equals 0 dB internal gain. In the following some possible settings for 6 dB gain steps are shown.
			51h	–12 dB
			5Ch	–6 dB
			67h*	0 dB
			72h	+6 dB
			7Dh	+12 dB
			08h	+18 dB
			13h	+24 dB
			1Eh	+30 dB
			29h	+36 dB
			34h	+42 dB
			3Fh	+48 dB
			XXh	don't care if D_FORCE = 0

9.3.9 Tuner IF AGC functions

Table 29. T_IF_AGC_SET register (address 15h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	POL_TIF	R/W		tuner IF AGC polarity
			0	inverted tuner IF AGC polarity
			1*	normal tuner IF AGC polarity: the higher the necessary gain, the higher the IF AGC voltage
6 to 0	T_IF_AGC_SPEED[6:0]	R/W		T_IF_AGC_SPEED determines the tuner IF AGC loop speed
			000 0001	–18 dB nominal
			000 0010	–12 dB nominal
			000 0100	–6 dB nominal
			000 1000*	nominal speed (determined by the tuner IF control slope)
			001 0000	+6 dB nominal
			010 0000	+12 dB nominal
			100 0000	+18 dB nominal

Table 30. T_IF_AGC_LIM register (address 16h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 4	UP_LIM[3:0]	R/W		The tuner IF AGC output voltage can be limited to interface with concepts having power supply < 3.3 V. UP_LIM determines the upper limit from ½ FS (= 0h) to FS (= Fh). The format is straight binary.
			1111*	set upper limit to maximum
3 to 0	LOW_LIM[3:0]	R/W		LOW_LIM determines the lower tuner IF AGC output limit from 0 (= 0h) to ½ FS (= Fh). The format is straight binary.
			0000*	set lower limit to minimum

Table 31. T_IF_AGC_FORCE register (address 17h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	T_FORCE	R/W		the tuner IF AGC output voltage can be forced externally to a fixed voltage, determined by T_FORCE_VAL
			0*	tuner IF AGC normal operation
			1	tuner IF AGC output voltage determined by T_FORCE_VAL
6 to 0	T_FORCE_VAL[6:0]	R/W		T_FORCE_VAL determines the tuner IF AGC forced value. So the tuner IF AGC can be fixed to a certain value for debugging purposes. Format is straight binary.
			3Fh*	$0.5 \times V_{DD(3V3)}$, i.e. 1.65 V nominally
			XXh	don't care if T_FORCE = 0

Table 32. T_IF_AGC_FS register (address 18h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 3	-	R/W	-	not used
2 to 0	T_IF_AGC_FS[2:0]	R/W		by increasing the IF AGC noise shaper sampling rate (f_s), the noise shaper in-band disturbance (line clamping noise) can be heavily reduced
			000	f_s = 13.5 MHz
			010*	f_s = 27 MHz
			100	f_s = 54 MHz

9.3.10 V-sync adjustment

Table 33. V_SYNC_DEL register (address 1Ch) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 and 6	VS_WIDTH[1:0]	R/W		VS_WIDTH determines the width (in horizontal lines) of the V-sync gating pulse (needed for gating of tuner RF AGC2)
			00	width 1 line (64 μs)
			01*	width 2 lines
			10	width 4 lines
			11	width 16 lines
5	VS_POL	R/W		VS_POL determines the polarity of the V-sync pulse: if VS_POL = 1, the first edge of the pulse is positive, else negative.
			0	first edge negative
			1*	first edge positive
4 to 0	VS_DEL[4:0]	R/W		VS_DEL determines the first edge position of the output V-sync pulse compared to the beginning of the vertical blanking interval: $pulse\_position = (VS\_DEL - 12)\ lines$
			0Fh*	first edge 3 lines after beginning of vertical interval

9.3.11 CVBS settings

Table 34. CVBS_SET register (address 1Dh) bit description
*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 3	-	R/W	-	not used
2	FOR_BLK	R/W		when active, the video output is always blanked, e.g. for channel change (forced blank)
			0*	no action
			1	video blanked
1	AUTO_BLK	R/W		when active, the video output is blanked if the horizontal line lock flag (N_H_LOCK, see Table 44) is not present
			0*	auto-blanking off
			1	auto-blanking on
0	VID_LVL	R/W		the video levelling stage ensures a constant and clipping free video output level (important for excessive picture carrier overmodulation)
			0	video levelling stage off
			1*	video levelling stage on

Table 35. CVBS_LEVEL register (address 1Eh) bit description
*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 0	CVBS_LVL[7:0]	R/W		With this byte, the nominal video output level is freely programmable. The format is unsigned integer (offset binary). Settings below 40h and above C0h, which correspond to –5 dB (40h) and +4.5 dB (C0h) related to the default value, are forbidden. In the following some possible settings in 1 dB steps are shown.
			51h	–3 dB nominal
			5Bh	–2 dB nominal
			66h	–1 dB nominal
			73h*	nominal: 1 V (p-p) video output level (sync-peak)
			81h	+1 dB nominal
			91h	+2 dB nominal
			A2h	+3 dB nominal

Table 36. CVBS_EQ register (address 1Fh) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 0	CVBS_EQ[7:0]	R/W		The video equalizer can be used for the compensation of a principal tuner tilt or to change the video frequency according to customer taste. The figures given are at 5 MHz CVBS with respect to low frequencies (see Figure 10).
			0000 0001	The video frequency response is –8 dB for 5 MHz.
			0000 0010	The video frequency response is –6 dB for 5 MHz.
			0000 0100	The video frequency response is –4 dB for 5 MHz.
			0000 1000*	The video frequency response is –2 dB for 5 MHz.
			0001 0000	The video frequency response is made flat in this mode.
			0010 0000	The video frequency response is +2 dB (peaking) for 5 MHz.
			0100 0000	The video frequency response is +4 dB (peaking) for 5 MHz.
			1000 0000	The video frequency response is +6 dB (peaking) for 5 MHz.

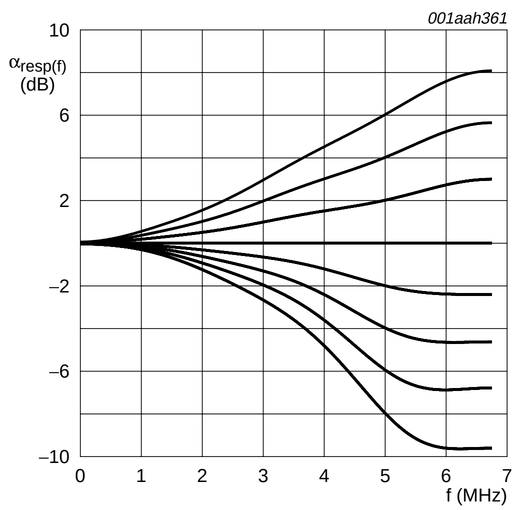


Fig 10. Video equalizer curves

9.3.12 SSIF and mono sound settings

Table 37. SOUNDSET_1 register (address 20h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	-	R/W	-	not used
6 and 5	AM_FM_SND[1:0]	R/W		Output mode for inbuilt FM/AM mono sound demodulator
			01*	FM sound
			10	AM sound (only L/L-accent standard)
			XX	don't care if SSIF output is chosen (SSIF_SND[1:0] = 10)
4 to 0	DEEMPH[4:0]	R/W		mono sound de-emphasis adjustment to compensate transmitter pre-emphasis; or low-pass filter to remove out of audio band interferers
			0 0001*	de-emphasis of 75 μs for M/N standard or non-European FM radio to compensate the transmitter pre-emphasis
			0 0010	de-emphasis of 50 μs for B/G/H, D/K and I standard or European FM radio to compensate the transmitter pre-emphasis
			0 0100	low-pass filter with 30 kHz −3 dB cut-off frequency to remove out of audio band interferers
			0 1000	low-pass filter with 140 kHz −3 dB cut-off frequency to drive an external BTSC stereo decoder
			1 0000	The de-emphasis filter is bypassed. This can be used for debugging or other purposes.

Table 38. SOUNDSET_2 register (address 21h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 5	-	R/W	-	not used
4	HD_DK	R/W		When active, the internal FM mono sound demodulator can handle excessive FM deviations up to 400 kHz. This might happen in D/K standard China. To activate this mode, it is mandatory to set D/K standard first. The sound output level has to be adapted accordingly by the microprocessor to avoid sound DAC clipping. E.g. for 400 kHz FM deviation, the −12 dB setting of the sound level register (see Table 39) is recommended.
			0*	high Deviation mode off
			1	high Deviation mode on
			X	don't care if SSIF output is chosen (SSIF_SND[1:0] = 10)

Table 38. SOUNDSET_2 register (address 21h) bit description *...continued*

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
3	FOR_MUTE	R/W		When active, the mono sound signal is always muted. This setting only makes sense in case the sound DAC output is also set to mono sound (SSIF_SND[1:0] = 01). FOR_MUTE has no function if SSIF_SND[1:0] = 10.
			0*	off
			1	on
			X	don't care if SSIF output is chosen (SSIF_SND[1:0] = 10)
2	AUTO_MUTE	R/W		When active, the mono sound signal is muted if the horizontal lock flag (N_H_LOCK) disappears. This setting only makes sense in case the sound DAC output is also set to mono sound (SSIF_SND[1:0] = 01). FOR_MUTE has no function if SSIF_SND[1:0] =10.
			0*	off
			1	on
			X	don't care if SSIF output is chosen (SSIF_SND[1:0] = 10)
1 and 0	SSIF_SND[1:0]	R/W		either mono sound or SSIF can be chosen for the sound DAC output
			01	mono sound
			10*	SSIF

Table 39. SOUND_LEVEL register (address 22h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 5	-	R/W	-	not used
4 to 0	SND_LVL[4:0]	R/W		mono sound output level
			0 0001	–12 dB nominal; implemented for flexibility reasons. With this setting, the adaptation to different standard requirements can be done.
			0 0010	–6 dB nominal; implemented for flexibility reasons. With this setting, the adaptation to different standard requirements can be done. It is chosen for FM radio because of the large FM deviation involved.
			0 0100	Nominal setting; FM deviations up to 100 kHz can be processed without sound DAC clipping. The clipping level is 535 mV (RMS) typically.
			0 1000*	+6 dB nominal; chosen for M/N standard due to less nominal frequency deviation
			1 0000	+12 dB nominal; implemented for flexibility reasons. With this setting, the adaptation to different standard requirements can be done.
			X XXXX	don't care if SSIF output is chosen (SSIF_SND[1:0] = 10)

Table 40. SSIF_LEVEL register (address 23h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 5	-	R/W	-	not used
4 to 0	SSIF_LVL[4:0]	R/W		SSIF output level
			0 0001	–12 dB nominal; implemented for flexibility reasons. With this setting, the adaptation to different standard requirements can be done.
			0 0010	–6 dB nominal; implemented for flexibility reasons. With this setting, the adaptation to different standard requirements can be done.
			0 0100*	Nominal setting; typical output level is 55 mV (RMS) for PC / SC ratio of 13 dB (see Section 12).
			0 1000	+6 dB nominal; implemented for flexibility reasons. With this setting, the adaptation to different standard requirements can be done.
			1 0000	+12 dB nominal; implemented for flexibility reasons. With this setting, the adaptation to different standard requirements can be done.
			X XXXX	don't care if mono sound output is chosen (SSIF_SND[1:0] = 01)

9.3.13 Status registers: ADC saturation, AFC, H/V PLL and AGC

Table 41. ADC_SAT register (address 24h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	ADC_SAT[7:0]	R	-	With ADC_SAT, the ADC saturation percentage in a period of 40 ms can be calculated by the following formula: $saturation = \frac{ADC\_SAT}{256}(\%)$.

Table 42. AFC register (address 25h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	AFC[7:0]	R	-	This is the readout for AFC. AFC contains the frequency deviation from nominal IF picture carrier. The format is twos complement, 13.2 kHz steps are done per LSB. See Table 43 for details. The frequency deviation could also be given by the following formula: $f_{IF} - f_{nom} = \frac{-AFC \times 6\,750}{256}(kHz)$. For a frequency deviation from the nominal IF picture carrier greater than the FPLL pull-in capability (–830.6 kHz to +843.8 kHz or –1674.3 kHz to +1687.5 kHz), the output reading is undefined. The AFC lock indication can be taken from the N_H_LOCK information from the H-sync PLL. The lock occurs inside a frequency window, which is determined by the pull-in capability of the FPLL.

Table 43. Calculation of frequency deviation from AFC value

Deviation from nominal IF frequency[1]	AFC[7]	AFC[6]	AFC[5]	AFC[4]	AFC[3]	AFC[2]	AFC[1]	AFC[0]
$f_{IF} = f_{nom} - 1674.3$ kHz	0	1	1	1	1	1	1	1
$f_{IF} = f_{nom} - 1661.1$ kHz	0	1	1	1	1	1	1	0
:	:	:	:	:	:	:	:	:
$f_{IF} = f_{nom} - 830.6$ kHz	0	0	1	1	1	1	1	1
$f_{IF} = f_{nom} - 817.4$ kHz	0	0	1	1	1	1	1	0
:	:	:	:	:	:	:	:	:
$f_{IF} = f_{nom} - 13.2$ kHz	0	0	0	0	0	0	0	1
$f_{IF} = f_{nom}$	0	0	0	0	0	0	0	0
$f_{IF} = f_{nom} + 13.2$ kHz	1	1	1	1	1	1	1	1
:	:	:	:	:	:	:	:	:
$f_{IF} = f_{nom} + 830.6$ kHz	1	1	0	0	0	0	0	1
$f_{IF} = f_{nom} + 843.8$ kHz	1	1	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
$f_{IF} = f_{nom} + 1674.3$ kHz	1	0	0	0	0	0	0	1
$f_{IF} = f_{nom} + 1687.5$ kHz	1	0	0	0	0	0	0	0

[1] See Section 12 for nominal IF frequencies.

Table 44. HVPLL_STAT register (address 26h) bit description

Bit	Symbol	Access	Value	Description
7 and 6	-	R	-	not used
5	NOISE_DET	R	-	This flag gets HIGH in case the video S/N (weighted) drops below 30 dB. For proper and noise free video signals it stays LOW. It can be used for debugging and other purposes.
4	MAC_DET	R	-	This flag indicates the presence of copy-guarded video content from STBs or VCRs. It can be used for debugging and other purposes.
3	FIDT	R	-	This flag indicates the frame rate (50 Hz or 60 Hz). When active, 60 Hz is detected. It can be used for debugging and other purposes.
2	V_LOCK	R	-	This flag is active, if a proper frame (50 Hz or 60 Hz) is detected. It can be used for debugging and other purposes.
1	F_H_LOCK	R	-	This flag is active, if a proper H-sync (15.625 kHz or 15.734 kHz) is detected (Fast mode). It can be used for debugging and other purposes.
0	N_H_LOCK	R	-	This flag is active, if a proper H-sync (15.625 kHz or 15.734 kHz) is detected (Normal mode). It can be used for debugging and other purposes.

Table 45. D_IF_AGC_STAT register (address 27h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	D_IF_AGC_STAT[7:0]	R	-	D_IF_AGC_STAT is the digital IF AGC status readout byte. Contains the digital IF AGC loop DC information. The format is twos complement. To get the internal gain in dB, the following formula can be used: $gain = \frac{D\_IF\_AGC\_STAT + 50}{3.675}(dB)$.

Table 46. T_IF_AGC_STAT register (address 28h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	T_IF_AGC_STAT[7:0]	R	-	T_IF_AGC_STAT is the IF AGC status readout byte. Contains the tuner IF AGC loop DC information. The format is offset binary.

9.3.14 Debug register for ADC and DAC test

Table 47. ANALOG_DEBUG register (address 2Ah) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 2	-	R/W	-	not used
1	ADC_TEST	R/W		If ADC_TEST is HIGH, the ADC input signal is interpolated to 108 MHz and fed to video and sound DAC output; the main circuitry is bypassed. This feature is intended mainly for debugging purposes and performance judgment.
			0*	Normal mode
			1	ADC Test mode
0	DAC_TEST	R/W		DAC Test mode; in this test mode an internally generated sine wave is given out to video and sound DAC. The amplitude at DAC output is −1.7 dBFS. The frequency can be set by DTO_PC. Please use the following formula: $f = \frac{DTO\_PC}{2^{24}} \times 13.5\ MHz$. Due to the sampling theorem only frequencies up to 6.75 MHz can be generated. This feature is intended mainly for debugging purposes and performance judgment.
			0*	Normal mode
			1	DAC Test mode
			X	don't care if ADC_TEST = 1

9.3.15 Chip identification and Standby mode

Table 48. IDENTITY register (address 2Fh) bit description

Bit	Symbol	Access	Value	Description
7 to 0	IDENTITY[7:0]	R	1000 1010	chip identification, value corresponds to TDA8295

Table 49. CLB_STDBY register (address 30h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 2	-	R/W	-	not used
1	STDBY	R/W		When STDBY is set to logic 1, the chip enters in Standby mode, and its power consumption is reduced. The IF AGC pin is set to high-ohmic. The default value is logic 0, which means that the chip is active.
			0*	Normal mode
			1	Standby mode
0	CLB	R/W		This signal clears the TDA8295 through the I²C-bus interface (software reset). To activate the reset, just write CLB = 0. This software reset will not affect the content of the registers.
			0	activate soft reset
			1*	normal operation

9.3.16 Status of clock PLL and video/sound DAC load

Table 50. ANALOG_STAT register (address 32h) bit description

Bit	Symbol	Access	Value	Description
7	-	R	-	not used
6	LOAD_DACV	R		output load identification video DAC
			0	Normal mode
			1	If active, the video DAC output voltage is above reference voltage.
5	LOAD_DACS	R		output load identification sound DAC
			0	Normal mode
			1	If active, the sound DAC output voltage is above reference voltage.
4	PLL_LOCK	R		clock PLL lock indicator
			0	clock PLL unlocked
			1	indicates that the clock PLL is locked
3 to 0	-	R	-	reserved

9.3.17 ADC control

In the TDA8295 a 12-bit ADC is implemented sampling with a 54 MHz clock (27 MHz optional).

Table 51. ADC_CTL register (address 33h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	GAINSET	R/W		The track and hold circuit in the converter has a programmable gain setting, which is controlled by the GAINSET parameter. In case the gain of the track and hold is increased, the input range of the ADC is decreased accordingly.
			0*	2.0 V (p-p)
			1	1.0 V (p-p) (6 dB gain)
6 to 4	CS[2:0]	R/W		The current consumption of the ADC can be programmed with these two bits. It is possible to increase or decrease the current by the following ratio:
			000	not allowed
			001	not allowed
			010*	0.50 (recommended for 54 MHz sampling)
			011	0.75
			100	1.00
			101	1.25
			110	1.50
			111	not allowed
3	DCIN	R/W		The input signal of the ADC can be either AC coupled by means of two capacitors or connected directly to the inputs (DC coupled).
			0*	AC coupling
			1	DC coupling
2	TWOS	R/W		This parameter controls the output format of the ADC.
			0	offset binary format
			1*	twos complement format
1	SLEEP	R/W		When HIGH, SLEEP sets the ADC into its Sleep mode. Both bias current and clock are switched off. In this mode, the current consumption is reduced by a factor of 6. The reference circuit will remain active in order to guarantee a fast recovery from Sleep mode.
			0*	Normal mode
			1	ADC Sleep mode
0	PD_ADC	R/W		When HIGH, PD_ADC sets the ADC into its Power-down mode. All internal currents are switched off. In this mode, the current consumption is near zero (leakage current only).
			0*	Normal mode
			1	ADC Power-down mode

Table 52. ADC_CTL_2 register (address 34h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 2	-	R/W	-	not used
1	AD_PLL_BYP	R/W		The clock PLL can be bypassed for the ADC sampling clock. Then the crystal output is directly taken for ADC sampling.
			0*	Normal mode
			1	Bypass mode
0	AD_SR54M	R/W		AD_SR54M sets the ADC sampling rate
			0	ADC sampling rate 27 MHz; first decimation filter is bypassed
			1*	ADC sampling rate 54 MHz

9.3.18 Video and sound DAC control

The TDA8295 implements two 10-bit DAC modules (CVBS and sound outputs) which are sampled by a 108 MHz clock. A reference module derives biasing currents for the two DACs.

Table 53. VIDEODAC_CTL register (address 35h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	-	R/W	0	reserved, must be set to logic 0
6 to 1	B_DA_V[5:0]	R/W		B_DA_V is the coarse output level adjustment parameters of the video DAC. See Section 13.3.
			00 0000	minimum current setting
			11 1111*	maximum current setting
0	PD_DA_V	R/W		When HIGH, PD_DA_V sets the video DAC into its Power-down mode.
			0*	Normal mode
			1	video DAC Power-down mode

Table 54. AUDIODAC_CTL register (address 36h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	-	R/W	0	reserved, must be set to logic 0
6 to 1	B_DA_S[5:0]	R/W		B_DA_S is the coarse output level adjustment parameters of the sound DAC. See Section 13.3.
			00 0000*	minimum current setting
			11 1111	maximum current setting
0	PD_DA_S	R/W		When HIGH, PD_DA_S sets the sound DAC into its Power-down mode.
			0*	Normal mode
			1	sound DAC Power-down mode

Table 55. DAC_REF_CLK_CTL register (address 37h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	-	R/W	-	not used
6	DA_CLK_INV	R/W		For debugging purposes, the DAC clock polarity can be inverted.
			0	inverted polarity
			1*	normal polarity
5	DA_PLL_BYP	R/W		If active, the clock PLL for DAC sampling can be bypassed. Then, the crystal output is directly taken for DAC sampling.
			0*	Normal mode
			1	Bypass mode
4 to 1	B_REF[3:0]	R/W		For accuracy, one external resistor connected to pin RSET and board ground controls the bias current. Moreover, B_REF permits to adjust this bias current from −7 % to +7 % (see Section 13.3). Format is signed binary.
			1111	minimum fine current
			0000*	nominal fine current
			0111	maximum fine current
0	PD_DA_REF	R/W		When HIGH, PD_DA_REF sets the reference module into its Power-down mode.
			0*	Normal mode
			1	Power-down mode

9.3.19 Clock generation (PLL and crystal oscillator)

The TDA8295 implements a crystal oscillator which can be used either in Slave mode or in Oscillator mode (see Section 13.7), and a multipurpose PLL which receives XIN as input clock, and delivers the system clock of the IC (108 MHz).

Table 56. PLL_REG00 register (address 38h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 and 6	-	R/W	00	reserved, must be set to logic 00
5	PLL_AUTO	R/W		clock PLL mode control
			0	The sequencing of the programming and monitoring of the PLL can be made ‘manually’ through CLK_EN, BYP_PLL, PD_PLL and LOCK, according to the following set of instructions: After a hardware reset: • Set PLL_AUTO to logic 0 • By default, CLK_EN = BYP_PLL = PD_PLL = 1, LOCK = 0, the PLL is in Power-down mode, is not locked, and the output clock is the clock of the quartz oscillator used to resynchronize reset signals in the TDA8295 Then: • Set BYP_PLL and CLK_EN to logic 0 • Set MSEL, NSEL and PSEL that are corresponding to the frequency required value • Set PD_PLL to logic 0, in order that the PLL takes those parameters into account and starts up • Then, wait for a minimum time of 500 μs (which is the maximum time the PLL should take to lock). This time could be used to make the programming of the other I^2C-bus registers. • Set CLK_EN to logic 1 to enable the sampling frequency to the rest of the chip • Optionally, verify that LOCK = 1
			1*	The sequencing of the programming and monitoring of the PLL is handled automatically by the TDA8295 at initialization and each time one of the M, N, P parameters is changed. Thus, the user has only to program M, N, P and then once the PLL is locked, its output clock becomes enabled automatically.
4 to 0	-	R/W	0 0000	reserved, must be set to logic 0 0000

Table 57. PLL_REG04 register (address 3Ch) bit description

Bit	Symbol	Access	Value	Description
7 to 3	-	R/W	-	not used
2 to 0	-	R/W	000	reserved, must be set to logic 000

Table 58. PLL_REG06 register (address 3Eh) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	-	R/W	0	reserved, must be set to logic 0
6	CLK_EN	R/W		CLK_EN controls the PLL output clock
			0	PLL output clock disable
			1*	PLL output clock enable
			X	don't care if PLL_AUTO = 1
5	BYP_PLL	R/W		When HIGH, the internal clocks (for logic, ADC, and DACs) are directly controlled by the pin XIN. BYP_PLL acts both on external multiplexers and on internal PLL bypass. When PLL initialization is automatic (PLL_AUTO = 1), BYP_PLL is not considered.
			0	internal clocks are controlled by PLL clock
			1*	internal clocks are controlled by pin XIN
			X	don't care if PLL_AUTO = 1
4	DIRECTO	R/W	0*	When DIRECTI is set to logic 1, the pre-divider is bypassed. If DIRECTO is equal to logic 1, then it is the post-divider, which is bypassed. Please see Table 59 for further details.
3	DIRECTI	R/W	0*	
2 and 1	-	R/W	00	reserved, must be set to logic 00
0	PD_PLL	R/W		Put the PLL in Power-down mode if equal to logic 1. When PLL initialization is automatic (PLL_AUTO = 1), PD_PLL is not considered.
			0	PLL active
			1*	PLL Power-down mode
			X	don't care if PLL_AUTO = 1

Table 59. Truth table for PLL output clock frequency

*Legend: * = default value.*

DIRECTI	DIRECTO	PLL output clock frequency[1]
1	1	$f_{clk(o)(PLL)} = f_{VCO} = f_i \times 2 \times M$
1	0	$f_{clk(o)(PLL)} = \frac{f_{VCO}}{2 \times P} = \frac{f_i \times M}{P}$
0	1	$f_{clk(o)(PLL)} = f_{VCO} = \frac{f_i \times 2 \times M}{N}$
0*	0*	$f_{clk(o)(PLL)} = \frac{f_{VCO}}{2 \times P} = \frac{f_i \times M}{N \times P}$

[1] For description of M, N and P see Table 60.

For optimum performances, the following relations must be respected:

- 275 MHz $\leq f_{VCO} \leq$ 550 MHz
- 4 kHz $\leq f_i \leq$ 150 MHz if DIRECTI = 1, else 4 kHz $\leq f_i / N \leq$ 150 MHz

Table 60. PLL_REG07, PLL_REG08, PLL_REG09 and PLL_REG10 register (address 3Fh to 42h) bit description

*Legend: * = default value.*

Address	Register	Bit	Symbol	Access	Value	Description
3Fh	PLL_REG07	7	-	R/W	-	not used
		6 to 0	-	R/W	00h	reserved, must be set to 00h
40h	PLL_REG08	7 to 0	MSEL[7:0]	R/W	1Ah*	It programs the M parameter (M = MSEL + 1). M is the PLL feedback-divider.
41h	PLL_REG09	7 to 1	NSEL[6:0]	R/W	01h*	It programs the N parameter (N = NSEL + 1). N is the PLL pre-divider.
		0	-	R/W	0	reserved, must be set to logic 0
42h	PLL_REG10	7 to 5	-	R/W	000	reserved, must be set to logic 000
		4 to 0	PSEL[4:0]	R/W	01h*	It programs the P parameter (P = PSEL + 1). P is the PLL post-divider.

Table 61. XTALOSC_CTL register (address 43h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 3	-	R/W	-	not used
2	HF	R/W		With HF, the transconductance of the oscillator gain stage can be set. For f_{XIN} > 20 MHz, HF should be set to logic 1.
			0*	recommended for standard application (16 MHz)
			1	recommended if f_{XIN} > 20 MHz
1 and 0	-	R/W	00	reserved, must be set to logic 00

9.3.20 GPIOs

In the TDA8295, three general purpose input/outputs are implemented.

Table 62. GPIOREG_0 register (address 44h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 4	GP1_CF[3:0]	R/W		It determines how the general purpose pin GPIO1 is configured.
			0000	The GPIO1 pin is in Input mode. The input value is stored in GP1_VAL.
			0001*	The GPIO1 pin is in Open-drain mode. The output value is determined by GP1_VAL.
			0011	The GPIO1 pin is in Output mode. The PLL output clock divided by two is delivered.
			0100 to 1011	The GPIO1 pin is in Output mode. HVPLL signals are delivered. The output is a one bit signal of HVPLL_BUS[7:0] according to Table 64.
			XXXX	Don't care if I2CSW_EN = 1. Then the pad is configured as I²C-bus feed-through like described in Table 63.
3 to 0	GP0_CF[3:0]	R/W		It determines how the general purpose pin GPIO0 is configured.
			0000	The GPIO0 pin is in Input mode. The input value is stored in GP0_VAL.
			0001*	The GPIO0 pin is in Open-drain mode. The output value is determined by GP0_VAL.
			0011	The GPIO0 pin is in Output mode. The PLL output clock divided by two is delivered.
			0100 to 1011	The GPIO0 pin is in Output mode. HVPLL signals are delivered. The output is a one bit signal of HVPLL_BUS[7:0] according to Table 64.

Table 63. GPIOREG_1 register (address 45h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	I2CSW_EN	R/W	0*	When I2CSW_EN = 1, GPIO1 and GPIO2 are configured as an I²C-bus feed-through independently of the GP1_CF and GP2_CF value. When I2CSW_ON = 0, the feed-through switch is open, and GPIO1 and GPIO2 are in 3-state. When the switch is closed (I2CSW_ON = 1), the I²C-bus clock and data signals (SCL and SDA) are available on the GPIO1 and GPIO2 pins.
6	I2CSW_ON	R/W	0*	
5 and 4	-	R/W	-	not used

Table 63. GPIOREG_1 register (address 45h) bit description *…continued*

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
3 to 0	GP2_CF[3:0]	R/W		It determines how the general purpose pin GPIO2 is configured.
			0000	The GPIO2 pin is in Input mode. The input value is stored in GP2_VAL.
			0001*	The GPIO2 pin is in Open-drain mode. The output value is determined by GP2_VAL.
			0011	The GPIO2 pin is in Output mode. The PLL output clock divided by two is delivered.
			0100 to 1011	The GPIO2 pin is in Output mode. HVPLL signals are delivered. The output is a one bit signal of HVPLL_BUS[7:0] according to Table 64.
			XXXX	Don't care if I2CSW_EN = 1. Then the pad is configured as I^{2}C-bus feed-through.

Table 64. HVPLL bus mapping

HVPLL_BUS bit	Signal
HVPLL_BUS[7]	V_SYNC
HVPLL_BUS[6]	H_SYNC
HVPLL_BUS[5]	NOISE_DET
HVPLL_BUS[4]	MAC_DET
HVPLL_BUS[3]	FIDT
HVPLL_BUS[2]	V_LOCK
HVPLL_BUS[1]	F_H_LOCK
HVPLL_BUS[0]	N_H_LOCK

Table 65. GPIOREG_2 register (address 46h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	CLK_INV_GP2	R/W	0*	With CLK_INV_GPx, the output clock polarity can be changed. This is only useful when GPx_CF[3:0] = 0011.
6	CLK_INV_GP1	R/W	0*	
5	CLK_INV_GP0	R/W	0*	
4 and 3	-	R/W	-	not used
2	GP2_VAL	R/W	1*	GP2_VAL controls the value of the pin GPIO2 when GP2_CF[3:0] = 0001. When GP2_CF[3:0] = 0000, GPIO2 is an input pin which value can be read through the I^{2}C-bus stored in GP2_VAL.
1	GP1_VAL	R/W	1*	GP1_VAL controls the value of the pin GPIO1 when GP1_CF[3:0] = 0001. When GP1_CF[3:0] = 0000, GPIO1 is an input pin which value can be read through the I^{2}C-bus stored in GP1_VAL.
0	GP0_VAL	R/W	1*	GP0_VAL controls the value of the pin GPIO0 when GP0_CF[3:0] = 0001. When GP0_CF[3:0] = 0000, GPIO0 is an input pin which value can be read through the I^{2}C-bus stored in GP0_VAL.

10. Limiting values

Table 66. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1][2]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DDDC(1V2)}$	core digital supply voltage (1.2 V)			–0.5	+3.32	V
$V_{DDA(ADC)(3V3)}$	ADC analog supply voltage (3.3 V)			–0.5	+5.63	V
$V_{DDA(PLL)(1V2)}$	PLL analog supply voltage (1.2 V)			–0.5	+3.32	V
$V_{DDA(OSC)(1V2)}$	oscillator analog supply voltage (1.2 V)			–0.5	+3.32	V
V_i	input voltage	pins IF_POS and IF_NEG		–0.5	+5.63	V
		digital input pins (5 V tolerant)		–0.5	+7.5	V
		pin XIN		–0.5	+4.0	V
T_{lead}	lead temperature			-	300	°C
P_{tot}	total power dissipation	T_{amb} = 70 °C		-	0.5	W
T_{stg}	storage temperature			–40	+125	°C
T_j	junction temperature			-	125	°C
T_{amb}	ambient temperature			0	70	°C
V_{esd}	electrostatic discharge voltage	pins SDA, SCL, SADDR0 and SADDR1; machine model	[3]	-	±150	V
		all other pins; machine model	[4]	-	±200	V

[1] Stresses above the absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

[2] The maximum allowed ambient temperature T_{amb} depends on the assembly condition of the package and especially on the design of the PCB. The application mounting must be done in such a way that the maximum junction temperature $T_{j(max)}$ is never exceeded.

[3] Class A according to EIA/JESD22-A115.

[4] Class B according to EIA/JESD22-A115.

11. Thermal characteristics

Table 67. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in still air	33	K/W

The thermal resistance depends strongly on the nature of the PCB used in the application and on its design. The thermal resistance given in Table 67 corresponds to the value that can be measured on a multilayer PCB (4 layers) as defined by EIA/JESD51-2. This value is given for information only.

The junction temperature influences strongly the reliability of an IC. The PCB used in the application contributes on a large part to the overall thermal characteristic. It must therefore be designed to insure that the junction temperature of the IC never exceeds $T_{j(max)}$ = 125 °C at the maximum ambient temperature.

The IC has to be soldered to ground with its die-attached paddle. Plenty of vias are recommended to remove the heat.

12. Characteristics

Table 68. Characteristics

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power supply							
$V_{DD(1V2)}$	supply voltage (1.2 V)	digital and analog		1.08	1.2	1.32	V
$V_{DD(3V3)}$	supply voltage (3.3 V)	digital and analog		2.97	3.3	3.63	V
$I_{DD(tot)(1V2)}$	total supply current (1.2 V)			-	28	33	mA
$I_{DD(tot)(3V3)}$	total supply current (3.3 V)		[1]	-	125	136	mA
P_{tot}	total power dissipation	default settings; 75 Ω drive; f_s = 54 MHz at ADC; including DAC loads; R_{RSET} = 1 kΩ	[1]	-	434	490	mW
		Power-save mode; f_s = 54 MHz at ADC; including DAC loads; R_{RSET} = 2 kΩ; see Section 13.6	[2]	-	324	369	mW
		Standby mode		-	7	10	mW
Digital I/Os							
V_{IH}	HIGH-level input voltage	all inputs (except pin XIN); including voltage on outputs in 3-state mode		0.7 × $V_{DD(3V3)}$	-	6.0	V
V_{IL}	LOW-level input voltage	all inputs (except pin XIN); including voltage on outputs in 3-state mode		-	-	0.8	V
V_{OH}	HIGH-level output voltage	source current 4 mA		$V_{DD(3V3)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	sink current 4 mA		-	-	0.4	V
C_i	input capacitance			-	-	5	pF
Master clock							
$f_{clk(o)(PLL)}$	PLL output clock frequency		[3]	-	108	-	MHz
$\Delta f/f_{clk}$	relative frequency deviation from clock frequency			-	-	±200	10^{-6}
Reference frequency in Slave mode							
$f_{clk(ext)}$	external clock frequency			-	16	-	MHz
$V_{i(RMS)}$	RMS input voltage	AC coupled		200	250	-	mV
SR_r	rising slew rate	external clock		30	-	-	mV/ns
$t_{jit(cc)}$	cycle-to-cycle jitter time	RMS value		-	12.5	-	ps
C_i	input capacitance	on pin XIN		-	3	-	pF
Reference frequency in Oscillator mode (with a crystal)							
f_{xtal}	crystal frequency			-	16	-	MHz
$\Delta f_{xtal}/f_{xtal}$	relative crystal frequency variation	temperature, ageing and spreading		-	-	±200	10^{-6}
$T_{amb(xtal)}$	crystal ambient temperature			0	-	70	°C

Table 68. Characteristics *…continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
IF input							
$V_{i(p-p)}$	peak-to-peak input voltage	for full-scale ADC input (0 dBFS)		1.8	2.0	2.2	V
$R_{i(dif)}$	differential input resistance			10	15	-	kΩ
$C_{i(dif)}$	differential input capacitance			-	2	3	pF
V_i	input voltage	operational input related to ADC full scale; all standards; sum of all signals		–3	–3	–3	dBFS
f_i	input frequency	PC / SC1					
		M/N standard		-	5.75 / 1.25	-	MHz
		B standard		-	6.75 / 1.25	-	MHz
		G/H standard		-	7.75 / 2.25	-	MHz
		I standard		-	7.75 / 1.75	-	MHz
		DK and L standard		-	7.75 / 1.25	-	MHz
		L-accent standard		-	1.25 / 7.75	-	MHz
		FM radio		-	1.25	-	MHz
IF selectivity							
$\alpha_{sup(stpb)}$	stop-band suppression	Hilbert filter stop-band		–60	-	-	dB
		decimation filter stop-band		–40	-	-	dB
		notch for NSC (NPC for L-accent standard)	[4]	–40	-	-	dB
Carrier recovery FPLL							
$B_{-3dB(cl)}$	closed-loop –3 dB bandwidth	ultrawide		280	280	280	kHz
		superwide		130	130	130	kHz
		wide		60	60	60	kHz
		medium		30	30	30	kHz
		narrow		15	15	15	kHz
Δf_{pullin}	pull-in frequency range		[5]	±830	±830	±830	kHz
$m_{over(PC)}$	picture carrier overmodulation index	black for L/L-accent standard; flat field white else		115	117	-	%
$f_{step(AFC)}$	AFC step frequency	128 steps	[5]	13	-	-	kHz
IF demodulation (video equalizer in Flat mode)							
$B_{T(tot)}$	total transition bandwidth	Nyquist filter; all standards		1	1	1	MHz
$\alpha_{sup(stpb)}$	stop-band suppression	Nyquist filter; all standards		–60	-	-	dB
		video low-pass filter (M/N, B/G/H, I, D/K, L/L-accent standard)		-	–60	-	dB

Table 68. Characteristics *…continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$B_{video(-1dB)}$	−1 dB video bandwidth	M/N standard		-	3.9	-	MHz
		B/G/H, I, D/K, L/L-accent standard		-	4.9	-	MHz
$t_{ripple(GDE)}$	group delay equalizer ripple time	peak value for B/G/H half, D/K half, I flat, M (FCC) full, L/L-accent full standard		-	20	40	ns
Digital IF AGC (internal loop)							
$B_{-3dB(cl)}$	closed-loop −3 dB bandwidth	negative modulation (all standards except L/L-accent)	[6]	400	-	-	Hz
		positive modulation (L/L-accent standard)		0.2	-	-	Hz
t_{resp}	response time	±20 dB level change; video settled within ±3 dB					
		negative modulation (all standards except L/L-accent)		3	3	3	ms
		positive modulation (L/L-accent standard)		100	100	100	ms
ΔG_{AGC}	AGC gain range			−20	-	+48	dB
Tuner IF AGC (external loop)							
t_{resp}	response time	at 60 dBμV (RMS) PC input; ±20 dB level change; video settled within ±3 dB	[7]				
		with TDA8275A; positive modulation		-	4000	-	ms
		with TDA8275A; negative modulation		-	500	-	ms
		with TDA1827x; positive modulation		-	3000	-	ms
		with TDA1827x; negative modulation		-	600	-	ms
$f_{-3dB(lpf)}$	low-pass filter −3 dB frequency	IF AGC postfilter		0.9	1.0	1.1	kHz

Table 68. Characteristics *…continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
CVBS output							
$V_{o(p-p)}$	peak-to-peak output voltage	negative PC modulation (all standards except L/L-accent); 75 Ω DC load; sync-white modulation					
		65 %		-	0.7	0.9	V
		90 % (nominal)		0.8	1.0	1.2	V
		115 %		-	1.0	1.2	V
		positive PC modulation (L/L-accent standard); 75 Ω DC load; sync-white modulation					
		65 %		-	0.7	0.9	V
		97 % (nominal)		0.8	1.0	1.2	V
		115 %		-	1.0	1.2	V
$B_{video(-3dB)}$	–3 dB video bandwidth	overall video response; CVBS equalizer flat					
		all standards except M/N		4.8	4.85	-	MHz
		M/N standard		3.9	4.05	-	MHz
$\alpha_{resp(f)}$	frequency response	video equalizer; 8 equally spaced settings; value at 3.9 MHz		–5	-	+4.5	dB
G_{dif}	differential gain	*"ITU-T J.63 line 330"*		-	1.5	3	%
φ_{dif}	differential phase	*"ITU-T J.63 line 330"*		-	1.5	3	deg
$V_{stlt}/V_{CVBS(p-p)}$	synchronization tilt voltage to peak-to-peak CVBS voltage ratio			-	1	2	%
$V_{ftlt}/V_{CVBS(p-p)}$	frame tilt voltage to peak-to-peak CVBS voltage ratio	all standards except L/L-accent		-	1	3	%
		L/L-accent standard in peak white AGC detection		-	1	5	%
$\Delta V_{tro}/V_{tro}$	relative transient response overshoot voltage variation	2T pulse	[8]	-	2	5	%
$\alpha_{IM(blue)}$	intermodulation suppression (blue)	carrier levels related to PC sync; PC = –3.2 dB; CC = –19.2 dB; SC = –13 dB					
		1.1 MHz (related to black-to-white in RMS, equals CC + 3.6 dB)		-	64	-	dB
		3.3 MHz (related to CC)		-	75	-	dB

Table 68. Characteristics *...continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\alpha_{IM(yellow)}$	intermodulation suppression (yellow)	carrier levels related to PC sync; PC = −10 dB; CC = −19.2 dB; SC = −13 dB				
		1.1 MHz (related to black-to-white in RMS, equals CC + 3.6 dB)	-	69	-	dB
		3.3 MHz (related to CC)	-	81	-	dB
$(S/N)_w$	weighted signal-to-noise ratio	all standards; unified weighting filter (*"ITU-T J.61"*); PC at −6 dBFS	58	62	-	dB

Table 68. Characteristics *…continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PSRR	power supply rejection ratio	f_{ripple} = 70 Hz; 100 mV (p-p); video signal: gray; level: 50 %; TDA8295 stand alone; input level: 60 dBμV (RMS) PC					
		positive video modulation; L standard; 1.2 V		-	52	-	dB
		positive video modulation; L standard; 3.3 V	[9]	-	30	-	dB
		negative video modulation; B standard; 1.2 V		-	51	-	dB
		negative video modulation; B standard; 3.3 V	[9]	-	30	-	dB
		f_{ripple} = 70 Hz; 100 mV (p-p); video signal: gray; level: 50 %; together with TDA8275A; input level: 60 dBμV (RMS) PC					
		positive video modulation; L standard; 1.2 V		-	26	-	dB
		positive video modulation; L standard; 3.3 V	[9]	-	22	-	dB
		negative video modulation; B standard; 1.2 V		-	43	-	dB
		negative video modulation; B standard; 3.3 V	[9]	-	32	-	dB
		f_{ripple} = 70 Hz; 100 mV (p-p); video signal: gray; level: 50 %; together with TDA1827x; input level: 60 dBμV (RMS) PC					
		positive video modulation; L standard; 1.2 V		-	26	-	dB
		positive video modulation; L standard; 3.3 V	[9]	-	22	-	dB
		negative video modulation; B standard; 1.2 V		-	43	-	dB
		negative video modulation; B standard; 3.3 V	[9]	-	32	-	dB
$\alpha_{sup(f)L(unw)}$	unwanted leakage frequency suppression	4.8 MHz video modulation; related to black-to-white in 10 MHz to 200 MHz band		-	56	-	dB

Table 68. Characteristics *…continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SSIF/mono sound output						
$f_{o(SSIF)}$	SSIF output frequency	SC1 or FM radio carrier [10]				
		M standard	-	4.5	-	MHz
		B/G/H standard	-	5.5	-	MHz
		I standard	-	6.0	-	MHz
		D/K/L/L-accent standard	-	6.5	-	MHz
		FM radio	-	5.5	-	MHz
$V_{o(SSIF)(RMS)}$	RMS SSIF output voltage	1 kΩ DC or AC load; no modulation; PC / SC1 = 13 dB; scaled linearly for all other ratios				
		all standards except B/G/H	30	35	40	mV
		B/G/H standard	27	32	37	mV
		FM radio (single carrier)	460	530	610	mV
$V_{o(AF)(RMS)}$	RMS AF output voltage	1 kΩ DC or AC load				
		M standard; 54 % modulation degree (±13.5 kHz FM deviation before pre-emphasis)	125	143	165	mV
		B, G/H, I, D, K standard; 54 % modulation degree (±27 kHz FM deviation before pre-emphasis)	125	143	165	mV
		L/L-accent standard; AM; m = 54 %	110	126	145	mV
		FM radio; 30 % modulation degree (±22.5 kHz FM deviation before pre-emphasis)	56	65	75	mV
		high Deviation mode (D/K standard China); FM deviation before pre-emphasis ±400 kHz; sound level setting: –12 dB	487	560	644	mV

Table 68. Characteristics *…continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\alpha_{hr(AF)}$	AF headroom	before clipping; 1 kΩ DC or AC load				
		M standard; related to ±25 kHz peak deviation before pre-emphasis	7	7	7	dB
		B, G/H, I, D, K standard; related to ±50 kHz peak deviation before pre-emphasis	7	7	7	dB
		L/L-accent standard; PC / SC1 ratio for start of audio output clipping; AM; m = 100 %; related to mean SC1	1	1	1	dB
		FM radio; 30 % modulation degree related to ±22.5 kHz peak deviation before pre-emphasis	7	7	7	dB
τ_{deemp}	de-emphasis time constant	M/N standard (mono); FM radio USA	75	75	75	µs
		B/G/H, I, D/K standard; FM radio Europe	50	50	50	µs
B_{-3dB}	–3 dB bandwidth	audio low-pass filter				
		L/L-accent standard	30	30	30	kHz
		M-BTSC standard	140	140	140	kHz
THD	total harmonic distortion	FM; for 50 kHz deviation before pre-emphasis (25 kHz for M standard)	-	0.1	0.2	%
		AM; m = 80 %	-	0.6	1	%
$B_{AF(-3dB)}$	–3 dB AF bandwidth	AM	20	27	-	kHz
		FM	40	50	-	kHz
α_{AM}	AM suppression	of FM demodulator; AM: f = 1 kHz; m = 54 % referenced to 27 kHz FM deviation	40	46	-	dB

Table 68. Characteristics *…continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$(S/N)_{w(AF)}$	AF weighted signal-to-noise ratio	via internal mono sound demodulator; *"ITU-R BS.468-4"*; FM mode related to 27 kHz deviation before pre-emphasis; 10 % residual PC; SC1				
		black picture	54	58	-	dB
		flat field white picture	53	57	-	dB
		6 kHz sine wave picture	52	56	-	dB
		250 kHz square wave picture	52	56	-	dB
		crosshatch picture	52	56	-	dB
		color bar picture	54	58	-	dB
		via internal mono sound demodulator; *"ITU-R BS.468-4"*; AM; m = 54 %; 3 % residual PC; SC1				
		black picture	43	45	-	dB
		flat field white picture	43	46	-	dB
		color bar picture	43	46	-	dB
		via internal mono sound demodulator; *"ITU-R BS.468-4"*; FM Radio mode	47	51	-	dB

Table 68. Characteristics *…continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$(S/N)_{w(SC1)}$	first sound carrier weighted signal-to-noise ratio	via external SSIF sound demodulator in Dual mode; *"ITU-R BS.468-4"*; FM mode related to 27 kHz deviation before pre-emphasis; 10 % residual PC				
		black picture	60	64	-	dB
		flat field white picture	60	64	-	dB
		6 kHz sine wave picture	54	58	-	dB
		250 kHz square wave picture	55	59	-	dB
		crosshatch picture	54	58	-	dB
		color bar picture	59	63	-	dB
		via SSIF sound demodulator; *"ITU-R BS.468-4"*; AM; m = 54 %; 3 % residual PC				
		black picture	40	43	-	dB
		flat field white picture	40	43	-	dB
		color bar picture	40	43	-	dB
$(S/N)_{w(SC2)}$	second sound carrier weighted signal-to-noise ratio	via external SSIF sound demodulator in Dual mode; *"ITU-R BS.468-4"*; FM mode related to 27 kHz deviation before pre-emphasis; 10 % residual PC				
		black picture	58	62	-	dB
		flat field white picture	58	62	-	dB
		6 kHz sine wave picture	54	58	-	dB
		250 kHz square wave picture	46	50	-	dB
		crosshatch picture	56	60	-	dB
		color bar picture	57	61	-	dB
$(S/N)_w$	weighted signal-to-noise ratio	FM radio; via SSIF sound demodulator in Mono mode; *"ITU-R BS.468-4"*	60	64	-	dB

Table 68. Characteristics *…continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PSRR	power supply rejection ratio	f_{ripple} = 70 Hz; 100 mV (p-p); video signal: gray; level: 50 %; TDA8295 stand alone					
		FM sound; 1.2 V		-	72	-	dB
		FM sound; 3.3 V	[9]	-	33	-	dB
		AM sound; 1.2 V		-	68	-	dB
		AM sound; 3.3 V	[9]	-	37	-	dB
		f_{ripple} = 70 Hz; 100 mV (p-p); video signal: gray; level: 50 %; together with TDA8275A; input level: 60 dBμV (RMS) PC					
		FM sound; 1.2 V		-	72	-	dB
		FM sound; 3.3 V	[9]	-	33	-	dB
		AM sound; 1.2 V		-	22	-	dB
		AM sound; 3.3 V	[9]	-	22	-	dB
		f_{ripple} = 70 Hz; 100 mV (p-p); video signal: gray; level: 50 %; together with TDA1827x; input level: 60 dBμV (RMS) PC					
		FM sound; 1.2 V		-	72	-	dB
		FM sound; 3.3 V	[9]	-	33	-	dB
		AM sound; 1.2 V		-	22	-	dB
		AM sound; 3.3 V	[9]	-	22	-	dB
$\alpha_{sup(f)L(unw)}$	unwanted leakage frequency suppression	related to SSIF (SC1) in 10 MHz to 200 MHz band		-	33	-	dB

[1] 50 % ADC current; 100 % video DAC current; 50 % sound DAC current.

[2] 50 % ADC current; 50 % video DAC current; 25 % sound DAC current.

[3] See Section 9.3.19 for PLL setting.

[4] Standard dependent located at 7.25 MHz, 8.25 MHz, 9.25 MHz, 9.75 MHz and 10.25 MHz.

[5] The pull-in range can be doubled to ±1660 kHz by I^{2}C-bus register like described in Table 16. Then the AFC read-out has 256 steps.

[6] To counteract a fast IF level reduction, the digital IF AGC loop has a speed-up circuit for positive video modulation.

[7] In the ordinary system application, this slow response is counteracted by the fast digital IF AGC loop. ADC clipping is practically avoided by fast-attack AGC characteristic.

[8] HAD: 250 ns for M standard, 200 ns for others.

[9] The values given are measured with an IF AGC time constant of 5 Hz. For that, capacitor C7 in Figure 12 must be chosen 220 nF instead of 2.2 nF. Doing so, the PSRR on 3.3 V together with the tuner can be improved.

[10] SC2 is not listed, but supported for all world standards.

13. Application information

13.1 Typical application

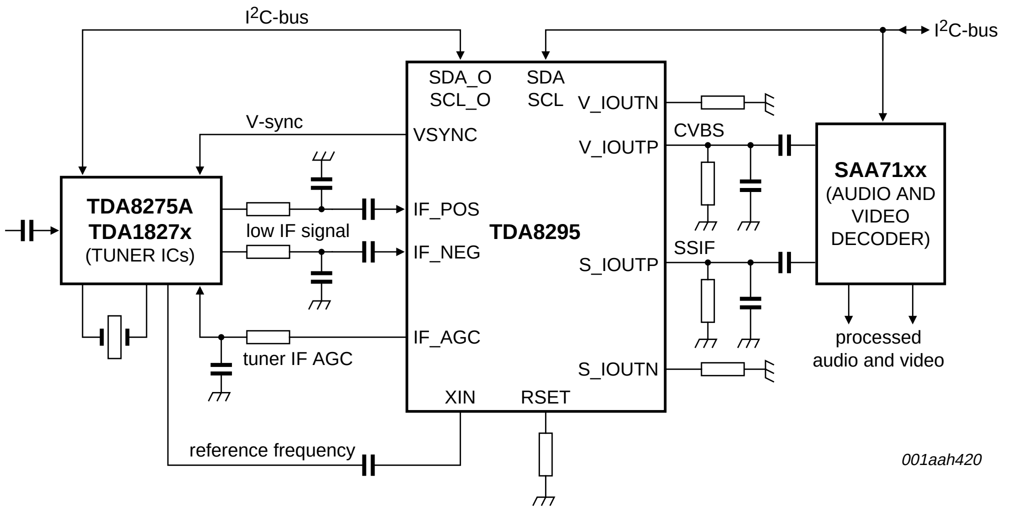
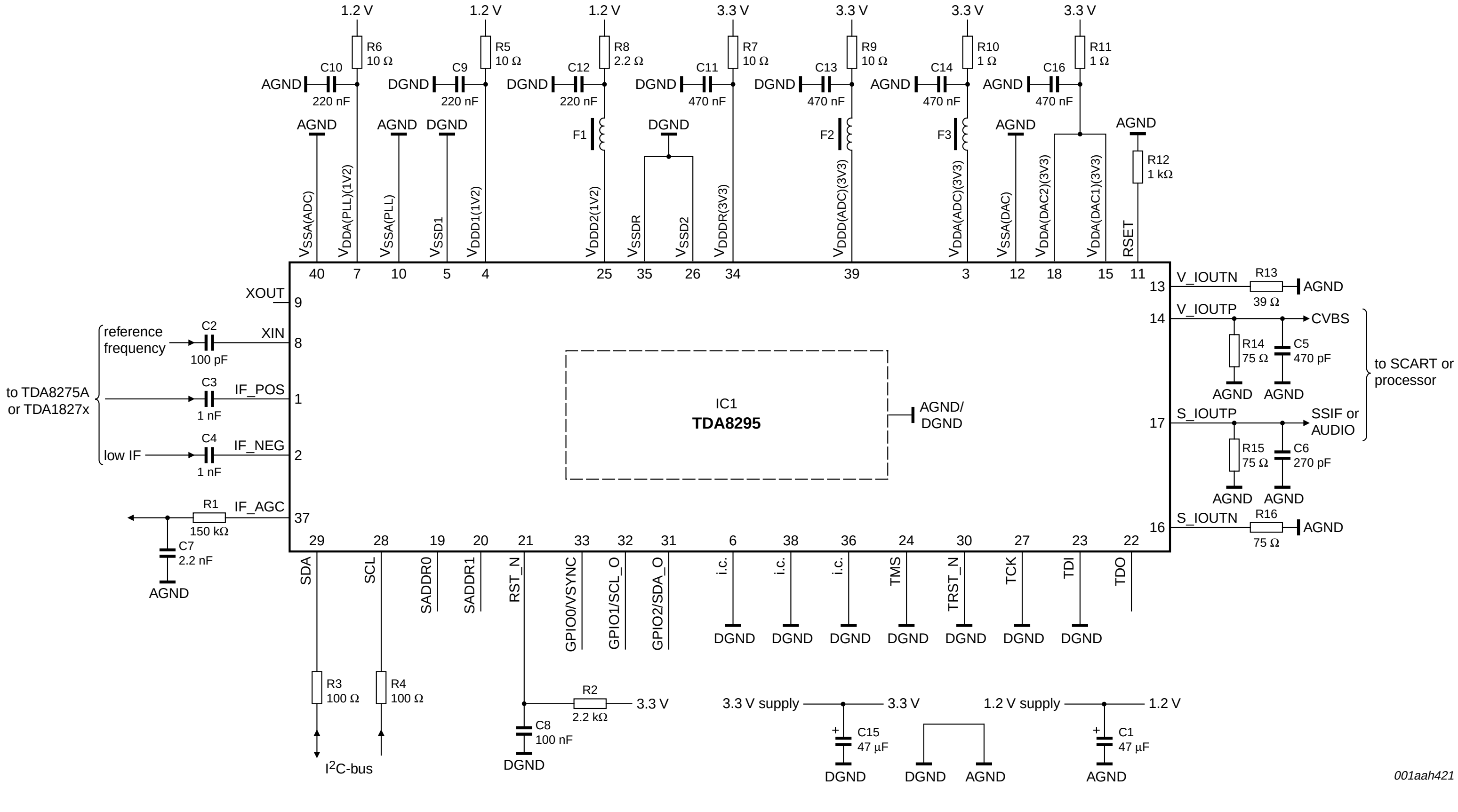


Fig 11. Typical application of TDA8295

13.2 Detailed application diagram



F1, F2, F3: BLM18AG102SN1 ferrite bead

Preferred components: SMD R1 has to be placed near to TDA8295 pin 37 and SMD C7 near to TDA8275A or TDA1827x

Fig 12. Detailed application diagram of TDA8295

13.3 DAC connection

This DAC has a differential current output capable of driving a doubly terminated 75 Ω transmission line without external buffers. But it can also be used in single-ended applications. In that case both outputs still need proper termination. The off-chip resistive load must be connected to ground.

With the B_DA_V and B_DA_S coarse output level adjustment registers, the output current can be increased (linearly) up to two times. However, the maximum output voltage at both V_IOUTP, V_IOUTN and S_IOUTP, S_IOUTN output nodes still is 1.5 V.

DNL and INL increase when the external biasing resistor is increased. When higher load resistances are used, distortion will increase linearly. About 12 dB increase in harmonic distortion is expected at 150 Ω.

Several measures can be taken in order to reach good performance. Decouple the $V_{DDA(DAC1)(3V3)}$ and the $V_{DDA(DAC2)(3V3)}$ supplies with at least 100 nF. Place the external bias resistor close to the chip. Do not add decoupling capacitance to pin RSET.

The following relation gives the value of the full-scale current I_{FS} in function of the bias resistance value, FineControl (B_REF) and CoarseControl (B_DA_V or B_DA_S):

$$I_{FS} = \frac{1.216}{RSET} \times \frac{100}{100 - FineControl} \times \frac{1}{5} \times \frac{64 + CoarseControl}{48} \times 64 \qquad (1)$$

$-7 \leq$ FineControl $\leq +7$

$0 \leq$ CoarseControl ≤ 63

For programming of FineControl (B_REF) see Table 55, for CoarseControl signals B_DA_V see Table 53, for B_DA_S see Table 54.

13.4 ADC connection

The input signals of the ADC (IF_POS and IF_NEG) can be either AC coupled by means of two capacitors or connected directly to the inputs (DC coupled). This selection is done by programming of DCIN, see Table 51.

In case of AC coupling, DCIN should be set to logic 0, which enables two resistive dividers between $V_{DDA(ADC)(3V3)}$ and V_{SSD1} take care of the correct DC biasing of the input signals. In case only a single-ended input signal is available, this signal should be connected to the IF_POS input by means of a coupling capacitor whereas the IF_NEG input should be connected to ground using a similar capacitor.

In case the input signal is DC coupled, the input resistor network can be switched off by setting the DCIN bit to logic 1. When using the ADC in this mode, the Common mode level of the input signals should be at $0.5 \times V_{DDA(ADC)(3V3)}$. In case of single-ended operation, the input signal should be connected directly to the IF_POS input and the IF_NEG input should be connected to a voltage equal to the Common mode level of the input signal ($0.5 \times V_{DDA(ADC)(3V3)}$).

The peak-to-peak input range can be set to 1 V (p-p) or 2 V (p-p) by programming of GAINSET (see Table 51). With a differential input the performances of the ADC are slightly better with GAINSET = 0 whereas with a single-ended input they are slightly better with GAINSET = 1.

13.5 Reset operation

13.5.1 Hardware reset

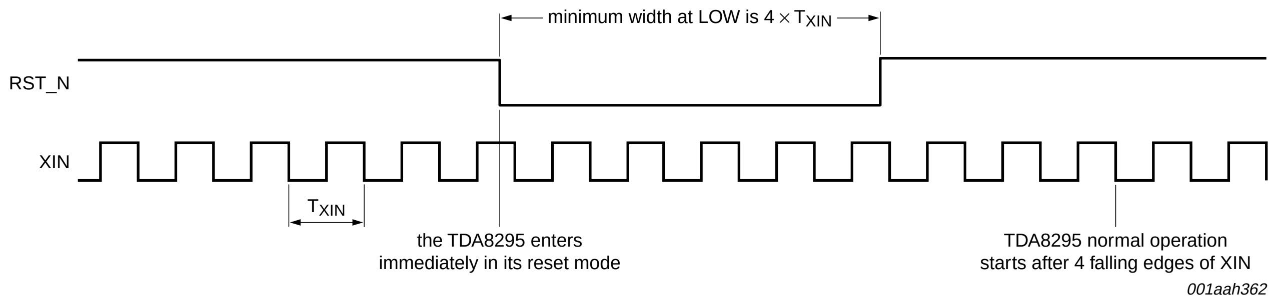


Fig 13. Hardware reset operation

After a hardware reset, the registers are set to default (power-on reset values) according to Table 10. M/N standard is the default standard.

13.5.2 Software reset

A software reset can be done each time something has been programmed. The software reset does not affect the content of the registers but clears the flip-flops in the design. For the activation of the software reset see Table 49 bit CLB.

13.6 Application hints

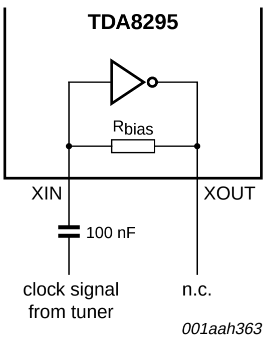
- In case GPIO1 and GPIO2 are configured as I^2C-bus feed-through, a capacitor C = 33 pF to GND must be added at pin 32 (GPIO1/SCL_O). This ensures a reliable behavior in Read mode.
- The detailed application diagram (see Figure 12) shows the video DAC connection driving a 75 Ω DC load and the sound DAC driving > 1 kΩ AC/DC load. Power-save mode: In order to reduce power consumption, the video DAC can be run with half current and the sound DAC with a quarter current by changing RSET (R12 in Figure 12) to 2 kΩ. This is possible, if the audio/video processor is rather high-ohmic (> 1 kΩ). The following components in Figure 12 have to be replaced then: R13 = 75 Ω; R15 and R16 = 150 Ω; C5 = 220 pF; C6 = 120 pF. A performance degradation is not expected in the Power-save mode.

The TDA8295 has been designed in such a way, that a simple upgrade of the predecessor TDA8290 is possible:

1. Change the 1.8 V power supply to 1.2 V. This can be done easily with a variable voltage regulator, where the sense pin is grounded. This delivers the band gap voltage of 1.25 V to the output. Or take a fixed regulator.
2. The RSET resistor (R12 in Figure 12) has to be decreased by 20 % in order to make the DAC output swing higher (1.5 V instead of 1.25 V).
3. Pin 6 and pin 36 (both internally connected pins) can still stay connected to the 1.2 V power supply, as done in the PCBs for the predecessor TDA8290 without harm. However, take grounds for new designs, because they are more easily accessible on a PCB.

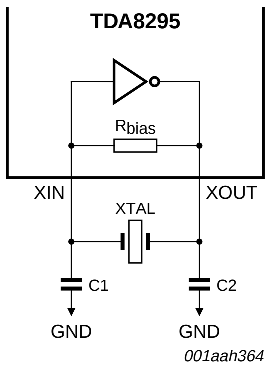
13.7 Crystal connection

The typical crystal frequency value is 16 MHz. The values of the passive components depend on crystal manufacturer. The oscillator can be set in two configurations depending on the origin of the crystal. Figure 14 describes the case of an crystal shared with the tuner and the TDA8295 (Slave mode), Figure 15 the case of an crystal dedicated to the TDA8295 (Oscillator mode).



Slave mode

Fig 14. Reference clock application



Oscillator mode

Fig 15. Oscillator application

In Oscillator mode, only a crystal and the load capacitances C1 and C2 need to be connected externally since the feedback resistance is integrated on chip. In this mode the oscillator gain stage can have a normal or large transconductance, determined by the HF bit (see also Table 61). A large transconductance is required for higher oscillation frequencies, higher series resistance of the crystal and higher external load capacitors. For an accurate time reference it is advised to use the load capacitors as specified in Table 69. C_L is the typical load capacitance of the crystal and is usually specified by the crystal manufacturer.

Table 69. Crystal parameters together with external components

Fundamental oscillation frequency	Crystal load capacitance $C_{L(xtal)}$ (pF)	Crystal series resistance $R_{s(xtal)}$ (Ω)	External load capacitors	
			C1 (pF)	C2 (pF)
Bit HF = 0				
1 MHz to 5 MHz	10	< 300	18	18
	20	< 300	39	39
	30	< 300	56	56
5 MHz to 10 MHz	10	< 300	18	18
	20	< 200	39	39
	30	< 100	56	56
10 MHz to 15 MHz	10	< 160	18	18
	20	< 60	39	39
15 MHz to 20 MHz	10	< 80	18	18

Table 69. Crystal parameters together with external components *...continued*

Fundamental oscillation frequency	Crystal load capacitance $C_{L(xtal)}$ (pF)	Crystal series resistance $R_{s(xtal)}$ (Ω)	External load capacitors	
			C1 (pF)	C2 (pF)
Bit HF = 1				
10 MHz to 15 MHz	10	< 200	18	18
	20	< 120	39	39
15 MHz to 20 MHz	10	< 180	18	18
	20	< 100	39	39
20 MHz to 25 MHz	10	< 160	18	18
	20	< 80	39	39
25 MHz to 30 MHz	10	< 130	18	18
	20	< 60	39	39
30 MHz to 35 MHz	10	< 120	18	18
35 MHz to 40 MHz	10	< 100	18	18
40 MHz to 45 MHz	10	< 80	18	18
45 MHz to 50 MHz	10	< 60	18	18

14. Test information

14.1 Boundary scan interface (*"IEEE Std. 1149.1"*)

The TDA8295 implements a boundary scan architecture to allow access to, and control of, board test support features within integrated circuits through a TAP. The TAP controller is a synchronous state machine that controls the sequence of operations on the TAP circuitry when the TMS signal changes. All state transitions occur on the basis of the TMS value on the rising edge of TCK. The instruction register is a shift register based design. It decodes the test to be performed and/or the test data register to be accessed. The instructions are shifted into the register through the TDI and are latched as the current instruction at the completion of the shifting process. The TDA8295 boundary scan architecture includes: a TAP controller, a scannable instruction register and three scannable test data registers: a boundary scan register, a device ID register, and a bypass register.

The supported instructions are: EXTEST, IDCODE, SAMPLE, INTEST, CLAMP, HIGHZ and BYPASS.

The boundary scan register is composed of 16 cells (see Table 70). Each cell is associated either to an input pad, an output pad, a bidirectional pad or to the bidirectional or 3-state command itself. All cells are of 'observe and control' type.

The device ID register is a 32-bit identification register that is included in the scan register itself and contains the ID number. It is a fixed value that identifies the chip.

ID number structure is:

ID version [3:0] = 1h

ID part number [15:0] = 224Ch

ID manufacturer [11:1] = 015h

ID mandatory [0] = 1h

IDCODE [31:0] = 1224 C02Bh

When the boundary scan function is not used, please connect the four dedicated input pins (TRST_N, TCK, TDI and TMS) to GND.

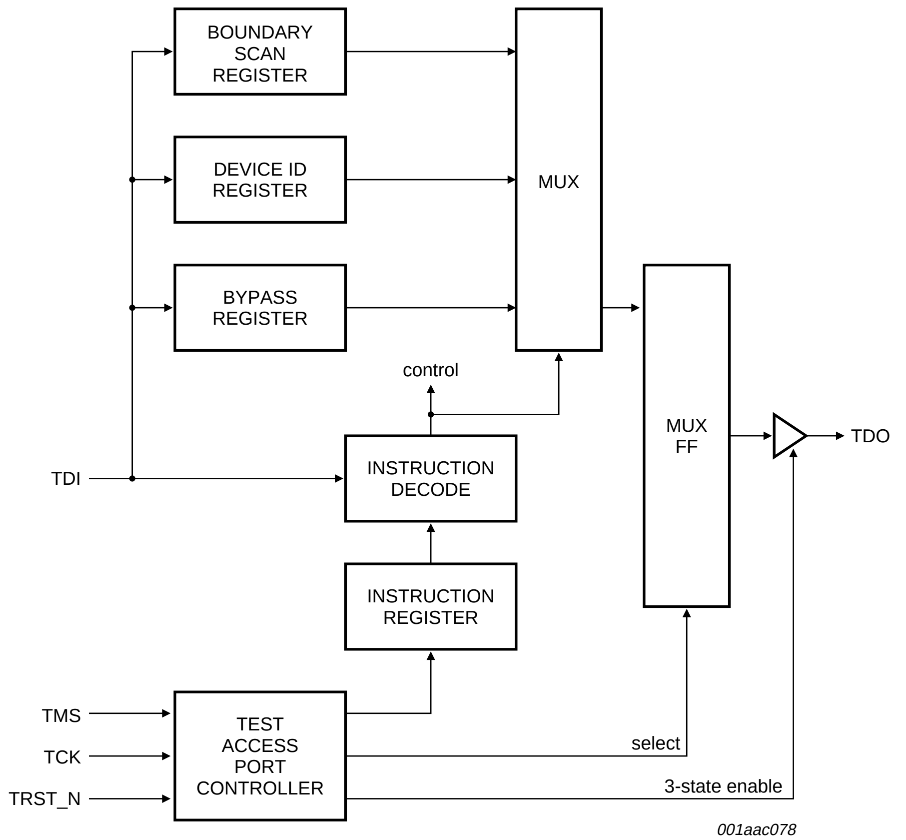


Fig 16. Boundary scan block diagram

Table 70. Boundary scan register list

Pad signal	Chain position	Pad type	Scan type	Control signal
IF_AGC	[1]	Bidir	control/observe	U1.vagc_cmd
	[2]	Ctrl	control/observe	U1.vagc_cmd
GPIO0	[3]	Bidir	control/observe	U1.gpio0_cmd
	[4]	Ctrl	control/observe	U1.gpio0_cmd
GPIO1	[5]	Bidir	control/observe	U1.gpio1_cmd
	[6]	Ctrl	control/observe	U1.gpio1_cmd
GPIO2	[7]	Bidir	control/observe	U1.gpio2_cmd
	[8]	Ctrl	control/observe	U1.gpio2_cmd
SDA	[9]	Bidir	control/observe	U1.sda_cmd
	[10]	Ctrl	control/observe	U1.sda_cmd
SCL	[11]	input	control/observe	-
RST_N	[12]	input	control/observe	-
SADDR1	[13]	Ctrl	control/observe	U1.saddr1_cmd
	[14]	Bidir	control/observe	U1.saddr1_cmd
SADDR0	[15]	Ctrl	control/observe	U0.saddr1_cmd
	[16]	Bidir	control/observe	U0.saddr1_cmd

Table 71. Boundary scan electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{cy}	cycle time	TCK	25	-	-	ns
t_{su}	set-up time	TDI and TMS	0	-	-	ns
t_h	hold time	TDI and TMS	4	-	-	ns
$t_{d(TDO)}$	delay time on pin TDO	on 50 pF	-	-	12	ns

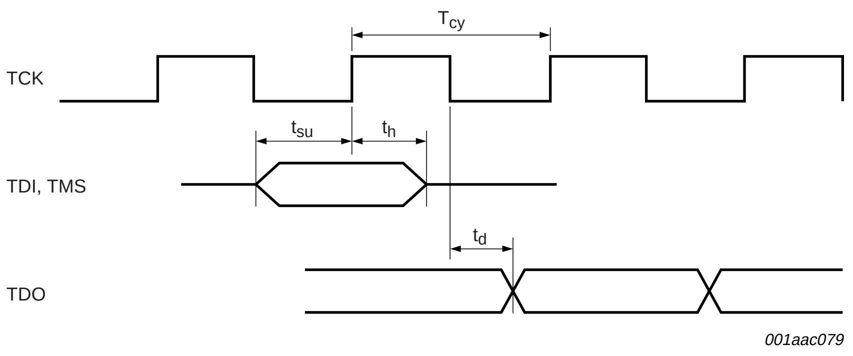
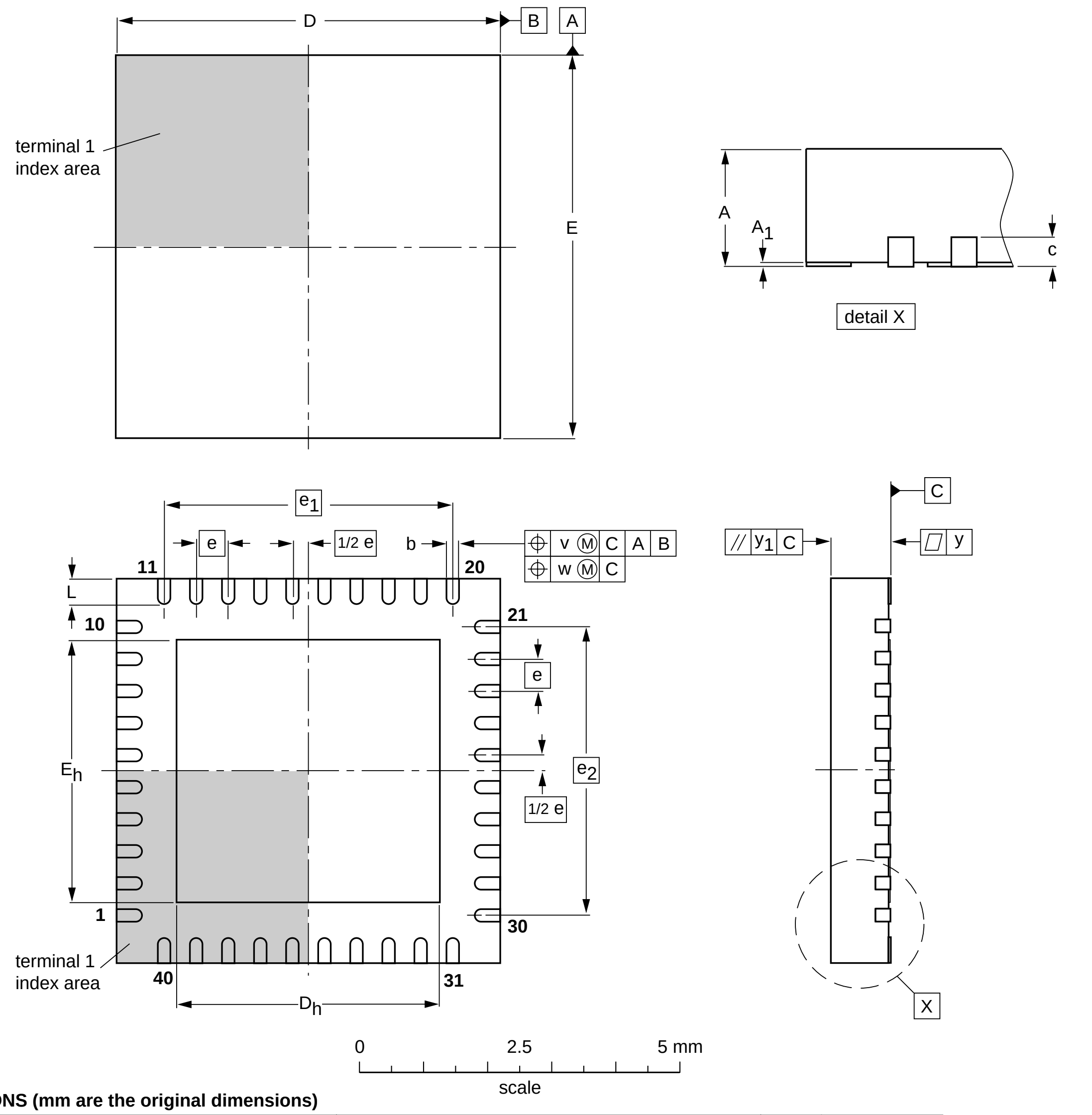


Fig 17. Boundary scan timing diagram

15. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	6.1 5.9	4.25 3.95	6.1 5.9	4.25 3.95	0.5	4.5	4.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT618-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 18. Package outline SOT618-1 (HVQFN40)

16. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 72 and 73

Table 72. SnPb eutectic process (from J-STD-020C)

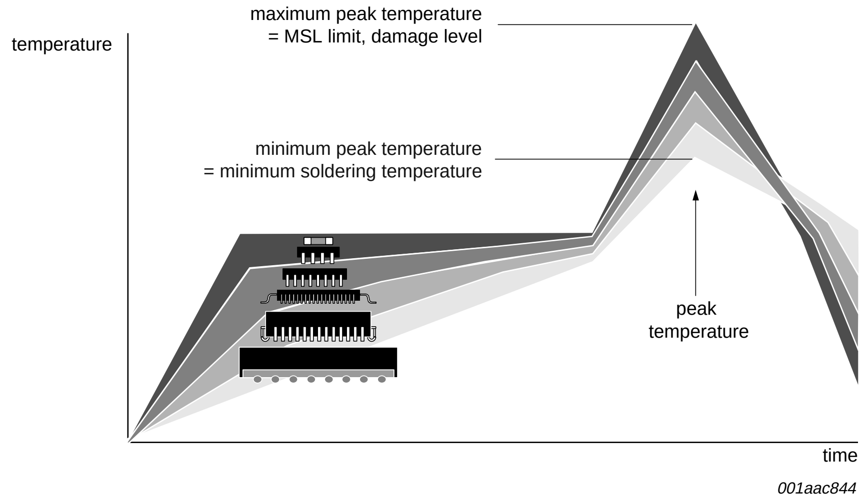
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 73. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



MSL: Moisture Sensitivity Level

Fig 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

17. Abbreviations

Table 74. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
CC	Color Carrier
CMOS	Complementary Metal-Oxide Semiconductor
CORDIC	COordinate Rotation DIgital Computer
CVBS	Color Video Blanking Signal
DAC	Digital-to-Analog Converter
DTO	Digitally Tuned Oscillator
DVD	Digital Versatile Disc
FIR	Finite Impulse Response
FLL	Frequency-Locked Loop
FPLL	Frequency Phase-Locked Loop
FS	Full Scale
GPIO	General Purpose Input Output
H/V	Horizontal and Vertical
HAD	Half Amplitude Duration
IC	Integrated Circuit
ICFM	Incidental Carrier Frequency Modulation

Table 74. Abbreviations *…continued*

Acronym	Description
ICPM	Incidental Carrier Phase Modulation
ID	IDentification
IF	Intermediate Frequency
NPC	Neighbor Picture Carrier
NSC	Neighbor Sound Carrier
PC	Picture Carrier
PCB	Printed-Circuit Board
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QSS	Quasi Split Sound
SAW	Surface Acoustic Wave
SC	Sound Carrier
SMD	Surface Mounted Device
SSIF	Second Sound Intermediate Frequency
STB	Set-Top Box
TAP	Test Access Port
VCR	Video Cassette Recorder
VITS	Vertical Interval Test Signal

18. Revision history

Table 75. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8295_1	20080204	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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