BUK3F00-50WDxx

Controller for TrenchPLUS FETs

Rev. 02 — 21 January 2008 Product data sheet

1. Introduction

This data sheet describes a family of integrated circuits which provide direct digital control of multiple power switches (TrenchPLUS FETs) for use in automotive applications, and which are available in various configurations.

2. General description

Eight channel high-side switch controller in a leaded plastic quad flat package, with digital control and diagnostics, plus load current measurement.

Specific configurations are denoted by the last 2 letters in the type number.

3. Features

- Standby mode with very low power consumption
- Programmable drain current tripping
- Serial Peripheral Interface (SPI) communications
- Outputs controllable via SPI-bus or direct input
- Diagnostic status reporting via SPI-bus
- Analog and digital drain current measurement
- Watchdog for invalid commands or inactive SPI, with programmable time-out
- Programmable interrupt generator
- Overtemperature protection
- Pulse-width modulation with programmable frequency and duty cycle
- ESD protection on all pins
- Protection for battery transient overvoltage and reversed polarity battery connection
- Open-circuit detection
- Configurable fail-safe channel control options

4. Applications

- Automotive applications such as DC and pulse-width modulation control in body control clusters, etc.

5. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	operating	[1]	5.5	13	52	V
T_j	junction temperature		[2]	–40	-	+150	°C

[1] When V_{BAT} < 9 V, the charge pump cannot be guaranteed to drive the external MOSFETs to achieve their specified R_{DSon}.

[2] When T_j > 125 °C, the device will function, but electrical parameters may deviate from the specified values.

6. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BUK3F00-50WDFE	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1
BUK3F00-50WDFM			
BUK3F00-50WDFY			

6.1 Ordering options

Table 3. Type number differences

Type number	Description
BUK3F00-50WDFE	channel 4 has analog trip ratio of $3 \times I_{meas(ADC)(fs)}$[1]
BUK3F00-50WDFM	-
BUK3F00-50WDFY	-

[1] $I_{meas(ADC)(fs)}$ = full-scale ADC measure current.

User-accessible registers; see Table 5.

Protected settings; see Table 19.

Additional metal mask options; see Table 35.

7. Block diagram

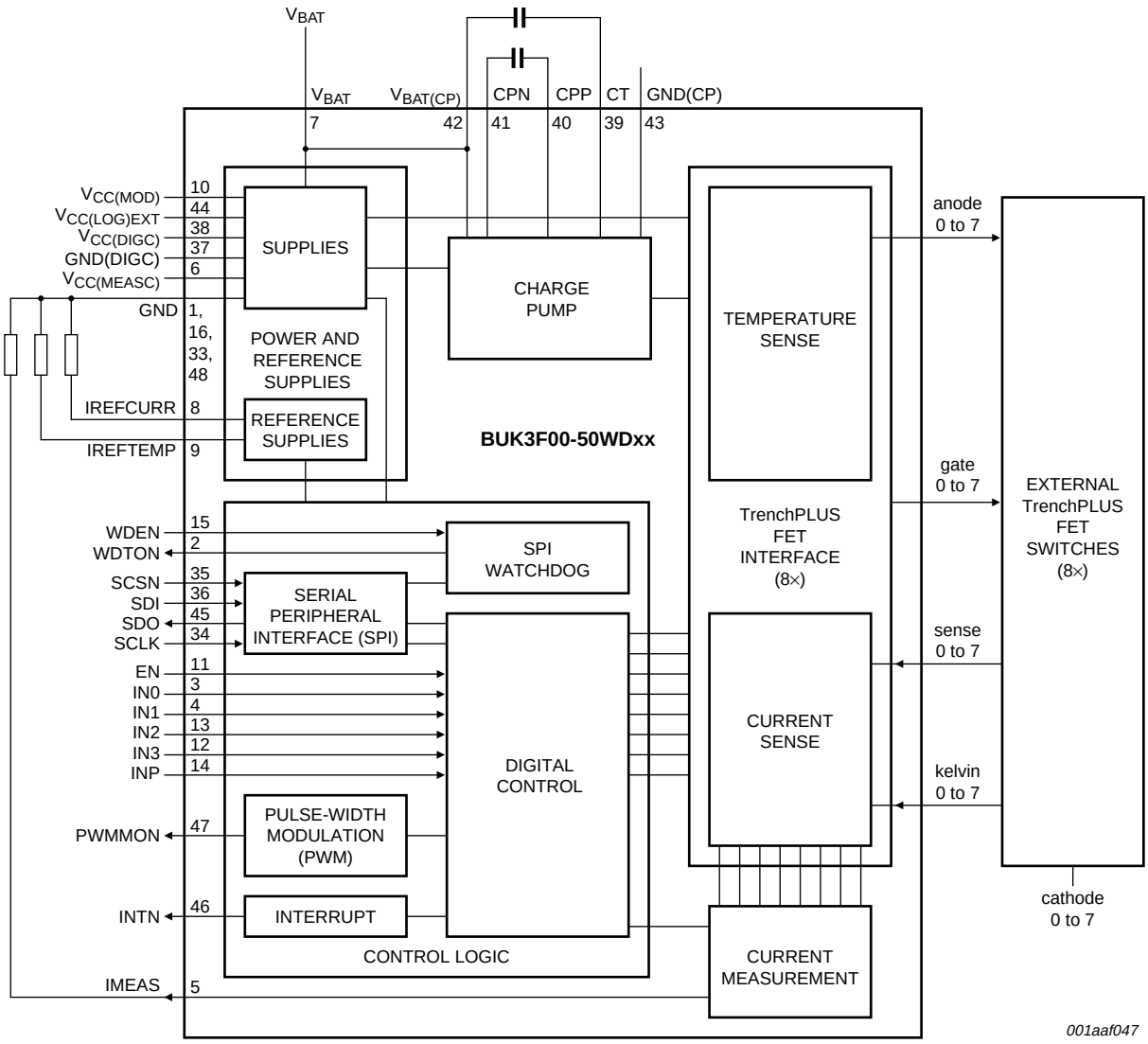


Fig 1. Block diagram

8. Pinning information

8.1 Pinning

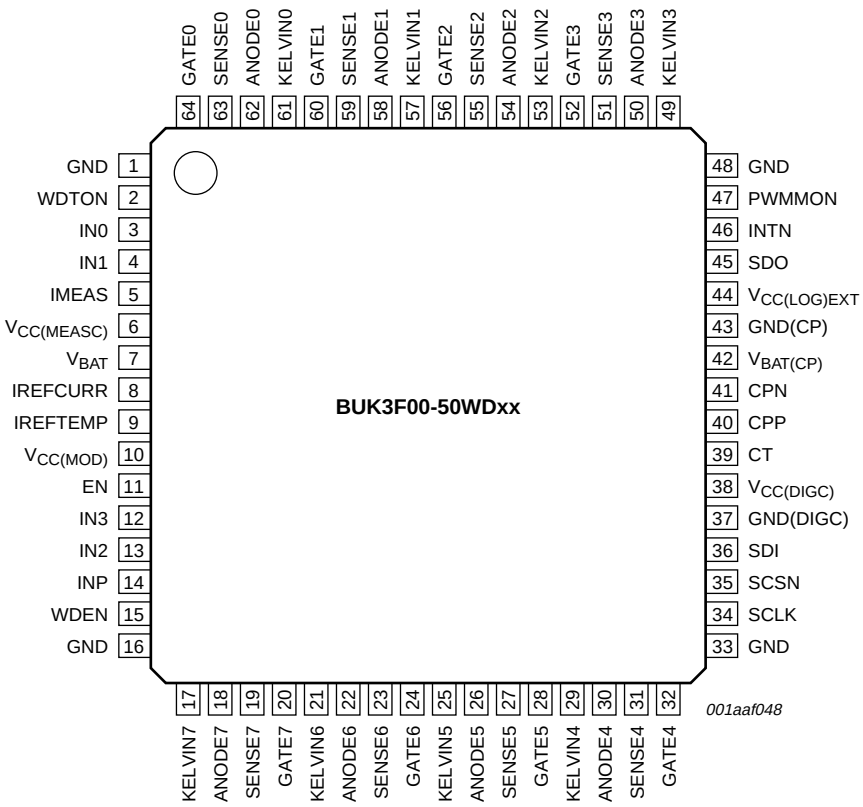


Fig 2. Pin configuration

8.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
Supplies		
V_{BAT}	7	battery supply voltage
GND	1, 16, 33, 48	battery ground
$V_{BAT(CP)}$	42	charge pump battery supply voltage
GND(CP)	43	charge pump ground
$V_{CC(DIGC)}$	38	digital core supply voltage
GND(DIGC)	37	digital core ground
$V_{CC(MOD)}$	10	module supply voltage
$V_{CC(LOG)EXT}$	44	external logic supply voltage for PWMMON and SDO outputs
$V_{CC(MEASC)}$	6	measurement circuit supply voltage

Table 4. Pin description *…continued*

Symbol	Pin	Description
Charge pump capacitors		
CPP	40	positive connection to external pump capacitor
CPN	41	negative connection to external pump capacitor
CT	39	connection to external storage capacitor
Digital		
EN	11	enable input; internal pull-down resistor
INTN	46	interrupt output; open-drain output
WDEN	15	watchdog enable input; internal pull-up resistor
WDTON	2	watchdog timed output; open-drain output
PWMMON	47	PWM frequency monitor output
Serial peripheral interface		
SCLK	34	SPI clock input; internal pull-down resistor
SCSN	35	SPI chip select input; internal pull-up resistor
SDI	36	SPI data input; internal pull-down resistor
SDO	45	SPI data output; 3-state when inactive
Analog		
IREFCURR	8	set reference for current measurement (with external resistor)
IREFTEMP	9	set reference for temperature sense (with external resistor)
IMEAS	5	analog current measurement output (for selected channel)
Direct input pins		
IN0	3	direct input 0; internal pull-down resistor
IN1	4	direct input 1; internal pull-down resistor
IN2	13	direct input 2; internal pull-down resistor
IN3	12	direct input 3; internal pull-down resistor
INP	14	PWM input; internal pull-down resistor
Connections for external TrenchPLUS switches		
Channel 0		
GATE0	64	gate
KELVIN0	61	source kelvin
SENSE0	63	current sense
ANODE0	62	anode of temperature sense diode
Channel 1		
GATE1	60	gate
KELVIN1	57	source kelvin
SENSE1	59	current sense
ANODE1	58	anode of temperature sense diode
Channel 2		
GATE2	56	gate
KELVIN2	53	source kelvin
SENSE2	55	current sense
ANODE2	54	anode of temperature sense diode

Table 4. Pin description *…continued*

Symbol	Pin	Description
Channel 3		
GATE3	52	gate
KELVIN3	49	source kelvin
SENSE3	51	current sense
ANODE3	50	anode of temperature sense diode
Channel 4		
GATE4	32	gate
KELVIN4	29	source kelvin
SENSE4	31	current sense
ANODE4	30	anode of temperature sense diode
Channel 5		
GATE5	28	gate
KELVIN5	25	source kelvin
SENSE5	27	current sense
ANODE5	26	anode of temperature sense diode
Channel 6		
GATE6	24	gate
KELVIN6	21	source kelvin
SENSE6	23	current sense
ANODE6	22	anode of temperature sense diode
Channel 7		
GATE7	20	gate
KELVIN7	17	source kelvin
SENSE7	19	current sense
ANODE7	18	anode of temperature sense diode

9. Functional description

The main functions of the device are:

- Power and reference supplies
- Charge pump
- Control logic
- Current measurement
- TrenchPLUS FET interface (8 ×)

9.1 Power and reference supplies

The main battery supplies power to the device and the eight TrenchPLUS FET switches. This device is intended for vehicle system applications that operate at a battery voltage of 12 V, 24 V or 42 V. The device has several different supply connections to ensure correct operation of the device within the application module.

9.1.1 Battery supply: pins V_{BAT} and GND

Pins V_{BAT} and GND are the direct supply connections of the device to the battery.

Low battery voltage is detected on the charge pump supply pin $V_{BAT(CP)}$. Channels are switched off during extended low battery supply conditions and switched on when normal battery conditions return.

Extended low battery voltage occurs when the battery supply voltage V_{BAT} goes below:

- the battery undervoltage threshold ($V_{th(uv)bat}$) for longer than the battery low time ($t_{low(bat)}$), or
- the battery low threshold voltage ($V_{th(low)bat}$)

Transient low battery voltage occurs when the battery supply voltage V_{BAT} goes below $V_{th(uv)bat}$ for less than $t_{low(bat)}$, but remains above $V_{th(low)bat}$. Transient low battery voltage conditions affect the overcurrent protection; for details see Section 9.5.2 “Overcurrent protection”.

Normal battery voltage occurs when the battery supply voltage exceeds $V_{th(uv)bat}$ for more than the battery high time ($t_{high(bat)}$).

Hysteresis on detection reduces the possibility of repeated switching when the battery supply voltage is close to the threshold values.

The supply circuit has an internal overvoltage clamp to protect the control IC from overvoltage transients and is also protected against ESD. All four GND pins must be connected together to ground.

If this supply is connected to a reverse polarity battery voltage then the FET switches are turned on to protect against conduction through the source-drain diode. This protection operates whether the device is enabled or not.

9.1.2 Module supply: pins $V_{CC(MOD)}$ and GND

Pins $V_{CC(MOD)}$ and GND supply power to the circuits in the device that need to be kept functioning when the main battery supply dips below its normal operating limit. It is anticipated that the connection will be to the protected supply of the application module control circuits. This can be created using a suitable diode and storage capacitor from the battery supply. The connection should be decoupled close to the device.

Low module voltage causes the device to go through a Power-On Reset (POR). This condition is detected when the module supply voltage goes below the module undervoltage threshold ($V_{th(uv)mod}$). The power-on reset is triggered when the supply voltage recovers and exceeds $V_{th(uv)mod}$. Hysteresis on this detection reduces the possibility of repeated resetting when the module supply is close to the threshold value.

The supply circuit has an internal overvoltage clamp to protect the control chip from overvoltage transients and is also protected against ESD. This supply should be protected against reverse battery connection in the application circuit.

9.1.3 External logic supply: pins $V_{CC(LOG)EXT}$ and GND

The external logic supply provides power for the SDO and PWMMON output pins. Pin $V_{CC(LOG)EXT}$ should be connected to the same supply (3.3 V or 5 V) used by the circuits that monitor these outputs.

9.1.4 Analog measurement supply: pins $V_{CC(MEASC)}$ and GND

This supply provides power for the IMEAS analog current measurement output. Pin $V_{CC(MEASC)}$ should be connected to the same supply (3.3 V or 5 V) used by the circuit that uses this output.

If this output is not needed, then pins $V_{CC(MEASC)}$ and IMEAS should be grounded.

9.1.5 Digital supply: pins $V_{CC(DIGC)}$ and GND(DIGC)

This supplies power to the internal regulator for the digital core and should be connected to the same potential as $V_{CC(MOD)}$ and GND. It is not internally connected to the module supply, ensuring that digital noise does not affect the measurement circuits. The connection should be decoupled close to the device.

The digital supply circuit has an internal overvoltage clamp to protect the BUK3F00-50WDxx from overvoltage transients and is also protected against ESD.

9.1.6 Reference supplies: pins IREFCURR and IREFTEMP

An internal band gap reference is used to ensure stable voltage and current references:

- Measured current reference pin IREFCURR: The full-scale analog output measurement current and the full-scale measurement current through the ADC are both set by connecting an external resistor between pins IREFCURR and GND.
- Temperature reference pin IREFTEMP: The forward current for the temperature sensing diodes in the TrenchPLUS FETs is set by connecting an external resistor between pins IREFTEMP and GND.

9.2 Charge pump

The controller has an internal charge pump circuit to supply the gate voltage required to operate the high-side FET switches. The charge pump uses an internal oscillator and internal switches with external pump and storage capacitors.

9.2.1 Charge pump supply: pins $V_{BAT(CP)}$ and GND(CP)

Pins $V_{BAT(CP)}$ and GND(CP) supply power to the internal charge pump. This is derived from the V_{BAT} supply either via an internal resistor between pins V_{BAT} and $V_{BAT(CP)}$ or by linking these pins externally. Pin GND(CP) should be connected to pin GND; the grounds are not internally connected to ensure any charge pump noise does not affect the measurement circuit. The connections should be decoupled close to the device.

The charge pump supply circuit has an internal overvoltage clamp to protect the BUK3F00-50WDxx from overvoltage transients and is also protected against ESD.

If connected to a reverse polarity battery voltage, the charge pump supply is protected by the internal resistor connection to V_{BAT}.

9.2.2 Charge pump boost mode

To ensure fast start-up, the charge pump has a boost mode that operates for a set time. This mode is triggered at power-on reset and when the charge pump voltage falls below the charge pump fault threshold or the battery voltage stays below the undervoltage threshold. If the charge pump voltage is below the fault threshold after the charge pump boost is completed, then no further boost is possible until the charge pump fault is cleared.

9.3 Control logic

The control logic is responsible for switching the individual FET channels on and off, depending on user settings and the implementation of protection methods. It contains registers used for storing the user settings for channel configurations, current reference and measurement, diagnostic and watchdog modes. Communication with a controller is via the SPI-bus.

The digital block is designed to support 8 channels; unused channels should be programmed off at all times.

9.3.1 Digital control

The device is enabled by pin EN. When pin EN is LOW, the device is in Standby mode and all FETs are held off by an active switch with a standby resistance between pins GATE and KELVIN. When pin EN is HIGH, the device is enabled for normal operation. Pin EN can be used as the reset signal by a controller for the control logic. When pin EN is reset to HIGH, the device goes through a power-on reset, registers are loaded with their default values and channels are switched on or off according to the mapping for the individual device type.

Digital control consists of a number of registers that control the functions. The default value is loaded during power-on reset and, if the WRITE_PROTECT option is enabled, for defined registers, when the SPI watchdog times out. For some registers the default setting can be programmed by metal mask options.

Table 5. User-accessible registers

Register[1]	Name	Description	Mask option	Version default value[2]		
				FE	FM	FY
Read/write registers[3]						
01h	CHAN_ONOFF	channels select: on/off	N	00h	00h	00h
02h	IN02_MAP	direct input pins IN0 and IN2 mapping	Y[4]	21h	10h	1Ch
03h	IN13_MAP	direct input pins IN1 and IN3 mapping	Y[4]	84h	40h	01h
04h	INP_MAP	PWM input pin INP mapping	Y[4]	10h	08h	00h
05h	ANDOR_MAP	direct input pin AND/OR operation	Y[4]	00h	00h	00h
06h	CURR_MEAS	channel select analog current measurement	N	00h	00h	00h
07h	SEL_CURR_TRIP_CHAN	select current tripping channel	Y[4]	00h	00h	00h
08h	CHAN_OT_FAULT_CLR	channel set overtemperature fault clear	Y[4]	00h	00h	00h
09h	PWM_SYNC	channel PWM synchronization	N	00h	00h	00h
0Ah	PWM_SAM_BEGINEND	channel PWM sample point begin or end	N	FFh	FFh	FFh
0Ch	CHAN_WD_MAP	select channel watchdog behavior	Y[4]	21h	58h	1Dh
0Dh	WD_TO	watchdog time-out period setting	Y[4]	3Fh	3Fh	3Fh
0Eh	CTRL_SET	controller settings	Y[4]	08h	08h	08h
0Fh	INT_PWM_FREQ	internal PWM frequency setting	Y[4]	B6h	BBh	B1h
10h	PWM_DC_CH0	internal PWM duty cycle setting for channel 0	Y[4][5]	FFh	FFh	FFh
11h	PWM_DC_CH1	internal PWM duty cycle setting for channel 1	Y[4][5]	FFh	FFh	FFh
12h	PWM_DC_CH2	internal PWM duty cycle setting for channel 2	Y[4][5]	FFh	FFh	FFh
13h	PWM_DC_CH3	internal PWM duty cycle setting for channel 3	Y[4][5]	FFh	FFh	FFh
14h	PWM_DC_CH4	internal PWM duty cycle setting for channel 4	Y[4][5]	FFh	FFh	FFh
15h	PWM_DC_CH5	internal PWM duty cycle setting for channel 5	Y[4][5]	FFh	FFh	FFh
16h	PWM_DC_CH6	internal PWM duty cycle setting for channel 6	Y[4][5]	FFh	FFh	FFh
17h	PWM_DC_CH7	internal PWM duty cycle setting for channel 7	Y[4][5]	FFh	FFh	FFh
18h	OT_TRIPLEV_CH30	overtemperature trip level channels 3 to 0	Y[4]	AAh	AAh	AAh
19h	OT_TRIPLEV_CH74	overtemperature trip level channels 7 to 4	Y[4]	AAh	AAh	AAh
1Ah	IFSC_CH30	full-scale reference current channels 3 to 0	Y[4]	AAh	FFh	FFh
1Bh	IFSC_CH74	full-scale reference current channels 7 to 4	Y[4]	AAh	FFh	FFh
1Ch	CURR_TRIPLEV_CH0	current trip level for channel 0	N[4]	FFh	FFh	FFh
1Dh	CURR_TRIPLEV_CH1	current trip level for channel 1	N[4]	FFh	FFh	FFh
1Eh	CURR_TRIPLEV_CH2	current trip level for channel 2	N[4]	FFh	FFh	FFh
1Fh	CURR_TRIPLEV_CH3	current trip level for channel 3	N[4]	FFh	FFh	FFh
20h	CURR_TRIPLEV_CH4	current trip level for channel 4	N[4]	FFh	FFh	FFh
21h	CURR_TRIPLEV_CH5	current trip level for channel 5	N[4]	FFh	FFh	FFh
22h	CURR_TRIPLEV_CH6	current trip level for channel 6	N[4]	FFh	FFh	FFh
23h	CURR_TRIPLEV_CH7	current trip level for channel 7	N[4]	FFh	FFh	FFh
24h	IRQ_MAP	interrupt request mapping	Y[4]	04h	19h	00h
25h	CURR_TRIP_BLANKTIME	current trip blanking time	Y[4]	2Fh	2Fh	2Fh
26h	OLDET_ONOFF	off-state open-circuit detection	N	FFh	FFh	FFh

Table 5. User-accessible registers *…continued*

Register[1]	Name	Description	Mask option	Version default value[2]		
				FE	FM	FY
27h	READBACK	register and diagnostic read back	N	30h	30h	30h
28h	IRQ_CHAN_MAP	interrupt generating channels	N[4]	FFh	FFh	FFh
Write-only registers[6]						
29h	CLEAR_CHAN_INTN	clear channels and interrupt				
2Ah	CLEAR_WD	clear watchdog state				
Read-only registers[7]						
30h	DIAG_BASIC	basic diagnostics				
31h	DIAG_CTRL	controller diagnostics				
32h	ISR	interrupt status register				
33h	VERSION	device version number				
34h	DIAG_CHAN_01	VOUTHIGH and VOUTLOW states[8]				
35h	DIAG_CHAN_02	TSNSOPEN signal state[9]				
38h	DIAG_DETAIL_CH0	detail diagnostics; channel 0				
39h	DIAG_DETAIL_CH1	detail diagnostics; channel 1				
3Ah	DIAG_DETAIL_CH2	detail diagnostics; channel 2				
3Bh	DIAG_DETAIL_CH3	detail diagnostics; channel 3				
3Ch	DIAG_DETAIL_CH4	detail diagnostics; channel 4				
3Dh	DIAG_DETAIL_CH5	detail diagnostics; channel 5				
3Eh	DIAG_DETAIL_CH6	detail diagnostics; channel 6				
3Fh	DIAG_DETAIL_CH7	detail diagnostics; channel 7				

[1] This column denotes either the address used to write to the indicated register, or the data sent to register READBACK (27h) to read back from the indicated register.

[2] Default values for read/write registers are either fixed or programmable as mask options for individual types.

[3] 8-bit read/write registers store settings that control the behavior of the device. Default values are stored at power-on reset and data can be changed via SPI-bus communication. To help provide security of operation these registers can also be read back.

[4] Another metal mask option is available, which means that WRITE_PROTECT is set. CHAN_WD_MAP and WD_TO registers are write-protected by this option. The other registers indicated will be reloaded with default values if an SPI watchdog time-out occurs.

[5] Only bit 7 is mask programmable.

[6] 8-bit write-only registers clear tripped channels, interrupt and watchdog states when data is written. The values are not stored and cannot be read back.

[7] 16-bit read-only registers contain data about the state of the device for diagnostic use. Data cannot be written to these registers.

[8] VOUTHIGH: high-side FET is in on-state for overcurrent protection ($> V_{th(on)(bat-KEL)}$).
VOUTLOW: high-side FET output voltage is below the voltage required for open-circuit detection ($< V_{det(oc)off}$).

[9] TSNSOPEN: temperature sensor open-circuit.

9.3.2 Serial Peripheral Interface (SPI)

The SPI is used for communication with a controller and provides control and diagnostic functions. The device is configured as an SPI slave.

The interface consists of SPI Chip Select (SCSN), Serial Clock (SCLK), Serial Data In (SDI) and Serial Data Out (SDO). SPI communication is enabled when SCSN is set LOW. Data is shifted out to pin SDO on the SCLK rising edge. The data shifted out depends on which register is addressed by register READBACK (27h). Data is shifted in from pin SDI on the SCLK falling edge.

The controller can be timed to send data to SDI on the SCLK rising edge with data valid on the falling edge. Data is valid for reading on the falling edge. For full timing requirements; see Table 25 “Recommended operating conditions” and Figure 9 “SPI timing definitions”.

SPI communication uses 16-bit words; see Figure 3. The most significant byte, the register address byte, is transferred first. The 2 most significant bits of the register address byte are not used, they must always be logic 0. The 6 least significant bits form the actual register address.

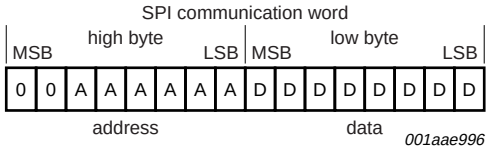


Fig 3. SPI communication format; full 16-bit operation

When SCSN is set HIGH after a 16-bit valid communication, then the SDO output becomes inactive and goes to high-impedance. The data in the low byte is then transferred to the address given in the high byte. After this is completed the SPI shift register is refreshed with the latest contents of the register addressed by the entry in register READBACK. When 8-bit registers are read, the least significant byte is padded with 55h.

Data is checked for validity after SCSN goes HIGH. It is valid if the count of SCLK negative edges is a multiple of 8 and the address part (high byte) of the 16-bit message contains a valid address. An invalid address will result in a value of 00h being sent on SDO. To allow time for validity checking, writing data and refreshing the shift register, SCSN must be disabled (HIGH) for a period $t_{w(SCSN)}$.

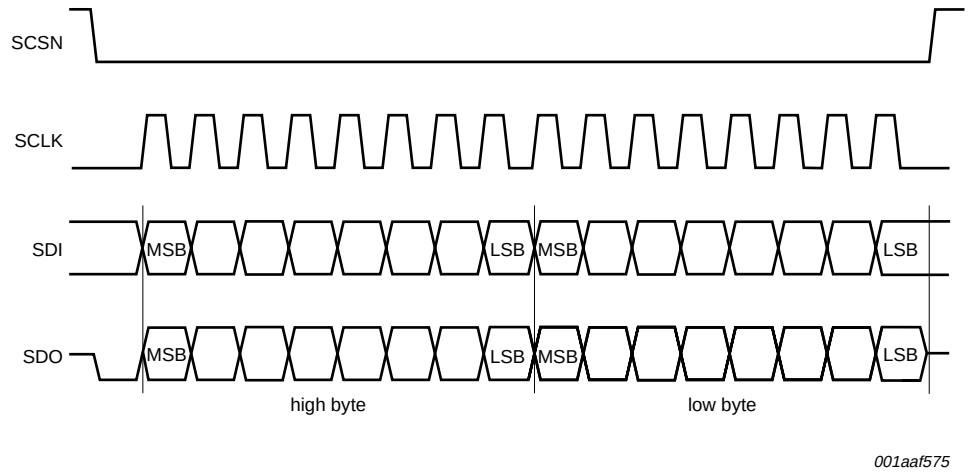


Fig 4. SPI communication frame: full 16-bit operation

To support 8-bit microcontrollers an 8-bit operation is possible; see Figure 5. In this operation, SCSN is taken HIGH between the 8-bit bytes. SDO is taken HIGH before the SCLK of the low byte to indicate that the low byte is to be sent.

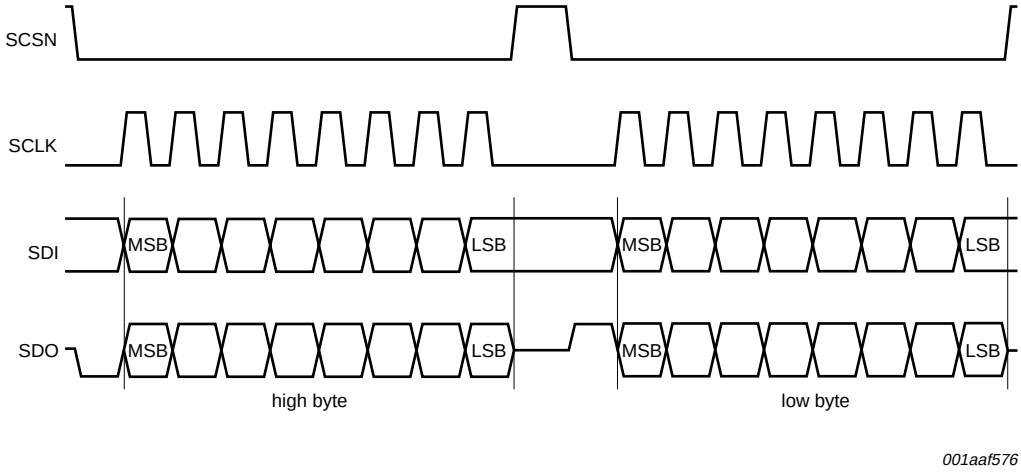


Fig 5. SPI communication frame: 8-bit operation

A number of devices can be daisy chained by connecting the SDO of the first device to the SDI of the next device and so on; see Figure 6.

All devices have their SCSN inputs connected to the same controller chip select so that they can be selected together. When n devices are daisy chained, then n SPI 16-bit word cycles must be executed to program all devices. Daisy chaining cannot be used with 8-bit SPI operation.

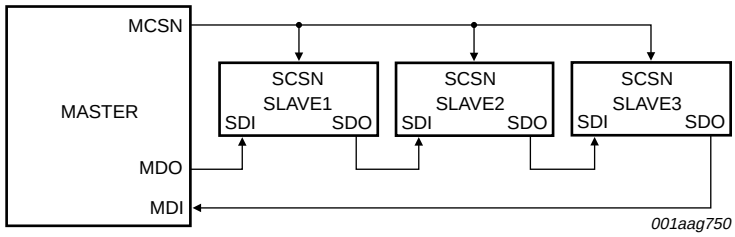


Fig 6. Daisy chain connection of three ASICs (requires three SPI 16-bit word cycles)

9.3.3 SPI watchdog

The SPI watchdog detects if there is a breakdown in the SPI communication with the controller. A timer is activated that resets when a valid communication is received. If no valid SPI communications are received within the specified time-out period, the watchdog will signal this to the control logic.

The SPI watchdog is enabled either by setting pin WDEN = HIGH or by enabling watchdog active with bit WD_TO[5]. FET channels can be turned either on or off when a watchdog time-out occurs as set by register CHAN_WD_MAP. Pin WDTON is set LOW for a selectable period when a watchdog time-out occurs and can be used as a reset for the controller. An interrupt on pin INTN can also be set when a watchdog time-out occurs.

Other functions of the device are not changed in Watchdog mode. In particular, if the SPI fault that caused the condition is resolved, SPI communication would work and diagnostics could be performed.

See Section 11.1 “Reset for interrupt and SPI watchdog” for details of clearing watchdog states.

Table 6. Select channel watchdog behavior register (address 0Ch) bit description

Address	Register	Bit	Description
0Ch	CHAN_WD_MAP[1]	7 to 0	behavior when watchdog time-out occurs in individual channels 7 to 0: 1 = turn selected channel on[2] 0 = turn selected channel off

[1] A metal mask option WRITE_PROTECT is available, which means that registers are write protected.

[2] Provided channel is not mapped to a direct input pin. If channel is mapped to a direct input pin, then the channel will only turn on if the direct input pin is HIGH.

Table 7. Watchdog time-out period setting register (address 0Dh) bit description

Address	Register	Bit	Description
0Dh	WD_TO	7 to 6	not used
		5	enable watchdog
		4 to 0	watchdog time-out period; see Table 8

Table 8. Watchdog time-out period

Given times are valid for nominal master clock frequency.

Time-out period							
Value	**Time**	**Value**	**Time**	**Value**	**Time**	**Value**	**Time**
00h	1.0 ms	08h	4.1 ms	10h	16 ms	18h	66 ms
01h	1.3 ms	09h	5.1 ms	11h	20 ms	19h	82 ms
02h	1.5 ms	0Ah	6.1 ms	12h	25 ms	1Ah	98 ms
03h	1.8 ms	0Bh	7.2 ms	13h	29 ms	1Bh	115 ms
04h	2.0 ms	0Ch	8.2 ms	14h	33 ms	1Ch	131 ms
05h	2.6 ms	0Dh	10 ms	15h	41 ms	1Dh	164 ms
06h	3.1 ms	0Eh	12 ms	16h	49 ms	1Eh	197 ms
07h	3.6 ms	0Fh	14 ms	17h	57 ms	1Fh	229 ms

9.3.4 Pulse-Width Modulation (PWM)

PWM can be implemented on selected channels by either an internally generated signal or an externally connected signal.

For the internally generated signal, it is possible to select frequency and duty cycle and to synchronize the selected channels. The internally generated signal is used when the duty cycle is set to less than 100 %. For both internal and external PWM signals it is possible to specify the point at which the FET current is sampled in the PWM period.

An external PWM signal can be connected to the input pin INP (intended for normal PWM operation) or pins IN0 to IN3 (intended for fail-safe operation). The required channels are then mapped accordingly.

Table 9. PWM setting registers (addresses 09h, 0Ah, 0Fh, 10h to 17h) bit description

Address	Register	Bit	Description
09h	PWM_SYNC[1]	7 to 0	PWM synchronization in individual channels 7 to 0: 1 = selected channel synchronized to previous channel in this mode 0 = selected channel one eighth of internal PWM cycle out of phase
0Ah	PWM_SAM_BEGINEND	7 to 0	PWM sample begin or end in individual channels 7 to 0[2]: 1 = selected channel set to end 0 = selected channel set to start
0Fh	INT_PWM_FREQ[3]	7 to 0	internal PWM frequency setting for all channels: 00h to 3Fh: f = {code + 01h} × 0.125 Hz, from 0.125 Hz to 8.0 Hz in 0.125 Hz steps 40h to 7Fh: f = {code – 3Fh} × 0.5 Hz, from 0.5 Hz to 32.0 Hz, in 0.5 Hz steps 80h to BFh: f = {code – 7Fh} × 2.0 Hz, from 2.0 Hz to 128.0 Hz, in 2.0 Hz steps C0h to FFh: f = {code – BFh} × 8.0 Hz, from 8.0 Hz to 512.0 Hz, in 8.0 Hz steps
10h to 17h	PWM_DC_CHn[3]	7 to 0	internal PWM duty cycle for specified channel 7 to 0; duty cycle δ = (n + 1) / 256, where n = decimal number set in register

[1] If channels are run out-of-phase each will be staggered by one eighth of a PWM cycle. When more than one channel is selected by this command then the master signal is the channel with the lowest number. This does not apply to the external PWM signal on pin INP.

[2] Controls the point of the on-time at which the current is sampled for digital current measurement. Only operates when duty cycle is set to < 100 % or channel is mapped to pin INP.

[3] A metal mask option WRITE_PROTECT is available which means that this register is reloaded with the default value if an SPI watchdog time-out occurs.

The PWM frequency can be monitored by making this an output on pin PWMMON. This is a controller setting; see Section 9.5.5 “Controller settings”.

9.3.5 Interrupt

An interrupt can be generated to notify a controller of an error condition. An interrupt will set pin INTN = LOW. Register settings define which faults can generate an interrupt and which FET channels can generate an interrupt for these faults.

Table 10. Interrupt setting registers (addresses 24h, 28h) bit description

Address	Register	Bit	Description
24h	IRQ_MAP[1]		interrupt request mapping; for each bit: 1 = INTN active 0 = INTN not active
		7	invalid SPI communication
		6	open-circuit
		5	controller fault (charge pump fault or V_{BAT} low)
		4	temperature sensor diode open-circuit
		3	watchdog time-out
		2	channel overcurrent (threshold reached or exceeded)
		1	channel overtemperature (threshold exceeded)
		0	channel tripped under fault condition
28h	IRQ_CHAN_MAP[1]	7 to 0	interrupt generation in individual channels 7 to 0: 1 = selected channel can generate interrupt 0 = selected channel cannot generate interrupt

[1] A metal mask option WRITE_PROTECT is available, which means that this register is reloaded with the default value if an SPI watchdog time-out occurs.

When an interrupt is generated, data in the interrupt status register will indicate the cause. See Section 11.1 “Reset for interrupt and SPI watchdog” for details of reading and clearing interrupt data.

9.4 Current measurement

The current measurement is able to monitor the current from the sense connections of the TrenchPLUS FETs. This is achieved by using one current measurement circuit for each channel. The current measurement circuits control conditions at the sense pin of each FET channel and can produce either an analog or digital measurement output. The digital output can be read by a controller.

The current measurement circuit monitors the sense current according to the sense ratio of the TrenchPLUS FET. This ratio is only valid when the sense and main FETs of the TrenchPLUS device are fully active with V_{GS} at about 4 V or greater, and with the same V_{GS}.

9.4.1 Current measurement circuits

For FET channels configured as high-side switches, the sense current is pulled from the sense connection. This current is adjusted until the voltage measured at the FET pin kelvin is the same as that measured at the FET pin sense. Since the main and sense

devices have common drain connections, the V_{DS} of the two devices are equal, and the correct sense current is being pulled. Current measurement is only possible when the voltage on pin KELVIN is above the $V_{th(on)(bat-KEL)}$ threshold.

9.4.2 Analog current measurement output

An analog current can be output on pin IMEAS that is proportional to the sense current measured on a selected FET channel. Any single channel can be multiplexed to this output at a time.

The accuracy and resolution of analog current measurement is determined by the voltage across the R_{IMEAS} resistor with the measurement output current and the measurement range used. The measurement current is given by $I_{meas} = (I_{SENSE} / I_{meas(ADC)(fs)}) \times 100\ \mu A$, where I_{SENSE} is the FET sense current and $I_{meas(ADC)(fs)}$ is the set full-scale current for the measurement range. For reliable current measurement, the voltage on pin IMEAS must be less than the measurement supply voltage on pin $V_{CC(MEASC)}$. A resistor value giving high resolution at low measurement output current (for example, up to $I_{meas(ADC)(fs)}$) may not provide the range for high measurement output current (for example, up to $8 \times I_{meas(ADC)(fs)}$). Conversely, a value giving the range for high measurement current will give less resolution for low measurement current.

When the selected channel uses PWM, the analog measurement is able to follow the switched waveform, except when the duty cycle is very low, and high-side FETs are in the turn-on state. The voltage on pin IMEAS is limited just below the measurement supply voltage.

Table 11. Analog current channel selection register (address 06h) bit description

Address	Register	Bit	Description
06h	CURR_MEAS	7 to 4	not used; must be set to logic 0
		3	current measurement setting: 1 = enables current measurement in selected channel 0 = disables current measurement in all channels
		2 to 0	selects measurement channel; binary value corresponds to channel number (0 to 7)

9.4.3 Digital current measurement output

8-bit successive approximation ADCs are used to measure the sense currents of the FET channels. The measured values are only considered valid when the FET has been on for the full conversion cycle. Digital measurements are stored and can be read by a controller. The reading from the ADC may not indicate zero if the channel is requested off. If PWM is not selected, the values are stored every ADC cycle. For PWM the digital measurement can be sampled at the start or end of the on time.

The ADC reading, up to the maximum 255 bits, is given by:
reading = $255 \times (I_{SENSE} / I_{meas(ADC)(fs)}) \times (50\ \mu A / I_{IREFCURR})$, where $I_{IREFCURR}$ is the current through the current reference resistor ($R_{IREFCURR}$). At $I_{IREFCURR} = 50\ \mu A$ this equation simplifies to give a direct relationship with the analog measurement current.

9.4.4 Low battery supply voltage conditions

The current measurement interface operates at voltages very near the battery voltage. To permit reasonable headroom in the circuit, the current measurement interface is powered from the charge pump. The circuit cannot operate correctly when it is close to ground, as

occurs in very low battery conditions. The current measurement interface may be non-functional, or may have degraded accuracy under low (out-of-specification) charge pump conditions.

9.5 TrenchPLUS FET interface

The FET interface provides channel switching (on and off) and protection with the following features, described in priority order.

9.5.1 Overtemperature protection

Overtemperature protection is adjusted by selecting the trip level of the temperature sense diode for each channel. To relate this to actual trip temperature, refer to the specification of the specific TrenchPLUS FET devices. Overtemperature protection can also be set to auto-reset with hysteresis (to reduce the possibility of repeated resets when the temperature remains high) or to latch on fault. The device also detects and reports a fault if the connection to a temperature sense diode is open-circuit.

Table 12. Overtemperature protection setting registers (addresses 08h, 18h, 19h) bit description

Address	Register	Bit	Description
08h	CHAN_OT_FAULT_CLR[1]	7 to 0	overtemperature fault clear in channels 3 to 0: 1 = selected channel set to auto reset with hysteresis 0 = selected channel set to latches on fault
18h	OT_TRIPLEV_CH30[1]		set overtemperature trip level in channels 3 to 0 to one of four voltage trip levels[2]: 00 = 2.31 V 01 = 2.25 V 10 = 2.16 V 11 = 2.00 V
		7, 6	channel 3 temperature sense diode threshold voltage
		5, 4	channel 2 temperature sense diode threshold voltage
		3, 2	channel 1 temperature sense diode threshold voltage
		1, 0	channel 0 temperature sense diode threshold voltage
19h	OT_TRIPLEV_CH74[1]		set overtemperature trip level in channels 7 to 4 to one of four voltage trip levels[2]: 00 = 2.31 V 01 = 2.25 V 10 = 2.16 V 11 = 2.00 V
		7, 6	channel 7 temperature sense diode threshold voltage
		5, 4	channel 6 temperature sense diode threshold voltage
		3, 2	channel 5 temperature sense diode threshold voltage
		1, 0	channel 4 temperature sense diode threshold voltage

[1] A metal mask option WRITE_PROTECT is available which means that this register is reloaded with the default value if an SPI watchdog time-out occurs.

[2] Nominal trip voltages quoted for each trip level. Refer to data sheet for TrenchPLUS FET devices for equivalent temperature measurement.

9.5.2 Overcurrent protection

The overcurrent protection on each channel allows for high inrush currents. This protection also allows for turn-on or transient low battery conditions that can occur with the configuration of high-side FET switches. Delay time in operating overcurrent protection is determined by the actual FET.

For high-side switches, FET turn-on is determined when the sense voltage exceeds the sense low threshold voltage ($V_{th(sense)low}$), within 40 µs (nominal), and when the battery-to-kelvin voltage exceeds the on-state threshold voltage between the battery and pin KELVIN ($V_{th(on)(bat-KEL)}$).

The following overcurrent protection is available:

Turn-on overcurrent trip (TONOCH) — For channels configured as high-side switches. Operates during FET turn-on or transient low battery conditions. The threshold level is a set multiple of $I_{meas(ADC)(fs)} \times (I_{IREFCURR} / 50\ \mu A)$. This is simplified when $I_{IREFCURR}$ = 50 µA. For low current sense voltage (< 2.5 V) the trip level is below the specified multiple of $I_{meas(ADC)(fs)}$. This protection cannot be disabled.

Overcurrent high trip (OCH) — For channels configured as high-side switches. This does not operate during FET turn-on or transient low battery conditions. The threshold level is a set multiple of $I_{meas(ADC)(fs)} \times (I_{IREFCURR} / 50\ \mu A)$. This is simplified when $I_{IREFCURR}$ = 50 µA. This protection cannot be disabled or delayed.

Overcurrent low trip (OCL) — Operates at set currents of the ADC output up to $I_{meas(ADC)(fs)}$ with the ADC measurement accuracy. The threshold level is set by register CURR_TRIPLEV_CHn. This protection can be disabled or delayed.

Table 13. FET channel protection setting registers (addresses 07h, 1Ah to 23h, 25h) bit description

Address	Register	Bit	Description
07h	SEL_CURR_TRIP_CHAN[1]	7 to 0	select current tripping for OCL in individual channels 7 to 0: 1 = selected 0 = not selected
1Ah	IFSC_CH30[1]		set $I_{meas(ADC)(fs)}$ data bits in channels 3 to 0 to one of four current trip levels: 00 = 0.5 mA 01 = 1.0 mA 10 = 1.5 mA 11 = 2.0 mA
		7, 6	set channel 3 full-scale current bits 1 and 0
		5, 4	set channel 2 full-scale current bits 1 and 0
		3, 2	set channel 1 full-scale current bits 1 and 0
		1, 0	set channel 0 full-scale current bits 1 and 0

Table 13. FET channel protection setting registers (addresses 07h, 1Ah to 23h, 25h) bit description *…continued*

Address	Register	Bit	Description
1Bh	IFSC_CH74[1]		set $I_{meas(ADC)(fs)}$ data bits in channels 7 to 4 to one of four current trip levels: 00 = 0.5 mA 01 = 1.0 mA 10 = 1.5 mA 11 = 2.0 mA
		7, 6	set channel 7 full-scale current bits 1 and 0
		5, 4	set channel 6 full-scale current bits 1 and 0
		3, 2	set channel 5 full-scale current bits 1 and 0
		1, 0	set channel 4 full-scale current bits 1 and 0
1Ch to 23h	CURR_TRIPLEV_CHn[1]	7 to 0	overcurrent trip threshold in channels 7 to 0; each bit represents $I_{meas(ADC)(fs)}$ / 255
25h	CURR_TRIP_BLANKTIME	7, 6	not used: must be set to logic 0
		5 to 0	set overcurrent trip blanking time; see Table 14

[1] A metal mask option WRITE_PROTECT is available, which means that this register is reloaded with the default value if an SPI watchdog time-out occurs.

Table 14. Overcurrent low trip blanking time

Blanking							
Value	**Time**	**Value**	**Time**	**Value**	**Time**	**Value**	**Time**
00h	0 ms	0Ch	0.51 ms	18h	4.1 ms	24h	33 ms
01h	0.08 ms	0Dh	0.64 ms	19h	5.1 ms	25h	41 ms
02h	0.10 ms	0Eh	0.77 ms	1Ah	6.1 ms	26h	49 ms
03h	0.11 ms	0Fh	0.90 ms	1Bh	7.2 ms	27h	57 ms
04h	0.13 ms	10h	1.0 ms	1Ch	8.2 ms	28h	66 ms
05h	0.16 ms	11h	1.3 ms	1Dh	10 ms	29h	82 ms
06h	0.19 ms	12h	1.5 ms	1Eh	12 ms	2Ah	98 ms
07h	0.22 ms	13h	1.8 ms	1Fh	14 ms	2Bh	115 ms
08h	0.26 ms	14h	2.0 ms	20h	16 ms	2Ch	131 ms
09h	0.32 ms	15h	2.6 ms	21h	20 ms	2Dh	164 ms
0Ah	0.38 ms	16h	3.1 ms	22h	25 ms	2Eh	197 ms
0Bh	0.45 ms	17h	3.6 ms	23h	29 ms	2Fh	229 ms

9.5.3 Gate inductive ring-off clamp

For high-side switches an inductive ring-off clamp can provide gate-source voltage to allow conduction through the FET. This protects the FET by reducing the possibility of high drain-source voltages when turning off current to an inductive load. The gate is initially set to the source voltage to turn the FET off. During turn-off an inductive load will force the source voltage negative and the gate will follow this until the voltage between gate and ground reaches the inductive ring-off clamp voltage V_{CL}. As the source voltage continues negative, the gate-to-source voltage will increase, turning the FET on and allowing conduction through the FET and preventing excessive voltage between drain and source.

The negative voltage on the source then forces current in the inductive load to reduce rapidly to zero. As the source voltage returns to ground, the gate-source voltage becomes zero and the FET is turned off.

9.5.4 Loss-of-ground protection

A loss-of-ground condition can occur if the ground connection for the circuit is disconnected with the load ground still connected. With the FET off, it is possible for the ground voltage to drift up to battery voltage with the FET source voltage still held at ground. A resistance between pins GATE and KELVIN will hold the FET off provided the inductive ring-off clamp voltage V_{CL} between gate and ground is not exceeded, otherwise the FET will start to turn on. Hence, loss of ground protection can only be guaranteed when $V_{BAT} < |V_{CL}|$.

9.5.5 Controller settings

It is possible to select a low switching rate for high-side switches at the beginning of turn-on and at the end of turn-off. This switching option improves EMC in the high-side switching application.

The PWM frequency can be monitored on pin PWMMON. This output has a 50 % duty cycle.

Table 15. Controller settings register (address 0Eh) bit description

Address	Register	Bit	Description
0Eh	CTRL_SET[1]	7 to 4	not applicable; set to logic 0
		3	sets switching rate at start of turn-on and end of turn-off: 1 = low switching rate 0 = high switching rate
		2	PWM signal on pin PWMMON: 1 = available 0 = not available[2]
		1 to 0	not used; must be set to logic 0

[1] A metal mask option WRITE_PROTECT is available which means that this register is reloaded with the default value if an SPI watchdog time-out occurs.

[2] When signal not available, this pin goes to 0 V.

9.5.6 Open-circuit detection

Open-circuit is normally detected when switches are in the on-state. The ADC checks that at least a minimal current is flowing through the sense circuit. The threshold level is determined by the setting DIG_OLTH[3:0] and is a mask option.

For high-side switches it is possible to detect an open-circuit in the off-state. The FET kelvin source voltage is monitored with a current $I_{det(oc)off}$ and an open-circuit is reported if the threshold voltage $V_{det(oc)off}$ is exceeded after a nominal 192 µs delay. This off-state open-circuit detection is independent of on-state open-circuit detection. For high-side switches in the off-state, it is also possible to detect when the voltage between pin KELVIN and V_{BAT} is less than $V_{th(on)(bat-KEL)}$ (a short-circuit).

Table 16. Off-state open-circuit detection register (address 26h) bit description

Address	Register	Bit	Description
26h	OLDET_ONOFF	7 to 0	off-state open-circuit detection[1] in individual channels 7 to 0: 1 = off-state open-circuit detection enabled in selected channel 0 = off-state open-circuit detection disabled in selected channel

[1] For high-side switches only.

9.5.7 Channel selection

Channel selection allows the FET channels to be switched on directly.

Table 17. Channel selection register (address 01h) bit description

Address	Register	Bit	Description
01h	CHAN_ONOFF	7 to 0	direct switch-on of individual channels 7 to 0: 1 = selected channel on 0 = selected channel off

9.5.8 Mapping channels for direct channel control and PWM

Channels can be mapped to the input pin INP (intended for an external PWM signal) or to pins IN0 to IN3 for direct control (intended for fail-safe channel control by connection to $V_{CC(LOG)EXT}$ and GND, or an external PWM signal). All channels (0 to 7) can be mapped to pin INP. Channels 0 to 3 can be mapped to pins IN0 and IN1. Channels 4 to 7 can be mapped to pins IN2 and IN3. Input pins IN0 plus IN1 and IN2 plus IN3 are combined according to the AND/OR operation. If a channel is switched on (by register CHAN_ONOFF), the channel is switched on irrespective of the state on the direct input pins IN0 to IN3; see Section 9.5.7.

Table 18. Channel selection and pin mapping register (addresses 02h to 05h) bit description

Address	Register	Bit	Description
02h	IN02_MAP[1][2]		direct input pins IN0 and IN2 mapping: 1 = mapped 0 = not mapped
		7 to 4	map individual channels 7 to 4 to pin IN2
		3 to 0	map individual channels 3 to 0 to pin IN0
03h	IN13_MAP[1][2]		direct input pins IN1 and IN3 mapping: 1 = mapped 0 = not mapped
		7 to 4	map individual channels 7 to 4 to pin IN3
		3 to 0	map individual channels 3 to 0 to pin IN1
04h	INP_MAP[2]	7 to 0	direct input pin INP map channels 7 to 0: 1 = mapped 0 = not mapped

Table 18. Channel selection and pin mapping register (addresses 02h to 05h) bit description *…continued*

Address	Register	Bit	Description
05h	ANDOR_MAP[1]		direct input pin AND/OR operation
		7 to 4	direct input AND/OR operation for individual channels 7 to 4: 1 = pin IN2 AND pin IN3 0 = pin IN2 OR pin IN3
		3 to 0	direct input AND/OR operation for individual channels 3 to 0: 1 = pin IN0 AND pin IN1 0 = pin IN0 OR pin IN1

[1] A metal mask option WRITE_PROTECT is available, which means that these registers are reloaded with the default value if an SPI watchdog time-out occurs.

[2] In Watchdog mode; pins IN0 to IN3 reset channel faults (such as short-circuit) when the pin is set to LOW; Pin INP does not reset channel faults. Hence, it is not recommended that an external PWM signal is connected to pins IN0 to IN3 for normal operation.

9.5.9 FET channel on/off control

Each FET channel can be switched by a request from different sources, the logical relationship between these sources is shown in Figure 7.

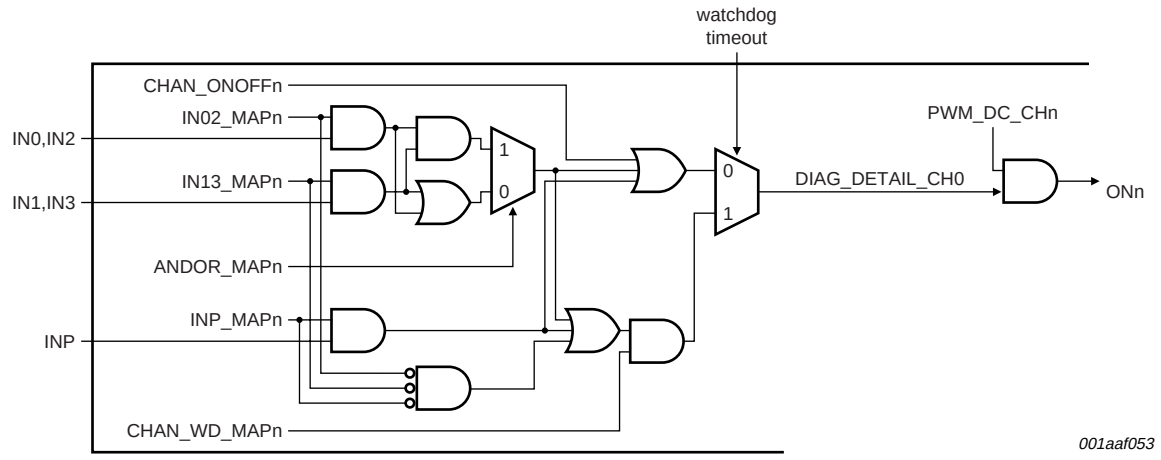


Fig 7. FET channel on/off request logic

9.5.10 Power dissipation

The FET interface comprises a significant part of the BUK3F00-50WD thermal budget. The dissipation is caused by the regulation of the SENSE pin voltage while sinking the sense current. The dissipation, per channel, can be estimated from the product of I_{SENSE} and V_{BAT}. Special care should be taken at high battery voltages that the power dissipation does not cause the device to overheat.

9.5.11 Trip and retry

This automatically handles short duration OCH, TONOCH and OCL faults. However, switching into a short-circuit imposes considerable stress on the MOSFET and may reduce its life. The user must ensure that the effects are fully evaluated before implementation. If there is any doubt, then trip and retry should not be used.

If trip and retry is used and a channel still trips off, then the channel should not be turned on again before the fault has been removed. This may require a lock-out feature in the controlling software.

The settings for trip and retry are given in Table 19 “Protected settings”.

9.5.12 Trip-latch

The faults listed will trip-latch a channel: this will not allow the channel to turn on unless the latch is cleared.

Overtemperature — with auto-reset turned off.

Analog overcurrent — with no retries allowed.

Turn-on overcurrent HIGH — (high-side switches only) with no retries allowed.

Overcurrent LOW — with no retries allowed and OCL tripping enabled.

To clear a channel trip-latch condition; see Section 11.1 “Reset for interrupt and SPI watchdog”.

10. Fixed functional settings

A number of settings are fixed mask options. These settings do not have a register address and cannot be read or changed by the user.

Table 19. Protected settings

Name	Bit	Description	Version setting values		
			FE	FM	FY
DIG_OLTH		open-circuit threshold level; 8-bit register	23h	23h	23h
	7 to 4	not applicable			
	3 to 0	high side: (0000) b3, b2, b1, b0			
DIG_FET		channel tripping behavior and filter times	0C1h	0C1h	0C1h
	8, 7	$t_{low(bat)}$ setting: 00/11 = 128 µs (min) to 144 µs (max) 01 = 256 µs (min) to 288 µs (max) 10 = 512 µs (min) to 576 µs (max)			
	6, 5	$t_{high(bat)}$ setting: 00/11 = 16 µs (min) to 20 µs (max) 01 = 32 µs (min) to 40 µs (max) 10 = 64 µs (min) to 80 µs (max)			
	4	high-side channels on low V_{BAT}: 1 = no trip 0 = trip			
	3, 2	trip channel output filter time: 00 = immediate			
	1, 0	TONOCH filter time (in turn-on state): 00 = immediate 01 = 1.0 µs 10 = 1.5 µs 11 = 2.0 µs (min) to 3.0 µs (max)			
CHAN_ALLOW_RETRY	7 to 0	allow trip and retry after OCH, TONOCH or OCL faults select channels 7 to 0: 1 = allowed 0 = not allowed	FFh	FFh	FFh
RETRY_SETTINGS		trip retry delay and number of retries	1Bh	1Bh	1Bh
	4, 3	wait time before retry: 00 = 64 µs (min) to 128 µs (max) 01 = 192 µs (min) to 256 µs (max) 10 = 320 µs (min) to 384 µs (max) 11 = 448 µs (min) to 512 µs (max)			
	2 to 0	number of retries, set binary number			
WRITE_PROTECT	0	write protect (registers WD_TO and CHAN_WD_MAP)[1]: 1 = no write access 0 = write access	1b	1b	1b

Table 19. Protected settings *…continued*

Name	Bit	Description	Version setting values		
			FE	FM	FY
WDPN_LOW_TIME	7 to 0	watchdog time-out LOW time pulse (on pin WDTON) 00h = 1.0 ms 0Bh = 7.2 ms 16h = 49 ms 01h = 1.3 ms 0Ch = 8.2 ms 17h = 57 ms 02h = 1.5 ms 0Dh = 10 ms 18h = 66 ms 03h = 1.8 ms 0Eh = 12 ms 19h = 82 ms 04h = 2.0 ms 0Fh = 14 ms 1Ah = 98 ms 05h = 2.6 ms 10h = 16 ms 1Bh = 115 ms 06h = 3.1 ms 11h = 20 ms 1Ch = 131 ms 07h = 3.6 ms 12h = 25 ms 1Dh = 164 ms 08h = 4.1 ms 13h = 29 ms 1Eh = 197 ms 09h = 5.1 ms 14h = 33 ms 1Fh = 229 ms 0Ah = 6.1 ms 15h = 41 ms	00h	00h	00h
VSBATLOW_DEB_EN	0	debounce on V_{BAT} low signal: 1 = debounce enabled 0 = debounce disabled	0b	0b	0b
NXIFSC_CH0	-	channel 0: ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	6	6	6
NXIFSC_CH1	-	channel 1: ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	6	6	6
NXIFSC_CH2	-	channel 2: ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	6	6	6
NXIFSC_CH3	-	channel 3: ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	6	6	6
NXIFSC_CH4	-	channel 4: ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	3	6	6
NXIFSC_CH5	-	channel 5: ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	6	6	6
NXIFSC_CH6	-	channel 6: ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	6	6	6
NXIFSC_CH7	-	channel 7: ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	6	6	6
HL_CH0 to HL_CH7	-	channel 0 to 7: FET configuration (high or low side)	high	high	high
FIXED_GATE_SLEW_RATE	-	rising and falling slew rates have fixed values during gate turn-on	no	yes	yes

[1] Also sets default register reload for watchdog time-out.

11. Diagnostic functions

11.1 Reset for interrupt and SPI watchdog

An interrupt or SPI watchdog time-out can be reset by writing to the relevant write-only register. Values are not stored and cannot be read back.

Table 20. Write-only (for reset) registers (addresses 29h, 2Ah) bit description

Address	Register	Bit	Description
29h	CLEAR_CHAN_INTN	7 to 0	clears all channels (7 to 0) and interrupt: writing any value other than 00h to this register clears the interrupt and ISR register writing a logic 1 to any bit in this register clears the interrupt and ISR register AND clears the trip latch (resetting the retry register) for that specific channel
2Ah	CLEAR_WD	7 to 0	clear watchdog state: writing any value to this register clears SPI Watchdog mode

11.2 Diagnostic data

Diagnostic data can be obtained by reading data from the relevant 16-bit read-only registers. Send the register address as data to register READBACK (27h).

Table 21. Read-only (for diagnostic data) registers (addresses 30h to 35h, 38h to 3Fh) bit description

Address	Register	Bit	Description	Bit latches
30h	DIAG_BASIC		basic diagnostics [1]	
		15, 14	channel 7 basic diagnostics	
		13, 12	channel 6 basic diagnostics	
		11, 10	channel 5 basic diagnostics	
		9, 8	channel 4 basic diagnostics	
		7, 6	channel 3 basic diagnostics	
		5, 4	channel 2 basic diagnostics	
		3, 2	channel 1 basic diagnostics	
		1, 0	channel 0 basic diagnostics	
31h	DIAG_CTRL		controller diagnostics	
		15	SPI error: wrong number of bits	yes[2]
		14	V_{BAT} low	yes[3][4]
		13	SPI error: invalid address	yes[2]
		12	charge pump fault	yes[3][4]
		11	not used	
		10	logic reset has occurred	yes[3]
		9	watchdog time-out has occurred	yes[3]
		8	watchdog is enabled	
		7 to 0	channel configuration: 1 = high side 0 = low side	

Table 21. Read-only (for diagnostic data) registers (addresses 30h to 35h, 38h to 3Fh) bit description *…continued*

Address	Register	Bit	Description		Bit latches
32h	ISR		interrupt status	[5]	
		15	channel overtemperature	[6][7]	yes
		14	logic reset has occurred	[8]	yes
		13	channel tripped by controller (low battery)	[8][12]	yes
		12	V_{BAT} too low	[8]	yes
		11	charge pump fault	[8]	yes
		10	watchdog time-out	[9]	yes
		9	wrong number of bits in SPI communication	[10]	yes
		8	invalid address in SPI communication	[10]	yes
		7 to 5	channel index generating interrupt (binary number)	[6]	yes
		4	channel tripped by overcurrent	[6][11][12]	yes
		3	channel tripped by overtemperature	[6][7]	yes
		2	channel overcurrent	[6][11][13]	yes
		1	channel open-circuit	[6][14]	yes
		0	channel temperature sensor diode open-circuit	[6][15]	yes
33h	VERSION		device version number		
		15 to 8	main version	[16]	
		7 to 0	sub-version code	[17]	
34h	DIAG_CHAN_01		high-side FET on-state and open-circuit detection	[18]	
		15 to 8	high-side FET in on-state for channels 7 to 0		
		7 to 0	high-side FET open-circuit detected on channels 7 to 0		
35h	DIAG_CHAN_02		TSNSOPEN and overtemperature detection states		
		15 to 8	value of TSNSOPEN signal for channels 7 to 0		
		7 to 0	not used		
38h to 3Fh	DIAG_DETAIL_CHn		detail diagnostics channels 7 to 0		
		15 to 8	digital current measurement		
		7	channel temperature sensor open-circuit		yes[18]
		6	open-circuit load detected		yes[18]
		5	not used		
		4	channel overcurrent	[13]	yes[18]
		3	channel overtemperature		yes[18]
		2	channel tripped by controller (low battery)		yes[18]
		1	shorted output to V_{BAT}		yes[18]
		0	channel requested by user		

[1] Values for each channel are (in priority order):
00 = no controller fault.
10 = channel selected (normal or PWM). Applies during the PWM period when the channel and PWM are both selected.
01 = channel not selected but controller fault (low battery). This is latched, only cleared by reading DIAG_CTRL or selecting channel.
11 = channel selected but tripped off. Applies when the channel is selected but tripped by overcurrent or overtemperature.

[2] Bit is cleared when register is read or by writing to CLEAR_CHAN_INTN (provided SPI fault is mapped to INTN).

[3] Bit is cleared when register is read or by writing to CLEAR_CHAN_INTN (provided controller fault is mapped to INTN).

[4] When bit is cleared, value 01 in DIAG_BASIC is also cleared.

[5] The bits in this register latch when an interrupt is generated by the given source, once captured no new data is latched. The register is cleared by writing to CLEAR_CHAN_INTN.

[6] Requires specific channel mapped in IRQ_CHAN_MAP.

[7] Requires channel overtemperature to be mapped in IRQ_MAP.

[8] Requires controller fault to be mapped in IRQ_MAP.

[9] Requires watchdog time-out to be mapped in IRQ_MAP.

[10] Requires SPI error to be mapped in IRQ_MAP.

[11] Requires channel overcurrent to be mapped in IRQ_MAP.

[12] Mapping channel tripped in IRQ_MAP also enables this bit.

[13] If OCL protection is disabled and current exceeds the OCL level, the register bit is still set and an interrupt generated (provided channel overcurrent is mapped in IRQ_MAP). This is also true if OCL is delayed and the current exceeds the OCL level during the delay period.

[14] Requires open-circuit detected to be mapped in IRQ_MAP.

[15] Requires temperature sensor diode open-circuit to be mapped in IRQ_MAP.

[16] Denotes main product version:
50WDFE: 0Ah
Other types: 0Bh

[17] Denotes type or mask version:
50WDFE: 02
50WDFM: 01
50WDFY: 02
Versions may change if mask changes occur during production.

[18] Bit is cleared when register is read or by writing to CLEAR_CHAN_INTN.

12. Application design-in information

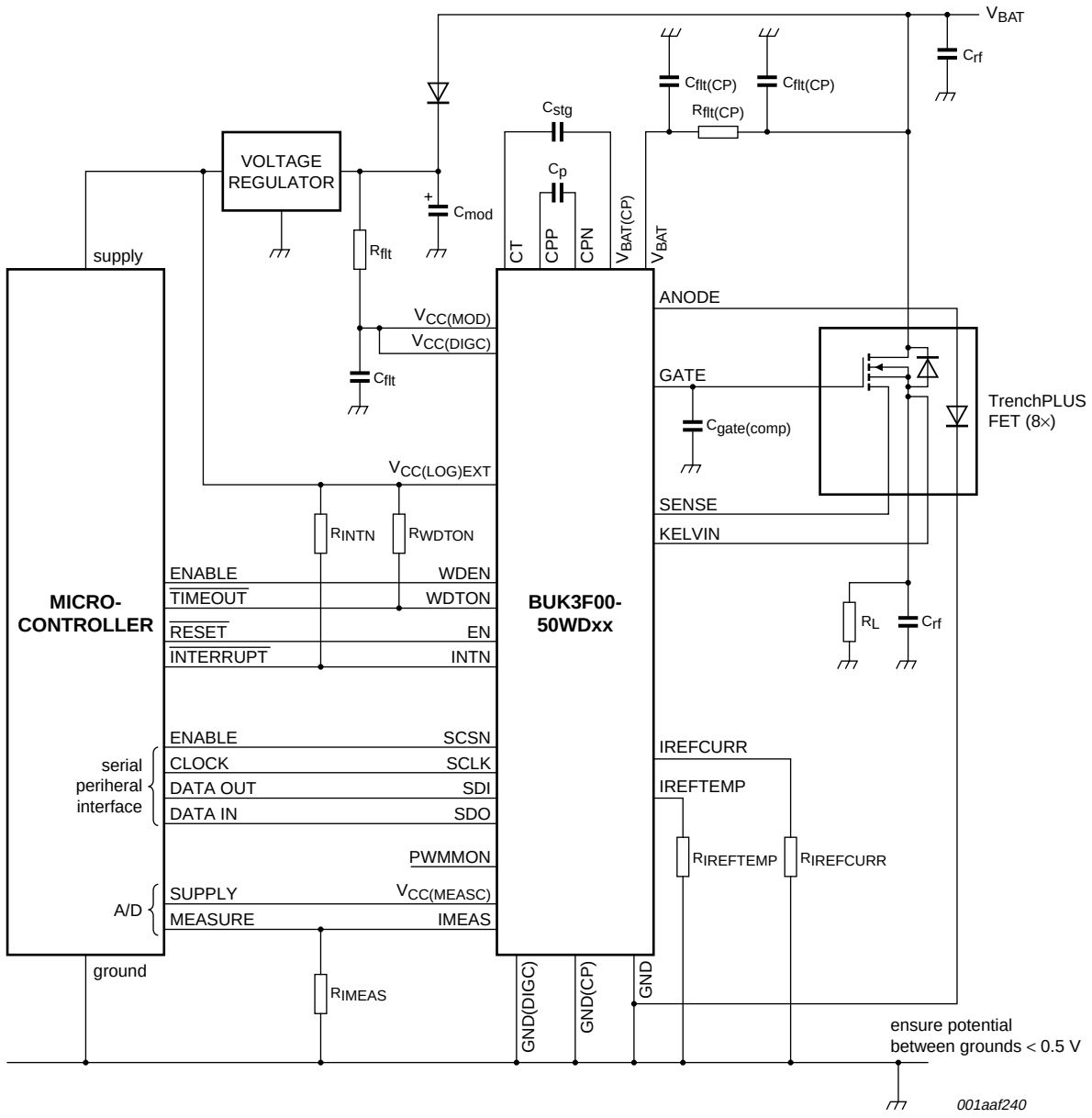


Fig 8. Application schematic

The charge pump pin $V_{BAT(CP)}$ can be connected in any one of the following ways:

- Connected directly to pin V_{BAT} and the battery supply.
- Connected through the internal resistor to pin V_{BAT} and the battery supply.
- Connected through the internal resistor to pin V_{BAT} and a filter circuit to the battery supply (as shown).

The method used depends on how important reducing the effect of charge pump noise is for the application circuit.

Table 22. External component requirements

Component	Remark		Value
Charge pump capacitors			
C_p	non-electrolytic; connect between pins CPP and CPN		20 nF (min)
C_{stg}	non-electrolytic; connect between pins $V_{BAT(CP)}$ and CT		1 µF (min)
Current reference and measurement resistors			
$R_{IREFTEMP}$	connect between pins IREFTEMP and GND	[1]	24.9 kΩ ± 1 %
$R_{IREFCURR}$	connect between pins IREFCURR and GND	[2]	24.9 kΩ ± 1 %
R_{IMEAS}	connect between pins IMEAS and GND		
	for sense currents up to 3 × $I_{meas(ADC)(fs)}$	[3]	10 kΩ ± 2 %
	for sense currents up to 8 × $I_{meas(ADC)(fs)}$	[3]	4.7 kΩ ± 2 %
Digital output pull-up resistors			
R_{INTN}	connect between pins INTN and $V_{CC(LOG)EXT}$		3.3 kΩ (min); 10 kΩ (typ); 100 kΩ (max)
R_{WDTON}	connect between pins WDTON and $V_{CC(LOG)EXT}$		3.3 kΩ (min); 10 kΩ (typ); 100 kΩ (max)
TrenchPLUS FET sense resistance		[4]	
R_{sense}	$I_{meas(ADC)(fs)}$ = 0.5 mA		100 Ω (min); 700 Ω (max)
	$I_{meas(ADC)(fs)}$ = 1.0 mA		50 Ω (min); 350 Ω (max)
	$I_{meas(ADC)(fs)}$ = 1.5 mA		33.3 Ω (min); 233.3 Ω (max)
	$I_{meas(ADC)(fs)}$ = 2.0 mA		25 Ω (min); 125 Ω (max)
Module supply decoupling			
C_{mod}	electrolytic		100 µF ± 20 %
R_{flt}	connect between pins $V_{CC(MOD)}$ plus $V_{CC(DIGC)}$ and supply	[5]	10 Ω ± 2 %
C_{flt}	non-electrolytic; connect between pins $V_{CC(MOD)}$ plus $V_{CC(DIGC)}$ and GND	[5]	100 nF ± 5 %
Optional charge pump filtering			
$R_{flt(CP)}$	charge pump filter resistor connect between pin V_{BAT} and battery supply	[6]	20 Ω (max)
$C_{flt(CP)}$	charge pump filter capacitors connect between pin V_{BAT} and GND and between $R_{flt(CP)}$ and GND		100 nF (max)
Optional gate C_{iss} compensation			
$C_{gate(comp)}$	for FETs with low C_{iss}		1 nF ± 5 %
Application circuit decoupling			
C_{rf}	value to be determined in the application circuit		-
Load resistor			
R_L	value to be determined in the application circuit		-
Direct input pin resistors (not shown)			
R_{INP}	connect between pins $V_{CC(LOG)EXT}$, $V_{CC(MOD)}$ and pins IN0 to IN3 as required.		50 kΩ ± 2 %

[1] Sets I_F to nominal 250 µA.

[2] Sets $I_{IREFCURR}$ to nominal 50 µA.

[3] Selection of R_{IMEAS} for sufficient dynamic range is also dependant on voltage of $V_{CC(MEASC)}$. Values quoted assume $V_{CC(MEASC)}$ = 5 V.

[4] R_{sense} is the drain-source resistance of the sense cells of the TrenchPLUS FET at the nominal drain current. It can be estimated from the product of the current-sense ratio and the drain-source resistance of the main FET.

[5] Pins $V_{CC(MOD)}$ and $V_{CC(DIGC)}$ can each have separate filtering for good decoupling.

[6] If $R_{flt(CP)}$ is not connected, then connect V_{BAT} directly with a short. If required, the charge pump can also be supplied directly from V_{BAT}.

Table 23. TrenchPLUS FET connections per channel

Connection	Description
Gate	gate of the output power MOSFET switch
Drain	drain of the output power MOSFET switch
Source	source of the output power MOSFET switch
Kelvin	kelvin source connection for current measurement
Sense	analog current measurement cell of the MOSFET switch (provides input for digital and analog current measurement)
Anode	temperature sense diode (electrically isolated from other connections)
Cathode	temperature sense diode (electrically isolated from other connections); connect to GND

13. Limiting values

Table 24. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	$T_{amb} \leq 85$ °C		-	1	W
T_j	junction temperature		[1]	–40	+150	°C
T_{stg}	storage temperature			–40	+150	°C
Power supplies						
V_{BAT}	battery supply voltage		[2]	–32	+60	V
$V_{CC(MOD)}$	module supply voltage			–0.5	+60	V
$V_{BAT(CP)}$	charge pump battery supply voltage			–32	+60	V
$V_{CC(DIGC)}$	digital core supply voltage			–0.5	+60	V
$V_{CC(LOG)EXT}$	external logic supply voltage		[3]	–0.5	+5.5	V
$V_{CC(MEASC)}$	measure circuit supply voltage			–0.5	+7	V
$\Delta V_{VBAT-VBAT(CP)}$	voltage difference between pin V_{BAT} and pin $V_{BAT(CP)}$		[4]	–0.5	+0.5	V
Ground levels[5]						
$\Delta V_{GND(bat-cp)}$	ground voltage difference from battery to charge pump	GND to GND(CP)		–0.5	+0.5	V
$\Delta V_{GND(bat-log)}$	ground voltage difference from battery to logic	GND to GND(DIGC)		–0.5	+0.5	V
$\Delta V_{GND(cp-log)}$	ground voltage difference from charge pump to logic	GND(CP) to GND(DIGC)		–0.5	+0.5	V
FET connection pins						
V_x	voltage on pin x	pins GATE, KELVIN, SENSE		–32	+60	V
		pin ANODE		–0.5	+7	V
ΔV	voltage difference	between pins KELVIN and V_{BAT}		–60	+2	V
		between KELVIN pins of 2 channels and between SENSE pins of 2 channels		–60	+60	V
$V_{I(cm)}$	common-mode input voltage	pins KELVIN and SENSE (for sense current measurement)		–40	V_{BAT} + 1	V

Table 24. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Digital input pins						
$V_{I(dig)}$	digital input voltage	pins EN, IN0, IN1, IN2, IN3, INP, SCLK, SCSN, SDI, WDEN		–1.5	-	V
$I_{I(dig)}$	digital input current			-	1	mA
Electrostatic discharge voltages						
V_{ESD}	electrostatic discharge voltage	CDM	[6]			
		corner pins		-	750	V
		other pins		-	500	V
		HBM	[7]	-	2	kV

[1] When T_j > 125 °C, the device will function, but electrical parameters may deviate from the specified values.

[2] Circuits will survive higher transient voltages, provided the clamp rating is not exceeded.

[3] This limiting value also applies to the open-drain output pins INTN and WDTON.

[4] Pin V_{BAT} can be connected from battery supply through pin $V_{BAT(CP)}$ and internal resistor.

[5] All 4 GND pins must be connected together to ground.

[6] CDM: C = 200 pF according to AEC-Q100-002 and 011.

[7] HBM: C = 100 pF; R = 1.5 kΩ according to AEC-Q100-002 and 011.

14. Recommended operating conditions

Table 25. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{BAT}	battery supply voltage	operating	[1]	5.5	13	52	V
$V_{BAT(CP)}$	charge pump battery supply voltage			9	13	52	V
$V_{CC(MOD)}$	module supply voltage			4.6	13	52	V
$V_{CC(DIGC)}$	digital core supply voltage			4.6	13	52	V
$V_{CC(LOG)EXT}$	external logic supply voltage			3.3	5	5.5	V
$V_{CC(MEASC)}$	measure circuit supply voltage			3.3	5	5.5	V
SR_{bat}	battery slew rate		[2]	-	-	100	V/µs
General							
T_{amb}	ambient temperature			–40	+25	+125	°C
FET connection pins							
$V_{I(cm)}$	common-mode input voltage	pins KELVIN and SENSE (for sense current measurement)		V_{BAT} – 2.5	-	V_{BAT} + 0.3	V
Direct input pins							
$f_{PWM(ext)}$	external PWM frequency	on pin INP		-	-	512	Hz
f_{sw}	switching frequency	on pins IN0, IN1, IN2 and IN3		-	-	512	Hz
SPI timing; see Figure 9	[3]						
f_{SPI}	SPI frequency			0	-	3	MHz
$t_{su(SCSN)}$	SCSN set-up time			10	-	-	ns
$t_{d(SCSN)}$	SCSN delay time			10	-	-	ns

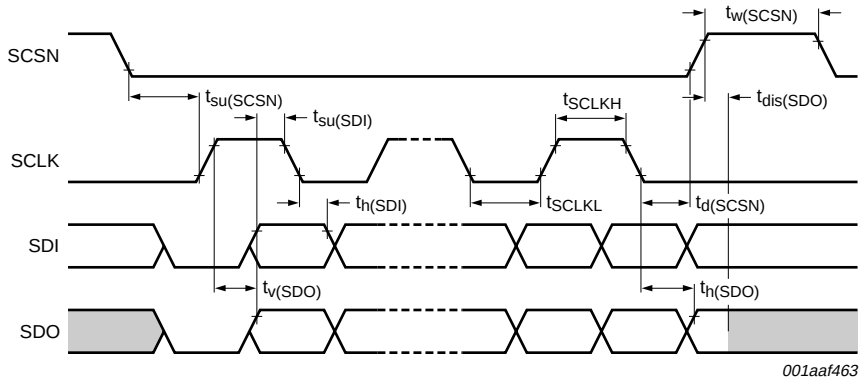
Table 25. Recommended operating conditions *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCSN)}$	SCSN pulse width		2	-	-	µs
$t_{su(SDI)}$	SDI set-up time		10	-	-	ns
$t_{h(SDI)}$	SDI hold time		10	-	-	ns
t_{SCLKH}	SCLK HIGH time		50	-	-	ns
t_{SCLKL}	SCLK LOW time		50	-	-	ns

[1] When V_{BAT} < 9 V, the charge pump cannot be guaranteed to drive the external MOSFETs to achieve their specified R_{DSon}.

[2] Higher slew rates can give uncontrolled device turn-on, device turn-off or channel switching.

[3] For SDO output characteristics; see Table 30 “SPI and watchdog characteristics”.



The shaded areas indicate the time that output data is not valid.

Fig 9. SPI timing definitions

15. Thermal characteristics

Table 26. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on single-layer PCB, size 11.43 cm × 7.62 cm (4.5 inch × 3.0 inch)		
		in free air	66	K/W
		at 1 m/s	54	K/W
		at 2.5 m/s	50	K/W
$R_{th(j-pcb)}$	thermal resistance from junction to printed-circuit board	board cooled by cold plate	23	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	case cooled at constant temperature	35	K/W

16. Characteristics

Table 27. Supplies characteristics

V_{BAT} = $V_{CC(MOD)}$ = 13 V; typical values are given at T_{amb} = 25 °C; limit values are given at T_{case} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies: pins V_{BAT}, $V_{BAT(CP)}$, $V_{CC(MOD)}$, $V_{CC(LOG)EXT}$ and $V_{CC(MEASC)}$							
Standby and quiescent currents (pin EN = LOW)							
$I_{stb(bat)}$	battery standby current	$V_{BAT} = V_{BAT(CP)}$ = 52 V	[1][2]	-	1.25	5	µA
$I_{stb(mod)}$	module standby current	$V_{CC(MOD)} = V_{CC(DIGC)}$ = 52 V	[3][2]	-	6.75	15	µA
$I_{q(log)ext}$	external logic quiescent current	$V_{CC(LOG)EXT}$ = 5 V; pins SCSN and WDEN not connected	[4]	-	-	1	µA
$I_{q(meas)}$	measure quiescent current	$V_{CC(MEASC)}$ = 5 V		-	-	1	µA
Operating currents (pin EN = HIGH)							
$I_{oper(bat)}$	battery operating current	$V_{BAT} = V_{BAT(CP)}$ = 13 V; I_{SENSE} = 2 mA [$I_{meas(ADC)(fs)}$]	[1][5]	3	-	10	mA
$I_{bat(M)}$	peak battery current	$V_{BAT} = V_{BAT(CP)}$ = 40 V; I_{SENSE} = 6 × 2 mA [$I_{meas(ADC)(fs)}$]	[1][5]	-	-	12.5	mA
$I_{oper(mod)}$	module operating current	$V_{CC(MOD)} = V_{CC(DIGC)}$ = 13 V; I_{SENSE} = 2 mA [$I_{meas(ADC)(fs)}$]	[3][5]	5	-	10	mA
$I_{mod(M)}$	peak module current	$V_{CC(MOD)} = V_{CC(DIGC)}$ = 40 V; I_{SENSE} = 6 × 2 mA [$I_{meas(ADC)(fs)}$]	[3][5]	-	-	12.5	mA
$I_{log(ext)M}$	peak external logic current	$V_{CC(LOG)EXT}$ = 5 V; pin WDEN = LOW; pin SDO at 3 MHz; C_L = 20 pF	[4]	-	-	450	µA
$I_{oper(meas)}$	measure operating current	$V_{CC(MEASC)}$ = 5 V; $R_{IREFCURR} = R_{IREFTEMP}$ = 24.9 kΩ		-	-	1.5 × $I_{O(meas)}$ + 30	µA
Transient voltages: pins V_{BAT}, $V_{CC(MOD)}$, $V_{CC(LOG)EXT}$, $V_{BAT(CP)}$, CPP, CPN, CT, GATE, KELVIN, SENSE							
V_{CL}	clamping voltage	I_{CL} = 10 mA; t_p = 300 µs		67.5	-	80	V
Battery supply: pin V_{BAT} and $V_{BAT(CP)}$							
Normal battery operation							
$V_{th(uv)bat}$	battery undervoltage threshold voltage	HIGH-to-LOW	[6]	4.7	-	5.2	V
		LOW-to-HIGH		4.95	-	5.4	V
$V_{hys(uv)bat}$	battery undervoltage hysteresis voltage		[6]	140	200	250	mV
$V_{th(low)bat}$	battery low threshold voltage	HIGH-to-LOW	[6]	1.85	-	2.15	V
		LOW-to-HIGH	[6]	2.1	-	2.4	V
$V_{hys(low)bat}$	battery low hysteresis voltage		[6]	150	225	300	mV
Reverse battery operation							
V_{G-bat}	voltage from gate to battery	V_{BAT} = −4 V		-	3.0	-	V
		V_{BAT} = −30 V		8	-	11	V
$I_{R(bat)}$	battery reverse current	$V_{BAT} = V_{BAT(CP)}$ = −30 V	[1]	-	-	10	mA
Module supply: pin $V_{CC(MOD)}$							
$V_{th(uv)mod}$	module undervoltage threshold voltage	HIGH-to-LOW		4.1	-	4.55	V
		LOW-to-HIGH		4.2	-	4.6	V

Table 27. Supplies characteristics *...continued*

V_{BAT} = $V_{CC(MOD)}$ = 13 V; typical values are given at T_{amb} = 25 °C; limit values are given at T_{case} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{hys(uv)mod}$	module undervoltage hysteresis voltage		25	50	130	mV
Reference outputs: pins IREFTEMP and IREFCURR						
$V_{O(ref)}$	reference output voltage	$R_{IREFCURR}$ = $R_{IREFTEMP}$ = 24.9 kΩ	1.20	1.24	1.28	V
$I_{O(ref)}$	reference output current		-	49.8	-	µA

[1] Total current = I_{BAT} + $I_{BAT(CP)}$.

[2] Standby currents valid provided V_{BAT} and $V_{CC(MOD)}$ > 9 V.

[3] Total current = $I_{CC(MOD)}$ + $I_{CC(DIGC)}$.

[4] Does not include current through pins INTN or WDTON pull-up resistors.

[5] All channels ON; with FET C_{rss} = 210 pF; f_{SPI} = 3 MHz.

[6] Monitored on pin $V_{BAT(CP)}$.

Table 28. Charge pump characteristics

V_{BAT} = $V_{CC(MOD)}$ = 13 V; typical values are given at T_{amb} = 25 °C; limit values are given at T_{case} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Charge pump: pins $V_{BAT(CP)}$, CPP, CPN and CT						
$f_{osc(cp)}$	charge pump oscillator frequency	V_{BAT} > 5.5 V	400	500	600	kHz
$V_{O(cp)}$	charge pump output voltage	V_{BAT} = 5.5 V to 9 V	4.5	-	-	V
		V_{BAT} > 9 V	6	6.5	7.5	V
$t_{bst(cp)}$	charge pump boost time	C_{stg} = 1 µF; V_{BAT} > 5.5 V	-	500	-	µs
$V_{th(fault)cp}$	charge pump fault threshold voltage	HIGH-to-LOW	-	-	3	V
		LOW-to-HIGH	2.6	-	-	V
$V_{hys(fault)cp}$	charge pump fault hysteresis voltage		50	150	250	mV

Table 29. Control circuits characteristics

V_{BAT} = $V_{CC(MOD)}$ = 13 V; typical values are given at T_{amb} = 25 °C; limit values are given at T_{case} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital control input: pin EN						
V_{IL}	LOW-level input voltage		1	-	-	V
V_{IH}	HIGH-level input voltage		-	-	2	V
$V_{hys(I)}$	input hysteresis voltage		150	-	550	mV
$V_{CL(i)}$	input clamping voltage		9.5	10.5	11.5	V
C_{in}	input capacitance		-	10	-	pF
R_{pd}	pull-down resistance		50	100	250	kΩ
t_{en}	enable time	[1]	-	-	100	µs
t_{dis}	disable time		-	1	1.6	ms
Interrupt output: pin INTN						
V_{OL}	LOW-level output voltage	I_I = 1.6 mA	-	-	0.4	V

Table 29. Control circuits characteristics *...continued*

V_{BAT} = $V_{CC(MOD)}$ = 13 V; typical values are given at T_{amb} = 25 °C; limit values are given at T_{case} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Direct channel control inputs: pins IN0, IN1, IN2 and IN3						
V_{IL}	LOW-level input voltage		1	-	-	V
V_{IH}	HIGH-level input voltage		-	-	2	V
$V_{hys(I)}$	input hysteresis voltage		200	-	700	mV
C_{in}	input capacitance		-	10	-	pF
R_{pd}	pull-down resistance		50	100	250	kΩ

[1] The time when both analog and digital circuits are enabled. High-side channels cannot be switched until the charge pump boost time has also elapsed.

Table 30. SPI and watchdog characteristics

V_{BAT} = $V_{CC(MOD)}$ = 13 V; typical values are given at T_{amb} = 25 °C; limit values are given at T_{case} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI input pins SCSN, SCLK, SDI and output pin SDO						
V_{IL}	LOW-level input voltage		1	-	-	V
V_{IH}	HIGH-level input voltage		-	-	2	V
$V_{hys(I)}$	input hysteresis voltage		200	-	700	mV
C_{in}	input capacitance		-	10	-	pF
V_{OL}	LOW-level output voltage	I_I = 1.6 mA	-	-	0.4	V
$V_{OH(log)(ext)}$	external logic HIGH-level output voltage	I_O = 1 mA	$V_{CC(LOG)EXT}$ − 0.4	-	-	V
R_{pd}	pull-down resistance	pins SCLK and SDI	50	100	250	kΩ
R_{pu}	pull-up resistance	pin SCSN	50	100	250	kΩ
$t_{h(SDO)}$	SDO hold time	C_L = 200 pF	-	-	100	ns
$t_{v(SDO)}$	SDO valid time		-	-	116	ns
$t_{dis(SDO)}$	SDO disable time		-	-	100	ns
Watchdog input pin WDEN and output pin WDTON						
V_{IL}	LOW-level input voltage		1	-	-	V
V_{IH}	HIGH-level input voltage		-	-	2	V
$V_{hys(I)}$	input hysteresis voltage		200	-	700	mV
$V_{CL(i)}$	input clamping voltage		9.5	10.5	11.5	V
C_{in}	input capacitance		-	10	-	pF
R_{pu}	pull-up resistance	pin WDEN	50	100	250	kΩ
V_{OL}	LOW-level output voltage	I_O = 1.6 mA	-	-	0.4	V
$\Delta t_{to(wd)}/t_{to(wd)}$	relative watchdog time-out time variation	pin WDEN = HIGH [1]	0	-	28	%

[1] Relative watchdog time-out time variation does not include clock frequency variation.

Table 31. Pulse-width modulation characteristics

V_{BAT} = $V_{CC(MOD)}$ = 13 V; typical values are given at T_{amb} = 25 °C; limit values are given at T_{case} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pulse-width modulator							
$\Delta f_{PWM}/f_{PWM}$	relative PWM frequency variation		[1]	−20	-	+20	%
PWM input: pin INP							
V_{IL}	LOW-level input voltage			1	-	-	V
V_{IH}	HIGH-level input voltage			-	-	2	V
$V_{hys(I)}$	input hysteresis voltage			200	-	700	mV
$V_{CL(i)}$	input clamping voltage			9.5	10.5	11.5	V
C_{in}	input capacitance			-	10	-	pF
R_{pd}	pull-down resistance			50	100	250	kΩ
PWM output: pin PWMMON							
V_{OL}	LOW-level output voltage	I_I = 1.6 mA		-	-	0.4	V
$V_{OH(log)(ext)}$	external logic HIGH-level output voltage	I_O = 1 mA		$V_{CC(LOG)EXT}$ − 0.4	-	-	V

[1] Relative PWM frequency error includes clock frequency variation.

Table 32. Current measurement characteristics

V_{BAT} = $V_{CC(MOD)}$ = 13 V; typical values are given at T_{amb} = 25 °C; limit values are given at T_{case} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Current measurement[1]							
$E_{ADC(I)}$	ADC error (current)	all ranges; $R_{IREFCURR}$ = 24.9 kΩ	[2]				
		0.01 × $I_{meas(ADC)(fs)}$	[3]	−2	-	+2	bit
		0.20 × $I_{meas(ADC)(fs)}$		−4	-	+4	bit
		0.80 × $I_{meas(ADC)(fs)}$					
		type 50WDFE		−11	-	+15	bit
		other 50WDxx types		−13	-	+13	bit
$I_{O(meas)}$	measure output current	all ranges; $V_{CC(MEASC)}$ = 5 V; R_{IMEAS} = 4.7 kΩ; $R_{IREFCURR}$ = 24.9 kΩ					
		0.00 × $I_{meas(ADC)(fs)}$		-	0	5	µA
		0.20 × $I_{meas(ADC)(fs)}$		15	20	25	µA
		1.00 × $I_{meas(ADC)(fs)}$		92.5	102.5	112.5	µA
		8.00 × $I_{meas(ADC)(fs)}$		660	820	980	µA

[1] If measured without a FET, then connect a suitable resistor between pins V_{BAT} and SENSE to ensure stability.

[2] ADC accuracy ensured when V_{BAT} and $V_{CC(MOD)}$ > 9 V.

[3] ADC used at this level for on-state open-circuit detection.

Table 33. Gate drive high-side switches characteristics

V_{BAT} = $V_{CC(MOD)}$ = 13 V; typical values are given at T_{amb} = 25 °C; limit values are given at T_{case} = –40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Gate drive for high-side switches							
V_{GS}	gate-source voltage	on-state					
		V_{BAT} = 5.5 V to 9 V		4.0	-	7.5	V
		V_{BAT} > 9 V		5.5	6.5	7.5	V
$V_{CL(G)}$	gate clamping voltage	inductive ring-off		–28.5	–22.5	–20	V
SR_r	rising slew rate	CTRL_SET[3] = 0 OR $V_{KELVIN-GND}$ > 2.5 V (high region); FET C_{rss} = 210 pF	[1]	0.5	1	1.2	V/µs
		CTRL_SET[3] = 1 AND $V_{KELVIN-GND}$ < 2.5 V (low region); FET C_{rss} = 210 pF		0.25	0.5	0.6	V/µs
SR_f	falling slew rate	CTRL_SET[3] = 0 OR $V_{KELVIN-GND}$ > 2.5 V (high region); FET C_{rss} = 210 pF	[1]	0.5	1	1.2	V/µs
		CTRL_SET[3] = 1 AND $V_{KELVIN-GND}$ < 2.5 V (low region); FET C_{rss} = 210 pF		0.25	0.5	0.6	V/µs
$R_{o(GATE-KELVIN)}$	output resistance between pin GATE and pin KELVIN	Standby mode; pin EN = LOW	[2]	70	130	230	Ω
		gate hold-off	[2]	70	130	230	Ω
		loss of ground; pin GND = V_{BAT}		30	80	190	kΩ
$I_{G(sc)}$	short-circuit gate current	channel on; short-circuit to ground		-	-	2.5	mA

[1] If fixed gate slew rate option is set, then rising and falling slew rates are constant irrespective of $V_{KELVIN-GND}$. For accurate measurement of slew rates, V_{BAT} supply must remain constant during test.

[2] Specification includes pin KELVIN series resistance.

Table 34. Protection circuits characteristics

V_{BAT} = $V_{CC(MOD)}$ = 13 V; typical values are given at T_{amb} = 25 °C; limit values are given at T_{case} = –40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Overtemperature protection							
I_F	forward current	$R_{IREFTEMP}$ = 24.9 kΩ		236	248	260	µA
$V_{trip(otp)}$	over-temperature protection trip voltage	$R_{IREFTEMP}$ = 24.9 kΩ	[1]				
		trip level setting = 00b		2.255	2.305	2.348	V
		trip level setting = 01b		2.198	2.248	2.291	V
		trip level setting = 10b		2.108	2.158	2.201	V
		trip level setting = 11b		1.953	2.003	2.046	V
$V_{hys(trip)otp}$	over-temperature protection trip hysteresis voltage			40	50	60	mV
$t_{fltr(trip)}$	trip filter time			26	-	57	µs
$V_{th(det)oc(TSD)}$	temperature sensor diode open-circuit detection threshold voltage	T_{amb} = –40 °C		2.5	-	3.9	V
		T_{amb} = +125 °C		2.4	-	3.8	V

Table 34. Protection circuits characteristics *...continued*

V_{BAT} = $V_{CC(MOD)}$ = 13 V; typical values are given at T_{amb} = 25 °C; limit values are given at T_{case} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Overcurrent protection[2]							
$V_{th(on)(bat-KEL)}$	on-state threshold voltage between battery and pin KELVIN	HIGH-to-LOW	[3]	1.65	1.95	2.25	V
		LOW-to-HIGH		1.50	1.80	2.10	V
$V_{hys(on)(bat-KEL)}$	on-state hysteresis voltage from battery to pin KELVIN			-	150	-	mV
$\Delta I_{trip}/I_{trip}$	relative trip current variation	OCH; $R_{IREFCURR}$ = 24.9 kΩ	[3][4]	−7.5	+3	+15	%
		TONOCH; $R_{IREFCURR}$ = 24.9 kΩ; high-side switch in turn-on state; V_{SENSE} = 2.5 V	[4][5]				
		trip ratio ≥ 5		−10	+5	+20	%
		trip ratio ≤ 4		−7.5	+7.5	+22.5	%
$\Delta t_{blank}/t_{blank}$	relative blanking time variation		[6]	0	-	28	%
$V_{th(sense)low}$	low sense threshold voltage	HIGH-to-LOW; TONOCH operation		1	1.25	1.5	V
Open-circuit detection							
$I_{det(oc)on}$	on-state open-circuit detection current	DIG_OLTH[3:0] = 3; $R_{IREFCURR}$ = 24.9 kΩ; all ranges					
		open-circuit not detected		-	-	0.5 / 255 × $I_{meas(ADC)(fs)}$	µA
		open-circuit detected		4.5 / 255 × $I_{meas(ADC)(fs)}$	-	-	µA
$I_{det(oc)off}$	off-state open-circuit detection current	V_{KELVIN} = 2.5 V					
		type 50WDFE		40	-	100	µA
		other 50WDxx types		55	-	115	µA
$V_{det(oc)off}$	off-state open-circuit detection voltage			2.4	2.6	2.8	V

[1] Nominal trip voltages quoted for each level. Refer to data sheet for TrenchPLUS FET devices for equivalent temperature measurement.

[2] If measured without a FET, then connect a suitable resistor between pins V_{BAT} and SENSE to ensure stability.

[3] Accuracy ensured when V_{BAT} and $V_{CC(MOD)}$ > 9 V.

[4] Nominal I_{trip} = n × $I_{meas(ADC)(fs)}$, where n is the OCH and TONOCH trip level ratio for the product type; see NXIFSC_CHn in Table 19.

[5] Until the channel is fully turned on, when voltage from battery to pin KELVIN < $V_{th(on)(bat-KEL)}$.

[6] Relative blanking time variation does not include clock frequency variation.

17. Application information

17.1 ElectroMagnetic Compatibility guidelines

In some applications, problems associated with electromagnetic interference can occur, such as false overcurrent tripping, false overtemperature tripping or unexpected turn-on of individual channels. Vulnerable points can be where currents are induced from wiring harness connectors positioned close to sensitive control tracks (such as control lines or FET gate, sense and kelvin lines). Good PCB and circuit design, following RF design principles, can ensure such problems are avoided. The following guidelines are provided to achieve this.

17.1.1 Ground layers

In multilayer PCB design, keep sensitive analog signals on the top PCB layer with a second ground layer acting as a shield. There should be no slits or breaks in this ground layer.

17.1.2 Circuit loops and tracks

Keep the area of circuit loops small and the length of sensitive tracks short with components positioned as closely as possible. This particularly applies to FET gate, sense and kelvin lines.

17.1.3 Connector decoupling

Decoupling capacitors should be fitted directly on, or as close as possible to, connectors, preventing currents being induced on FET or control tracks.

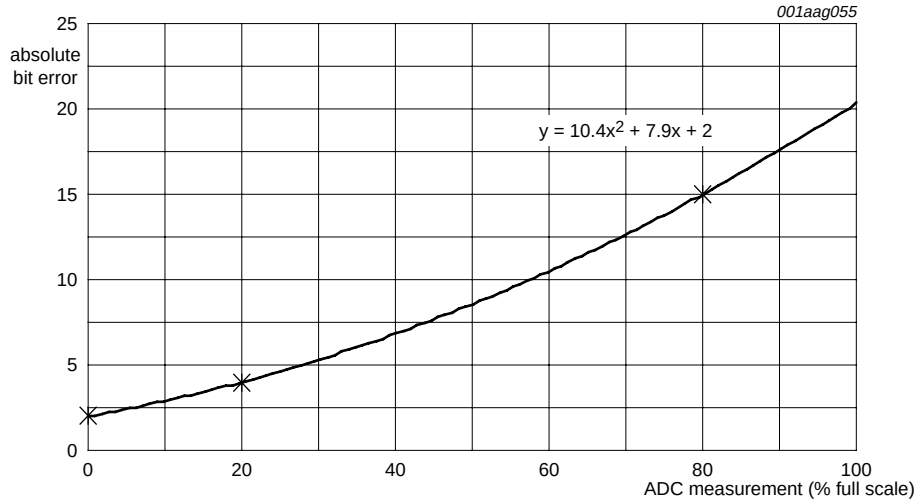
17.1.4 Module supply decoupling

This supply can be decoupled for EMC with a small ferrite bead.

Circuit analysis should include assessment of possible paths for EMC-induced currents from different wiring harnesses connected to the PCB.

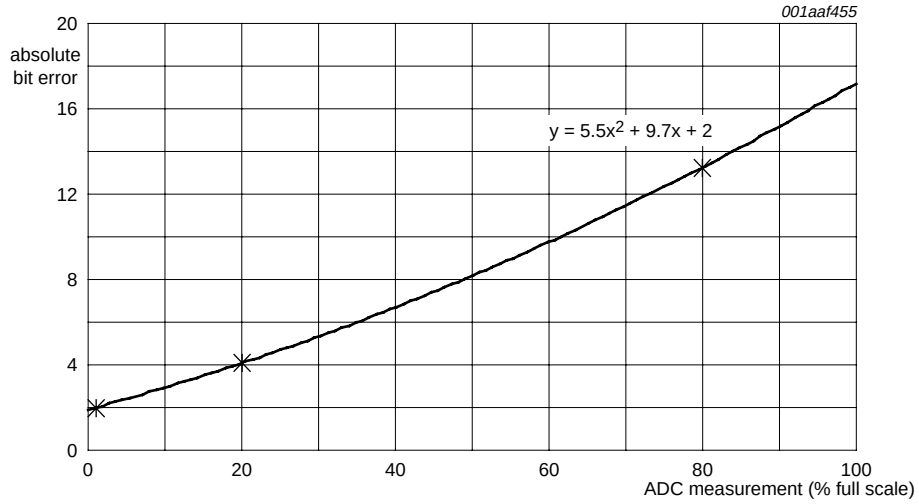
17.2 ADC accuracy

The ADC accuracy can be calculated at different measurement points using the graphs Figure 10 and Figure 11 or associated equation. The effect of additional errors in the reference current resistor can be estimated as a proportion of the resistor value.



$R_{IREFCURR}$ = 24.9 kΩ.

Fig 10. Maximum ADC bit errors (type 50WDFE)



$R_{IREFCURR}$ = 24.9 kΩ.

Fig 11. Maximum ADC bit errors (other 50WDxx types)

17.3 Additional metal mask options

Additional metal mask options can be provided with different default settings. Table 35 can be used to submit these requirements for assessment.

Table 35. Registers for mask options

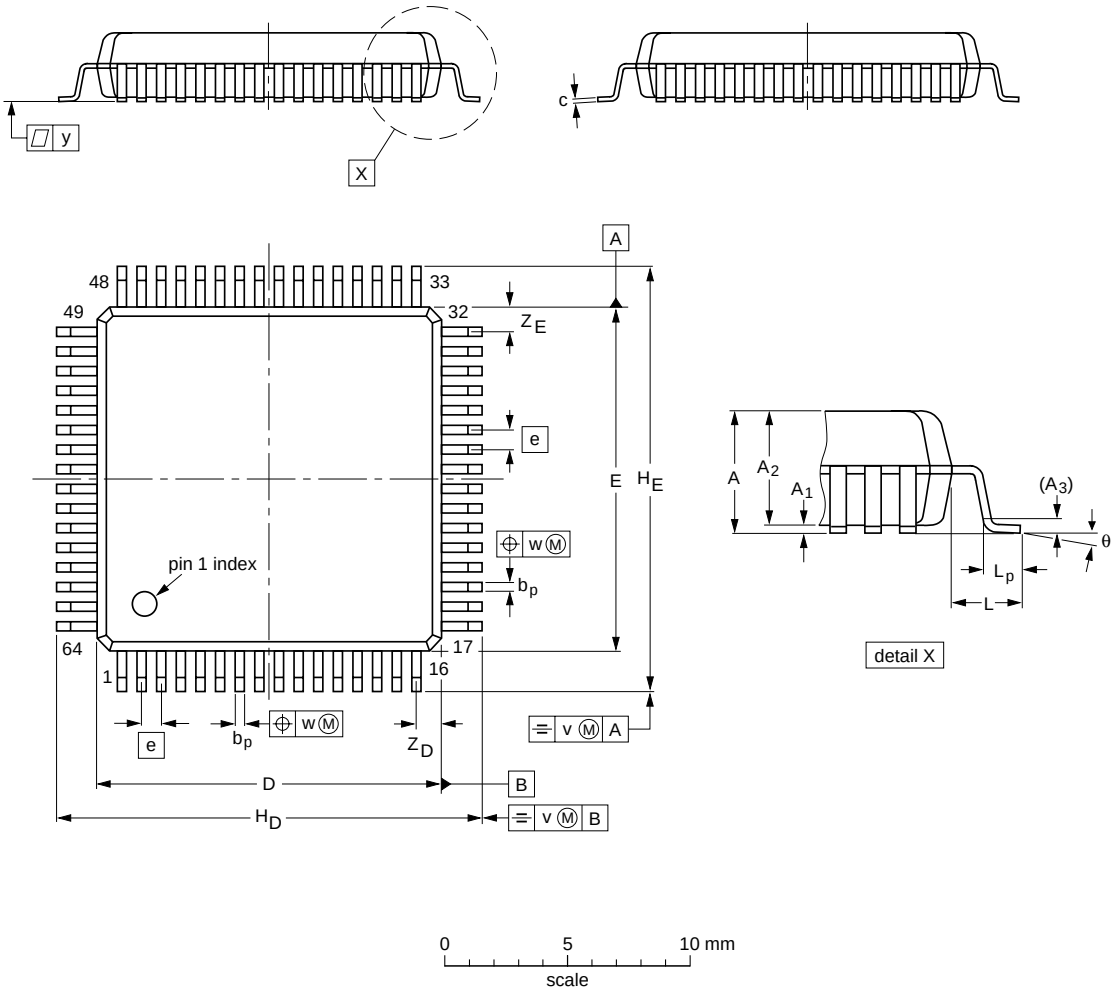
Register	Name	Description	Setting required
02h	IN02_MAP	direct input pins IN0 and IN2 mapping	
03h	IN13_MAP	direct input pins IN1 and IN3 mapping	
04h	INP_MAP	PWM input pin INP mapping	
05h	ANDOR_MAP	direct input pin AND/OR operation	
07h	SEL_CURR_TRIP_CHAN	select current tripping channel	
08h	CHAN_OT_FAULT_CLR	channel set overtemperature fault clear	
0Ch	CHAN_WD_MAP	select channel watchdog behavior	
0Dh	WD_TO	watchdog time-out period setting	
0Eh	CTRL_SET	controller settings	
0Fh	INT_PWM_FREQ	internal PWM frequency setting	
10h	PWM_DC_CH0	internal PWM duty cycle setting for channel 0	
11h	PWM_DC_CH1	internal PWM duty cycle setting for channel 1	
12h	PWM_DC_CH2	internal PWM duty cycle setting for channel 2	
13h	PWM_DC_CH3	internal PWM duty cycle setting for channel 3	
14h	PWM_DC_CH4	internal PWM duty cycle setting for channel 4	
15h	PWM_DC_CH5	internal PWM duty cycle setting for channel 5	
16h	PWM_DC_CH6	internal PWM duty cycle setting for channel 6	
17h	PWM_DC_CH7	internal PWM duty cycle setting for channel 7	
18h	OT_TRIPLEV_CH30	overtemperature trip level channels 3 to 0	
19h	OT_TRIPLEV_CH74	overtemperature trip level channels 7 to 4	
1Ah	IFSC_CH30	full-scale reference current channels 3 to 0	
1Bh	IFSC_CH74	full-scale reference current channels 7 to 4	
24h	IRQ_MAP	interrupt request mapping	
25h	CURR_TRIP_BLANKTIME	current trip blanking time	
-	DIG_OLTH	open-circuit threshold level	
-	DIG_FET	channel tripping behavior and filter times	
-	CHAN_ALLOW_RETRY	channel allow trip and retry after OCH or TONOCH faults	
-	RETRY_SETTINGS	trip retry delay and number of retries	
-	WRITE_PROTECT	write protect (registers WD_TO and CHAN_WD_MAP)	
-	WDPN_LOW_TIME	watchdog time-out LOW time pulse (pin WDTON)	
-	VSBATLOW_DEB_EN	debounce on V_{BAT} LOW signal	
-	NXIFSC_CH0	channel 0 ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	
-	NXIFSC_CH1	channel 1 ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	
-	NXIFSC_CH2	channel 2 ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	
-	NXIFSC_CH3	channel 3 ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	
-	NXIFSC_CH4	channel 4 ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	

Table 35. Registers for mask options *…continued*

Register	Name	Description	Setting required
-	NXIFSC_CH5	channel 5 ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	
-	NXIFSC_CH6	channel 6 ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	
-	NXIFSC_CH7	channel 7 ratio OCH and TONOCH trip level to $I_{meas(ADC)(fs)}$	
-	HL_CH0	channel 0 FET configuration (high or low side)	only high side available
-	HL_CH1	channel 1 FET configuration (high or low side)	
-	HL_CH2	channel 2 FET configuration (high or low side)	
-	HL_CH3	channel 3 FET configuration (high or low side)	
-	HL_CH4	channel 4 FET configuration (high or low side)	
-	HL_CH5	channel 5 FET configuration (high or low side)	
-	HL_CH6	channel 6 FET configuration (high or low side)	
-	HL_CH7	channel 7 FET configuration (high or low side)	
-	FIXED_GATE_SLEW_RATE	rising and falling slew rate to have fixed or variable values during gate turn-on	

18. Package outline

QFP64: plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 x 14 x 2.7 mm **SOT393-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3	0.25 0.10	2.75 2.55	0.25	0.45 0.30	0.23 0.13	14.1 13.9	14.1 13.9	0.8	17.45 16.95	17.45 16.95	1.6	1.03 0.73	0.16	0.16	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT393-1	134E07	MS-022				~~00-01-19~~ 03-02-20

Fig 12. Package outline SOT393-1 (QFP64)

19. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

19.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

19.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

19.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

19.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 36 and 37

Table 36. SnPb eutectic process (from J-STD-020C)

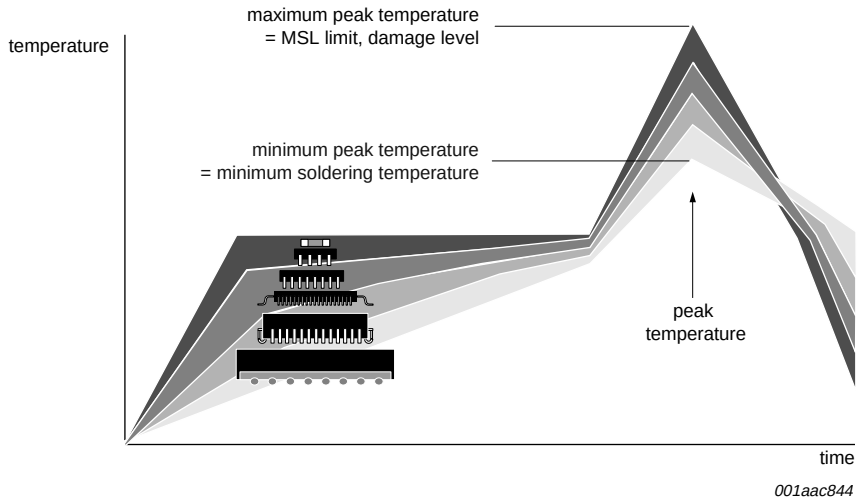
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 37. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.



MSL: Moisture Sensitivity Level

Fig 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

20. Abbreviations

Table 38. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
ASIC	Application Specific Integrated Circuit
CDM	Charge Device Model
EMC	ElectroMagnetic Compatibility
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HBM	Human Body Model
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse-Width Modulation
RF	Radio Frequency
SPI	Serial Peripheral Interface

21. Revision history

Table 39. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK3F00-50WDXX_2	20080121	Product data sheet	-	BUK3F00-50WDXX_1
Modifications:	• Table 27, $V_{hys(uv)mod}$ = module undervoltage hysteresis voltage: max value changed from 100 to 130.			
BUK3F00-50WDXX_1	20071128	Product data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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