High Precision Tri-Axis Inertial Sensor

ADIS16354

FEATURES

Tri-axis gyroscope with digital range scaling
±75°/s, ±150°/s, ±300°/s settings
14-bit resolution
Tri-axis accelerometer
±1.7 *g* measurement range, 14-bit resolution
350 Hz bandwidth
Factory calibrated sensitivity, bias, and alignment
Calibration temperature range: −20°C to +70°C
Operating temperature range: −40°C to +85°C
Digitally controlled bias calibration
Digitally controlled sample rate
Digitally controlled filtering
Programmable condition monitoring
Auxiliary digital input/output
Digitally activated self-test
Programmable power management
Embedded temperature sensor
SPI-compatible serial interface
Auxiliary 12-bit ADC input and DAC output
Single-supply operation: 4.75 V to 5.25 V
2000 *g* shock survivability

APPLICATIONS

Guidance and control
Platform control and stabilization
Motion control and analysis
Inertial measurement units
General navigation
Image stabilization
Robotics

FUNCTIONAL BLOCK DIAGRAM

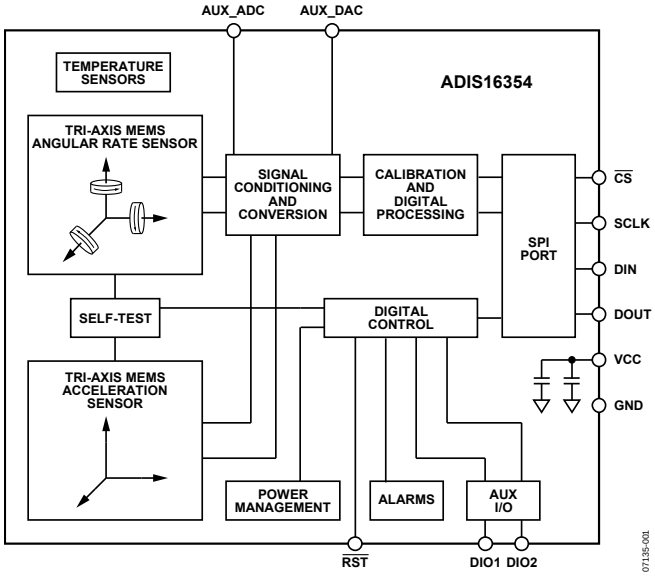

Figure 1.

GENERAL DESCRIPTION

The ADIS16354 *i*Sensor™ is a complete triple axis gyroscope and triple axis accelerometer inertial sensing system. This sensor combines the Analog Devices, Inc., *i*MEMS® and mixed signal processing technology to produce a highly integrated solution, providing calibrated, digital inertial sensing. An SPI interface and simple output register structure allow for easy access to data and configuration controls.

The SPI port provides access to the following embedded sensors: X-, Y-, and Z-axis angular rates; X-, Y-, and Z-axis linear acceleration; internal temperature; power supply; and auxiliary analog input. The inertial sensors are precision-aligned across axes, and are calibrated for offset and sensitivity over a temperature range of −20°C to +70°C. An embedded controller dynamically compensates for all major influences on the MEMS sensors, thus maintaining highly accurate sensor outputs without further testing, circuitry, or user intervention.

The following programmable features simplify system integration:

- In-system autobias calibration
- Digital filtering and sample rate
- Self-test
- Power management
- Condition monitoring
- Auxiliary digital input/output

This compact module is approximately 23 mm × 23 mm × 23 mm and provides a convenient flex-based connector system.

Rev. 0

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REVISION HISTORY

1/08—Revision 0: Initial Version

SPECIFICATIONS

T_A = −40°C to +85°C, V_{CC} = 5.0 V, angular rate = 0°/s, dynamic range = 300°/sec, ±1 *g*, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
GYROSCOPE SENSITIVITY	Each axis				
Initial Sensitivity	25°C, dynamic range = ±300°/s	0.0725	0.07326	0.0740	°/s/LSB
	25°C, dynamic range = ±150°/s		0.03663		°/s/LSB
	25°C, dynamic range = ±75°/s		0.01832		°/s/LSB
Temperature Coefficient	See Figure 6, −20°C to +70°C		40		ppm/°C
Gyroscope Axis Nonorthogonality	25°C, difference from 90° ideal		±0.05		Degree
Gyroscope Axis Misalignment	25°C, relative to base-plate and guide pins		±0.5		Degree
Nonlinearity	Best fit straight line		0.1		% of FS
GYROSCOPE BIAS					
In Run Bias Stability	25°C, 1 σ		0.015		°/s
Angular Random Walk	25°C		4.2		°/√hr
Temperature Coefficient	See Figure 7, −20°C to +70°C		0.01		°/s/°C
Linear Acceleration Effect	Any axis, 1 σ (linear acceleration bias compensation enabled)		0.05		°/s/*g*
Voltage Sensitivity	V_{CC} = 4.75 V to 5.25 V		0.25		°/s/V
GYROSCOPE NOISE PERFORMANCE					
Output Noise	25°C, ±300°/s range, 2-tap filter setting		0.60		°/s rms
	25°C, ±150°/s range, 8-tap filter setting		0.35		°/s rms
	25°C, ±75°/s range, 32-tap filter setting		0.17		°/s rms
Rate Noise Density	25°C, f = 25 Hz, ±300°/s, no filtering		0.05		°/s/√Hz rms
GYROSCOPE FREQUENCY RESPONSE					
3 dB Bandwidth			350		Hz
Sensor Resonant Frequency			14		kHz
GYROSCOPE SELF-TEST STATE					
Change for Positive Stimulus	±300°/s range setting	432	723	1105	LSB
Change for Negative Stimulus	±300°/s range setting	−432	−723	−1105	LSB
Internal Self-Test Cycle Time			35		ms
ACCELEROMETER SENSITIVITY	Each axis				
Dynamic Range		±1.7			*g*
Initial Sensitivity	25°C	0.4578	0.4625	0.4672	m*g*/LSB
Temperature Coefficient	−20°C to +70°C		40		ppm/°C
Axis Nonorthogonality	25°C, difference from 90° ideal		±0.2		Degree
Axis Misalignment	25°C, relative to base-plate and guide pins		±0.5		Degree
Nonlinearity	Best fit straight line		±0.2		% of FS
ACCELEROMETER BIAS					
Velocity Random Walk	25°C		0.135		m/s/√hr
Temperature Coefficient			0.25		m*g*/°C
ACCELEROMETER NOISE PERFORMANCE					
Output Noise	25°C, no filtering		4.7		m*g* rms
Noise Density	25°C, no filtering		0.24		m*g*/√Hz rms
ACCELEROMETER FREQUENCY RESPONSE					
3 dB Bandwidth			350		Hz
Sensor Resonant Frequency			5.5		kHz
ACCELEROMETER SELF-TEST STATE					
Output Change When Active		434	744	1052	LSB
TEMPERATURE SENSOR					
Output at 25°C			0		LSB
Scale Factor			6.88		LSB/°C

Parameter	Conditions	Min	Typ	Max	Unit
ADC INPUT					
Resolution			12		Bits
Integral Nonlinearity			±2		LSB
Differential Nonlinearity			±1		LSB
Offset Error			±4		LSB
Gain Error			±2		LSB
Input Range		0		2.5	V
Input Capacitance	During acquisition		20		pF
DAC OUTPUT	5 kΩ/100 pF to GND				
Resolution			12		Bits
Relative Accuracy	For Code 101 to Code 4095		±4		LSB
Differential Nonlinearity			±1		LSB
Offset Error			±5		mV
Gain Error			±0.5		%
Output Range				2.5	V
Output Impedance			2		Ω
Output Settling Time			10		µs
LOGIC INPUTS[1]					
Input High Voltage, V_{INH}		2.0			V
Input Low Voltage, V_{INL}				0.8	V
	For –CS signal when used to wake up from sleep mode			0.55	V
Logic 1 Input Current, I_{INH}	V_{IH} = 3.3 V		±0.2	±10	µA
Logic 0 Input Current, I_{INL}	V_{IL} = 0 V				
All Except $\overline{RST}$			–40	–60	µA
$\overline{RST}$			–1		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[1]					
Output High Voltage, V_{OH}	I_{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1.6 mA			0.4	V
SLEEP TIMER					
Timeout Period[2]		0.5		128	Sec
FLASH MEMORY					
Endurance[3]		10,000			Cycles
Data Retention[4]	T_J = 85°C	20			Years
CONVERSION RATE					
Maximum Sample Rate	SMPL_PRD = 0x01		819.2		SPS
Minimum Sample Rate	SMPL_PRD = 0xFF		0.413		SPS
START-UP TIME[5]					
Initial Power-Up			150		ms
Sleep Mode Recovery			3		ms
POWER SUPPLY					
Operating Voltage Range, V_{CC}		4.75	5.0	5.25	V
Power Supply Current	Normal mode at 25°C		33		mA
	Fast mode at 25°C		57		mA
	Sleep mode at 25°C		500		µA

[1] The digital I/O signals are driven by an internal 3.3 V supply and the inputs are 5 V tolerant.
[2] Guaranteed by design.
[3] Endurance is qualified as per JEDEC Standard 22, Method A117 and measured at –40°C, +25°C, +85°C, and +125°C.
[4] Retention lifetime equivalent at junction temperature (T_J) 85°C as per JEDEC Standard 22, Method A117. Retention lifetime decreases with junction temperature.
[5] This is defined as the time from wake-up to the first conversion. This time does not include sensor settling time, which is dependent on the filter settings.

TIMING SPECIFICATIONS

T_A = 25°C, V_{CC} = 5.0 V, angular rate = 0°/s, unless otherwise noted.

Table 2.

Parameter	Description	Min[1]	Typ	Max[1]	Unit
f_{SCLK}	Fast mode, SMPL_PRD ≤ 0x09 (f_S ≥ 164 Hz)	0.01		2	MHz
	Normal mode, SMPL_PRD ≥ 0x0A (f_S ≤ 149 Hz)	10		300	kHz
$t_{DATARATE}$	Data rate time, fast mode, SMPL_PRD ≤ 0x09 (f_S ≥ 164 Hz)	40			µs
	Data rate time, normal mode, SMPL_PRD ≥ 0x0A (f_S ≤ 149 Hz)	160			µs
$t_{DATASTALL}$	Data stall time, fast mode, SMPL_PRD ≤ 0x09 (f_S ≥ 164 Hz)	9			µs
	Data stall time, normal mode, SMPL_PRD ≥ 0x0A (f_S ≤ 149 Hz)	75			µs
t_{CS}	Chip select to clock edge	48.8			ns
t_{DAV}	Data output valid after SCLK falling edge[2]			100	ns
t_{DSU}	Data input setup time before SCLK rising edge	24.4			ns
t_{DHD}	Data input hold time after SCLK rising edge	48.8			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge[3]	5			ns

[1] Guaranteed by design, not production tested.

[2] The MSB presents an exception to this parameter. The MSB clocks out on the falling edge of $\overline{CS}$. The rest of the DOUT bits are clocked after the falling edge of SCLK and are governed by this specification.

[3] This parameter may need to be expanded to allow for proper capture of the LSB. After $\overline{CS}$ goes high, the DOUT line goes into a high impedance state.

TIMING DIAGRAMS

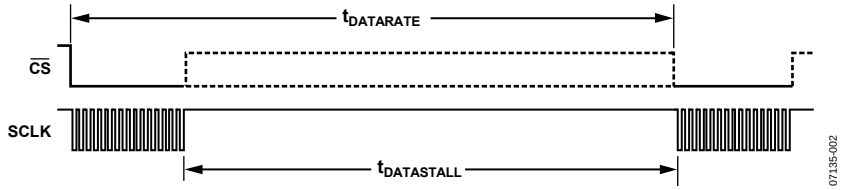

Figure 2. SPI Chip Select Timing

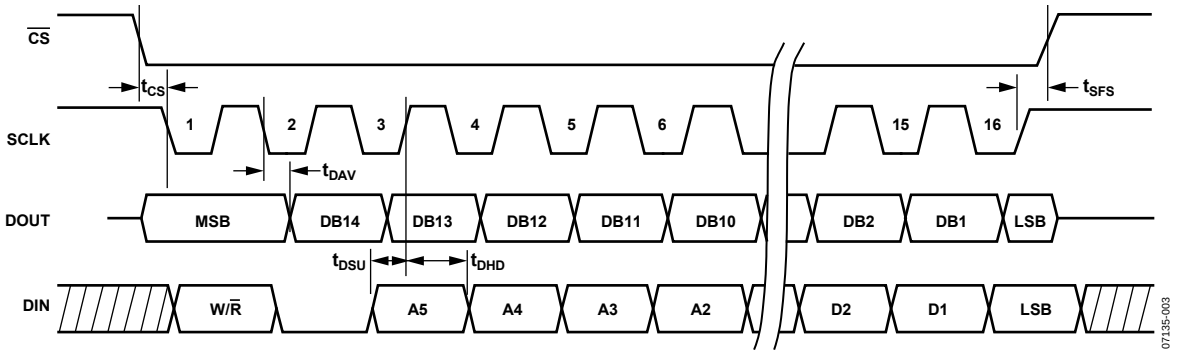

Figure 3. SPI Timing, Utilizing SPI Settings Typically Identified as Phase = 1, Polarity = 1

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	2000 *g*
Any Axis, Powered	2000 *g*
VCC to GND	−0.3 V to +6.0 V
Digital Input/Output Voltage to COM	−0.3 V to +5.3 V
Analog Inputs to COM	−0.3 V to +3.6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C[1, 2]

[1] Extended exposure to temperatures outside the specified temperature range of −40°C to +85°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the parts within the specified operating range of −40°C to +85°C.

[2] Although the device is capable of withstanding short-term exposure to 150°C, long-term exposure threatens internal mechanical integrity.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
24-Lead Module	39.8°C/W	14.2°C/W	16 grams

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

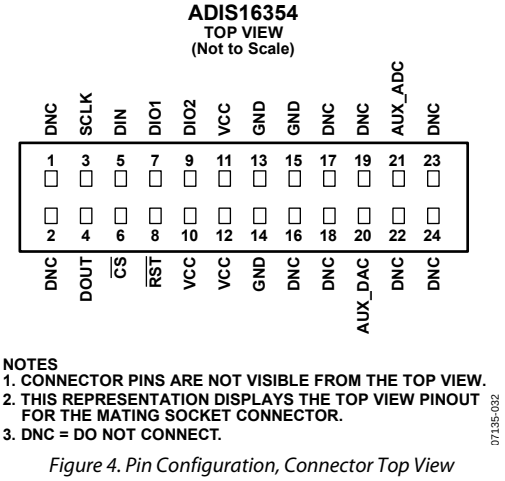

Figure 4. Pin Configuration, Connector Top View

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 2, 16 to 19, 22 to 24	DNC	N/A	Do Not Connect
3	SCLK	I	SPI Serial Clock
4	DOUT	O	SPI Data Output
5	DIN	I	SPI Data Input
6	$\overline{CS}$	I	SPI Chip Select
7	DIO1	I/O	Digital Input/Output
8	$\overline{RST}$	I	Reset
9	DIO2	I/O	Digital Input/Output
10 to 12	VCC	S	Power Supply
13 to 15	GND	S	Power Ground
20	AUX_DAC	O	Auxiliary, 12-Bit, DAC Output
21	AUX_ADC	I	Auxiliary, 12-Bit, ADC Input

[1] S = supply, O = output, I = input.

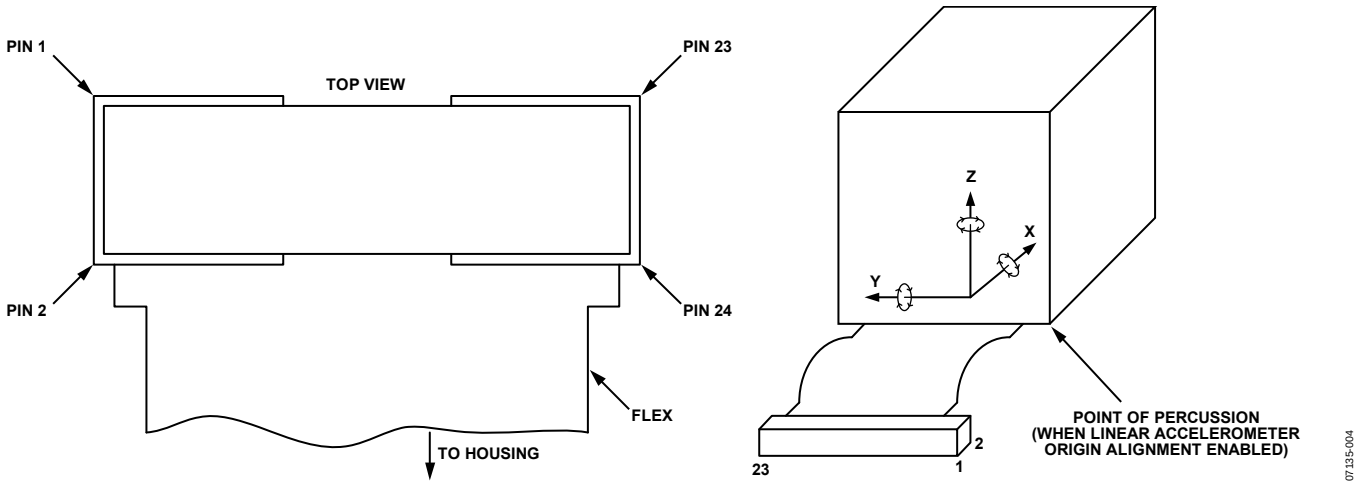

Figure 5. Pin Configuration, Connector Top View

TYPICAL PERFORMANCE CHARACTERISTICS

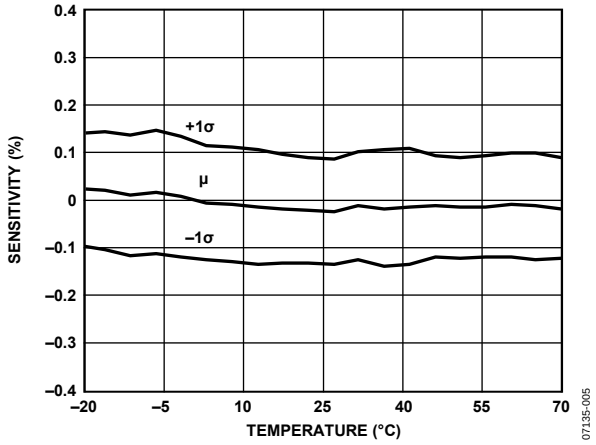

Figure 6. Gyroscope Sensitivity vs. Temperature

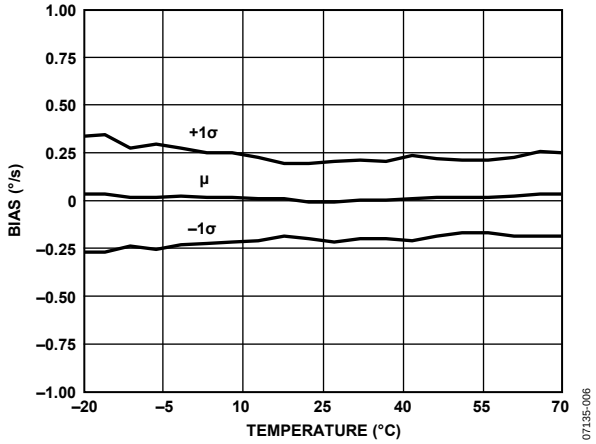

Figure 7. Gyroscope Bias vs. Temperature

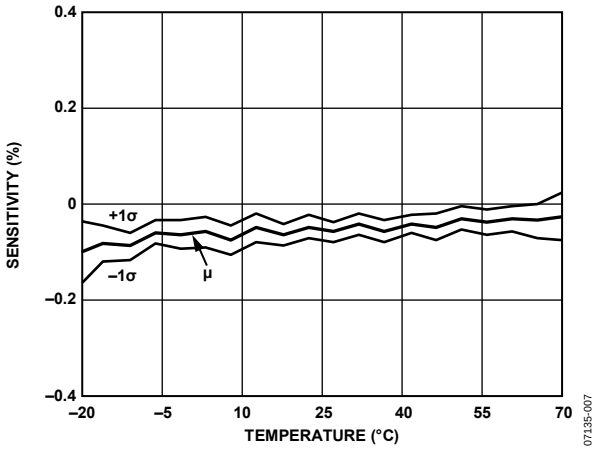

Figure 8. Accelerometer Sensitivity vs. Temperature

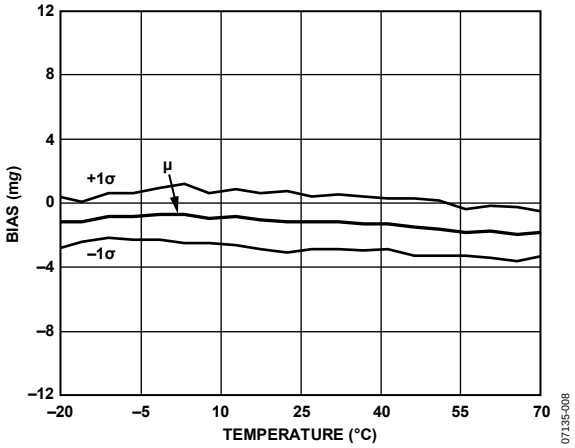

Figure 9. Accelerometer Bias vs. Temperature

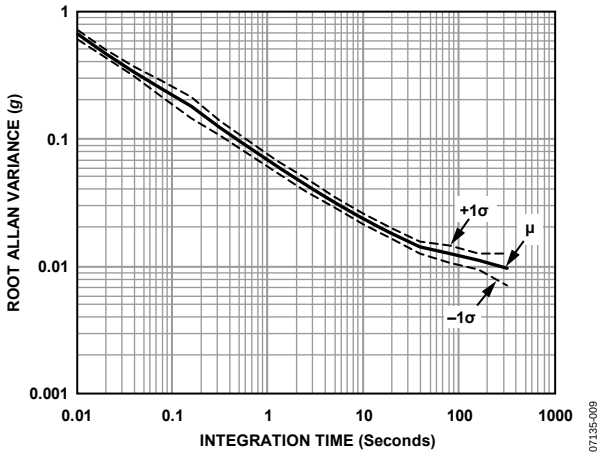

Figure 10. Gyroscope Root Allan Variance

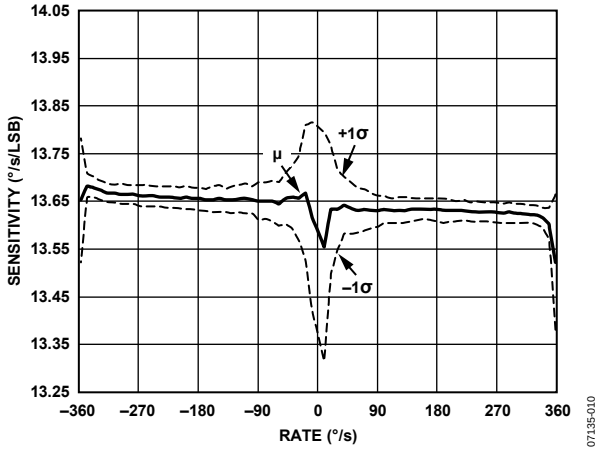

Figure 11. Gyroscope Linearity

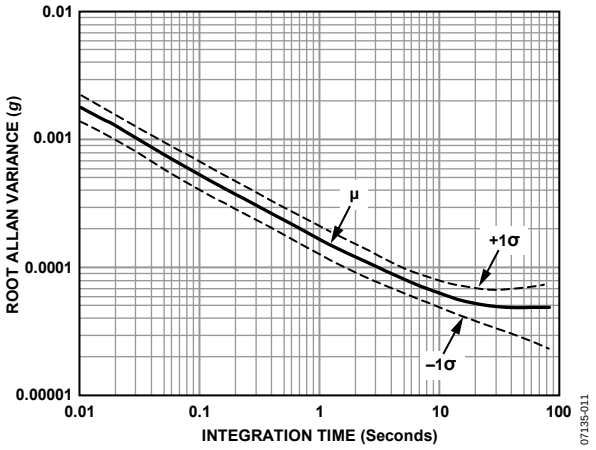

Figure 12. Accelerometer Root Allan Variance

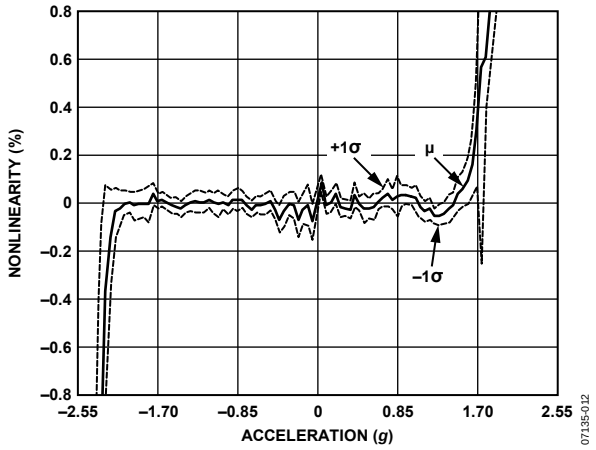

Figure 13. Accelerometer Nonlinearity

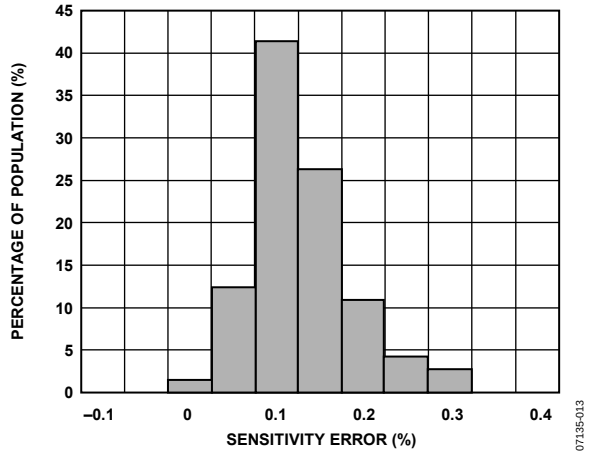

Figure 14. Gyroscope Sensitivity Error, 25°C

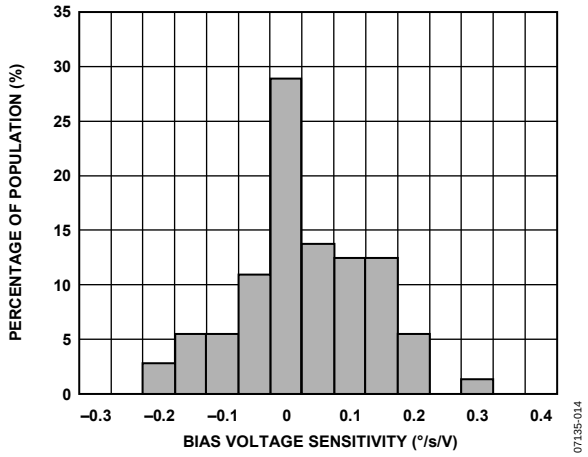

Figure 15. Gyroscope Bias Voltage Power Supply Sensitivity, 25°C

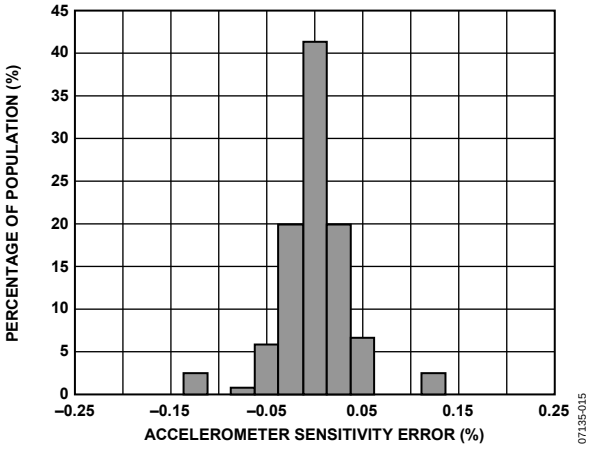

Figure 16. Accelerometer Sensitivity Error Distribution, 25°C

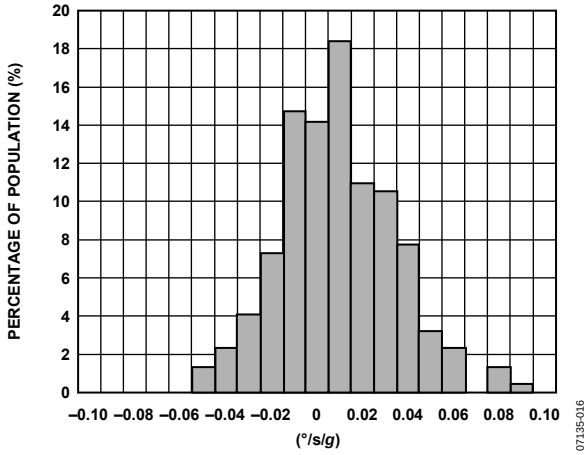

Figure 17. Gyroscope Bias Sensitivity to Linear Acceleration, 25°C

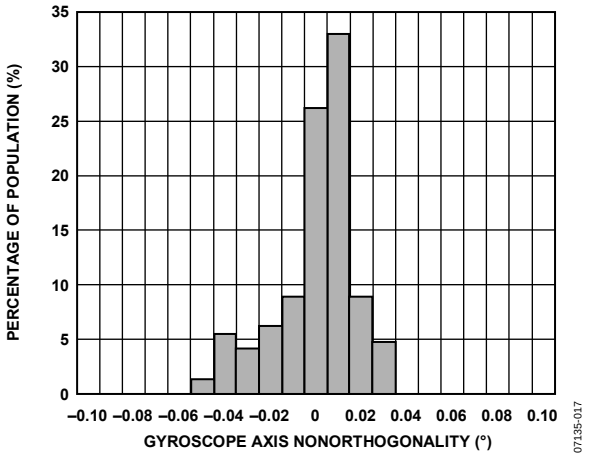

Figure 18. Gyroscope Alignment Distribution, 25°C

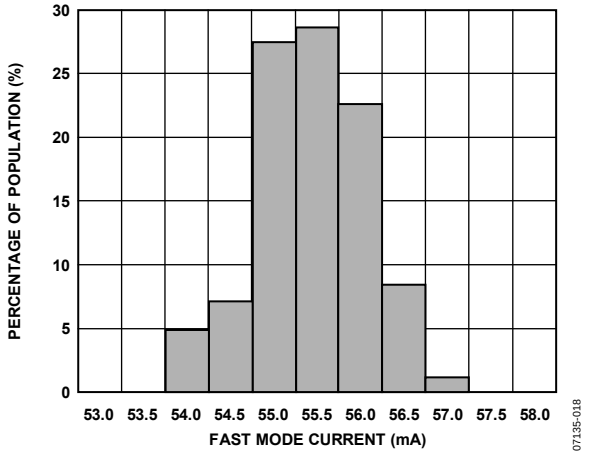

Figure 19. Fast Mode Power Supply Current Distribution, 25°C

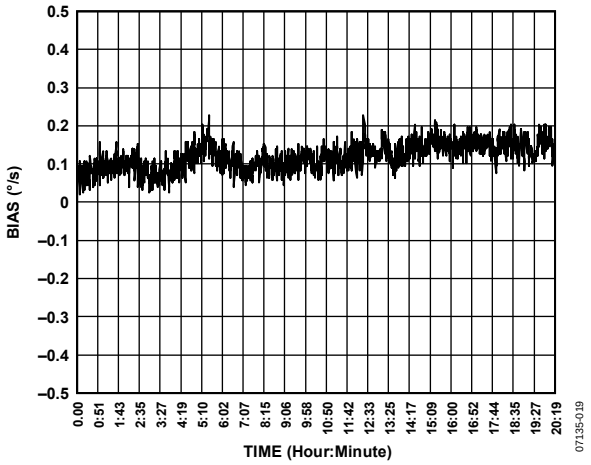

Figure 20. Long-Term Bias Stability, 25°C

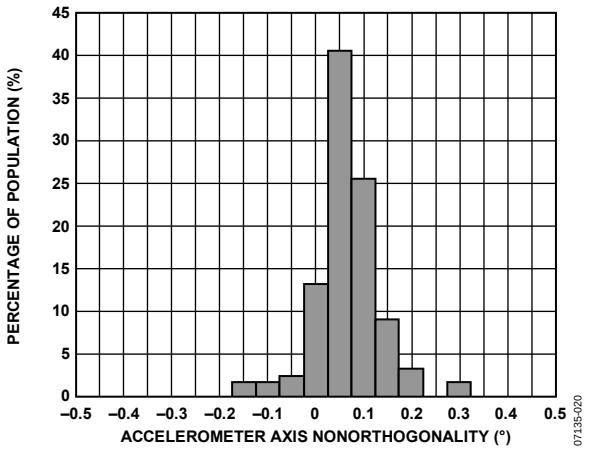

Figure 21. Accelerometer Alignment Distribution, 25°C

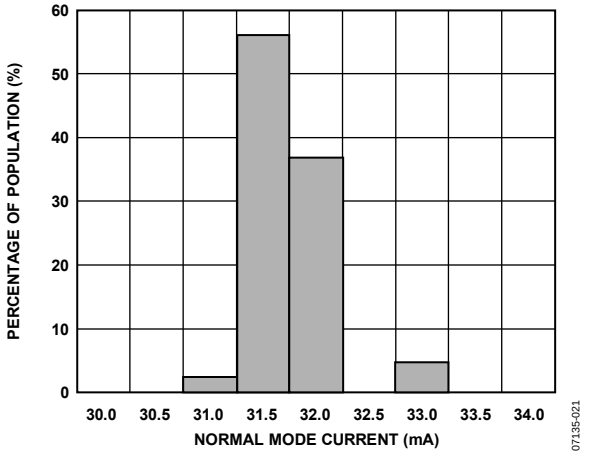

Figure 22. Normal Mode Power Supply Current Distribution, 25°C

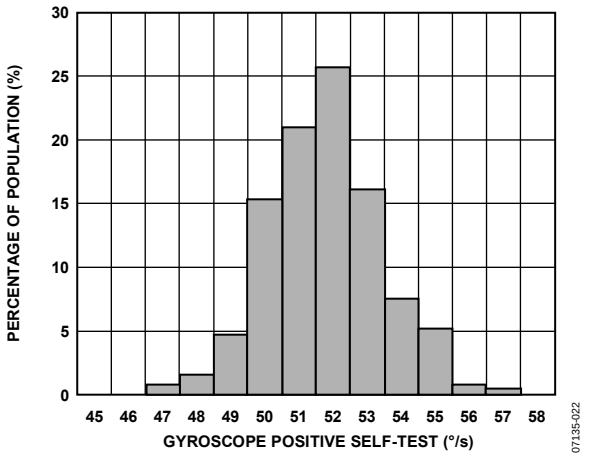

Figure 23. Gyroscope Positive Self-Test Distribution, 25°C

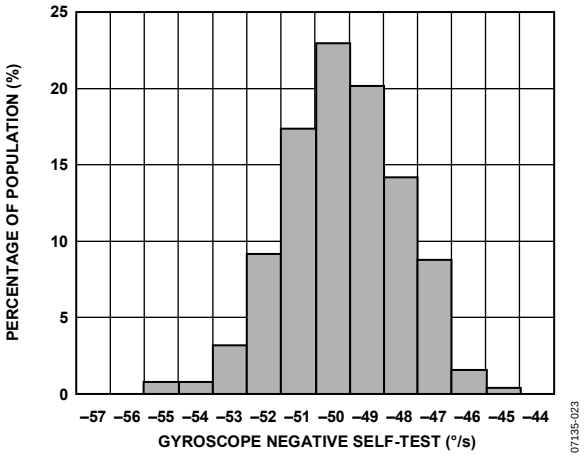

Figure 24. Gyroscope Negative Self-Test Distribution, 25°C

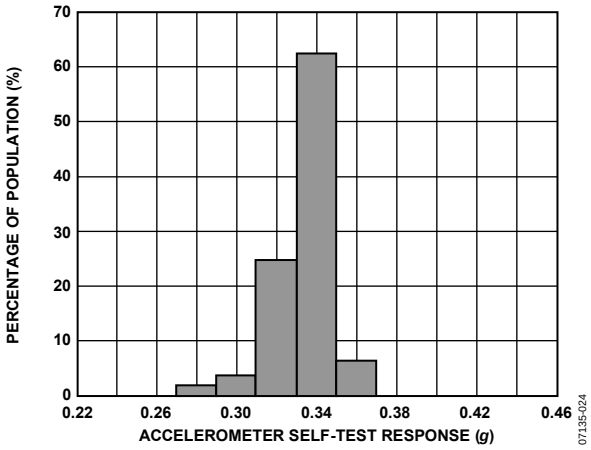

Figure 25. Accelerometer Self-Test Distribution, 25°C

THEORY OF OPERATION

OVERVIEW

The ADIS16354 integrates three orthogonal axes of gyroscope sensors with three orthogonal axes of accelerometer sensors, creating the basic six degrees of freedom (6DOF) in a single package. The accelerometers are oriented along the axis of rotation for each gyroscope. These six sensing elements are held together by a mechanical structure that provides tight force and motion coupling. Each sensor's output signal is sampled using an ADC, and then the digital data is fed into a proprietary digital processing circuit. The digital processing circuit applies the correction tables to each sensor's output, manages the input/output function using a simple register structure and serial interface, and provides many other features that simplify system-level designs.

GYROSCOPE SENSOR

The core MEMS angular rate sensor (gyroscope) used in the ADIS16354 operates on the principle of a resonator gyroscope. Two polysilicon sensing structures each contain a dither frame, which is electrostatically driven to resonance. This provides the velocity element required to produce a Coriolis force during rotation. At two of the outer extremes of each frame, orthogonal to the dither motion, are movable fingers, which are placed between fixed fingers to form a capacitive pickoff structure that senses Coriolis motion. The resulting signal is fed to a series of gain and demodulation stages that produce the electrical rate signal output.

ACCELEROMETER SENSOR

The core acceleration sensor used in the ADIS16354 is a surface micromachined polysilicon structure built on top of the silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide a resistance against acceleration forces. Deflection of the structure is measured using a differential capacitor that consists of independent fixed plates and central plates attached to the moving mass. Acceleration deflects the beam and unbalances the differential capacitor, resulting in a differential output that is fed to a series of gain and demodulation stages that produce the electrical rate signal output.

FACTORY CALIBRATION

The ADIS16354 provides a factory calibration that simplifies the process of integrating it into system-level designs. This calibration provides correction for initial sensor bias and sensitivity, power supply variation, temperature variation, axial alignment, and linear acceleration (gyroscopes). An extensive, three-dimensional characterization provides the basis for generating correction tables for each individual sensor.

CONTROL REGISTER STRUCTURE

The ADIS16354 provides configuration control to many critical operating parameters by using a dual-memory register structure. The volatile SRAM register locations control operation of the part while the nonvolatile flash memory locations preserve the configuration settings. Updating a register's contents only affects its SRAM location. Preserving the updates in its corresponding flash memory location requires initiation of the flash update command. This helps reduce the number of write cycles to the flash memory and consequently increases the endurance of the flash memory. During startup and reset-recovery sequences, the flash memory contents are automatically loaded into the SRAM register locations.

AUXILIARY ADC FUNCTION

The auxiliary ADC function integrates a standard 12-bit ADC into the ADIS16354 to digitize other system-level analog signals. The output of the ADC can be monitored through the AUX_ADC register, as defined in Table 7. The ADC is a 12-bit successive approximation converter. The output data is presented in straight binary format with the full-scale range extending from 0 V to 2.5 V.

Figure 26 shows the equivalent circuit of the analog input structure of the ADC. The input capacitor (C1) is typically 4 pF and can be attributed to parasitic package capacitance. The two diodes provide ESD protection for the analog input. Care must be taken to ensure that the analog input signals are never outside the range of −0.3 V to +3.5 V. Signals outside this range causes the diodes to become forward-biased and to start conducting. The diodes can handle 10 mA without causing irreversible damage. The resistor is a lumped component that represents the on resistance of the switches. The value of this resistance is typically 100 Ω. Capacitor C2 represents the ADC sampling capacitor and is typically 16 pF.

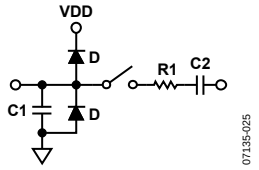

Figure 26. Equivalent Analog Input Circuit
Conversion Phase: Switch Open
Track Phase: Switch Closed

For ac applications, removing high frequency components from the analog input signal is recommended by the use of a low-pass filter on the analog input pin.

In applications where harmonic distortion and signal-to-noise ratios are critical, the analog input must be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This can necessitate the use of an input buffer amplifier. When no input amplifier is used to drive the analog input, the source impedance should be limited to values lower than 1 kΩ.

BASIC OPERATION

The ADIS16354 is designed for simple integration into system designs, requiring only a 5.0 V power supply and a 4-wire, industry-standard serial peripheral interface (SPI). All outputs and user-programmable functions are handled by a simple register structure. Each register is 16 bits in length and has its own unique bit map. The 16 bits in each register consist of an upper byte (D8 to D15) and a lower byte (D0 to D7), each with its own 6-bit address.

SERIAL PERIPHERAL INTERFACE (SPI)

The ADIS16354 serial peripheral interface (SPI) port includes four signals: chip select ($\overline{CS}$), serial clock (SCLK), data input (DIN), and data output (DOUT). The $\overline{CS}$ line enables the ADIS16354 SPI port and frames each SPI event. When this signal is high, the DOUT line is in a high impedance state and the signals on DIN and SCLK have no impact on operation. A complete data frame contains 16 clock cycles. Because the SPI port operates in full-duplex mode, it supports simultaneous, 16-bit receive (DIN) and transmit (DOUT) functions during the same data frame. This enables the user to configure the next read cycle, while, at the same time, receiving the data associated with the previous configuration.

Refer to Table 2, Figure 2, and Figure 3 for detailed information regarding timing and operation of the SPI port.

Writing to Registers

Figure 27 displays a typical data frame for writing a command to a control register. In this case, the first bit of the DIN sequence is a 1, followed by a 0, the 6-bit address of the target register, and the 8-bit data command. Because each write command covers a single byte of data, two data frames are required when writing the entire 16-bit space of a register.

Reading from Registers

Reading the contents of a register requires a modification to the sequence illustrated in Figure 27. In this case, the first two bits in the DIN sequence are 0, followed by the address of the register. Each register has two addresses (an upper address and a lower address), but either one can be used to access the entire 16 bits of data. The final eight bits of the DIN sequence are irrelevant and can be counted as don't cares during a read command. During the next data frame, the DOUT sequence contains the register's 16-bit data, as shown in Figure 28. Although a single read command requires two separate data frames, the full-duplex mode minimizes this overhead, requiring only one extra data frame when continuously sampling.

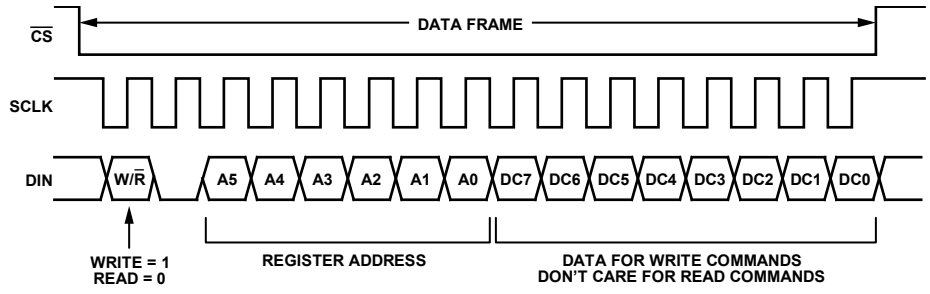

Figure 27. DIN Bit Sequence

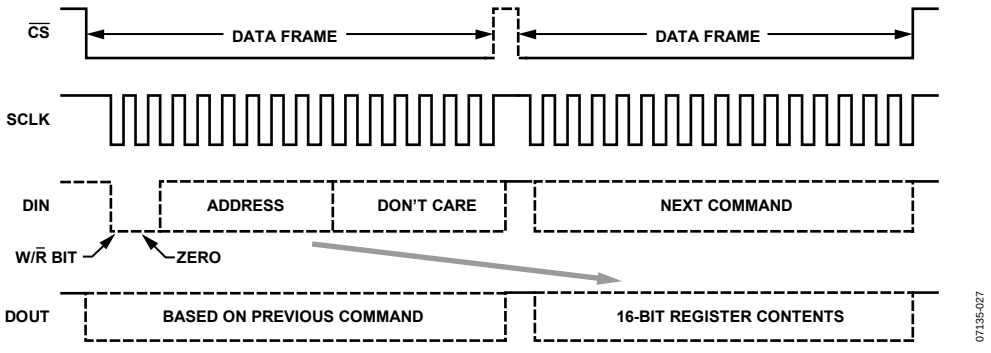

Figure 28. SPI Sequence for Read Commands

DATA OUTPUT REGISTER ACCESS

The ADIS16354 provides access to a full 6DOF set of calibrated motion measurements, power supply measurements, temperature measurements, and an auxiliary 12-bit ADC channel. This output data is continuously updated internally, regardless of user read rates. Table 6 describes the structure of all ADIS16354 output data registers.

Table 6. Output Register Bit Map

MSB							LSB
ND	EA	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

The MSB holds the new data (ND) indicator. When the output registers are updated with new data, the ND bit goes to a 1 state. After the output data is read, it returns to a 0 state.

The EA bit indicates a system error or an alarm condition that can result from various conditions, such as a power supply out-of-range condition. See the Status and Diagnostics section for more details. The output data is either 12 bits or 14 bits in length. For the 12-bit output data, Bit D13 and Bit D12 are assigned don't-care status.

The output data register map is located in Table 7 and provides all of the necessary details for accessing each register's data. Table 8 displays the output coding for the gyroscope output registers and Table 9 provides the output coding for the acceleration registers. Figure 29 provides an example of an SPI read cycle for the XGYRO_OUT register.

Table 7. Data Output Register Information

Name	Function	Addresses	Data Length	Data Format	Scale Factor (per LSB)
SUPPLY_OUT	Power supply measurement	0x03, 0x02	12 bits	Binary	1.8315 mV
XGYRO_OUT	X-axis gyroscope output measurement	0x05, 0x04	14 bits	Twos complement	0.07326 °/s[1]
YGYRO_OUT	Y-axis gyroscope output measurement	0x07, 0x06	14 bits	Twos complement	0.07326 °/s[1]
ZGYRO_OUT	Z-axis gyroscope output measurement	0x09, 0x08	14 bits	Twos complement	0.07326 °/s[1]
XACCL_OUT	X-axis acceleration output measurement	0x0B, 0x0A	14 bits	Twos complement	0.4672 m*g*
YACCL_OUT	Y-axis acceleration output measurement	0x0D, 0x0C	14 bits	Twos complement	0.4672 m*g*
ZACCL_OUT	Z-axis acceleration output measurement	0x0F, 0x0E	14 bits	Twos complement	0.4672 m*g*
XTEMP_OUT[2]	X-axis gyroscope sensor temperature measurement	0x11, 0x10	12 bits	Twos complement	0.1453°C
YTEMP_OUT[2]	Y-axis gyroscope sensor temperature measurement	0x13, 0x12	12 bits	Twos complement	0.1453°C
ZTEMP_OUT[2]	Z-axis gyroscope sensor temperature measurement	0x15, 0x14	12 bits	Twos complement	0.1453°C
AUX_ADC	Auxiliary analog input data	0x17, 0x16	12 bits	Binary	0.6105 mV

[1] Assumes that the scaling is set to 300°/s.
[2] Typical condition, 25°C = 0 LSB.

Table 8. Output Coding Example, XGYRO_OUT, YGYRO_OUT, and ZGYRO_OUT[1, 2]

Rate of Rotation					
±300°/s Range	±150°/s Range	±75°/s Range	Binary Output	Hexadecimal Output	Decimal
80°/s	40°/s	20°/s	00 0100 0100 0100	0x0444	1092
40°/s	20°/s	10°/s	00 0010 0010 0010	0x0222	546
0.07326°/s	0.03663°/s	0.018315°/s	00 0000 0000 0001	0x0001	1
0°/s	0°/s	0°/s	00 0000 0000 0000	0x0000	0
−0.07326°/s	−0.03663°/s	−0.018315°/s	11 1111 1111 1111	0x3FFF	−1
−40°/s	−20°/s	−10°/s	11 1101 1101 1110	0x3DDE	−546
−80°/s	−40°/s	−20°/s	11 1011 1011 1100	0x3BBC	−1092

[1] The binary output includes the data bits for the output registers, which, in this case, are D0 to D13, per Table 6. Bits assigned EA and ND are not included.
[2] Zero offset null performance is assumed.

Table 9. Output Coding Example, XACCL_OUT, YACCL_OUT, and ZACCL_OUT[1, 2]

Acceleration (*mg*)	Binary Output	Hexadecimal Output	Decimal
467.2	00 0011 1110 1000	0x03E8	1000
185.2	00 0001 1000 1101	0x018D	397
0.4672	00 0000 0000 0001	0x0001	1
0	00 0000 0000 0000	0x0000	0
−0.4672	11 1111 1111 1111	0x3FFF	−1
−185.2	11 1110 0111 0011	0x3E73	−397
−467.2	11 1100 0001 1000	0x3C18	−1000

[1] The binary output includes the data bits for the output registers, which, in this case, are D0 to D13, per Table 6. Bits assigned EA and ND are not included.
[2] Zero offset null performance is assumed.

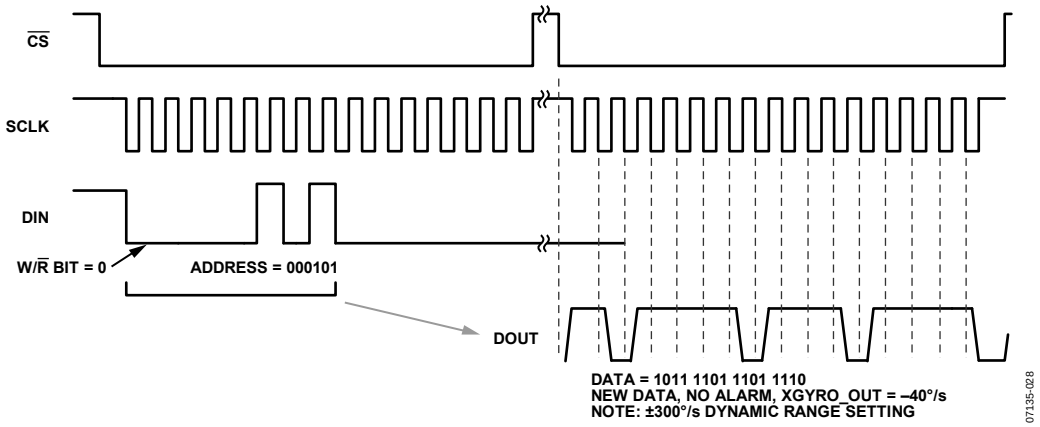

Figure 29. Example Read Cycle

PROGRAMMING AND CONTROL

CONTROL REGISTER OVERVIEW

The ADIS16354 offers many programmable features controlled by writing commands to the appropriate control registers using the SPI. The following sections describe these controls and specify each function, along with the corresponding register configuration. The features available for configuration in this register space are:

- Calibration
- Global commands
- Operational control
  - Sample rate
  - Power management
  - Digital filtering
  - Dynamic range
  - DAC output
  - Digital input/output
- Operational status and diagnostics
  - Self-test
  - Status conditions
  - Alarms

CONTROL REGISTER STRUCTURE

The ADIS16354 uses a temporary, RAM-based memory structure to facilitate the control registers listed in Table 10. The operational configuration is stored in a flash memory structure that automatically loads into the control registers during the start-up sequence. Each nonvolatile register has a corresponding flash memory location for storing the latest configuration contents. The contents of each nonvolatile register must be stored to flash manually.

Note that the contents of these registers are nonvolatile after they are stored to flash. The flash update command, available in the COMMAND register, provides this function. The ENDURANCE register provides a counter, which allows for reliability management against the flash memory's write cycle specification.

Table 10. Control Register Mapping

Register Name	Type	Volatility	Addresses	Bytes	Function	Reference Tables
ENDURANCE	R	Nonvolatile	0x00, 0x01	2	Flash memory write count	Table 30
	R	Volatile	0x02 to 0x17	22	Output data	Table 7
			0x18, 0x19	2	Reserved	
XGYRO_OFF	R/W	Nonvolatile	0x1A, 0x1B	2	X-axis gyroscope bias offset factor	Table 11, Table 12
YGYRO_OFF	R/W	Nonvolatile	0x1C, 0x1D	2	Y-axis gyroscope bias offset factor	Table 11, Table 12
ZGYRO_OFF	R/W	Nonvolatile	0x1E, 0x1F	2	Z-axis gyroscope bias offset factor	Table 11, Table 12
XACCL_OFF	R/W	Nonvolatile	0x20, 0x21	2	X-axis acceleration bias offset factor	Table 13, Table 14
YACCL_OFF	R/W	Nonvolatile	0x22, 0x23	2	Y-axis acceleration bias offset factor	Table 13, Table 14
ZACCL_OFF	R/W	Nonvolatile	0x24, 0x25	2	Z-axis acceleration bias offset factor	Table 13, Table 14
ALM_MAG1	R/W	Nonvolatile	0x26, 0x27	2	Alarm 1 amplitude threshold	Table 33, Table 34
ALM_MAG2	R/W	Nonvolatile	0x28, 0x29	2	Alarm 2 amplitude threshold	Table 33, Table 34
ALM_SMPL1	R/W	Nonvolatile	0x2A, 0x2B	2	Alarm 1 sample period	Table 35, Table 36
ALM_SMPL2	R/W	Nonvolatile	0x2C, 0x2D	2	Alarm 2 sample period	Table 35, Table 36
ALM_CTRL	R/W	Nonvolatile	0x2E, 0x2F	2	Alarm control	Table 37, Table 38
AUX_DAC	R/W	Volatile	0x30, 0x31	2	Auxiliary DAC data	Table 23, Table 24
GPIO_CTRL	R/W	Volatile	0x32, 0x33	2	Auxiliary digital input/output control	Table 25, Table 26
MSC_CTRL	R/W	Nonvolatile[1]	0x34, 0x35	2	Miscellaneous control	Table 28, Table 29
SMPL_PRD	R/W	Nonvolatile	0x36, 0x37	2	Internal sample period (rate) control	Table 17, Table 18
SENS/AVG	R/W	Nonvolatile	0x38, 0x39	2	Dynamic range/digital filter control	Table 21, Table 22
SLP_CNT	R/W	Volatile	0x3A, 0x3B	2	Sleep mode control	Table 19, Table 20
STATUS	R	Volatile	0x3C, 0x3D	2	System status	Table 31, Table 32
COMMAND	W	N/A	0x3E, 0x3F	2	System command	Table 15, Table 16

[1] The contents of the lower byte are nonvolatile; the contents of the upper byte are volatile.

CALIBRATION

For applications that require point-of-use calibration, the ADIS16354 provides bias correction registers for all six sensors. Table 11, Table 12, Table 13, and Table 14 provide the details required for using these registers to calibrate the ADIS16354 sensors.

Table 11. Gyroscope Bias Correction Registers

Register	Addresses	Common Parameters
XGYRO_OFF	0x1B, 0x1A	Default value = 0x0000
YGYRO_OFF	0x1D, 0x1C	Scale = 0.018315°/s per LSB
ZGYRO_OFF	0x1F, 0x1E	Twos complement, read/write

Table 12. Gyroscope Bias Correction Register Bits

Bits	Description
[15:13]	Not used
[12:0]	Data bits, typical adjustment range = ±75°

Table 13. Accelerometer Bias Correction Registers

Register	Addresses	Common Parameters
XACCL_OFF	0x21, 0x20	Default value = 0x0000
YACCL_OFF	0x23, 0x22	Scale = 0.4672 m*g* per LSB
ZACCL_OFF	0x25, 0x24	Twos complement, read/write

Table 14. Accelerometer Bias Correction Register Bits

Bits	Description
[15:12]	Not used
[11:0]	Data bits, typical adjustment range = ±947 m*g*

Manual Bias Calibration

Because each offset bias register has read/write access, the bias of each sensor is adjustable. For example, if an output offset of 0.18°/s is observed in the Z-axis gyroscope, the ZGYRO_OFF register provides the calibration factor necessary to improve the accuracy. Using its sensitivity of 0.018315°/s, an adjustment of −10 LSBs is required. The twos complement, hexadecimal code of −10 LSBs is 0x1FF6.

To implement this calibration factor, use the following pseudocode:

Write 0xF6 to Address 0x1E, then write 0x1F to Address 0x1F

This step reduces the 0.18°/s error term to 0.00315°/s.

Automatic Bias Null Calibration

The ADIS16354 provides a single-command, automatic bias calibration for all three gyroscope sensors. The COMMAND register provides this function, which measures all three gyroscope output registers, then loads the three bias correction registers with values that return their outputs to zero (null). A single register write command starts this process (see Table 16).

Write 0x01 to Address 0x3E

Precision Automatic Bias Null Calibration

The ADIS16354 also provides a single-command function that incorporates the optimal averaging time for generating the appropriate bias correction factors for all three gyroscope sensors. This command requires approximately 30 seconds to complete. For optimal calibration accuracy, the device should be stable (no motion) for this entire period. Once it has started, a reset command is required to stop it prematurely, if required. The following sequence starts this calibration option (see Table 16):

Write 0x10 to Address 0x3E

Restoring Factory Calibration

The ADIS16354 factory calibration can be restored by returning the contents of each bias correction register to their default value of zero. This command also flushes all of the data from the digital filter taps. To accomplish this function for all six sensor signal paths (see Table 16),

Write 0x02 to Address 0x3E

Linear Acceleration Bias Compensation (Gyroscopes)

The ADIS16354 provides compensation for acceleration influences on the gyroscopes' bias behavior, using the MSC_CTRL register.

Set Bit 7 of Address 0x34 to 1 (see Table 29)

Linear Acceleration Origin Alignment

The ADIS16354 provides origin alignment for the accelerometers to the point of percussion (see Figure 5), using the MSC_CTRL register.

Set Bit 6 of Address 0x34 to a 1 (see Table 29)

GLOBAL COMMANDS

The ADIS16354 provides global commands for common operations such as calibration, flash update, auxiliary DAC latch, and software reset. Each global command has a unique control bit assigned to it in the COMMAND register and is initiated by writing a 1 to its assigned bit.

The flash update command writes the contents of each non-volatile register into flash memory for storage. This process takes approximately 100 ms and requires the power supply voltage to be within specification for the duration of the event. Note that this operation also automatically follows the autonull, precision autonull, and factory reset commands. After waiting the appropriate time for the flash update to complete, verify successful completion by reading the STATUS register (flash update error = 0, if successful).

The DAC latch command loads the contents of AUX_DAC into the DAC latches, which control the actual output level. This overcomes the challenge of discontinuous outputs that would otherwise be associated with two separate write cycles for upper and lower bytes. Finally, the software reset command sends the ADIS16354 digital processor into a restart sequence, effectively accomplishing the same tasks as the $\overline{\text{RST}}$ line.

Table 15. COMMAND Register Definition

Address	Default	Format	Access
0x3F, 0x3E	N/A	N/A	Write only

Table 16. COMMAND Bit Descriptions

Bits	Description
[15:8]	Not used
[7]	Software reset command
[6:5]	Not used
[4]	Precision autonull command
[3]	Flash update command
[2]	Auxiliary DAC data latch
[1]	Factory calibration restore command
[0]	Autonull command

OPERATIONAL CONTROL

Internal Sample Rate

The internal sample rate defines how often data output variables are updated, independent of the rate at which they are read out on the SPI port. The SMPL_PRD register controls the ADIS16354 internal sample rate and has two parts: a time base and a multiplier. The sample period can be calculated using the following equation:

$$T_S = T_B \times (N_S + 1)$$

where:
T_S is the sample period.
T_B is the time base.
N_S is the multiplier.

The default value is the minimum register setting, 0x01, which corresponds to the maximum sample rate of 819.2 samples per second. The contents of this register are nonvolatile.

Table 17. SMPL_PRD Register Definition

Address	Default	Format	Access
0x37, 0x36	0x0001	N/A	R/W

Table 18. SMPL_PRD Bit Descriptions

Bits	Description
[15:8]	Not used
[7]	Time base, 0 = 0.61035 ms, 1 = 18.921 ms
[6:0]	Multiplier (add 1 before multiplying by the time base)

An example calculation of the sample period for the device is

If *SMPL_PRD* = 0x0007, Bits [7:0] = 00000111

Bit 7 = 0, so T_B = 0.61035 ms

Bits [6:0] = 0000111 = 7 = N_S

$T_S = T_B \times (N_S + 1)$ = = 0.61035 ms × (7 + 1) = 4.8828 ms

$f_S = 1/T_S$ = 204.8 SPS

The sample rate setting has a direct impact on the SPI data rate capability. For SMPL_PRD settings ≤ 0x09 (fast mode), the SPI SCLK can run at a rate up to 2.0 MHz. For SMPL_PRD settings > 0x09 (normal mode), the SPI SCLK can run at a rate up to 300 kHz.

The sample rate setting also affects the power dissipation. The normal mode power dissipation is approximately 67% less than the fast mode power dissipation. The two different modes of operation offer a system-level trade-off between performance (sample rate, serial transfer rate) and power dissipation.

Power Management

The ADIS16354 offers two different shutdown options: programmable shutdown period and indefinite shutdown. Raising Bit 8 activates the indefinite shutdown period. Writing the appropriate sleep time to the lower byte of the SLP_CNT register shuts the device down for the specified time. The following example illustrates this relationship:

Bits [7:0] = 00000110 = 6 codes = 3 seconds

At the completion of the programmed duration, the ADIS16354 returns to normal operation. If measurements are required before sleep period completion or if it is necessary to end the indefinite shutdown, the ADIS16354 can be awakened by pulling the $\overline{CS}$ line down to a 0 state, then returning it to a 1 state. Otherwise, the $\overline{CS}$ line must be kept in a 1 state to maintain sleep mode.

When writing a sleep time to the SLP_CNT register, the $\overline{CS}$ signal must be raised to a 1 before the command takes effect. Power cycle recovery will be a normal startup, because the contents of SLP_CNT are volatile.

Table 19. SLP_CNT Register Definition

Address	Scale[1]	Default	Format	Access
0x3B, 0x3A	0.5 sec	0x0000	Binary	R/W

[1] Scale is the weight of each LSB in the lower byte of this register.

Table 20. SLP_CNT Bit Descriptions

Bits	Description
[15:9]	Not used
[8]	Indefinite shutdown control bit
[7:0]	Data bits, 0.5 sec/LSB

Digital Filtering

Each sensor's signal conditioning circuit has an analog bandwidth of approximately 350 Hz. The ADIS16354 provides a Bartlett Window FIR filter for additional noise reduction on all of the output data registers. The SENS/AVG register controls the number of taps in power-of-two step sizes, from zero to six

Filter setup requires one simple step: write the appropriate M factor to the assigned bits in the SENS/AVG register. The bit assignments are listed in Table 22. The frequency response relationship for this filter is:

$$H_B(f) = H_A^2(f) \quad H_A(f) = \frac{\sin(\pi \times N \times f \times t_s)}{N \times \sin(\pi \times f \times t_s)}$$

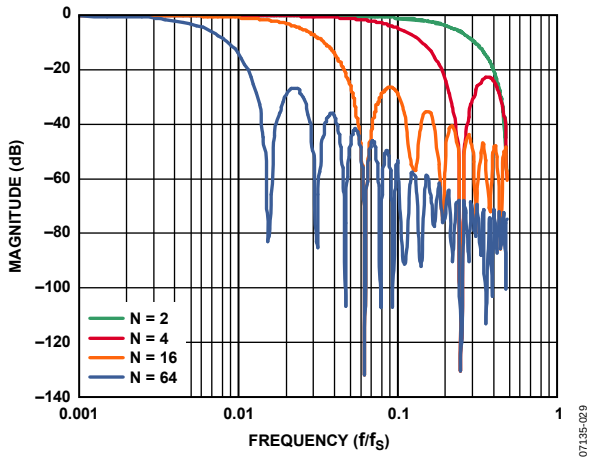

Figure 30. Bartlett Window FIR Frequency Response

Dynamic Range

The ADIS16354 provides three dynamic range settings: ±75°/s, ±150°/s, and ±300°/s. The lower dynamic range settings (75, 150) limit the minimum filter tap sizes in order to maintain the resolution as the measurement range decreases. The recommended order for programming the SENS/AVG register is upper byte (sensitivity), followed by lower byte (filtering). The contents of the SENS/AVG register are nonvolatile.

Table 21. SENS/AVG Register Definition

Address	Default	Format	Access
0x39, 0x38	0x0402	N/A	R/W

Table 22. SENS/AVG Bit Descriptions

Bits	Value	Description
[15:11]		Not used
[10:8]		Measurement range (sensitivity) selection
	100	300°/s (default condition)
	010	150°/s, filter taps ≥ 4 (Bits [2:0] ≥ 0x02)
	001	75°/s, filter taps ≥ 16 (Bits [2:0] ≥ 0x04)
[7:3]		Not used
[2:0]		Filter tap setting, number of taps, $N = 2^M$, for example, 011, $N = 2^3 = 8$ taps

Auxiliary DAC

The auxiliary DAC provides a 12-bit level adjustment function. The AUX_DAC register controls the operation of this feature. It offers a rail-to-rail buffered output that has a range of 0 V to 2.5 V. The DAC can drive its output to within 5 mV of the ground reference when it is not sinking current. As the output approaches ground, the linearity begins to degrade (100 LSB beginning point). As the sink current increases, the nonlinear range increases. The DAC output latch function, contained in the COMMAND register, provides continuous operation while writing each byte of this register. The contents of this register are volatile, which means that the desired output level must be set after every reset and power cycle event.

Table 23. AUX_DAC Register Definition

Address	Default	Format	Access
0x31, 0x30	0x0000	Binary	R/W

Table 24. AUX_DAC Bit Descriptions

Bits	Description
[15:12]	Not used
[11:0]	Data bits 0x0000 = 0 V output, 0x0FFF = 2.5 V output

See the COMMAND register for use of the DAC latch command, which enables the DAC to update its output based on the value in the AUX-DAC register.

General-Purpose Input/Output

The ADIS16354 provides two general-purpose pins that enable digital input/output control using the SPI. The GPIO_CTRL control register establishes the configuration of these pins and handles the SPI-to-pin controls. Each pin provides the flexibility of both input (read) and output (write) operations.

For example, writing 0x0202 to this register establishes Line 2 as an output and sets its level as a 1. Writing 0x0000 to this register establishes both lines as inputs, and their status can be read through Bit 8 and Bit 9 of this register.

The digital input/output lines are also available for data-ready and alarm/error indications. In the event of conflict, the following priority structure governs the digital input/output configuration:

1. MSC_CTRL
2. ALM_CTRL
3. GPIO_CTRL

Table 25. GPIO_CTRL Register Definition

Address	Default	Format	Access
0x33, 0x32	0x0000	N/A	R/W

Table 26. GPIO_CTRL Bit Descriptions

Bits	Description
[15:10]	Not used
[9]	General-purpose input/output Line 2 data level 1 = high, 0 = low
[8]	General-purpose input/output Line 1 data level 1 = high, 0 = low
[7:2]	Not used
[1]	General-purpose input/output Line 2, data direction control 1 = output, 0 = input
[0]	General-purpose input/output Line 1, data direction control 1 = output, 0 = input

The contents of the GPIO_CTRL register are volatile.

STATUS AND DIAGNOSTICS

The ADIS16354 provides a number of status and diagnostic functions. Table 27 provides a summary of these functions, along with their appropriate control registers.

Table 27. Status and Diagnostic Functions

Function	Register
Data-ready input/output indicator	MSC_CTRL
Self-test, mechanical check for sensor element	MSC_CTRL
Status: Check for predefined error conditions	STATUS
Flash memory endurance	ENDURANCE
Alarms: Configure and check for user-specific conditions	ALM_MAG1 ALM_MAG2 ALM_SMPL1 ALM_SMPL2 ALM_CTRL

Data-Ready Input/Output Indicator

The data-ready function provides an indication of updated output data. The MSC_CTRL register allows the user to configure either of the general-purpose input/output pins (DIO1 or DIO2) as a data-ready indicator signal.

Table 28. MSC_CTRL Register Definition

Address	Default	Format	Access
0x35, 0x34	0x0000	N/A	R/W

Table 29. MSC_CTRL Bit Descriptions

Bits	Description
[15:11]	Not used
[10]	Internal self-test enable (clears on completion) 1 = enabled, 0 = disabled
[9]	Manual self-test, negative stimulus 1 = enabled, 0 = disabled
[8]	Manual self-test, positive stimulus 1 = enabled, 0 = disabled
[7]	Linear acceleration bias compensation for gyroscopes 1 = enabled, 0 = disabled
[6]	Linear accelerometer origin alignment 1 = enabled, 0 = disabled
[5:3]	Not used
[2]	Data-ready enable 1 = enabled, 0 = disabled
[1]	Data-ready polarity 1 = active high, 0 = active low
[0]	Data-ready line select 1 = DIO2, 0 = DIO1

Self-Test

The MSC_CTRL register also provides a self-test function, which verifies the MEMS sensor's mechanical integrity. There are two different self-test options: internal self-test and external self-test.

The internal test provides a simple, two-step process for checking the MEMS sensor.

1. Start the process by writing a 1 to Bit 10 in the MSC_CTRL register.
2. Check the result by reading Bit 5 of the STATUS register.

If a failure is indicated, then Bits [10:15] of the STATUS register indicate which of the six sensors it is associated with.

The entire cycle takes approximately 35 ms and the output data is not available during this time. The external self-test is a static condition that can be enabled and disabled. In this test, both positive and negative gyroscope MEMS sensor movements are available. For the accelerometers, only positive MEMS sensor movement is available.

After writing to the appropriate control bit, the output registers reflect the changes after a delay that reflects the response time associated with the sensor/signal conditioning circuit. For example, the standard 350 Hz bandwidth reflects an exponential response with a time constant of 0.45 ms. Note that the digital filtering impacts this delay as well. The appropriate bit definitions for self-test are listed in Table 28 and Table 29.

Flash Memory Endurance

The ENDURANCE register maintains a running count of writes to the flash memory. It provides up to 32,768 counts. Note that if this count is exceeded, the register wraps around and goes back to zero, before beginning to increment again.

Table 30. ENDURANCE Register Definition

Address	Default	Format	Access
0x01, 0x00	N/A	Binary	Read only

Status Conditions

The STATUS register contains the following error condition flags: alarm conditions, self-test status, overrange, SPI communication failure, control register update failure, and power supply range failure. See Table 31 and Table 32 for the appropriate register access and bit assignment for each flag.

The bits assigned for checking power supply range and sensor overrange automatically reset to zero when the error condition no longer exists. The remaining error flag bits in the STATUS register require a read to return them to zero. Note that a STATUS register read clears all of the bits to zero. If any error conditions remain, the bits revert to 1 during the next internal output register update cycle.

Table 31. STATUS Register Definition

Address	Default	Format	Access
0x3D, 0x3C	0x0000	N/A	Read only

Table 32. STATUS Bit Descriptions

Bits	Description
[15]	Z-axis accelerometer self-diagnostic error flag 1 = failure, 0 = passing
[14]	Y-axis accelerometer self-diagnostic error flag 1 = failure, 0 = passing
[13]	X-axis accelerometer self-diagnostic error flag 1 = failure, 0 = passing
[12]	Z-axis gyroscope self-diagnostic error flag 1 = failure, 0 = passing
[11]	Y-axis gyroscope self-diagnostic error flag 1 = failure, 0 = passing
[10]	X-axis gyroscope self-diagnostic error flag 1 = failure, 0 = passing
[9]	Alarm 2 status 1 = active, 0 = inactive
[8]	Alarm 1 status 1 = active, 0 = inactive
[7:6]	Not used
[5]	Self-test diagnostic error flag 1 = error condition, 0 = normal operation
[4]	Sensor overrange (any of the six) 1 = error condition, 0 = normal operation
[3]	SPI communications failure 1 = error condition, 0 = normal operation
[2]	Control register update failed 1 = error condition, 0 = normal operation
[1]	Power supply in range above 5.25 V 1 = above 5.25 V, 0 = below 5.25 V (normal)
[0]	Power supply below 4.75 V 1 = below 4.75 V, 0 = above 4.75 V (normal)

Alarms

The ADIS16354 provides two independent alarm options for event detection. Event detections occur when output register data meets the configured conditions. Configuration options include the following:

- All output data registers are available for monitoring as the source data.
- The source data can be filtered or unfiltered.
- Comparisons can be static or dynamic (rate of change).
- The threshold levels and times are configurable.
- Comparison can be greater than or less than.

The ALM_MAG1 register and the ALM_MAG2 register both establish the threshold level for detecting events. These registers take on the format of the source data and provide a bit for establishing the greater than/less than comparison direction.

When making dynamic comparisons, the ALM_SMPL1 register and the ALM_SMPL2 register establish the number of averages taken for the source data as a reference for comparison. In this configuration, each subsequent source data sample is subtracted from the previous one, establishing an instantaneous delta. The ALM_CTRL register controls the source data selection, static/dynamic selection, filtering selection, and digital input/output usage for the alarms.

The rate of change calculation is

$$Y_C = \frac{1}{N_{DS}} \sum_{n=1}^{N_{DS}} y(n+1) - y(n)$$

Rate of change alarm is determined by comparing Y_C with M_C according to ALM_MAG1/ALM_MAG2 settings.

where:
N_{DS} is the number of samples in ALM_SMPL1 and ALM_SMPL2.
$y(n)$ is the sampled output data.
M_C is the magnitude for comparison in ALM_MAG1 and ALM_MAG2.
Y_C is the factor to compare with M_C.

Table 33. ALM_MAG1 and ALM_MAG2 Register Definitions

Register	Addresses	Default	Format	Access
ALM_MAG1	0x27, 0x26	0x0000	N/A	R/W
ALM_MAG2	0x29, 0x28	0x0000	N/A	R/W

Table 34. ALM_MAG1 and ALM_MAG2 Bit Descriptions

Bits	Description
[15]	Comparison polarity: 1 = greater than, 0 = less than
[14]	Not used
[13:0]	Data bits, format matches source data format

Table 35. ALM_SMPL1 and ALM_SMPL2 Register Definitions

Registers	Addresses	Default	Format	Access
ALM_SMPL1	0x2B, 0x2A	0x0000	Binary	R/W
ALM_SMPL2	0x2D, 0x2C	0x0000	Binary	R/W

Table 36. ALM_SMPL1 and ALM_SMPL2 Bit Descriptions

Bits	Description
[15:8]	Not used
[7:0]	Data bits

Table 37. ALM_CTRL Register Definition

Addresses	Default	Format	Access
0x2F, 0x2E	0x0000	N/A	R/W

Table 38. ALM_CTRL Bit Descriptions

Bits	Value	Description
[15:12]		Alarm 2 source selection
	0000	Disable
	0001	Power supply output
	0010	X-axis gyroscope output
	0011	Y-axis gyroscope output
	0100	Z-axis gyroscope output
	0101	X-axis accelerometer output
	0110	Y-axis accelerometer output
	0111	Z-axis accelerometer output
	1000	X-axis gyroscope temperature output
	1001	Y-axis gyroscope temperature output
	1010	Z-axis gyroscope temperature output
	1011	Auxiliary ADC input
[11:8]		Alarm 1 source selection (same as Alarm 2)
[7]		Rate of change (ROC) enable for Alarm 2 1 = rate of change, 0 = static level
[6]		Rate of change (ROC) enable for Alarm 1 1 = rate of change, 0 = static level
[5]		Not used
[4]		Comparison data filter setting 1 = filtered data, 0 = unfiltered data
[3]		Not used
[2]		Alarm output enable 1 = enabled, 0 = disabled
[1]		Alarm output polarity 1 = active high, 0 = active low
[0]		Alarm output line select 1 = DIO2, 0 = DIO1

APPLICATIONS INFORMATION

INSTALLATION GUIDELINES

Installing the ADIS16354 requires two steps: mechanical attachment of the body, followed by the electrical connection. This device is designed for postsolder reflow installation. It is not designed to survive the temperatures associated with normal solder reflow processes.

Mechanical Attachment

The ADIS16354 is designed for simple mechanical attachment. The open mounting tabs on each side of the body provide enough room for 2 mm (or 2-56) machine screws. Note that 316 stainless steel and aluminum screws are available for use in this attachment.

When planning the installation process, the primary trade-off to consider is the attachment strength advantage of stainless steel against the nonmagnetic properties of aluminum for systems that employ magnetic sensors. In addition, the ADIS16354 provides alignment pinholes, one on each side.

Location accuracy of the mating holes may force the use of a smaller pin. Figure 31 provides a graphical display of the mechanical attachment, and Figure 32 provides a recommendation for the physical layout of all the holes required for attaching the ADIS16354.

Electrical Connections

The electrical interface for the ADIS16354 is a single connector, which is attached to a flexible circuit extension.

One option for mating connectors can be found in Samtec's CLM family. In this case, the part number starts with CLM-112-02. The flexible circuit has stress relief points to absorb environmental stresses, such as temperature cycling and vibration. Figure 32 provides the alignment hole locations for designs that employ the suggested connector mate. This connection is held by friction only. This figure assumes that the ADIS16354 and mating connector are on the same surface (plane).

Proper Removal

The flexible circuit interface can tear under excessive force conditions. An example of excessive force is attempting to break the electrical connection by pulling on the body of the ADIS16354, placing all of the stress on the flexible circuit.

The electrical connector must be broken by an appropriate tool, which is designed to apply even pressure to each side of the rigid part of the flex cable. The recommended extraction sequence is to break the mate between the electrical interface, and then to remove the mechanical attachment hardware.

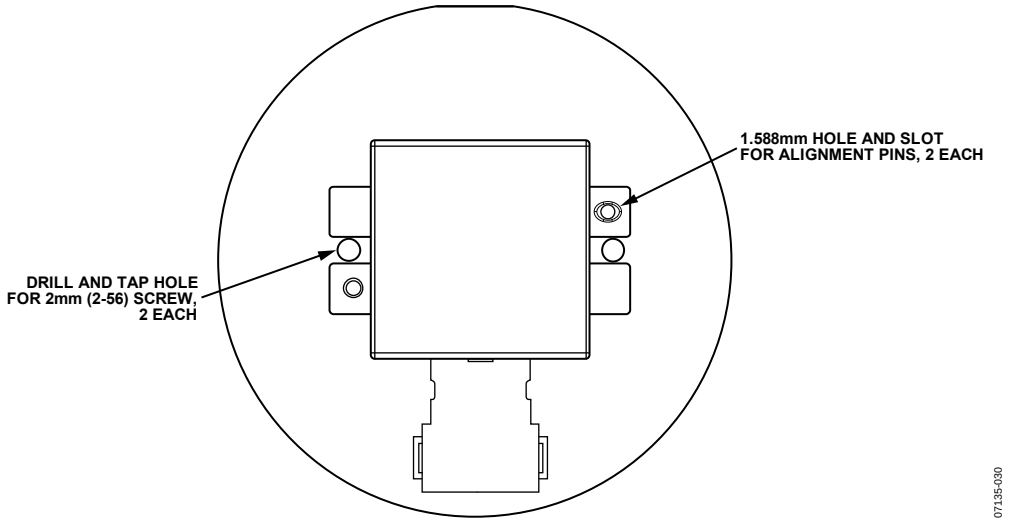

Figure 31. Mechanical Attachment

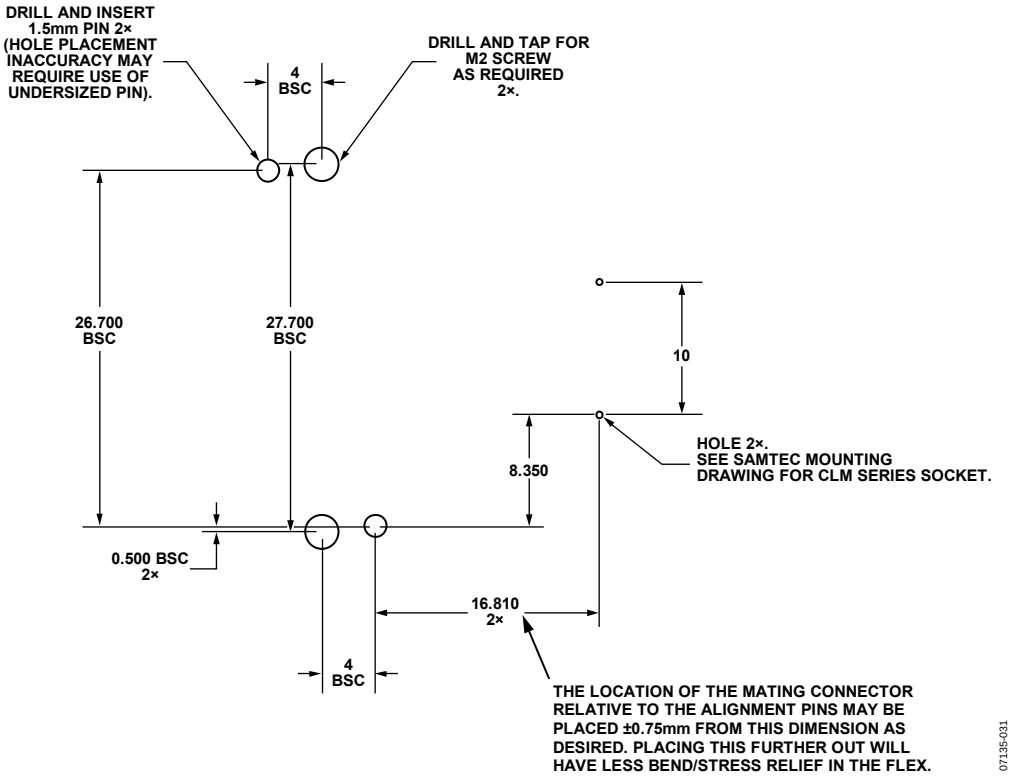

Figure 32. Hole Locations

OUTLINE DIMENSIONS

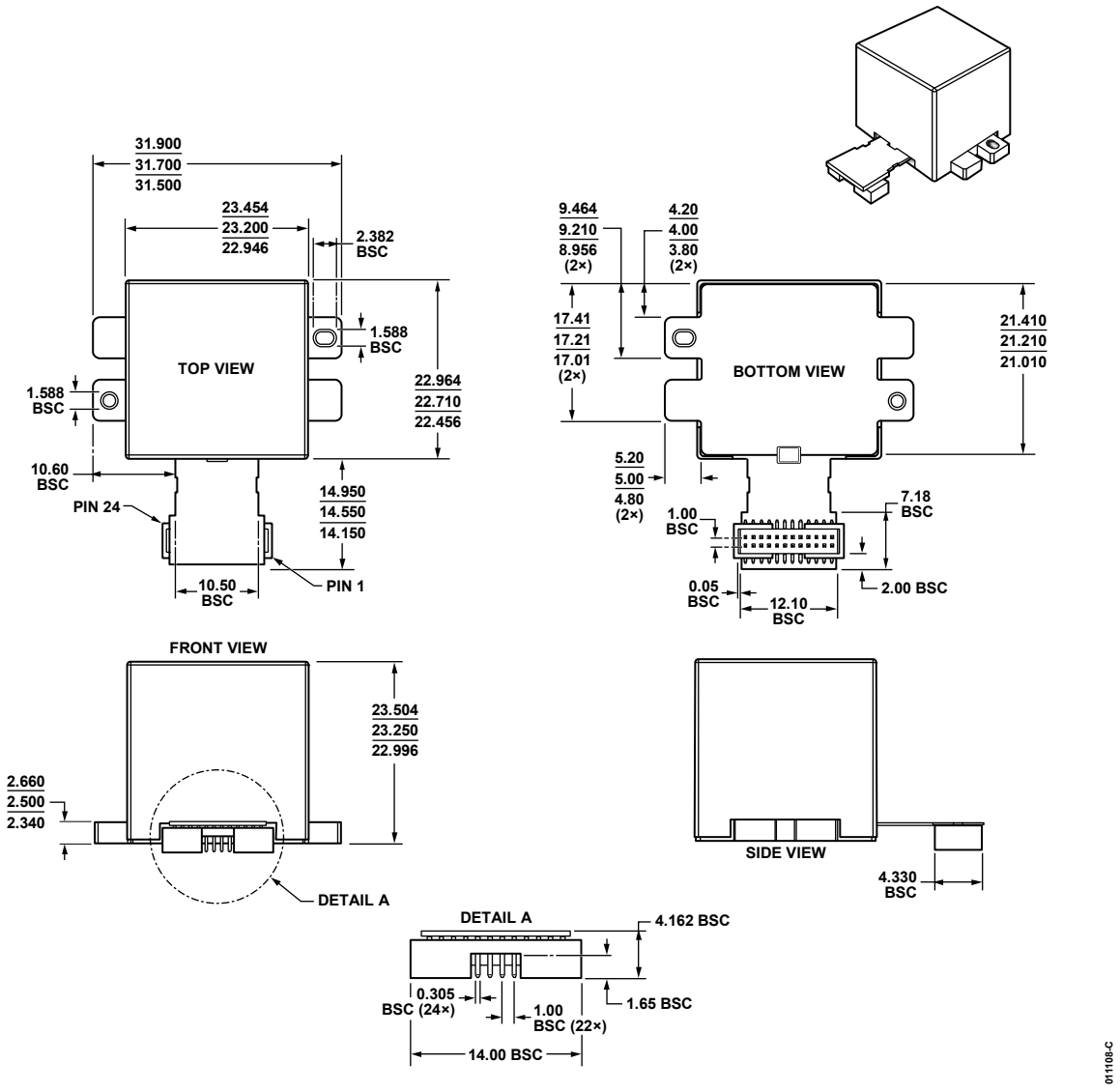

Figure 33. 24-Lead Module with Connector Interface
(ML-24-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADIS16354AMLZ[1]	−40°C to +85°C	24-Lead Module with Connector Interface	ML-24-2
ADIS16354/PCBZ[1]		Interface Board	
ADIS16354/EVALZ[1]		PC Evaluation System	

[1] Z = RoHS Compliant Part.

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