Description

The SK4429 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

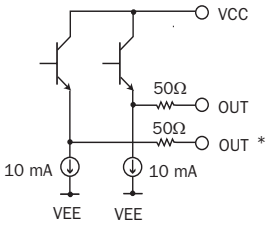
The SK4429 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

- Point to point, double terminated, timing critical lines
- Point to point, series terminated, timing critical lines

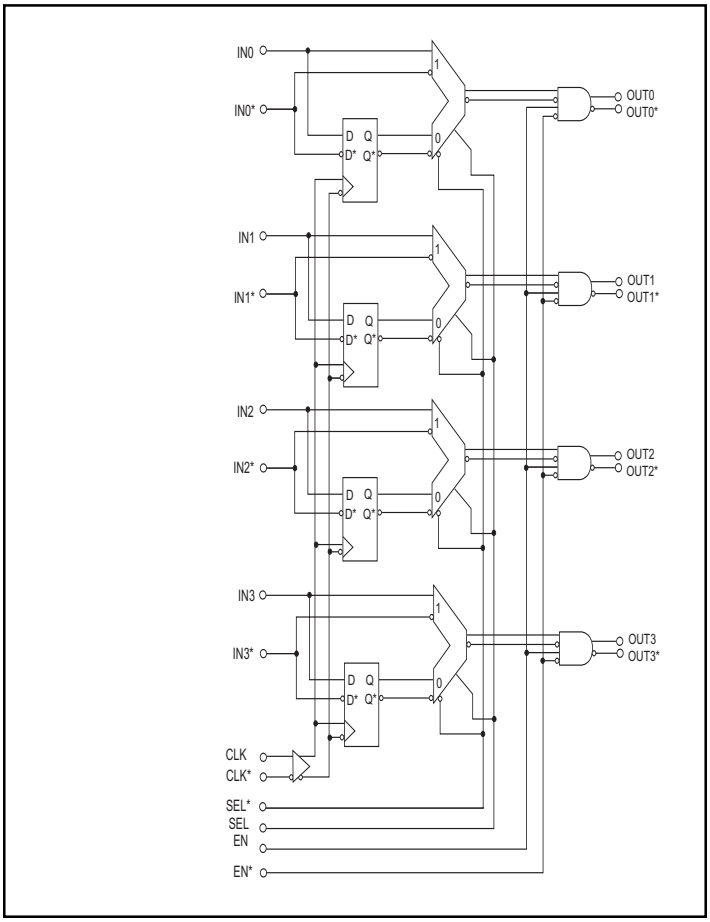
Features

- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to PECL Translation
- Available in 32 lead, 5mm X5mm, TQFP Package

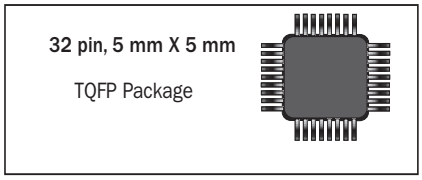
Input Options	Output Options
Open	50Ω Source / Sink
IN<0 - 3>	
IN<0 - 3>*	



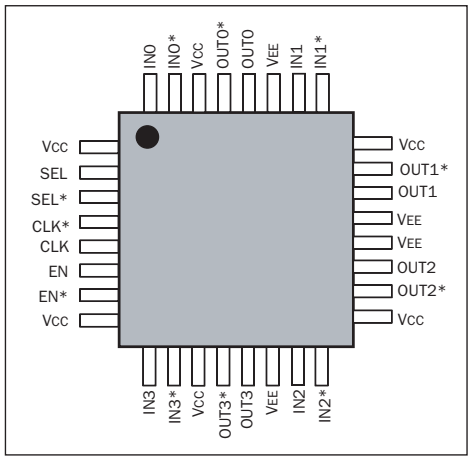
Functional Block Diagram



Package Information

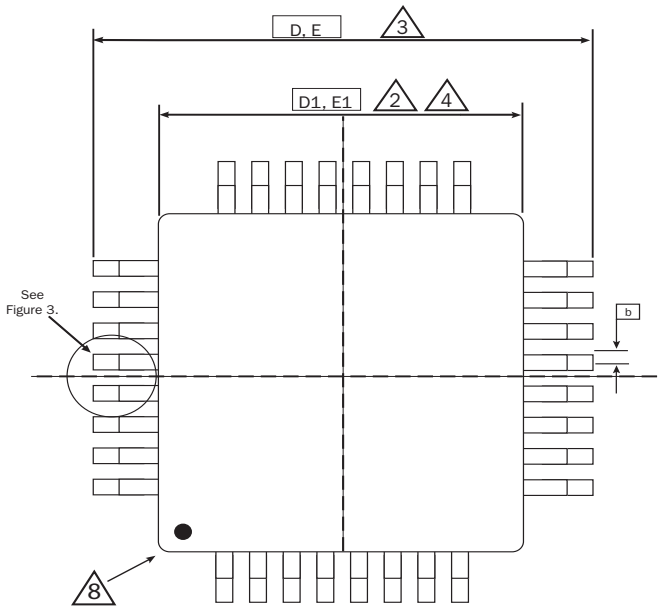


Pin Description

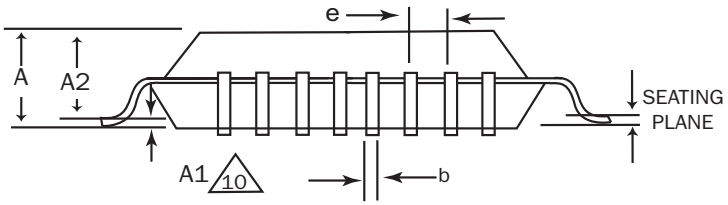


Package Information

32 Pin, 5mm x 5mm TQFP Package



Top View



Side View

Package Information *(continued)*

32 Pin, 5mm x 5mm TQFP Package

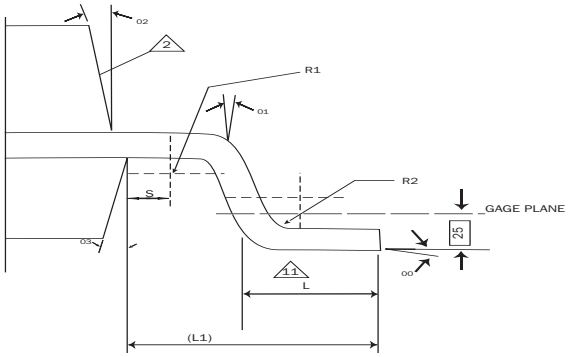


Figure 1.

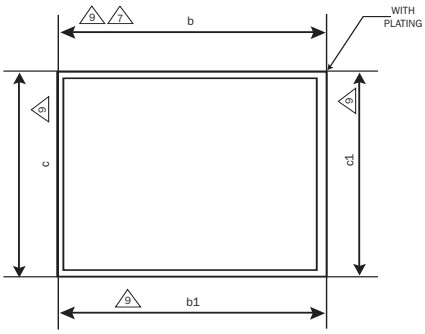


Figure 2.

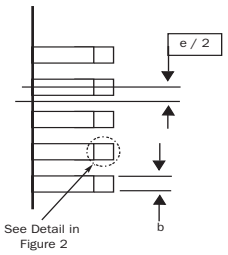


Figure 3.

1. All dimensions and tolerancing conforms to ANSI Y14.5M-1982.
2. The top package body size may be smaller than the bottom package body size by as much as 0.15 mm.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Details of Pin 1 identifier optional, but must be located within the zone indicated.
6. All dimensions are in millimeters.
7. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
8. Exact shape of each corner is optional.
9. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. A1 is defined as the distance from the seating plane to the lowest point of the package body.

JEDEC Variation All Dimensions in Millimeters					
Symbol	MIN	NOM	MAX	Note	Comments
A	1.00	1.10	1.20		Package Stand Off Height
A1	0.05	0.10	0.15		Air Gap
A2	0.95	1.00	1.05		Package Body Thickness
D		7.00 BSC		3	
D1		5.00 BSC		4, 2	Package Body Length
E		7.00 BSC		3	
E1		5.00 BSC		4, 2	Package Body Width
N		32			Lead Count
e		0.50 BSC			Lead Pitch
b	0.17	0.22	0.27	7	Lead Thickness
b1	0.17	0.20	0.23		
R1	0.08	–	–		
R2	0.08	–	0.20		
θ0	0°	3.5°	7°		
θ1	0°	–	–		
θ2	11°	12°	13°		
θ3	11°	12°	13°		
S	0.20	–	–		
c	0.09	–	0.20		
c1	0.09	–	0.16		
L	0.45	0.60	0.75		
L1		1.00 REF			
aaa		0.20			
bbb		0.20			
ccc		0.08			
ddd		0.08			

Absolute Maximum Ratings*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	-8.0 to 0	V
V_{CC}	Power Supply (V_{EE} = 0V)	+8.0 to 0	V
V_I	Input Voltage	VCC≥VI≥VEE	V
I_{OUT}	Output Current Continuous Surge	 50 100	 mA mA
T_{stg}	Storage Temperature	-65 to +150	^{0}C
T_{sol}	Solder Temperature (<2 to 3 seconds: 245^{0}C desired)	265	^{0}C

* Maximum Ratings are those values beyond which damage to the device may occur.

Note 1: Device is ESD sensitive and requires protective handling.

DC Characteristics

(V_{CC} = 2.0V to 3.6V; VEE = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - 0.2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	| VIH - VIL |	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	IIH IIL	-5.0 -1	+8.0 <0.5	+25 +1	µA µA
Timing Inputs (IN / IN*) Input High Current, Input Low Current	IIH, IIL	-20	<40	80	µA
Functional Inputs (EN / EN*, SEL / SEL*) Input Current	IIH, IIL	-500	<200	+500	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.5 8.0 40	780 VCC -1.3 10.5 50	 VCC - 1.1 13.5 60	mV V mA Ω
Power Supply					
Power Supply Current	IEE		170	235	mA

DC Test Conditions: Outputs unterminated.

AC Characteristics

(V_{CC} = 2.0V to 3.6V; VEE = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0) SEL to OUT [0:3] EN to OUT [0:3]	 Tpd Tpd Tpd Tpd	 200 430 300 250	 350 580 450 350	 550 780 650 600	 ps ps ps ps
Channel to Channel Skew			15	40	ps
Maximum Operating Frequency [1]	Fmax	3			GHz
Minimum Pulse Width [1]	PW min	250			ps
IN to CLK Set Up Time Hold Time	 Ts Th	 120 120			 ps ps
Output Rise and Fall Times (20% / 80%) [1]	Tr / Tf		125	165	ps
Temperature Coefficient [1]	ΔTpd / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note 1: Guaranteed by characterization. Not production tested.

Ordering Information

Ordering Code	Package ID
SK4429ATF	32 Pin - TQFP 5 X 5 mm
S4429ATF-T	Tape and Reel

Notes:

1. For Tape and Reel information, see TMD Part Ordering Information Data Sheet.

Application Notes

AN1001 - EPIC Family Product Line
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Contact Information

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